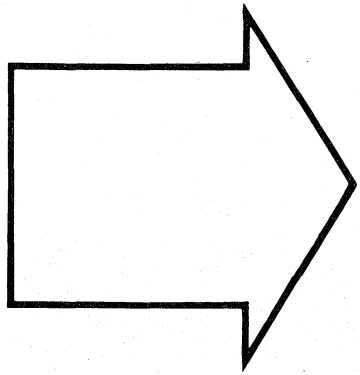
LSI Databook

Seventh Edition

PROMS
PLE DEVICES
PAL® DEVICES
HAL®/ZHAL™ DEVICES
SYSTEMS BUILDING BLOCKS/HMSI™
FIFOS
MEMORY SUPPORT
ARITHMETIC ELEMENTS AND LOGIC
MULTIPLIERS
8-BIT INTERFACE
DOUBLE-DENSITY PLUS™ INTERFACE
ECL10KH
LOGIC CELL ARRAY

Monolithic Memories MMI



LSI DATABOOK

SEVENTH EDITION

Monolithic Memories

Monolithic Memories Inc. • 2175 Mission College Blvd. • Santa Clara, CA 95054-1592 • (408) 970-9700 • (910) 970-9700 • (910) 338-2374

Introduction

This book has been prepared to give the user a concise list of all LSI Products offered by Monolithic Memories. It is divided by products into sections on Military Products Division, PROMs, PLE™ devices, PAL® devices, HAL®/ZHAL devices, System Building Blocks/HMSI™, FIFOs, Memory Support, Arithmetic Elements and Logic, Multipliers, 8-Bit Interface, Double-Density PLUS Interface, (CMOS products included), Logic Cell Array, ECL10KH products and a General Information Section which has definition of Terms and Waveforms. Each section has been designed to allow the user the most useable format for the products described. Cross reference and selection guides are given where applicable. FIFO, PAL devices, System Building Blocks/HMSI™, Multipliers, 8-Bit Interface, Double-Density PLUS Interface and ECL10KH data sheets are shown in detail for each product. Advance Information Sheets are included to inform you of soon-to-be released products. This LSI databook was formatted with you, the user, in mind.

For more information, contact the local Monolithic Memories sales representative or franchised distributor. In section 19 of this book Monolithic Memories Sales Reps and Franchised Distributors are listed, for your convenience.

Products listed in the Advance Information section were due for imminent release at the time of printing. Please contact Monolithic Memories for current availability and full parametric specifications.

Prices

All prices are in U.S. dollars and are subject to change without notice.

Terms

70%/30 days, 30%/45 days from date of invoice, FOB Sunnyvale, California.

Minimum Order Requirements

For all orders placed in the factory there is a minimum order requirement of $1000 ($100 per line item) except for the following:

HAL® Circuits—A Non-Recurring Engineering (NRE) charge is made to cover mask and test vector generation. This charge may be amortized over the initial production commitment. Minimum production commitments and NRE charges are as follows:

	NRE	MIN. ANNUAL QTY	MIN. QTY PER DELY
20 and 24 pin HAL devices:			
Combinatorial patterns	$2.5K	5,000 pcs	2,000 pcs
Sequential patterns	$2750	5,000 pcs	2,000 pcs
ZHAL™20/20A/24A	$4K	5,000 pcs	2,500 pcs
MegaHAL™:			
HAL32R16	$5K	2,500 pcs	500 pcs
ZHAL64R32	$5K	1,000 pcs	200 pcs

ProPAL™ Circuits—ProPAL circuits are programmed PAL devices which are functionally tested by Monolithic Memories prior to shipment. The NRE charge covers setup and test vector generation costs and may be amortized over the initial production commitment quantities. A nominal per unit programming and testing charge is also made and varies according to device type. NREs and minimum order requirements for ProPAL circuits are as follows:

	NRE	MIN. ANNUAL QTY	MIN. QTY PER DELY
20 and 24 pin devices:			
Combinatorial patterns	$500	2,500 pcs	500 pcs
Sequential patterns	$750	2,500 pcs	500 pcs
MegaPAL™:			
PAL32R16	$1K	1,000 pcs	200 pcs
PAL64R32	$1K	500 pcs	100 pcs

General

Unless otherwise specified, the standard packages are "J" or "N" packages. In some instances the "D" package is the only package available. Other non-standard packages and military Level 883B devices not listed may be available. Contact a sales representative of Monolithic Memories. Non-standard devices are considered nonreturnable by distribution to Monolithic Memories.

In-House PROM Programming Guidelines

1) Minimum Order Size.
   ¼K–8K 5K pcs/yr/pattern
   500 pcs/shipment
   16K–32K 2.5K pcs/yr/pattern
   250 pcs/shipment
2) Lead Time: Initial code acceptance six weeks.
   Standard lead time plus two weeks after code acceptance.
3) Cancellations: 60 Days
4) Schedule Change: 30 Days
5) Price Adder:
   A nominal per unit programming and testing charge is made and varies according to device type. Price includes ink marking with customer pattern number.
6) Inputs: Truth Table, Paper Tape, Disk, Master; a combination of two inputs are required. If only one input is supplied, a sample lot must be signed off by the customer.

Commercial/Industrial/Military Codes

The letter codes "C," "I," and "M" are used to denote commercial, industrial, and military device limits as follows:

Commercial—T_A = 0°C to +75°C
V_{CC} = 5V±5%
Industrial—T_A = −40°C to +85°C
V_{CC} = 5V±10%
Military—T_A = −55°C to +125°C
V_{CC} = 5V±10%

Package Codes

All devices ordered must include a package code as a suffix to the part number. The package code definitions are shown below.

PACKAGE CODE	DESCRIPTION
J	Ceramic dual-in-line
JS	Ceramic dual-in-line SKINNYDIP®
N	Plastic dual-in-line
NS	Plastic dual-in-line SKINNYDIP®
NL	Molded leaded chip carrier
D	Side brazed ceramic dual-in-line
F	Flat Pack—Bottom Brazed
L	Leadless—Ceramic chip carrier
T	Inverted "D" package
P	Pin Grid Array
W	Cerpack

See "Part Numbering Systems" for complete part descriptions.

DIP Package Width Configuration

	300 mil	600 mil	900 mil
16, 18, 20 pin	N, J		
24 pin	NS, JS	N, J	
28, 40, 48, 52 pin		N, J	
64 pin			D

Screening Options

PROCESS LEVEL	PART MARKING
MIL-STD-883 Method 5004 and 5005 Level B	883B (Suffix)

PAL®
Programmable Array Logic Circuits

PAL 16 L 8 B -4 C N STD H01234

FAMILY TYPE
- PAL = Programmable Array Logic
- PAL10H = ECL 10KH Programmable Array Logic
- HAL = Hard Array Logic
- ZHAL = Zero-power Hard Array Logic

NUMBER OF ARRAY INPUTS

OUTPUT CELL
- L = Active Low
- H = Active High
- C = Complementary
- P = Programmable Polarity
- RP = Registered Programmable Polarity
- S = Shared
- RS = Registered Shared
- X = Exclusive-OR
- A = Arithmetic
- VX = Varied Exclusive-OR
- RA = Registered Asynchronous
- G = Latched

NUMBER OF OUTPUTS

SPEED
- Blank = Standard
- A = High Speed
- B = Very High Speed
- D = Ultra High Speed

POWER
- Blank = Standard
- -2 = 1/2 Power
- -4 = 1/4 Power

OPERATING CONDITIONS
- C = Commercial
- I = Industrial
- M = Military

PACKAGE
- N = Plastic DIP
- J = Ceramic DIP
- NS = Plastic SKINNYDIP
- JS = Ceramic SKINNYDIP
- NL = Plastic Leaded Chip Carrier
- P = Pin Grid Array
- L = Leadless Chip Carrier
- W = Cerpack
- F = Flat Pack

PROCESSING
- STD = Standard
- XXXX = Other

BIT PATTERN NUMBER

PLE™ Programmable Logic Element

PLE5P8 C N STD

- PREFIX: PLE = Programmable Logic Element
- NUMBER OF INPUTS
- OUTPUT TYPE: P = Programmable Polarity; R = Registered
- NUMBER OF OUTPUTS
- TEMPERATURE CODE: C = Commercial; M = Military
- PACKAGE: N = Plastic DIP; J = Ceramic DIP; NS = Plastic SKINNYDIP; JS = Ceramic SKINNYDIP; NL = Plastic Leaded Chip Carrier; L = Leadless Chip Carrier; W = Cerpack; F = Flat Pack
- PROCESSING: STD = Standard; XXXX = Other

High Performance PROMs

63S3281 A N STD

- TEMPERATURE CODE: 6 = Commercial; 5 = Military
- PRODUCT: 3 = Programmable Read-Only Memory (PROM)
- FAMILY: S = Schottky; RA = Registered Asynchronous; RS = Registered Synchronous; D = Diagnostic; DA = Diagnostic Asynchronous
- MEMORY SIZE: 0 = 256 bits; 1 = 1024 bits; 2 = 2048 bits; 4 = 4096 bits; 8 = 8192 bits; 16 = 16384 bits; 32 = 32768 bits; 64 = 65536 bits
- NUMBER OF OUTPUTS
- OUTPUT DESIGNATOR: 0 = Open Collector; 1 = Three-State; 2 = Three-State (Alternate Enables); 3 = Two-State; 5 = Alternate Pinout
- PERFORMANCE: None = Standard; A = Enhanced
- PACKAGE: N = Plastic DIP; J = Ceramic DIP; NS = Plastic SKINNYDIP; JS = Ceramic SKINNYDIP; NL = Plastic Leaded Chip Carrier; L = Leadless Chip Carrier; W = Cerpack; F = Flat Pack
- PROCESSING: STD = Standard; XXXX = Other

ECL 10KH Logic

MC 10H 101 NL

- STANDARD PREFIX
- FAMILY: 10KH = High-Speed 10K ECL
- UNIQUE THREE-DIGIT PART NUMBER
- PACKAGE: N = Plastic DIP; J = Ceramic DIP; NL = Plastic Leaded Chip Carrier

FIFOs

C67401 A NL

- CASCADABILITY: C = Cascadable; Blank = Standalone
- TEMPERATURE CODE: 67 = Commercial
- PART NUMBER
- SPEED: Blank = Standard; A/B = Enhanced
- PACKAGE: N = Plastic DIP; J = Ceramic DIP; NL = Plastic Leaded Chip Carrier

Memory Support/Arithmetic/ HSMI/ Double-Density PLUS™ Interface

SN54LS646 J 883B

- STANDARD PREFIX
- TEMPERATURE CODE: 74 = Commercial; 54 = Military
- FAMILY: S = Schottky; LS = Low-Power Schottky; ACT = Advanced CMOS, TTL-Compatible
- UNIQUE THREE-DIGIT PART NUMBER
- PACKAGE TYPE: J = Ceramic DIP; L = Leadless Chip Carrier; W = Cerpack; NS = Plastic SKINNYDIP; JS = Ceramic SKINNYDIP; NL = Plastic Leaded Chip Carrier
- HI-REL SCREENING LEVEL: 883B = Mil-Std-883, Class B

Table of Contents

ECL10KH

LOGIC CELL ARRAY

GENERAL INFORMATION

ADVANCE INFORMATION

Monolithic Memories

Terms and Conditions of Sale

General Provisions

1. ACCEPTANCE THE TERMS OF SALE CONTAINED HEREIN APPLY TO ALL QUOTATIONS MADE AND PURCHASE ORDERS ENTERED INTO BY THE SELLER. SOME OF THE TERMS SET OUT HERE MAY DIFFER FROM THOSE IN BUYER'S PURCHASE ORDER AND SOME MAY BE NEW. THIS ACCEPTANCE IS CONDITIONAL ON BUYER'S ASSENT TO THE TERMS SET OUT HERE IN LIEU OF THOSE IN BUYER'S PURCHASE ORDER. SELLER'S FAILURE TO OBJECT TO PROVISIONS CONTAINED IN ANY COMMUNICATION FROM BUYER SHALL NOT BE DEEMED A WAIVER OF THE PROVISIONS OF THIS ACCEPTANCE. ANY CHANGES IN THE TERMS CONTAINED HEREIN MUST SPECIFICALLY BE AGREED TO IN WRITING BUY AN OFFICER OF THE SELLER BEFORE BECOMING BINDING ON EITHER THE SELLER OR THE BUYER. All orders or contracts must be approved and accepted by the Seller at its home office. These terms shall be applicable whether or not they are attached to or enclosed with the products to be sold hereunder.

2. TAXES Unless otherwise specifically provided herein, the amount of any present or future sales, revenue, excise or other tax applicable to the products covered by this order or the manufacture of sale thereof, shall be added to the purchase price and shall be paid by the Buyer, or in lieu thereof the Buyer shall provide the Seller with a tax exemption certificate acceptable to the taxing authorities. In the event Seller is required to pay any such tax, fee, or charge, at the time of sale or thereafter, the Buyer shall reimburse Seller therefore.

3. RELEASE Prices apply only if the quantity hereunder is released within twelve (12) months and shipments scheduled no more than eighteen (18) months from the date of Seller's receipt of Buyer's order; otherwise, Seller's standard prices in effect at the time of release date shall apply to the quantity shipped, and Buyer shall be invoiced for the difference in price, if any.

4. FOB POINT Shipments of goods within and outside the U.S. shall be delivered FOB Seller's plant, and title and liability for loss or damage thereto shall pass to Buyer upon Seller's tender of delivery of the goods to a carrier for shipment to Buyer, and any loss or damage thereafter shall not relieve Buyer of any obligation hereunder. Buyer shall reimburse Seller for taxes and any other expenses incurred or licenses or clearance required at port of entry and destination. Seller may deliver the goods in installments. Unless otherwise agreed, all items shall be packaged and packed in accordance with Seller's normal practices.

5. DELIVERY All shipping dates are estimates only and are dependent upon prompt receipt of all necessary information from Buyer. Shipments may be made in installments. Seller shall be excused from performance and shall not be liable for any delay in delivery or for nondelivery, in whole or in part, caused by the occurrence of any contingency beyond the reasonable control of Seller, including but not limited to, war (whether or not an actual declaration thereof is made), sabotage, insurrection, riot or other act of civil disobedience, act of a public enemy, failure or delay in transportation, act of any government or any agency or subdivision thereof affecting the terms of this contract or otherwise, judicial action, labor dispute, accident, defaults of suppliers, fire, explosion, flood, storm or other acts of God, shortage of labor, fuel, raw material or machinery or technical or yield failures where Seller has exercised ordinary care in the prevention thereof. If any such contingency occurs, Seller may at its sole discretion allocate production and delivery among Seller's customers.

6. PAYMENT TERMS (a) Unless otherwise agreed, payment terms are 70% thirty (30) days; 30% forty-five (45) days after date of invoice. No discounts are authorized. Shipments, deliveries, and performance of work shall at all times be subject to the approval of the Seller's credit department and the Seller may at any time decline to make any shipments or deliveries or perform any work except upon receipt of payment or upon terms and condition or security satisfactory to such department.

(b) If in the judgment of the Seller, the financial condition of the Buyer at any time does not justify continuation of production or shipment on the terms of payment originally specified, the Seller may require full or partial payment in advance and, in the event of the bankruptcy or insolvency of the Buyer or in the event any proceeding is brought by or against the Buyer under the bankruptcy or insolvency laws, the Seller shall be entitled to cancel any order then outstanding and shall receive reimbursement for its cancellation charges.

(c) Each shipment shall be considered a separate and independent transaction, and payment therefore shall be made accordingly. If shipments are delayed by the Buyer, payments shall become due on the date when the Seller is prepared to make shipment. If the work covered by the purchase order is delayed by the Buyer, payments shall be made based on the purchase price and the percentage of completion. Products held for the Buyer shall be at the risk and expense of the Buyer.

7. INSPECTION Unless otherwise specified and agreed upon, the material to be furnished under this order shall be subject to the Seller's standard inspection at the place of manufacture. If it has been agreed upon and specified in this order that Buyer is to inspect or provide for inspection at place of manufacture such inspection shall be so conducted as to not interfere unreasonably with Seller's operations and consequent approval or rejection shall be made before shipment of the materials. Notwithstanding the foregoing, if, upon receipt of such material by Buyer, the same shall appear not to conform to the contract, the Buyer shall immediately notify the Seller of such conditions and afford the Seller a reasonable opportunity to inspect the material. No material shall be returned without Seller's consent. Seller's Return Material Authorization form must accompany such returned material.

8. LIMITED WARRANTY AND LIMITED REMEDY The Seller warrants that the products to be delivered under this purchase order will be free from defects in material and workmanship under normal use and service. Seller's obligations under this Warranty are limited to replacing or repairing or giving credit for, at its option, at its factory, any of said products which shall, within one (1) year after shipment, be returned to the Seller's factory of origin, transportation charges prepaid, and which are, after examination, disclosed to the Seller's satisfaction to be thus defective. THIS WARRANTY IS EXPRESSED IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, STATUTORY OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AND OF ALL OTHER OBLIGATIONS OR LIABILITIES ON THE SELLER'S PART, AND IT NEITHER ASSUMES NOR AUTHORIZES ANY OTHER PERSON TO ASSUME FOR THE SELLER ANY OTHER LIABILITIES IN CONNECTION WITH THE SALE OF THE SAID ARTICLES. This Warranty shall not apply to any of such products which shall have been repaired or altered, except by the Seller, or which shall have been subjected to misuse, negligence, or accident. The aforementioned provisions do not extend the original warranty period of any product which has either been repaired or replaced by Seller.

It is understood that if this order calls for the delivery of semiconductor devices which are not furnished and fully encapsulated, that no warranty, statutory, expressed or implied, including the implied warranty of merchantability and fitness for a particular purpose, shall apply. All such devices are sold as-is, where-is.

9. PATENT INDEMNIFICATION Buyer shall hold Seller harmless from and defend Seller against any cost, expenses, damages or liabilities arising from Seller's compliance with Buyer's designs or specifications. Except as set forth above, the Seller agrees to protect and hold harmless the Buyer from any and all claims, demands, proceedings, actions, liabilities and costs resulting from any alleged infringement of patents in the United States owned by third parties by Products purchased by Buyer from Seller, provided the Buyer gives to Seller prompt notice of any such claim made against the Buyer and authorizes the Seller to settle or defend any such claim, demand, proceeding or action and assists the Seller in so doing (at the Seller's expense) upon request by the Seller. Should, as a result of any such claim, demand, proceeding or action, the Buyer be enjoined from selling or using the product, the Seller shall either (1) procure for the Buyer the right to use or sell the product; (2) modify the product so that it becomes noninfringing; (3) upon return of the product provide to the Buyer a noninfringing product meeting the same functional specifications as the product; or (4) authorize the return of the product to the Seller and upon its receipt refund to the Buyer the cost of the product plus transportation charges. The foregoing states the entire liability of the Seller for infringement of the patents of third parties and, in particular, the Seller has no obligation to indemnify the buyer for infringement of patents resulting from combinations of the product with other products whether or not supplied by the Seller. THIS PROVISION IS STATED IN LIEU OF ANY OTHER EXPRESSED, IMPLIED, OR STATUTORY WARRANTY AGAINST INFRINGEMENT AND SHALL BE THE SOLE AND EXCLUSIVE REMEDY FOR PATENT INFRINGEMENT OF ANY KIND.

10. DAMAGE LIMITATION INDEPENDENTLY OF ANY OTHER LIMITATION HEREOF AND REGARDLESS OF WHETHER THE PURPOSE OF SUCH LIMITATION IS SERVED, IT IS AGREED THAT IN NO EVENT SHALL SELLER BE LIABLE FOR SPECIAL, INCIDENTAL OR CONSEQUENTIAL DAMAGES OF ANY KIND UNDER THIS ORDER.

11. SALE CONVEYS NO LICENSE Seller's products are offered for sale and are sold by Seller subject in every case to the condition that such sale does not convey any license, expressly or by implication, estoppel or otherwise, under any patent claim with respect to which Seller can grant licenses covering a completed equipment, or any assembly, circuit, combination, method or process in which any such products are used as components (notwithstanding the fact that such products may have been designed for use in or may only be useful in, such patented

Monolithic Memories

Terms and Conditions of Sale

General Provisions

equipment, assembly, circuit, combination, method or process and that such products may have been purchased and sold for such use). Seller expressly reserves all its rights under such patent claims.

12. RETURNS AND ADJUSTMENTS Products may only be returned with prior written approval of Seller. Adjustments for defective products are subject to Seller's concurrence that the alleged defects exist, to Seller's satisfaction, after suitable inspection and test by Seller. Adjustments may include credit or replacement at the option of the Seller.

13. TERMINATION AND CANCELLATION (a) Buyer may terminate this contract in whole or, from time to time, in part upon written notice to Seller. In such event Buyer shall be liable for termination charges which shall include a price adjustment based on the quantity of goods actually delivered, and all costs, direct and indirect, incurred and committed for this contract together with a reasonable allowance for prorated expenses and anticipated profits.

(b) Unless otherwise specified on the face hereof, all quantities must be released no more than twelve (12) months and shipments scheduled no more than eighteen (18) months from the date of Seller's receipt of Buyer's order, otherwise this contract may be cancelled by Seller and Buyer shall be liable for termination charges as provided herein.

14. NONWAIVER OF DEFAULT In the event of any default by Buyer, Seller may decline to make further shipments. If Seller elects to continue to make shipments, Seller's action shall not constitute remedies for any such default.

15. APPLICABLE LAW The validity, performance and construction of this contract shall be governed by the laws of the State of California.

16. U.S. GOVERNMENT CONTRACTS If Buyer's original purchase order indicates by contract number, that it is placed under a government contract, only the following provisions of the current Federal Acquisition Regulations are applicable in accordance with the terms thereof, with an appropriate substitution of parties, as the case may be—i.e., "Contracting Officer" shall mean "Buyer," "Contractor" shall mean "Seller," and the "Contract" shall mean this order.

52.202-1. Definitions: 52.232-11, Extras; 52.212-9, Variation in Quantity; 52.232-23, Assignment of Claims; 52.228-2, Additional Bond Security; 52.225-11, Certain Communist Areas; 52.222-4, Contract Work Hours and Safety Standards Act —Overtime Compensation; 52.222-20, Walsh-Healy Public Contracts Act; 52.22-25, Equal Opportunity; Officials Not to Benefit; 52.203-5, Covenant Against Contingent Fees; 52.249-1, Termination for Convenience of the Government (Fixed Price) (Short Form) (only to the extent that Buyer's contract is terminated for the convenience of the government); 52.2-1, Contractor Inspection Requirements; 52.227-1, Authorization and Consent; 52.227-2, Notice and Assistance Regarding Patent and Copyright Information; 52.247-1, Commercial Bills of Lading Notations; 52.223-35, Affirmative Action for Special Disabled and Vietnam Era Veterans; 52.222-1, Notice to the Government of Labor Disputes; 52.215-1, Examination of Records by Comptroller General; 52.220-3, Utilization of Labor Surplus Area Concerns.

17. ASSIGNMENT This contract shall be binding upon and inure to the benefit of the parties and the successors and assigns of the entire business and good will of either Seller or Buyer, or of that part of the business of either used in the performance of this contract, but shall not be otherwise assignable.

18. MODIFICATION This contract constitutes the entire agreement between the parties relating to the sale of goods described on the face hereof, and no addition to or modification of any provision upon the face or reverse of this contract shall be binding upon Seller unless made in writing and signed by a duly authorized representative of Seller located in Santa Clara, California. Buyer hereby acknowledges that he has not entered into this agreement in reliance upon any warranty or representation by any person or entity except for the warranties or representations specifically set forth herein.

19. GENERAL The Seller represents that with respect to the production of the articles and/or the performance of the services covered by this order, it will fully comply with all requirements of the Fair Labor Standards Act of 1938, as amended.

20. PROPERTY RIGHTS AND TOOLING The design, development or manufacture by Seller of a product for a specific customer shall not be deemed to produce a work made for hire and shall not give to the customer any copyright interest in the product or any interest in all or any portion of the mask works relating to the product. All such rights shall remain the property of Seller. Notwithstanding the foregoing, Seller will provide a custom product (e.g., personalized gate array, cell library or full custom) utilizing a logic design supplied by a customer exclusively to that customer absent written agreement to the contrary with the customer.

21. VARIATION IN QUANTITY If this order calls for a product not listed in Seller's current catalog, or for a product which is specially programmed for Buyer, it is agreed that Seller may ship a quantity which is five percent (5%) more or less than the ordered quantity and that such quantity shipped will be accepted and paid for in full satisfaction of each party's obligation hereunder for the quantity ordered.

Quality System

The quality system at Monolithic Memories is based on MIL-Q-9858, "Quality Program Requirements," MIL-I-45208, "Inspection System Requirements," and MIL-M-38510, Appendix A, "Product Assurance Program." Mil-M-38510 plays a significant role in structuring Monolithic Memories' Quality Program as specified herein.

Monolithic Memories has facilities certified by DESC, Defense Electronics Supply Center, to qualify and manufacture Class B Schottky Bipolar PROMS and Programmable Array Logic devices, in accordance with the requirements of MIL-M-38510. This certification included a successful audit of our quality system to the stringent requirements of Appendix A of MIL-M-38510 which defines a Product Assurance Program tailored for integrated circuit manufacturers by DESC. This same quality system has also met the strict requirements of both "controlled" and "captive" line programs connected with our special Hi-Rel programs.

The quality accent at Monolithic Memories is on process control as reflected in the use of many monitors and audits rather than gate inspection. This philosophy is consistent with building in quality and reliability rather than attempting to screen for it.

Process Control

Monolithic Memories manufacturing process uses advanced techniques to reduce random defects and produce consistent optimum quality. Typical techniques employed are:

- Redundant Masking
- Pellicalized Masks
- Direct Step on Wafer Processing

These processes although more costly, result in significant quality and reliability improvements. During the initial production stages of new designs and periodically thereafter, engineering characterizes the design process compatibility by careful sample selection of lots reflecting process variable extremes.

Product Reliability Programs

Monolithic Memories has an ongoing reliability program for military and commercial products, each utilizing the appropriate test methods of MIL-STD-883. This program provides for a consistent database in the following areas:

- Product/Process Reliability Data
- Qualification of Raw Materials
- Customer Quality Conformance
- Reliability verification of state of the art design and production techniques.

Quality Monitors

MMI constantly monitors product quality and reliability through the following ongoing programs:

- Reliability assessments of all products, processes and packages.
- Inprocess and Final product quality measurements.
- Process and product quality feedback at all key manufacturing points.
- Positive corrective action and verification.

Screening

Much of the assembly and processing is performed offshore at facilities owned by or qualified by MMI. These facilities are routinely monitored by Monolithic Memories personnel to our quality system requirements.

Standard Commercial product receives the following screens and monitors to insure the highest possible quality.

- Precap Inspection — MIL-Standard 883 Level B
- Temperature Cycle
- Constant Acceleration
- Fine and Gross Leak
- Final Electrical Test
- Visual and Mechanical Inspection

— Ongoing daily monitor to confirm the AQL levels are met or exceeded.

The standard product AQL levels which Monolithic Memories guarantees are listed in the table on this page.

Quality Assurance (AQL) Levels

TEST	AQL TEMPERANCE
Hermeticity (includes fine and gross)	.1
Electrical	
DC at 25°C	.065
Functional at 25°C	.065
AC at 25°C	.25
DC at Temperature Extremes	.25
Functional at Temperature Extremes	.25
AC at Temperature Extremes	.25

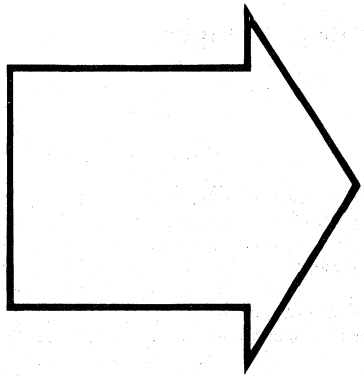


Table of Contents

MILITARY PRODUCTS DIVISION

Introduction

In August, 1982 Monolithic Memories Inc. formed a Military Products Division. Although Monolithic Memories has participated in the defense market for some time, we feel that by focusing on this very demanding customer base with a totally dedicated resource, we can provide aerospace and military systems manufacturers with a new industry standard of service and responsiveness.

Monolithic Memories offers devices to a full complement of military screening levels:

Monolithic Memories Inc. Level S
JAN 38510 Class B
DESC Drawing Program
Mil-Std-883 Class B
Monolithic Memories Inc Mil-Temp Product

In addition, we welcome the opportunity to review and quote to customer source control drawings. Our spec Review group is measured to a 2 week turn-around time on drawing reviews, so our customers will receive a timely response on our ability to meet custom requirements.

Monolithic Memories is Certified by the Defense Electronics Supply Center to assemble and test JAN 38510 Class B devices at its Sunnyvale, California.

Offshore Assembly facilities for Mil-Std-883 Class B devices are located in Penang, Malaysia.

Standard Processing Flows

Monolithic Memories Processing and Screening flows are organized to provide a broad selection of processing options, structured around the most commonly requested customer flows.

Standard processing flows which the Military Products Division currently operates to include:

Monolithic Memories Inc. Modified Level S
JAN 38510 Class B
DESC Drawing Program
Mil-Std-883 Class B
Monolithic Memories Inc. Mil-Temp Product

In addition, these flows are expanded to provide for factory programming on PAL circuits and PROMS, when required by our customers.

Major benefits can be realized by ordering product to standard flows whenever possible:

- Minimize need for source control drawings.
- Cost savings on unit cost — no price adders for custom processing.
- Improved lead time — no spec review or negotiation time, plus the ability to pull product from various work-in-process stages or purchase product from finished goods inventory.

It is the policy of Monolithic Memories to always operate to the most current revision of Mil-Std-883.

Quality Programs

The Military Product Division quality system conforms to the following Mil-Standards:

Mil-M-38510, Appendix A, "Product Assurance Program"
Mil-Q-9858, "Quality Program Requirements"
Mil-I-45208, "Inspection System Requirements"

Monolithic Memories facilities in Sunnyvale are certified by the Defense Electronics Supply Center (DESC), to manufacture and qualify Schottky Bipolar PROMs and PAL circuits in accordance with Mil-M-38510 Class B. This certification was a result of a successful audit of our production and quality systems to the stringent requirements of Mil-M-38510. Monolithic Memories has also demonstrated compliance with the strict requirements of both controlled and captive lines connected with special Military programs.

Quality Assurance

Following 100% screening, the Military Products Division samples all products processed in conformance with MIL-STD-883 Class B to the following LTPD levels:

Test	LTPD
DC 25°C	2
DC +125°C	3
DC -55°C	5
Functional at 25°C	2
Functional at Temperature Extremes	5
AC 25°C	2
AC +125°C	3
AC -55°C	5

The Military Products Division ensures outgoing product quality and integrity by performing inspection Lot Group A's and B's per Mil-Std-883 Method 5005, conducting self audits in all areas involved in screening tests per Method 5004 of Mil-Std-883, gating all shipments to our customers, and maintaining a calibration control system in accordance with Mil-Std-45662.

For products requiring programming prior to AC tests, testing is performed utilizing MIL-M-38510 Slash Sheet sample plans.

Product Qualification/ Quality Conformance Inspection (QCI)

The Military Products Division has a quality conformance testing program in accordance with Mil-Std-883, Method 5005. Quality Conformance Testing provides necessary feedback and monitors several areas:

- Reliability of Product/Processes
- Vendor Qualification for Raw Materials
- Customer Quality Requirements
- Maintain Product Qualification
- Engineering Monitor on Products/Processes

Standard procedures for new product release specify that Monolithic Memories' Reliability Department, as a minimum, conduct full qualification testing per Method 5005 of Mil-Std-883. Once qualified, each package type (from each assembly line) and device (by technology group as delineated in Mil-M-38510) are incorporated into Monolithic Memories Quality Conformance Inspection program which utilizes the requirements of Mil-M-38510.

When Military Programs do not require that QCI data be run on the specific lot shipped, Monolithic Memories Quality Conformance program allows customers to obtain generic data on all product families manufactured by the Military Products Division. Generic Qualification Data enables customers to eliminate costly qualification and desctruct unit charges, and also improves delivery time by a factor of eight to ten weeks. The following generic data is available:

Group B—Package related tests

- QCI is performed every 6 weeks of manufacture on each package type.
- Any device type in the same package type may be used regardless of the specific part number.
- Purpose: To monitor assembly integrity.

Group C—Product/Process related tests

- QCI is performed every 13 weeks of manufacture, on representative devices from the same microcircuit group.
- Life test data may be used to qualify similar technologies.
- Purpose: To monitor the reliability of the process and parametric performance for each product technology.

Prices

All prices are in U.S. dollars and are subject to change without notice.

Minimum Order Requirements

For all orders placed in the factory there is a minimum order requirement of $1000 ($250 per line item) except for the following:

HAL® Circuits—The $3-4K N.R.E. and mask charge can be amortized over the initial production commitment. The minimum initial production commitment is 5K units within one year; the minimum quantity per line item release is 2K.

ProPAL Circuits—When purchased, the initial phase of HAL Circuit, there is no additional N.R.E. and there is a nominal adder for programming and testing. The minimum quantity per release is 500 units. When purchased without a follow-on the $1-2K N.R.E. can be amortized over a minimum initial production commitment of $2500 units.

There will be a minimum of $250 and $50 per line item for drop-ship orders.

Terms

70%/30 days, 30%/45 days from date of invoice, FOB Sunnyvale, California.

Commercial Code

The letter code "C" is used to denote commercial device limits as follows:

Commercial—TA = 0°C to + 75°C
VCC = 5 V ±5%

General

Unless otherwise specified the standard packages are "J" or "N" packages. In some instances the "D" package is the only package available. Other non-standard packages may be available. Contact a sales representative of Monolithic Memories. Non-standard devices are considered nonreturnable by distribution to Monolithic Memories.

Package Codes

All devices ordered must include a package code as a suffix to the part number. The package code definitions are shown below.

PACKAGE CODE	DESCRIPTION
J	Ceramic dual-in-line*
JS	Ceramic dual-in-line*
N	Plastic dual-in-line*
NS	Plastic dual-in-line*
NL	Molded Leadless Chip Carrier

*See "Part Numbering Systems" for complete part descriptions.

Dip Package Width Configuration

	300 mil	600 mil
20 pin	N, J	–
24 pin	NS, JS	N, J

In-House PROM Programming Guidelines

1) Minimum Order Size:
   1/4K-8K 5K pcs/yr/pattern
   500 pcs/shipment
   16K-32K 2.5K pcs/yr/pattern
   250 pcs/shipment
2) Lead Time: Initial code acceptance—six weeks.
   Standard lead time plus weeks after code acceptance.
3) Cancellations: 60 Days
4) Schedule Change: 30 Days
5) Price Adder:
   Price includes ink marking with customer pattern number.
6) Inputs: Truth Tape
   Paper Tape
   Disk
   Master
   A combination of two inputs are required.
   If only one input is supplied, a sample lot must be signed off by the customer.

Order Size

DENSITY	MIN-10K	10K-25K	25K +
1/4-2K	50¢	40¢	30¢
4K-8K	60¢	50¢	40¢
16K-32K REG/DIAG	85¢	70¢	55¢

Monolithic Memories Software

SYSTEM	PALASM 2 OBJECT	PALASM 2 SOURCE
	$200	$500
DEC VAC VMS MT	PAL2-VMSE-MT	PAL2-VMSS-MT
IBM PC (DOS) 5D	PAL2-IPCE-5D	PAL2-IPCS-5D
ASCII MT		PAL2-ASCS-NJ

JAN Program

Monolithic Memories is certified by the Defense Electronics Supply Center to fabricate wafers in our 4-inch fab lines and to assemble and test MIL-M-38510 Class B PROMs and PAL circuits in our Sunnyvale facilities. Monolithic Memories has, in addition, been awarded full laboratory suitability to conduct all qualification and conformance testing in accordance with MIL-STD-883, Method 5005.

Selected devices will be further qualified in leadless chip carriers.

Long term QPL I plans include FIFO's Double-Density PLUS Interface, New PAL Families as they are introduced, and Registered/Standard PROMs.

Our goal in the Military Products Division is to support the JAN38510 Program with a continual flow of new high-performance, Advanced Technology Products.

Monolithic Memories Products for which slash sheet specifications currently exist are listed in the "M38510 Slash Sheet Cross Reference to Generic Part Number."

Listings are based on QPL-38510-65, dated October 1985
M38510 (Part I Qualified Devices)
Slash Sheet Cross Reference to Generic Part Number

M38510	01	02	03	04	05	06	07	08	09	10
206		53S441								
209								53S841		
503	10H8	12H6	14H4			10L8	12L6	14L4		
504	16L8A	16R8A	16R6A	16R4A						

Near future QPL I plans include:

PAL16L8A-2
PAL16R8A-2
PAL16R6A-2
PAL16R4A-2
PAL20L8A
PAL20R8A
PAL20R6A
PAL20R4A

DESC Drawing Program

Monolithic Memories is an active participant in the DESC Drawing Program. For contracts invoking MIL-STD-454 we offer our full PAL product line to DESC Drawings 81035 and 81036. Monolithic Memories is also approved to supply the 32K PROM to DESC Drawing 82008. The idea behind the DESC Drawing Program is to standardize MIL-STD-883B microcircuits where fully qualified JAN product is not available. The advantage to the user is that DESC Drawings are a cost effective alternative to source control drawings and are offered as off-the-shelf stocking items by IC manufacturers participating in the program.

Since semiconductor demand is on the rise, and lead times will be a major concern, DESC Drawings should always be considered to improve availability over source control drawings. It is standard practice at Monolithic Memories to convert our 883B processing to DESC Drawings for all products which we are approved to supply. Monolithic Memories Inc. then dual marks devices with both the DESC Drawing Number and the Generic Part Number. DESC approved products can then be procured to either part number as standard product through both OEM and distributor channels.

The following cross reference will allow you to determine the appropriate DESC Drawing part numbers for each PAL product and the 32K PROM. Future DESC print activity will include new PAL products and registered PROMs. Monolithic Memories will work with DESC to continually generate new drawings, which will provide a steady flow of advanced technology products to standardized specifications.

DESC Drawing/Generic Part Type Cross Reference

DESC DRAWING PART NO.: 81035	01	R	X*
DRAWING	DEVICE TYPE	CASE OUTLINE	LEAD FINISH

PAL DEVICES

DESC DRAWING	GENERIC PART NUMBER	REPLACEMENT JAN SPECIFICATION PART NUMBER
8103501RA*	PAL10H8MJ883B	M38510/50301BRX
81035012C	PAL10H8ML883B	M38510/50301B2X
8103501YC	PAL10H8MF883B	M38510/50301BYX
8103502RA	PAL12H6MJ883B	M38510/50302BRX
81035022C	PAL12H6ML883B	M38510/50302B2X
8103502YC	PAL12H6MF883B	M38510/50302BYX
8103503RA	PAL14H4MJ883B	M38510/50303BRX
81035032C	PAL14H4ML883B	M38510/50303B2X
8103503YC	PAL14H4MF883B	M38510/50303BYX
8103504RA	PAL16H2MJ883B	M38510/50304BRX
81035042C	PAL16H2ML883B	M38510/50304B2X
8103504YC	PAL16H2MF883B	M38510/50304BYX
8103505RA	PAL16C1MJ883B	M38510/50305BRX
81035052C	PAL16C1ML883B	M38510/50305B2C
8103505YC	PAL16C1MF883B	M38510/50305BYX
8103506RA	PAL10L8MJ883B	M38510/50306BRX
81035062C	PAL10L8ML883B	M38510/50306B2X
8103506YC	PAL10L8MF883B	M38510/50306BYX
8103507RA	PAL12L6MJ883B	M38510/50307BRX
81035072C	PAL12L6ML883B	M38510/50307B2X
8103507YC	PAL12L6MF883B	M38510/50307BYX
8103508RA	PAL14L4MJ883B	M38510/50308BRX
81035082C	PAL14L4ML883B	M38510/50308B2X
8103508YC	PAL14L4MF883B	M38510/50308BYX
8103509RA	PAL16L2MJ883B	M38510/50309BRX
81035092C	PAL16L2ML883B	M38510/50309B2X
8103509YC	PAL16L2MF883B	M38510/50309BYX

*Lead Finishes A = Solder Dip
C = Gold Plate

DESC Drawing/Generic Part Type Cross Reference continued

DESC DRAWING	GENERIC PART NUMBER	REPLACEMENT JAN SPECIFICATION PART NUMBER
8103607RA	PAL16L8AMJ883B[1]	M38510/50401BRX
81036072C	PAL16L8AML883B	M38510/50401B2X
8103607SA	PAL16L8AMW883B	M38510/50401BYX
8103608RA	PAL16R8AMJ883B[1]	M38510/50402BRX
81036082C	PAL16R8AML883B	M38510/50402B2X
8103608SA	PAL16R8AMW883B	M38510/50402BYX
8103609RA	PAL16R6AMJ883B[1]	M38510/50403BRX
81036092C	PAL16R6AML883B	M38510/50403B2X
8103609SA	PAL16R6AMW883B	M38510/50403BYX
8103610RA	PAL16R4AMJ883B[1]	M38510/50404BRX
81036102C	PAL16R4AML883B	M38510/50404B2X
8103610SA	PAL16R4AMW883B	M38510/50404BYX
8103611RA	**PAL16L8A-2MJ883B	M38510/50407BRX
81036112C	**PAL16L8A-2ML883B	M38510/50407B2X
8103611SC	PAL16L8A-2MF883B	— — —
8103612RA	**PAL16R8A-2MJ883B	M38510/50408BRX
81036122C	**PAL16R8A-2ML883B	M38510/50408B2X
8103612SC	PAL16R8A-2MF883B	— — —
8103613RA	**PAL16R6A-2MJ883B	M38510/50409BRX
81036132C	**PAL16R6A-2ML883B	M38510/50409B2X
8103613SC	PAL16R6A-2MF883B	— — —
8103614RA	**PAL16R4A-2MJ883B	M38510/50410BRX
81036142C	**PAL16R4A-2ML883B	M38510/50410B2X
8103614SC	PAL16R4A-2MF883B	— — —
8412901LA	PAL20L8AMJS883B	M38510/50501BJX
84129013C	PAL20L8AML883B	M38510/50501B3X
8412901KA	PAL20L8AMW883B	— — —
8412902LA	PAL20R8AMJS883B	M38510/50502BJX
84129023C	PAL20R8AML883B	M38510/50502B3X
8412902KA	PAL20R8AMW883B	— — —
8412903LA	PAL20R6AMJS883B	M38510/50503BJX
84129033C	PAL20R6AML883B	M38510/50503B3X
8412903KA	PAL20R6AMW883B	— — —
8412904LA	PAL20R4AMJS883B	M38510/50504BJX
84129043C	PAL20R4AML883B	M38510/50504B3X
8412904KA	PAL20R4AMW883B	— — —
8412905LA	PAL20L10AMJS883B	— — —
84129053C	PAL20L10AML883B	— — —
8412906LA	PAL20X8AMJS883B	— — —
84129063C	PAL20X8AML883B	— — —
8412907LA	PAL20X10AMJS883B	— — —
84129073C	PAL20X10AML883B	— — —

**Converting from "A" to "B" PAL in third quarter 1986.
1. Inactive for new designes using R Case Outline only. Use applicable QPL 38510 device.

DESC Drawing/Generic Part Type Cross Reference continued

DESC DRAWING	GENERIC PART NUMBER	REPLACEMENT JAN SPECIFICATION PART NUMBER
8412908LA	PAL20X4AMJ883B	— — —
84129083C	PAL20X4AML883B	— — —
8506501RA	**PAL16L8A-4MJ883B	— — —
85065012C	**PAL16L8A-4ML883B	— — —
8506501SC	**PAL16L8A-4MF883B	— — —
8506502RA	**PAL16R8A-4MJ883B	— — —
85065022C	**PAL16R8A-4ML883B	— — —
8506502SC	**PAL16R8A-4MF883B	— — —
8506503RA	**PAL16R6A-4MJ883B	— — —
85065032C	**PAL16R6A-4ML883B	— — —
8506503SC	**PAL16R6A-4MF883B	— — —
8506504RA	**PAL16R4A-4MJ883B	— — —
85065042C	**PAL16R4A-4ML883B	— — —
8506504SC	**PAL16R4A-4MF883B	— — —
8515501RA[1]	PAL16L8BPJ883B	— — —
85155012C[1]	PAL16L8BPL883B	— — —
8515502RA[1]	PAL16R8BPJ883B	— — —
85155022C[1]	PAL16R8BPL883B	— — —
8515503RA[1]	PAL16R6BPJ883B	— — —
85155032C[1]	PAL16R6BPL883B	— — —
8515504RA[1]	PAL16R4BPJ883B	— — —
85155042C[1]	PAL16R4BPL883B	— — —
8515505RA[1]	PAL16L8BM-2J883B	— — —
85155052C[1]	PAL16L8BM-2L883B	— — —
8515506RA[1]	PAL16R8BM-2J883B	— — —
85155062C[1]	PAL16R8BM-2L883B	— — —
8515507RA[1]	PAL16R6BM-2J883B	— — —
85155072C[1]	PAL16R6BM-2L883B	— — —
8515508RA[1]	PAL16R4BM-2J883B	— — —
85155082C[1]	PAL16R4BM-2L883B	— — —
PROM: 82008B1JA	53S3281MJ883B	M38510/21102BJX
82008B13C	53S3281ML883B	M38510/21102B3X
82008B2JA	53S3281AJ883B	— — —
82008B23C	53S3281AL883B	— — —

**Converting from "A" to "B" PAL in fourth quarter 1986.
[1]DESC Print 85155 to be released approx. 6/86

Group D—In-depth package related tests

- QCI is conducted every 26 weeks using devices which represent the same package construction and lead finish.
- Any device type in the same package type may be used regardless of the specific part number.
- Purpose: To monitor the reliability and integrity of various package materials and assembly processes.

Generic Data:

Monolithic Memories Generic Data Program is based on MIL-M-38510, which allows for shipments based on 26 weeks of coverage for Group C Testing and 36 weeks of coverage for Group D Testing.

Should circumstances arise where generic coverage to MIL-M-38510 is not possible, Monolithic Memories reserves the right to ship product based on 52 weeks of generic Group C and/or D coverage per MIL-M-883 Revision C.

Manufacturing and Screening Locations

JAN Products, Monolithic Memories Modified Level "S," and customer orders which call for U.S.A. assembly, are manufactured in our DESC certified assembly line in Sunnyvale, California.

Mil-Std-883 Class B products, and orders to source control drawings, where stateside build is not required, are assembled at our Penang, Malaysia facility. This facility is qualified by Monolithic Memories Quality Department, as well as by many of our customers, to manufacture Mil-Std-883 Class B product. Conformance to Mil-Std-883 requirements is routinely monitored through audits at the Penang facility, as well as incoming inspections in Sunnyvale. Manufacturing capabilities for each Monolithic Memories facility are highlighted on the chart below.

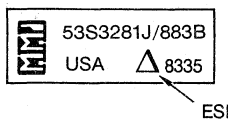
Manufacturing Capabilities

	Sunnyvale	Penang
Assembly	X	X
Precap Inspection	X	X
Environmental Testing	X	X
Electrical Pre-Test	X	X
Burn-In	X	X
Post Burn-In Electricals	X	X
Group A Testing	X	X
Mark	X	X
Factory Programming (when applicable)	X	
Qualification and Quality Conformance Testing	X	

To identify the assembly location of each military device, the Country of origin is marked on all products prior to shipment. Products assembled in our stateside facility in Sunnyvale, California, will have "USA" marked on the topside of the device. The exception to this is JAN 38510 product, which is marked to the Mil-M-38510 requirements only.

Offshore built product, which is manufactured in Penang, Malaysia, will have "Malaysia" or "Malay" marked on the bottom side of the device.

Marking Example:



Process Audits

Process Audits are performed in accordance with Mil-M-38510, Appendix A, paragraph 20.1.3.9, self audits by the Quality Assurance Department.

AC Testing

Although Monolithic Memories offers a large selection of programmable products, it must be pointed out that AC Testing cannot be performed on many of our product types without their being programmed. For those devices which must be programmed prior to AC Tests and are ordered unprogrammed, Monolithic Memories must "guarantee" their AC Performance.

Newer devices in the PROM/PLE and PAL families do allow preprogram AC testability at 25°C.

Since the **guaranteeing** of parameters can be a serious concern for the Military user, we have outlined several approaches to address the AC screening issue.

1. Monolithic Memories can pull a **Sample** from a lot using our own **Standard patterns** (designed to blow in excess of 50 percent of the fuses) and perform AC testing.
   a) PAL/PROM products processed to DESC prints include programmability samples and AC testing at 25°C.
   b) PROM/PLE AC testing can be performed at 25°C, −55°C, 125°C temperatures.
2. Monolithic Memories can program PROM/PLE's using custom patterns submitted by the customer. AC can then be done with the following options:
   a) Sample AC at 25°C
   b) Sample AC at 25°C, −55°C, 125°C
   c) 100% AC at 25°C
   d) 100% AC at 25°C, −55°C and 125°C

Note: For PALs contact the factory

On PAL products where custom programming is performed and AC testing is required, additional vector generation and fault coverage analysis is required, as well as AC program generation and checkout.

To give you an idea of delivery differences for the options discussed above, general lead times are as follows:

- Unprogrammed:
  Cerdip, 4–6 weeks
  Cerpack/Flat pack, 8–12 weeks
  Leadless chip carrier, 6–12 weeks
  (consult monthly leadtime guide for individual part types).
- Unprogrammed product using our standard pattern to verify AC at room temperature on sample basis (option 1). Add 2 weeks to standard delivery.
- Programmed product using customer programs with sample AC (option 2a and b). Contact factory for delivery. Delivery quoted will be after receipt of customer design package.
- 100% AC testing at 25°C—Standard Monolithic Memories pattern or customer pattern, (option c). Contact factory.

Remember, for ProPALs, customer must provide design package including Boolean Equations, "Seed" function test sequence, package stipulation and AC test vectors, when required. Delivery quotes for this type of product begin **after** receipt of this data from the customer.

VIL/VIH Parametric Information

V_{IL} and V_{IH} parameters are, in effect, input conditions of D.C. and Functional output tests and are not directly tested. V_{IL} is specified at ≤ 0.8 V, and V_{IH} is specified at ≥ 2.0 V.

ElectroStatic Discharge

The Military Products Division of Monolithic Memories has fully implemented static control procedures throughout its facilities in Penang, Malayasia and Sunnyvale, California.

All manufacturing areas where product is processed or handled, including our Reliability Labs, Engineering Labs, etc., have full static control such as wrist straps, antistatic smocks, grounded stainless steel tables, conductive mats and ion generators wherever necessary.

All product is moved throughout our facilities and shipped to customers in static shielded containers.

In addition, MPD distributors must demonstrate that they meet the same stringent standards governing ESD handling and control procedures as the factory. Individual distributor locations are audited and approved annually by MPD's Quality Assurance Department.

An ESD identifier is marked on all products in front of the date code, and all shipping containers are labeled with an ESD Caution Message. These procedures have been implemented, and will continually be reviewed, to ensure that our customers receive only the highest quality product from the Military Products Division.

Package Information

Leadless Chip Carrier/Pin Grid Array

Monolithic Memories' Military Products Division offers, with few exceptions, our entire product line in square, ceramic leadless chip carriers.

8-BIT INTERFACE
- 20 square LCC

PROM CIRCUITS (Programmable Read Only Memories)
- 20 square LCC
- 28 square LCC

PLE CIRCUITS (Programmable Logic Elements)
- 20 square LCC
- 28 square LCC

PAL/HAL* CIRCUITS (Programmable Array Logic)
- 20 square LCC
- 28 square LCC
- 44 square LCC

HMSI CIRCUITS (High-Complexity Medium Scale Integration)
- 28 square LCC

FIFO CIRCUITS (First-In-First-Out Memories)
- 20 square LCC

DOUBLE-DENSITY INTERFACE CIRCUITS
- 20 square LCC
- 28 square LCC

MULTIPLIER CIRCUITS
- 44 square LCC

*HALs are the mask-programmable versions of PAL.

Military Ordering Information

PAL/PROM/PLE Programming Inputs:

A. Two masters (programmed device) and checksum
B. Master and truthtable (or product terms for PAL)
C. Master and magnetic tape (VAX compatible)
D. Master and floppy disk (VAX compatible)
E. PALASM/PLEASM IBM compatible floppies, VAX compatible magnetic tape or floppies
F. Master only (least preferred)

NOTES:

If options A, B, C, D or E are submitted, Monolithic Memories may require customer approval of prototypes before proceeding with programming.

If option F is submitted, Monolithic Memories will require customer approval of factory generated prototypes before proceeding.

Military Ordering Information

Minimum Order Guidelines:

- Standard (unprogrammed/non-programmable) product
  Mil-Std-883, Class B
  DESC Print Devices
  JAN Devices
  Requires a $1000.00 ($250 per line item) per order
- Source Control Drawings (unprogrammed/non-programmable) product
  Requires a $1000.00 ($250 per line item) per order
- ProPAL32R16
  $5K per pattern
  500 units min per pattern
  200 units min per request date per pattern
- HAL20RA10 & 24RS Family
  $5K per pattern*
  2500 units min per pattern
  1000 units min per request date per pattern
- HAL20/24
  $3K per combinatorial pattern
  $4K per sequential pattern
  2500 units min per pattern
  1000 units min per request date per pattern

*Applicable to 20RA10 only. Assumes customers provide a set of test vectors, verifiable to 90% fault grading for all HAL devices.

Military Ordering Information

Cancellation Policy:

HAL (Mask Programmable Devices)

- 60 days firm.
- 90 days uncancellable.
- 61–90 days can be rescheduled once up to 60 days out.
- Any line item shortage of less than 5% can be rescheduled for next delivery date (or cancelled).

ProPAL/ProPROM/ProPLE (Programmed Devices)

- 30 days firm.
- 60 days uncancellable.
- 31–60 days can be rescheduled once up to 60 days out.
- Any line item shortage of less than 5% can be rescheduled for next delivery date (or cancelled).

Terms:

70%/30 Days, 30%/45 Days from date of invoice, F.O.B. Sunnyvale, California.

PAL®
Programmable Array Logic Circuits

PAL16L8B -4 M J 883B

FAMILY TYPE
- PAL = Programmable Array Logic
- HAL = Hard Array Logic

NUMBER OF ARRAY INPUTS

OUTPUT CELL
- A = Arithmetic
- C = Complementary
- H = Active High
- L = Active Low
- R = Registered
- RA = Registered Asynchronous
- RS = Registered Shared
- S = Shared
- X = Exclusive-OR

NUMBER OF OUTPUTS

SPEED
- Blank = Standard
- A = High Speed
- B = Very High Speed

POWER
- Blank = Standard
- -2 = 1/2 Power
- -4 = 1/4 Power

TEMPERATURE CODE
- M = Military

PACKAGE TYPE
- F = Ceramic Solder Seal Flat Pack
- J = Ceramic DIP
- JS = Ceramic SKINNYDIP
- L = Ceramic Leadless Chip Carrier
- W = Cerpack

PROCESSING
- 883B = Mil-Std-883 Class B

High Performance PROMs

53S328 1 A J 883B

TEMPERATURE CODE
- 5 = Military

PRODUCT
- 3 = Programmable

FAMILY
- S = Schottky
- RA = Registered Asynchronous
- RS = Registered Synchronous
- D = Diagnostic
- DA = Diagnostic Asynchronous

MEMORY SIZE
- 0 = 256 bits
- 1 = 1024 bits
- 2 = 2048 bits
- 4 = 4096 bits
- 8 = 8192 bits
- 16 = 16384 bits
- 32 = 32768 bits

NUMBER OF OUTPUTS
- 4 = 4 bits
- 8 = 8 bits

OUTPUT DESIGNATOR
- 0 = Open Collector
- 1 = Three State
- 3 = Two State

PERFORMANCE
- A = Enhanced
- None = Standard

PACKAGE TYPE
- JS = Ceramic SKINNYDIP
- J = Ceramic DIP
- F = Ceramic Solder Seal Flat Pack
- L = Ceramic Leadless Chip Carrier
- W = Cerpack

HI-REL SCREENING LEVEL
- 883B = Mil-Std-883 Class B

PLE™
Programmable Logic Element

PLE5P8 M J 883B

PREFIX
PROGRAMMABLE LOGIC ELEMENT

NUMBER OF INPUTS

OUTPUT TYPE
- P = Programmable Polarity
- RA = Registered Asynchronous
- RS = Registered Synchronous

NUMBER OF OUTPUTS

TEMPERATURE CODE
- M = Military

PACKAGE TYPE
- JS = Ceramic SKINNYDIP
- J = Ceramic DIP
- F = Ceramic Solder Seal Flat Pack
- L = Leadless Chip Carrier
- W = Cerpack

HI-REL SCREENING LEVEL
- 883B = Mil-Std-883 Class B

FIFO

C57401 A J 883B

- PREFIX
  - C = Cascadable
  - None = Standalone
- TEMPERATURE CODE
  - 57 = Military
- POWER
  - None = Standard Power
- UNIQUE THREE-DIGIT NUMBER
- PERFORMANCE
  - A = Enhanced
  - None = Standard
- PACKAGE TYPE
  - J = Ceramic DIP
  - L = Ceramic Leadless Chip Carrier
- HI-REL SCREENING LEVEL
  - 883B = Mil-Std-883 Class B

Power Strobe

HDI6600 -8 J

- PREFIX
- UNIQUE FOUR-DIGIT NUMBER
- PACKAGE TYPE
  - J = Ceramic DIP
- TEMPERATURE CODE SCREENING LEVEL
  - -2 = Military Temperature
  - -8 = Mil-Std-883, Class B

Bipolar Digital Logic

SN54S730 -1 J 883B

- PREFIX
- TEMPERATURE CODE
  - 54 = Military
- FAMILY TYPE
  - S = Schottky
  - LS = Low-Power Schottky
- UNIQUE THREE-DIGIT NUMBER
- -1 = Resistor Option
  - None = Standard
- PACKAGE TYPE
  - JS = Ceramic SKINNYDIP
  - J = Ceramic DIP
  - L = Ceramic Leadless Chip Carrier
  - W = Cerpack
- HI-REL SCREENING LEVEL
  - 883B = Mil-Std-883 Class B

DESC Drawing Numbering System

82008 B2 J X

- DRAWING NUMBER FOR PRODUCT OR FAMILY
- PROGRAMMING PROCEDURE/ DEVICE TYPE
- CASE OUTLINE (same as JAN 38510 Outlines)
- LEAD FINISH
  - A = Hot Solder DIP
  - C = Gold Plate
  - X = Any Lead Finish

JAN Part Numbering System

JM38510/ 503 01 B R A

- JAN DESIGNATOR
  - Parts cannot be marked with a "J" unless qualified and approved for listing on QPL
- GENERAL PROCUREMENT SPEC
- REFERS TO DETAIL SPEC
  - 206 = 4K PROM (1Kx4)
  - 209 = 8K PROM (2Kx4)
  - 503 = Programmable Array Logic
  - 504 = Programmable Array Logic
- DEFINES DEVICE TYPE
- PROCESSING LEVEL
  - Class B
- PACKAGE TYPE
  - R = 20 Lead 1/4x1-1/16 DIP
  - V = 18 Lead 1/4x15/16 DIP
  - 2 = 20 Lead 0.35x0.35 LCC
- LEAD FINISH
  - A = Hot Solder DIP
  - C = Gold Plate
  - X = Any Lead Finish

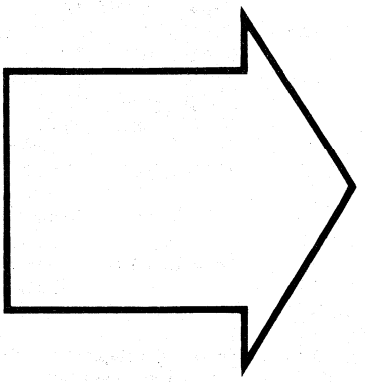


Table of Contents

PROM Performance Analysis
(Maximum Commercial Limits)

		MMI (TiW)		MMI (NiCr) (REFERENCE ONLY)		AMD		FUJITSU		HARRIS		NATIONAL		SIGNETICS		TI	
Type	Output	Part No.	TAA*/ICC	Part No.	TAA/ICC	Part No.	TAA*/ICC	Part No.	TAA*/ICC	Part No.	TAA/ICC	Part No.	TAA*/ICC	Part No.	TAA/ICC	Part No.	TAA/ICC
1/4K (32x8)	OC	63S080	25/125	6330-1	50/125	27S18	40/115	7111E	35/100	7602	50/130	74S188	35/110	82S23	50/96	18SA030	40/110
						27S18A	25/115	7111H	25/100					82S23A	25/96		
	TS	63S081	25/125	6331-1	50/125	27S19	40/115	7112E	35/100	7603	50/130	74S288	35/110	82S123	50/96	18S030	40/110
		63S081A	15/125			27S19A	25/115	7112H	25/100					82S123A	25/96		
								7112Y	20/100								
1K (256x4)	OC	63S140	45/130	6300-1	55/130	27S20	45/130	7113	30/100	7610	60/130	74S387	50/130	82S126	50/120	24SA10	65/100
						27S20A	30/130			7610A	45/110			82S126A	30/120		
										7610B	35/110						
	TS	63S141	45/130	6301-1	55/130	27S21	45/130	7114	30/100	7611	60/130	74S287	50/130	82S129	50/120	24S10	55/100
		63S141A	30/130			27S21A	30/130			7611A	45/110			82S129A	27/120		
										7611B	35/110						
2K (256x8)	OC	63S280	45/140	6308-1	70/155			7117E	45/140							28LA22	75/100
								7117H	35/140								
	TS	63S281	45/140	6309-1	70/155			7118E	45/140			74LS471	60/100	82S135	45/155	28L22	70/100
		63S281A	28/140					7118H	35/140								
2K (256x8) 24-Pin DIP	TS	63S285	45/160	6336-2	70/155												
2K (512x4)	OC	63S240	45/130	6305-1	60/130	27S12	50/130	7115E	45/120	7620	70/130	74S570	55/130	82S130	50/140		
						27S12A	30/130	7115H	35/120	7620A	50/120	74S570A	45/130	82S130A	33/140		
										7620B	40/120						
	TS	63S241	45/130	6306-1	60/130	27S13	50/130	7116E	45/120	7621	70/130	74S571	55/130	82S131	50/140		
		63S241A	35/130			27S13A	30/130	7116H	35/120	7621A	50/120	74S571A	45/130	82S131A	30/140		
								7116Y	30/120	7621B	40/120	74S571B	35/130				
4K (512x8)	OC	63S480	45/155	6348-1	70/155	27S28	55/160	7123E	45/170			74S473	60/155			28SA42	65/135
						27S28A	35/160	7123H	35/170			74S473A	45/155				
	TS	63S481	45/155	6349-1	70/155	27S29	55/160	7124E	45/170	7649	60/170	74S472	60/155	82S147	60/155	28L42	95/85
		63S481A	30/155	6349-2	55/155	27S29A	35/160	7124H	35/170	7649A	45/170	74S472A	45/155	82S147A	45/155	28S42	60/135
												74S472B	35/155				
4K (512x8) 24-Pin DIP	TS	63S485	45/160	6341-1	70/155	27S31	55/175			7641	70/170	74S474	65/170	82S141	60/175	28S46	60/135
				6341-2	55/155	27S31A	35/175			7641A	45/170	74S474A	45/170				
												74S474B	35/170				
4K (512x8) Registered	TS	63RA481	20/180			27S25	27/185	7226RA/RS-25	25/170			87SR25	27/185				
		63RA481A	15/180			27S25A	20/185	7226RA/RS-20	20/170			87SR25B	20/185				
4K (1Kx4)	OC	63S440	45/140	6352-1	60/175	27S32	55/140	7121E	45/150	7642	60/140	74S572	60/140			24SA41	60/140
						27S32A	35/140	7121H	35/150	7642A	50/140	74S572A	45/140				
										7642B	45/140						
	TS	63S441	45/140	6353-1	60/175	27S33	55/140	7122E	45/150	7643	60/140	74S573	60/140	82S137	60/140	24S41	60/140
		63S441A	35/140	6353-2	50/140	27S33A	35/140	7122H	35/150	7643A	50/140	74S573A	45/140	82S137A	45/140		
								7122Y	30/150	7643B	45/140	74S573B	35/140	82S137B	35/140		

PROM Performance Analysis
(Maximum Commercial Limits)

Type	Output	MMI (TiW) Part No.	MMI (TiW) TAA*/ICC	MMI (NiCr) (REFERENCE ONLY) Part No.	MMI (NiCr) (REFERENCE ONLY) TAA/ICC	AMD Part No.	AMD TAA*/ICC	FUJITSU Part No.	FUJITSU TAA*/ICC	HARRIS Part No.	HARRIS TAA/ICC	NATIONAL Part No.	NATIONAL TAA*/ICC	SIGNETICS Part No.	SIGNETICS TAA/ICC	TI Part No.	TI TAA/ICC
4K (1Kx4) Diagnostic	TS	63DA441 63DA442	18/180 18/180			27S65 27S65A	15/185 12/185										
8K (1Kx8) 600-mil DIP	TS	63S881 63S881A	45/160 30/160	6381-1 6381-2	90/175 55/170	27S181 27S181A	60/185 35/185	7132E 7132H 7132Y	55/175 45/175 35/175	7681 7681A	70/170 50/170	87S181 87S181A	55/170 45/170	82S181 82S181A 82S181B	70/175 55/175 45/175	28S86A	65/165
8K (1Kx8) 300-mil DIP	TS	63S881NS 63S881ANS	45/160 30/160	6381-1NS 6381-2NS	90/175 55/170	27S281 27S281A	60/185 35/185	7132E-SK 7132H-SK 7132Y-SK	55/175 45/175 35/175	6-7681 6-7681A	70/170 50/170	87S281	55/170	82S181N3 82S181AN3	70/175 55/175		
8K (1Kx8) Registered	TS	63RS881 63RS881A	20/180 15/180			27S35/37 27S35/37A	25/185 20/185	7232RA/RS-25 7232RA/RS-20	25/185 20/185			87SR181	20/175				
8K (2Kx4)	TS	63S841 63S841A	50/150 35/150	6389-1 6389-2	70/170 55/155	27S185 27S185A	50/150 35/150	7128E 7128H 7128Y	55/155 45/155 35/155	7685 7685A	70/170 50/170	87S185 87S185A 87S185B	55/140 45/140 35/140	82S185 82S185A 82S185B	100/120 50/155 45/155	24S81	70/175
8K (2Kx4) Diagnostic	TS	63DA841	20/185			27S75 27S75A	15/185 12/185										
16K (2Kx8) 600-mil DIP	TS	63S1681 63S1681A	50/185 35/185			27S191 27S191A	50/185 35/185	7138E 7138H 7138Y	55/180 45/180 35/180	76161 76161A	60/180 50/180	87S191 87S191A 87S191B	65/175 45/175 35/175	82S191 82S191A 82S191B	80/185 55/185 45/185	28S166	75/175
16K (2Kx8) 300-mil DIP	TS	63S1681NS 63S1681ANS	50/185 35/185			27S291 27S291A	50/185 35/185	7138E-SK 7138H-SK 7138Y-SK	55/180 45/180 35/180	6-76161 6-76161A	60/180 50/180	87S291	65/175	82S191BN3	45/185		
16K (2Kx8) Registered	TS	63RA/RS1681 63RA/RS1681A	20/185 15/185			27S45/47 27S45/47A	25/185 20/185										
16K (4Kx4)	TS	63S1641 63S1641A	50/175 35/175			27S41 27S41A	50/165 35/165	7152E 7152H 7152Y	55/170 45/170 35/170	76165	60/170	87S195A 87S195B	45/170 35/170	82HS195	45/155		
16K (4Kx4) Diagnostic	TS 2S	63D1641 63DA1643	20/190 20/190			27S85 27S85A	15/185 12/185										
32K (4Kx8)	TS	63S3281 63S3281A	45/190 35/190			27S43 27S43A	55/185 40/185	7142E 7142H	65/185 55/185	76321	65/190	87S321	55/185	82S321 82HS321	70/175 45/175		
64K (8Kx8)	TS	63S6481** 63S6481A	55/190 45/190			27S49 27S49A	55/190 40/190	7144E 7144H	65/190 55/190	76641	85/190						

*tCLK for Registered and Diagnostic PROMs
**Preliminary Information

High Performance 32x8 PROM TiW PROM Family

53/63S080 53/63S081 63S081A

Features/Benefits

- 15-ns maximum access time
- Reliable titanium-tungsten fuses (TiW) guarantee greater than 98% programming yields
- Low-voltage generic programming
- PNP inputs for low input current
- Open collector or three-state outputs.

Applications

- Programmable logic element (PLE™) 5 inputs, 8 outputs, 32 product terms
- Address decoder
- Priority encoder

Description

The 53/63S080, 53/63S081 and 63S081A feature low input current PNP inputs, full Schottky clamping and three-state and open collector outputs. The titanium-tungsten fuses store a logical low and are programmed to the high-state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

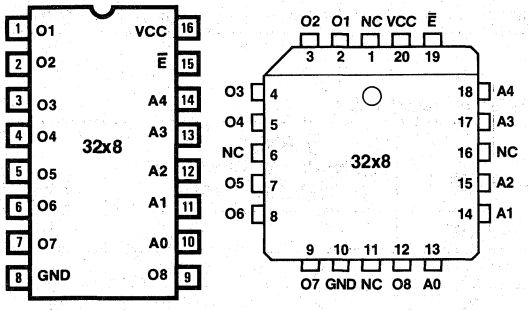
Programming

The 53/63S080, 53/63S081 and 63S081A are programmed with the same programming algorithm as all other Monolithic Memories' generic TiW PROMs. For details contact the factory.

Selection Guide

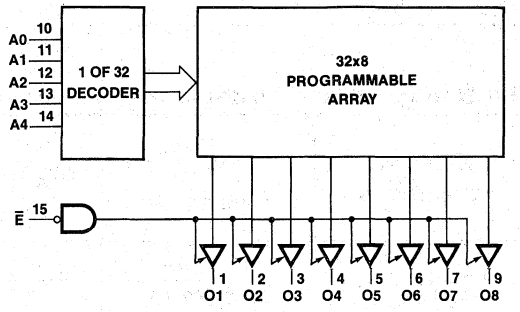
MEMORY			PACKAGE		PERFORMANCE	PART NUMBER	
SIZE	ORGANIZATION	OUTPUT	PINS	TYPE		0°C to +75°C	-55°C to +125°C
1/4 K	32x8	TS	16 (20)	N,J,W (NL),(L)	Enhanced	63S081A	—
		TS			Standard	63S081	53S081
		OC				63S080	53S080

Pin Configurations



Plastic Chip Carrier

Block Diagram



PLE™ is a trademark of Monolithic Memories.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories MMI

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	−0.5 V to 7 V	12 V
Input voltage	−1.5 V to 7 V	7 V
Input current	−30 mA to +5 mA	
Off-state output voltage	−0.5 V to 5.5 V	12 V
Storage temperature	−65 °C to +150 °C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA				−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V				−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16 mA	Com			0.45	V
				Mil			0.5	
V_{OH}	High-level output voltage*	V_{CC} = MIN	Com I_{OH} = −3.2 mA		2.4			V
			Mil I_{OH} = −2 mA					
I_{OZL}	Off-state output current*	V_{CC} = MAX	V_O = 0.4 V				−40	μA
I_{OZH}			V_O = 2.4 V				40	
I_{CEX}	Open collector output current	V_{CC} = MAX	V_O = 2.4 V				40	μA
			V_O = 5.5 V				100	
I_{OS}	Output short-circuit current**	V_{CC} = 5 V	V_O = 0 V		−20		−90	mA
I_{CC}	Supply current	V_{CC} = MAX. All inputs grounded. All outputs open.				90	125	mA

Switching Characteristics Over Operating Conditions (See standard test load)

OPERATING CONDITIONS	DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME TYP†	t_{AA} (ns) ADDRESS ACCESS TIME MAX	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME TYP†	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME MAX	UNIT
COMMERCIAL	63S081A	9	15	9	20	ns
	63S080, 63S081	9	25	9	20	
MILITARY	53S080, 53S081	9	35	9	30	

* Three-state only.

** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typicals at 5.0 V V_{CC} and 25°C T_A.

High Performance 256x4 PROM TiW PROM Family

53/63S140
53/63S141
53/63S141A

3

Features/Benefits

- 30-ns maximum access time
- Reliable titanium-tungsten fuses (TiW) guarantee greater than 98% programming yields
- Low-voltage generic programming
- PNP inputs for low input current
- Open collector or three-state outputs

Applications

- Microprogram control store
- Microprocessor program store
- Look-up table
- Character generator
- Code converter
- Programmable Logic Element (PLE™) with 8 inputs, 4 outputs, and 256 product terms

Description

The 53/63S140 and 53/63S141/A are 256x4 bipolar PROMs featuring low input current PNP inputs, full Schottky clamping, and open collector or three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

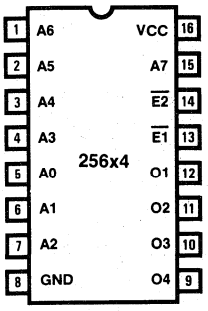
Programming

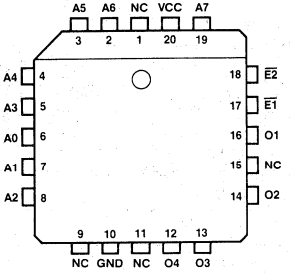
The 53/63S140 and 53/63S141/A PROMs are programmed with the same programming algorithm as all other Monolithic Memories' generic TiW PROMs. For details contact the factory.

Selection Guide

MEMORY			PACKAGE		PERFORMANCE	PART NUMBER	
SIZE	ORGANIZATION	OUTPUT	PINS	TYPE		0°C to +75°C	–55°C to +125°C
1 K	256x4	TS	16 (20)	N,J,W, (NL),(L)	Enhanced	63S141A	53S141A
		TS			Standard	63S141	53S141
		OC				63S140	53S140

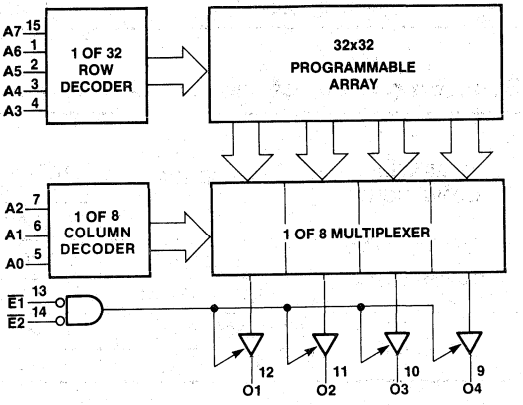
Pin Configurations





Plastic Chip Carrier

Block Diagram



PLE™ is a trademark of Monolithic Memories

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	−0.5 V to 7 V	12 V
Input voltage	−1.5 V to 7 V	7 V
Input current	−30 mA to +5 mA	
Off-state output voltage	−0.5 V to 5.5 V	12 V
Storage temperature	−65° to +150°C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA				−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V				−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16 mA	Com			0.45	V
				Mil			0.5	
V_{OH}	High-level output voltage*	V_{CC} = MIN	Com I_{OH} = −3.2 mA		2.4			V
			Mil I_{OH} = −2 mA					
I_{OZL}	Off-state output current*	V_{CC} = MAX	V_O = 0.4 V				−40	μA
I_{OZH}			V_O = 2.4 V				40	
I_{CEX}	Open collector output current	V_{CC} = MAX	V_O = 2.4 V				40	μA
			V_O = 5.5 V				100	
I_{OS}	Output short-circuit current**	V_{CC} = 5 V	V_O = 0 V		−20		−90	mA
I_{CC}	Supply current	V_{CC} = MAX. All inputs grounded. All outputs open.				80	130	mA

Switching Characteristics Over Operating Conditions (See standard test load)

OPERATING CONDITIONS	DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME TYP†	t_{AA} (ns) ADDRESS ACCESS TIME MAX	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME TYP†	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME MAX	UNIT
COMMERCIAL	63S141A	20	30	10	20	ns
	63S140, 63S141	20	45	10	25	
MILITARY	53S141A	20	40	10	30	
	53S140, 53S141	20	55	10	30	

* Three-state only.

** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typicals at 5.0 V V_{CC} and 25°C T_A.

High Performance 512x4 PROM Ti-W PROM Family

53/63S240 53/63S241 53/63S241A

Features/Benefits

- 35-ns maximum access time
- Reliable titanium-tungsten fuses (TiW) guarantee greater than 98% programming yields
- Low-voltage generic programming
- PNP inputs for low input current
- Open collector or three-state outputs

Applications

- Microprogram control store
- Microrocessor program store
- Look-up table
- Character generator
- Code converter
- Programmable logic element (PLE™) with 9 inputs, 4 outputs, 512 product terms

Description

The 53/63S240 and 53/63S241/A are 512x4 bipolar PROMs featuring low input current PNP inputs, full Schottky clamping, and open collector or three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high-state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

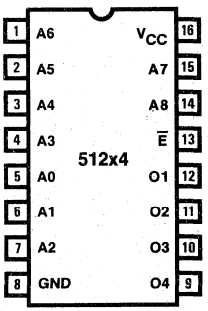
Programming

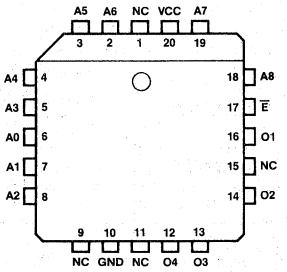
The 53/63S240 and 53/63S241/A PROMs are programmed with the same programming algorithm as all other Monolithic Memories generic Ti-W PROMs. For details contact the factory.

Selection Guide

MEMORY			PACKAGE		PERFORMANCE	PART NUMBER	
SIZE	ORGANIZATION	OUTPUT	PINS	TYPE		0°C to +75°C	−55°C to +125°C
2 K	512x4	TS	16 (20)	N,J,W, (NL),(L)	Enhanced	63S241A	53S241A
		TS			Standard	63S241	53S241
		OC				63S240	53S240

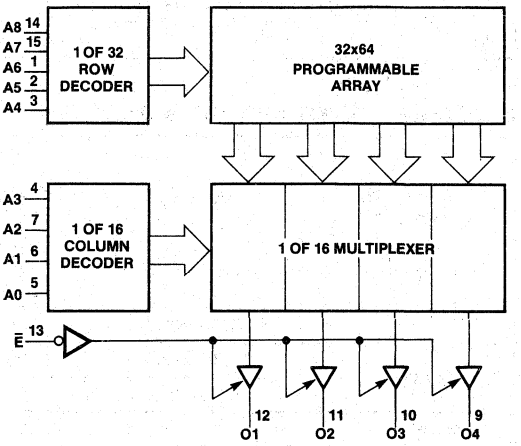
Pin Configurations





Plastic Chip Carrier

Block Diagram



PLE™ is a trademark of Monolithic Memories.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories MMI

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5 V to 7 V	12 V
Input voltage	-1.5 V to 7 V	7 V
Input current	-30 mA to +5 mA	
Off-state output voltage	-0.5 V to 5.5 V	12 V
Storage temperature	-65° to +150°C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	-55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA				-1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V				-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16 mA	Com			0.45	V
				Mil			0.5	
V_{OH}	High-level output voltage*	V_{CC} = MIN	Com I_{OH} = -3.2 mA		2.4			V
			Mil I_{OH} = -2 mA					
I_{OZL}	Off-state output current*	V_{CC} = MAX	V_O = 0.4 V				-40	μA
I_{OZH}			V_O = 2.4 V				40	
I_{CEX}	Open collector output current	V_{CC} = MAX	V_O = 2.4 V				40	μA
			V_O = 5.5 V				100	
I_{OS}	Output short-circuit current**	V_{CC} = 5 V	V_O = 0 V		-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX. All inputs grounded. All outputs open.				80	130	mA

Switching Characteristics Over Operating Conditions (See standard test load)

OPERATING CONDITIONS	DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME TYP†	t_{AA} (ns) ADDRESS ACCESS TIME MAX	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME TYP†	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME MAX	UNIT
COMMERCIAL	63S241A	25	35	12	20	ns
	63S240, 63S241	25	45	12	25	
MILITARY	53S241A	25	45	12	30	
	53S240, 53S241	25	55	12	30	

* Three-state only.

** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typicals at 5.0 V V_{CC} and 25° C T_A.

High Performance 256x8 PROM TiW PROM Family

53/63S280 53/63S281 53/63S281A

Features/Benefits

- 28-ns maximum access time
- Reliable titanium-tungsten fuses (TiW) guarantee greater than 98% programming yields
- Low-voltage generic programming
- PNP inputs for low input current
- Open collector or three-state outputs

Applications

- Microprogram control store
- Microprocessor program store
- Look-up table
- Character generator
- Code converter
- Programmable Logic Element (PLE™) with 8 inputs, 8 outputs, and 256 product terms

Description

The 53/63S280 and 53/63S281/A are 256x8 bipolar PROMs featuring low input current PNP inputs, full Schottky clamping, and open collector or three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

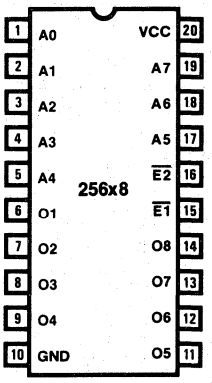
Programming

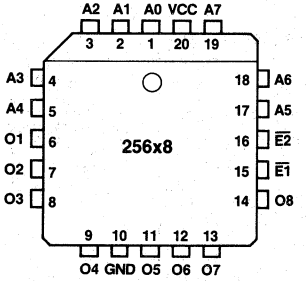
The 53/63S280 and 53/63S281/A PROMs are programmed with the same programming algorithm as all other Monolithic Memories' generic TiW PROMs. For details contact the factory.

Selection Guide

MEMORY			PACKAGE		PERFORMANCE	PART NIMBER	
SIZE	ORGANIZATION	OUTPUT	PINS	TYPE		0°C to +75°C	-55°C to +125°C
2 K	256x8	TS	20	N,J,W NL,L	Enhanced	63S281A	53S281A
		TS			Standard	63S281	53S281
		OC				63S280	53S288

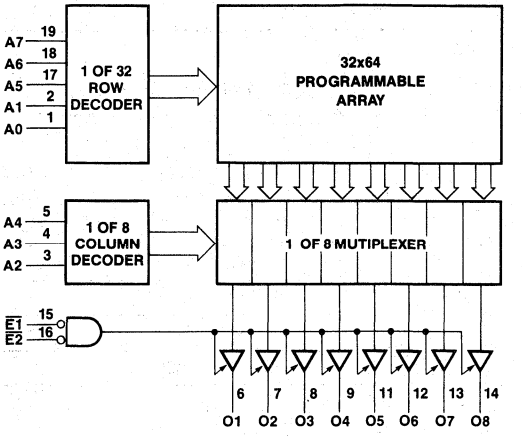
Pin Configurations





Plastic Chip Carrier

Block Diagram



PLE™ is a trademark of Monolithic Memories.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Monolithic Memories MMI

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5 V to 7 V	12 V
Input voltage	-1.5 V to 7 V	7 V
Input current	-30 mA to +5 mA	
Off-state output voltage	-0.5 V to 5.5 V	12 V
Storage temperature	-65° to +150°C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	-55		125	0		75	°C

DC Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA				-1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V				-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16 mA	Com			0.45	V
				Mil			0.5	
V_{OH}	High-level output voltage*	V_{CC} = MIN	Com I_{OH} = -3.2 mA		2.4			V
			Mil I_{OH} = -2 mA					
I_{OZL}	Off-state output current*	V_{CC} = MAX	V_O = 0.4 V				-40	μA
I_{OZH}			V_O = 2.4 V				40	
I_{CEX}	Open collector output current	V_{CC} = MAX	V_O = 2.4 V				40	μA
			V_O = 5.5 V				100	
I_{OS}	Output short-circuit current**	V_{CC} = 5 V	V_O = 0 V		-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX. All inputs grounded. All outputs open.				90	140	mA

Switching Characteristics Over Operating Conditions (See standard test load)

OPERATING CONDITIONS	DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME TYP†	t_{AA} (ns) ADDRESS ACCESS TIME MAX	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME TYP†	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME MAX	UNIT
COMMERCIAL	63S281A	21	28	18	25	ns
	63S280, 63S281	21	45	18	25	
MILITARY	53S281A	21	40	18	30	
	53S280, 53S281	21	50	18	30	

* Three-state only. ** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typicals at 5.0 V V_{CC} and 25° C T_A.

High Performance 256x8 PROM TiW PROM Family

63S285

3

Features/Benefits

- Replaces 24-pin 256x8 NiCr PROM (6336)
- Upward pinout-compatible with higher density PROMs
- 45-ns maximum access time
- Reliable titanium-tungsten fuses (TiW) guarantee greater than 99% programming yields
- Low voltage generic programming
- PNP inputs for low input current
- Three-state outputs with four enable pins

Applications

- Microprogram control store
- Microprocessor program store
- Look-up table
- Character generator
- Code converter

Description

The 63S285 is a 256x8 bipolar PROM featuring low-current PNP inputs, full Schottky clamping, and three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range.

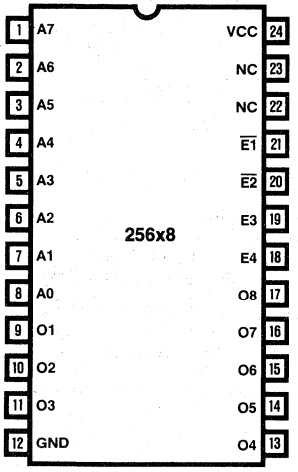
Programming

The 63S285 PROM is programmed with the same programming algorithm as all other Monolithic Memories generic TiW PROMs. For details contact the factory.

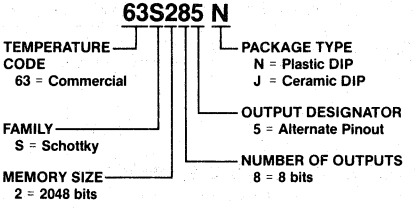
Selection Guide

MEMORY		PACKAGE		OUTPUT	PERFORMANCE	PART NUMBER
SIZE	ORGANIZATION	PINS	TYPE			0°C to +75°C
2K	256x8	24	N,J	TS	Standard	63S285

Pin Configuration



Part Numbering System



2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5 V to 7 V	12 V
Input voltage	-1.5 V to 7 V	7 V
Input current	-30 mA to +5 mA	
Off-state output voltage	-0.5 V to 5.5 V	12 V
Storage temperature	-65° to +150°C	

Operating Conditions

SYMBOL	PARAMETER	COMMERCIAL MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
T_A	Operating free-air temperature	0		75	°C

DC Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage	Guaranteed input logical low voltage for all inputs††				0.8	V
V_{IH}	High-level input voltage	Guaranteed input logical high voltage for all inputs††		2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA			-1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX			40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16 mA			0.45	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = -3.2 mA	2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4 V			-40	μA
I_{OZH}			V_O = 2.4 V			40	
I_{OS}	Output short-circuit current*	V_{CC} = 5 V	V_O = 0 V	-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX. All inputs grounded. All outputs open.			115	160	mA

Switching Characteristics Over Operating Conditions (See standard test load)

OPERATING CONDITIONS	DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME		t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME		UNIT
		TYP†	MAX	TYP†	MAX	
COMMERCIAL	63S285	26	45	18	30	ns

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typicals at 5.0 V V_{CC}, and 25°C T_A.

†† V_{IL} and V_{IH} limits are absolute values with respect to the device ground pin(s) and include all overshoots due to test equipment noise.

High Performance 1024x4 PROM TiW PROM Family

53/63S440 53/63S441 53/63S441A

Features/Benefits

- 35-ns maximum access time
- Reliable titanium-tungsten fuses (TiW) guarantee greater than 98% programming yields
- Low-voltage generic programming
- PNP inputs for low input current
- Open collector or three-state outputs

Applications

- Microprogram control stores
- Microprocessor program store
- Look-up table
- Character generator
- Code converter
- Programmable logic element (PLE™) 10 inputs, 4 outputs, 1024 product terms

Description

The 53/63S440 and 53/63S441/A are 1024x4 bipolar PROMs featuring low input current PNP inputs, full Schottky clamping with open collector or three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high-state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

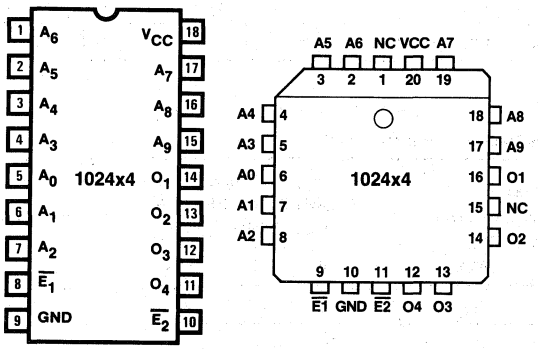
Programming

The 53/63S440 and 53/63S441/A PROMs are programmed with the same programming algorithm as all other Monolithic Memories' generic TiW PROMs. For details contact the factory.

Selection Guide

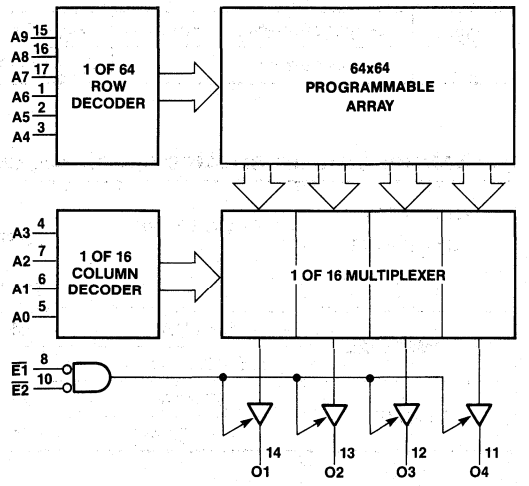
MEMORY			PACKAGE		PERFORMANCE	PART NUMBER	
SIZE	ORGANIZATION	OUTPUT	PINS	TYPE		0°C to +75°C	-55°C to +125°C
4 K	1024x4	TS	18 (20)	N,J,W, (NL),(L)	Enhanced	63S441A	53S441A
		TS			Standard	63S441	53S441
		OC				63S440	53S440

Pin Configuration



Plastic Chip Carrier

Block Diagram



2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Monolithic Memories

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5 V to 7 V	12 V
Input voltage	-1.5 V to 7 V	7 V
Input current	-30 mA to +5 mA	
Off-state output voltage	-0.5 V to 5.5 V	12 V
Storage temperature	-65° to +150°C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	-55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA				-1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V				-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16 mA	Com			0.45	V
				Mil			0.5	
V_{OH}	High-level output voltage*	V_{CC} = MIN	Com I_{OH} = -3.2 mA		2.4			V
			Mil I_{OH} = -2 mA					
I_{OZL}	Off-state output current*	V_{CC} = MAX	V_O = 0.4 V				-40	μA
I_{OZH}			V_O = 2.4 V				40	
I_{CEX}	Open collector output current	V_{CC} = MAX	V_O = 2.4 V				40	μA
			V_O = 5.5 V				100	
I_{OS}	Output short-circuit current**	V_{CC} = 5 V	V_O = 0 V		-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX. All inputs grounded. All outputs open.				95	140	mA

Switching Characteristics Over Operating Conditions (See standard test load)

OPERATING CONDITIONS	DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME TYP†	t_{AA} (ns) ADDRESS ACCESS TIME MAX	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME TYP†	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME MAX	UNIT
COMMERCIAL	63S441A	24	35	16	25	ns
	63S440, 63S441	24	45	16	25	
MILITARY	53S441A	24	50	16	30	
	53S440, 53S441	24	55	16	30	

* Three-state only.

** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typicals at 5.0 V V_{CC} and 25°C T_A.

High Performance 512x8 PROM TiW PROM Family

53/63S480
53/63S481
53/63S481A

Features/Benefits

- 30 ns maximum access time
- Reliable titanium-tungsten fuses (TiW) guarantee greater than 98% programming yields
- Low voltage generic programming
- PNP inputs for low input current
- Open collector or three-state outputs

Applications

- Microprogram control store
- Microprocessor program store
- Look-up table
- Character generator
- Code converter
- Programmable Logic Element (PLE™) with 9 inputs, 8 outputs, and 512 product terms

Description

The 53/63S480 and 53/63S481/A are 512x8 bipolar PROMs featuring low input current PNP inputs, full Schottky clamping, and open collector or three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

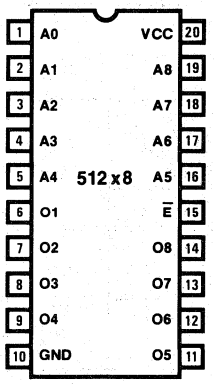
Programming

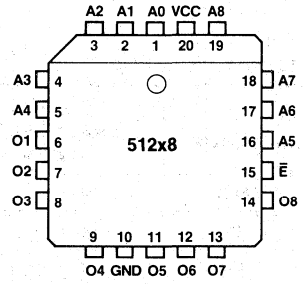
The 53/63S480 and 53/63S481/A PROMs are programmed with the same programming algorithm as all other Monolithic Memories' generic TiW PROMs. For details contact the factory.

Selection Guide

MEMORY			PACKAGE		PERFORMANCE	PART NUMBER	
SIZE	ORGANIZATION	OUTPUT	PINS	TYPE		0°C to +75°C	–55°C to +125°C
4 K	512x8	TS	20	N,J,F, NL,L	Enhanced	63S481A	53S481A
		TS			Standard	63S481	53S481
		OC				63S480	53S480

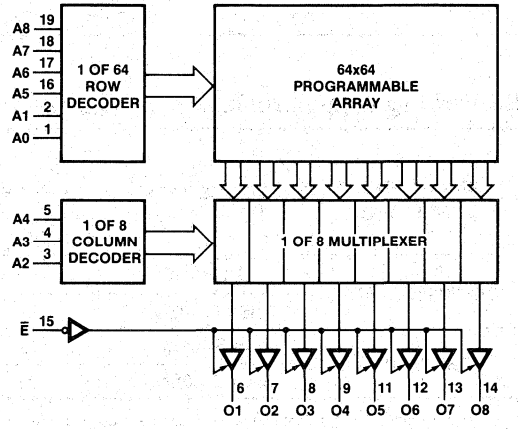
Pin Configurations





Plastic Chip Carrier

Block Diagram



PLE™ is a trademark of Monolithic Memories.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374

TWX: 910-338-2376

Monolithic Memories

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5 V to 7 V	12 V
Input voltage	-1.5 V to 7 V	7 V
Input current	-30 mA to +5 mA	
Off-state output voltage	-0.5 V to 5.5 V	12 V
Storage temperature	-65° to +150°C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	-55		125	0		75	°C

DC Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA				-1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V				-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16 mA	Com			0.45	V
				Mil			0.5	
V_{OH}	High-level output voltage*	V_{CC} = MIN	Com I_{OH} = -3.2 mA		2.4			V
			Mil I_{OH} = -2 mA					
I_{OZL}	Off-state output current*	V_{CC} = MAX	V_O = 0.4 V				-40	μA
I_{OZH}			V_O = 2.4 V				40	
I_{CEX}	Open collector output current	V_{CC} = MAX	V_O = 2.4 V				40	μA
			V_O = 5.5 V				100	
I_{OS}	Output short-circuit current**	V_{CC} = 5 V	V_O = 0 V		-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX. All inputs grounded. All outputs open.				104	155	mA

Switching Characteristics Over Operating Conditions (See standard test load)

OPERATING CONDITIONS	DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME TYP†	t_{AA} (ns) ADDRESS ACCESS TIME MAX	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME TYP†	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME MAX	UNIT
COMMERCIAL	63S481A	22	30	18	25	ns
	63S480, 63S481	22	45	18	25	
MILITARY	53S481A	22	40	18	30	
	53S480, 53S481	22	50	18	35	

* Three-state only. ** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typicals at 5.0 V V_{CC} and 25° C T_A.

High Performance 512x8 PROM TiW PROM Family

53/63S485

Features/Benefits

- Upward pinout-compatible with higher density PROMs
- 45-ns maximum access time
- Reliable titanium-tungsten fuses (TiW) guarantee greater than 99% programming yields
- Low-voltage generic programming
- PNP inputs for low input current
- Three-state outputs with four ANDed enable pins
- Saves space with 24-pin SKINNYDIP® package

Description

The 53S485 and 63S485 are 512x8 bipolar PROMs featuring low current PNP inputs, full Schottky clamping, and three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

Applications

- Microprogram control store
- Microprocessor program store
- Look-up table
- Character generator
- Code converter

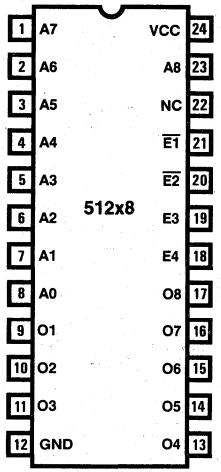
Programming

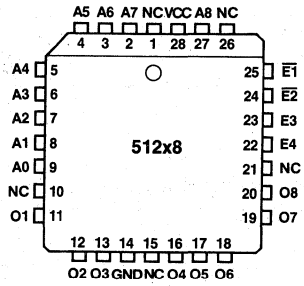
The 53S485 and 63S485 PROMs are programmed with the same programming algorithm as all other Monolithic Memories generic TiW PROMs. For details contact the factory.

Selection Guide

MEMORY		OUTPUT	PACKAGE		PERFORMANCE	PART NUMBER	
SIZE	ORGANIZATION		PINS	TYPE		0°C to +75°C	−55°C to +125°C
4K	512x8	TS	24 (28)	NS,JS,N,J,W, (NL),(L)	Standard	63S485	53S485

Pin Configurations





Plastic Chip Carrier

SKINNYDIP® is a registered trademark of Monolithic Memories.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Monolithic Memories

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	−0.5 V to 7 V	12 V
Input voltage	−1.5 V to 7 V	7 V
Input current	−30 mA to +5 mA	
Off-state output voltage	−0.5 V to 5.5 V	12 V
Storage temperature	−65°C to +150°C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

DC Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage	Guaranteed input logical low voltage for all inputs					0.8	V
V_{IH}	High-level input voltage	Guaranteed input logical high voltage for all inputs			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA				−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V				−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16 mA	Com			0.45	V
				Mil			0.5	
V_{OH}	High-level output voltage	V_{CC} = MIN	Com I_{OH} = −3.2 mA		2.4			V
			Mil I_{OH} = −2 mA					
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4 V				−40	μA
I_{OZH}			V_O = 2.4 V				40	
I_{OS}**	Output short-circuit current**	V_{CC} = 5 V	V_O = 0 V		−20		−90	mA
I_{CC}	Supply current	V_{CC} = MAX. All inputs grounded. All outputs open.				115	160	mA

Switching Characteristics Over Operating Conditions (See standard test load)

OPERATING CONDITIONS	DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME TYP†	t_{AA} (ns) ADDRESS ACCESS TIME MAX	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME TYP†	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME MAX	UNIT
COMMERCIAL	63S485	26	45	18	30	ns
MILITARY	53S485	26	55	18	35	

** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typical at 5.0 V V_{CC}, and 25°C T_A.

High Performance 2048x4 PROM TiW PROM Family

53/63S841
53/63S841A

3

Features/Benefits

- **35-ns maximum access time**
- **Reliable titanium-tungsten fuses (TiW) guarantee greater than 98% programming yields**
- **Low-voltage generic programming**
- **PNP inputs for low input current**

Applications

- **Microprogram control store**
- **Microprocessor program store**
- **Look-up table**
- **Character generator**
- **Code converter**
- **Programmable Logic Element (PLE™) with 11 inputs, 4 outputs and 2048 product terms per output**

Description

The 53/63S841 and 53/63S841A are 2048x4 bipolar PROMs featuring low input current PNP inputs, full Schottky clamping, and three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

Programming

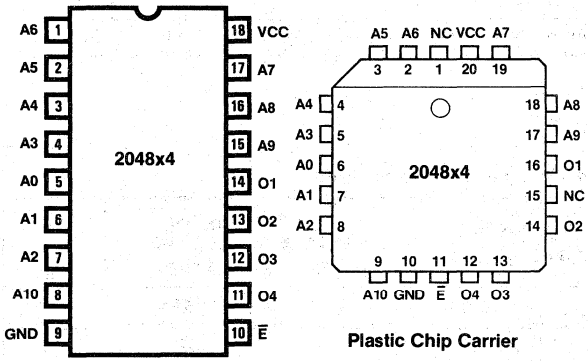
The 53/63S841 and 53/63S841A PROMs are programmed with the same programming algorithm as all other Monolithic Memories generic TiW PROMs. For details contact the factory.

Selection Guide

MEMORY			PACKAGE		PERFORMANCE	PART NUMBER	
SIZE	ORGANIZATION	OUTPUT	PINS	TYPE		0°C to +75°C	−55°C to +125°C
8 K	2048x4	TS	18 (20)*	N,J,W, (NL),(L)	Enhanced	63S841A	53S841A
					Standard	63S841	53S841

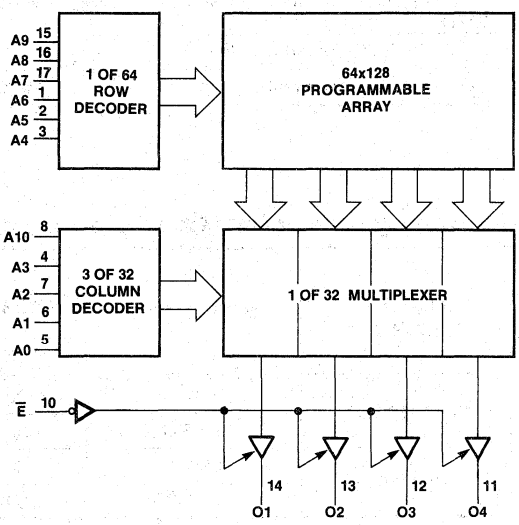
* Available in either a 20 or 28 terminal ceramic Leadless Chip Carrier.

Pin Configurations



Plastic Chip Carrier

Block Diagram



PLE™ is a trademark of Monolithic Memories.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5 V to 7 V	12 V
Input voltage	-1.5 V to 7 V	7 V
Input current	-30 mA to +5 mA	
Off-state output voltage	-0.5 V to 5.5 V	12 V
Storage temperature	-65° to +150°C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	-55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA				-1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V				-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16 mA	Com			0.45	V
				Mil			0.5	
V_{OH}	High-level output voltage	V_{CC} = MIN	Com I_{OH} = -3.2 mA		2.4			V
			Mil I_{OH} = -2 mA					
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4 V				-40	μA
I_{OZH}			V_O = 2.4 V				40	
I_{OS}	Output short-circuit current*	V_{CC} = 5 V	V_O = 0 V		-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX. All inputs grounded. All outputs open.				110	150	mA

Switching Characteristics Over Operating Conditions (See standard test load)

OPERATING CONDITIONS	DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME TYP†	t_{AA} (ns) ADDRESS ACCESS TIME MAX	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME TYP†	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME MAX	UNIT
COMMERCIAL	63S841A	30	35	12	25	ns
	63S841	30	50	12	25	
MILITARY	53S841A	30	50	12	30	
	53S841	30	55	12	30	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typicals at 5.0 V V_{CC} and 25°C T_A.

High Performance 1024x8 PROM TiW PROM Family

53/63S881 53/63S881A

3

Features/Benefits

- 30-ns maximum access time
- Reliable titanium-tungsten fuses (TiW) guarantee greater than 99% programming yields
- Low-voltage generic programming
- PNP inputs for low input current
- Three-state outputs
- 24-pin SKINNYDIP® or 600-mil DIP package

Applications

- Microprogram control stores
- Microprocessor program store
- Look-up table
- Character generator
- Code converter
- Programmable Logic Element (PLE™) with 10 inputs, 8 outputs and 1024 product terms

Description

The 53/63S881 and 53/63S881A are 1024x8 bipolar PROMs featuring low input current PNP inputs, full Schottky clamping, and three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

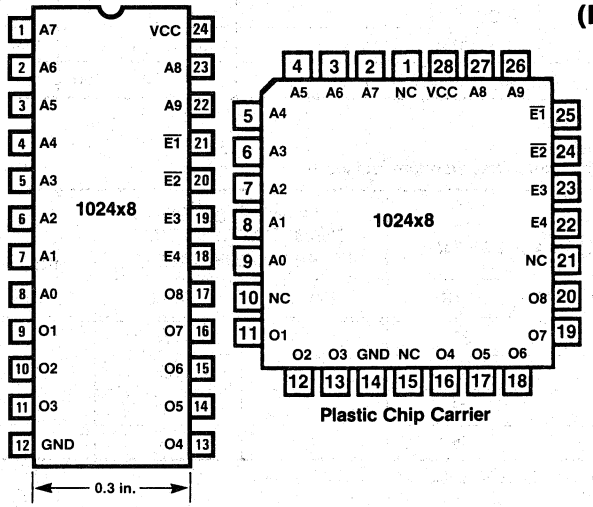
Programming

The 53/63S881 and 53/63S881A PROMs are programmed with the same programming algorithm as all other Monolithic Memories generic TiW PROMs. For details contact the factory.

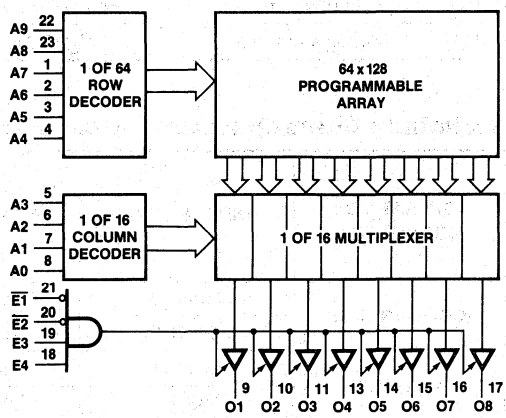
Selection Guide

MEMORY		OUTPUT	PACKAGE		PERFORMANCE	PART NUMBER	
SIZE	ORGANIZATION		PINS	TYPE		0°C to +75°C	–55°C to +125°C
8K	1024x8	TS	24 (28)	NS,JS,N,J,W, (NL),(L)	Enhanced	63S881A	53S881A
					Standard	63S881	53S881

Pin Configurations



Block Diagram (DIP Pinout)



SKINNYDIP® is a registered trademark of Monolithic Memories.
PLE™ is a trademark of Monolithic Memories.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Monolithic Memories MMI

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5 V to 7 V	12 V
Input voltage	-1.5 V to 7 V	7 V
Input current	-30 mA to +5 mA	
Off-state output voltage	-0.5 V to 5.5 V	12 V
Storage temperature	-65°C to +150°C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	-55		125	0		75	°C

DC Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage	Guaranteed input logical low voltage for all inputs					0.8	V
V_{IH}	High-level input voltage	Guaranteed input logical high voltage for all inputs			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA				-1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V				-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16 mA	Com			0.45	V
				Mil			0.5	
V_{OH}	High-level output voltage	V_{CC} = MIN	Com I_{OH} = -3.2 mA		2.4			V
			Mil I_{OH} = -2 mA					
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4 V				-40	μA
I_{OZH}			V_O = 2.4 V				40	
I_{OS}	Output short-circuit current*	V_{CC} = 5 V	V_O = 0 V		-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX. All inputs grounded. All outputs open.				92	160	mA

Switching Characteristics Over Operating Conditions (See standard test load)

OPERATING CONDITIONS	DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME TYP†	t_{AA} (ns) ADDRESS ACCESS TIME MAX	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME TYP†	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME MAX	UNIT
COMMERCIAL	63S881A	26	30	18	25	ns
	63S881	26	45	18	30	
MILITARY	53S881A	26	45	18	30	
	53S881	26	55	18	35	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typical at 5.0 V V_{CC}, and 25°C T_A.

High Performance 4096x4 PROM TiW PROM Family

53/63S1641 53/63S1641A

3

Features/Benefits

- 35-ns maximum access time
- Reliable titanium-tungsten fuses (TiW)
- Low-voltage generic programming
- PNP inputs for low input current

Applications

- Microprogram control stores
- Microprocessor program store
- Look-up table
- Character generator
- Code converter
- Programmable Logic Element (PLE™) 12 inputs, 4 outputs, 4096 product terms

Description

The 53/63S1641 features low input current PNP inputs, full Schottky clamping and three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide pre-programming testing which assures high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

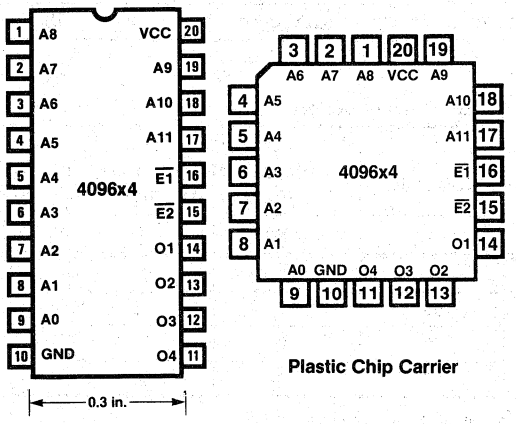
Programming

The 53/63S1641 PROM is programmed with the same programming algorithm as all other Monolithic Memories' generic TiW PROMs. For details contact the factory.

Selection Guide

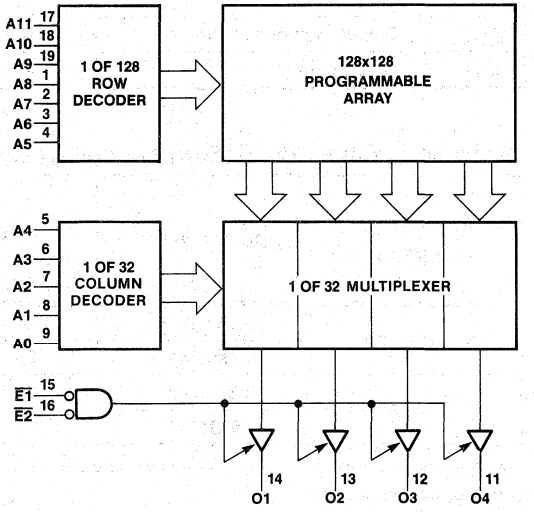
MEMORY			PACKAGE	PERFORMANCE	PART NUMBER	
SIZE	ORGANIZATION	OUTPUT			0°C to +75°C	−55°C to +125°C
16 K	4Kx4	TS	N,J, NL	Enhanced	63S1641A	53S1641A
				Standard	63S1641	53S1641

Pin Configuration



Plastic Chip Carrier

Block Diagram



PLE™ is a trademark of Monolithic Memories.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5V to 7V	12V
Input voltage	-1.5V to 7V	7V
Input current	-30mA to +5mA	
Off-state output voltage	-0.5V to 5.5V	12V
Storage temperature	-65°C to +150°C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	-55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA				-1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V				-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16 mA	Com			0.45	V
				Mil			0.5	
V_{OH}	High-level output voltage	V_{CC} = MIN	Com I_{OH} = -3.2 mA		2.4			V
			Mil I_{OH} = -2 mA					
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4 V				-40	μA
I_{OZH}			V_O = 2.4 V				40	
I_{OS}	Output short-circuit current*	V_{CC} = 5 V	V_O = 0 V		-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX. All inputs grounded. All outputs open.				130	175	mA

Switching Characteristics Over Operating Conditions (See standard test load)

OPERATING CONDITIONS	DEVICE TIME	t_{AA} (ns) ADDRESS ACCESS TIME TYP†	t_{AA} (ns) ADDRESS ACCESS TIME MAX	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME TYP†	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME MAX	UNIT
COMMERCIAL	63S1641A	28	35	12	25	ns
	63S1641	28	50	12	25	
MILITARY	53S1641A	28	50	12	30	
	53S1641	28	65	12	30	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typicals at 5.0 V V_{CC} and 25°C T_A.

High Performance 2048x8 PROM TiW PROM Family

53/63S1681
53/63S1681A

3

Features/Benefits

- **35-ns maximum access time**
- **16384-bit memory**
- **Reliable titanium-tungsten fuses (TiW)**
- **Available in space saving SKINNYDIP® package**

Applications

- **Microprogram control stores**
- **Microprocessor program store**
- **Look-up table**
- **Character generator**
- **Code converter**
- **Programmable Logic Element (PLE™) 11 inputs, 8 outputs, 2048 product terms**

Description

The 53/63S1681 is a high-speed 2Kx8 PROM which uses industry standard package and pin out. In addition, the device is available in the 24-pin (0.3 in.) SKINNYDIP®.

The family features low current PNP inputs, full Schottky clamping and three-state outputs. The Titanium-Tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide preprogramming tests which assure high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

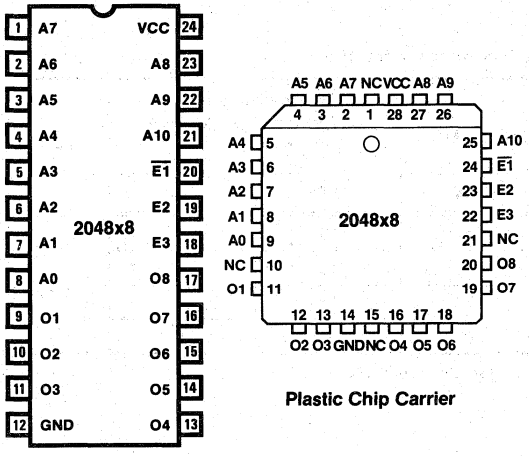
Programming

The 53/63S1681 PROM is programmed with the same programming algorithm as all other Monolithic Memories' generic TiW PROMs. For details contact the factory.

Selection Guide

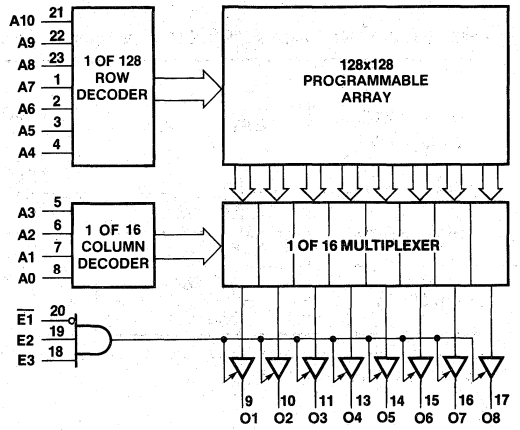
MEMORY		OUTPUT	PACKAGE		PERFORMANCE	PART NUMBER	
SIZE	ORGANIZATION		PINS	TYPE		0°C to +75°C	−55°C to +125°C
16K	2048x8	TS	24 (28)	N,NS,J,JS,W, (NL),(L)	Enhanced	63S1681A	53S1681A
					Standard	63S1681	53S1681

Pin Configurations



Plastic Chip Carrier

Block Diagram



2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374
Monolithic Memories MMI

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5 V to 7 V	12 V
Input voltage	-1.5 V to 7 V	7 V
Input current	-30 mA to +5 mA	
Off-state output voltage	-0.5 V to 5.5 V	12 V
Storage temperature	-65°C to +150°C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature	-55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA				-1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V				-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16 mA	Com			0.45	V
				Mil			0.5	
V_{OH}	High-level output voltage	V_{CC} = MIN	Com I_{OH} = -3.2 mA		2.4			V
			Mil I_{OH} = -2 mA					
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4 V				-40	μA
I_{OZH}			V_O = 2.4 V				40	
I_{OS}	Output short-circuit current*	V_{CC} = 5 V	V_O = 0 V		-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX. All inputs grounded. All outputs open.				135	185	mA

Switching Characteristics Over Operating Conditions (See standard test load)

OPERATING CONDITIONS	DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME TYP†	t_{AA} (ns) ADDRESS ACCESS TIME MAX	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME TYP†	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME MAX	UNIT
COMMERCIAL	63S1681A	27	35	18	25	ns
	63S1681	27	50	18	30	
MILITARY	53S1681A	27	50	18	30	
	53S1681	27	60	18	35	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typicals at 5.0 V V_{CC} and 25° C T_A.

High Performance 4096x8 PROM TiW PROM Family

53/63S3281 53/63S3281A

3

Features/Benefits

- 35-ns maximum access time
- 32768-bit memory
- Reliable titanium-tungsten fuses (TiW)
- PNP inputs for low input current

Applications

- Microprogram control stores
- Microprocessor program store
- Look-up table
- Character generator
- Code converter
- Programmable Logic Element (PLE™) with 12 inputs, 8 outputs and 4096 product terms

Description

The 53/63S3281 is a high-speed 4Kx8 PROM which uses industry standard pin out.

The family features low-current PNP inputs, full Schottky clamping and three-state outputs. The Titanium-Tungsten fuses store a logical low and are programmed to the high state.

Special on-chip circuitry and extra fuses provide preprogramming testing which assure high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

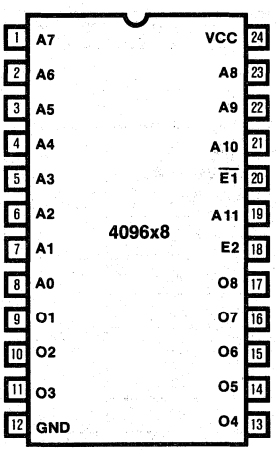
Programming

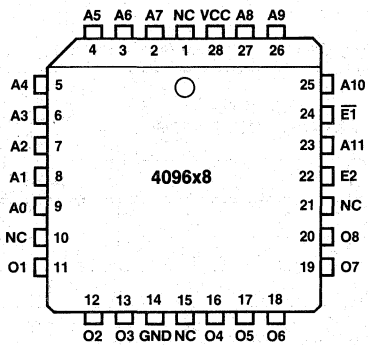
The 53/63S3281 PROM is programmed with the same programming algorithm as all other Monolithic Memories' generic TiW PROMs. For details contact the factory.

Selection Guide

MEMORY			PACKAGE		PERFORMANCE	PART NUMBER	
SIZE	ORGANIZATION	OUTPUT	PINS	TYPE		0°C to +75°C	−55°C to +125°C
32 K	4096x8	TS	24 (28)*	N,J,W, (NL),(L)	Enhanced	63S3281A	53S3281A
					Standard	63S3281	53S3281

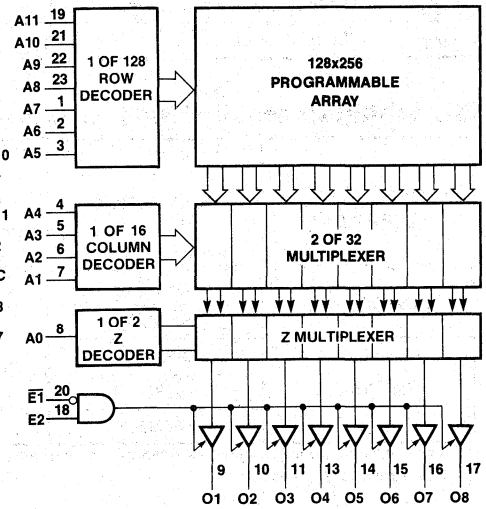
Pin Configurations





Plastic Chip Carrier

Block Diagram



PLE™ is a trademark of Monolithic Memories.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Monolithic Memories

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	−0.5 V to 7 V	12 V
Input voltage	−1.5 V to 7 V	7 V
Input current	−30 mA to +5 mA	
Off-state output voltage	−0.5 V to 5.5 V	12 V
Storage temperature	−65°C to +150°C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA				−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V				−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16 mA	Com			0.45	V
				Mil			0.5	
V_{OH}	High-level output voltage	V_{CC} = MIN	Com I_{OH} = −3.2 mA		2.4			V
			Mil I_{OH} = −2 mA					
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4 V				−40	μA
I_{OZH}			V_O = 2.4 V				40	
I_{OS}	Output short-circuit current*	V_{CC} = 5 V	V_O = 0 V		−20		−90	mA
I_{CC}	Supply current	V_{CC} = MAX. All inputs grounded. All outputs open.				150	190	mA

Switching Characteristics Over Operating Conditions (See standard test load)

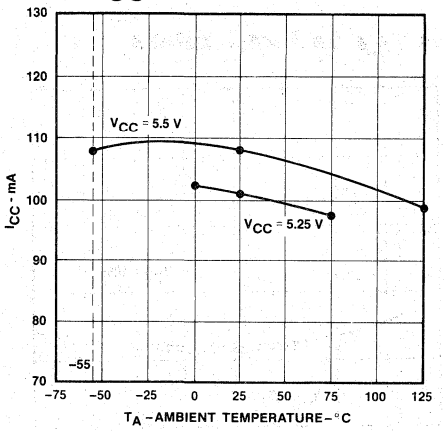
OPERATING CONDITIONS	DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME TYP†	t_{AA} (ns) ADDRESS ACCESS TIME MAX	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME TYP†	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME MAX	UNIT
COMMERCIAL	63S3281A	26	35	18	30	ns
	63S3281	26	45	18	30	
MILITARY	53S3281B	26	40	18	35	
	53S3281A	26	50	18	35	
	53S3281	26	60	18	35	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

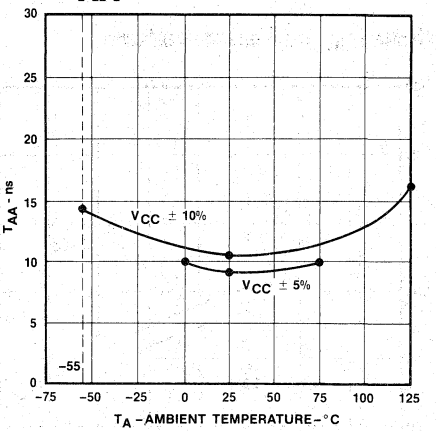
† Typicals at 5.0 V V_{CC} and 25° C T_A.

53/63S080 53/63S081 63S081A

Typical I_{CC} vs Temperature

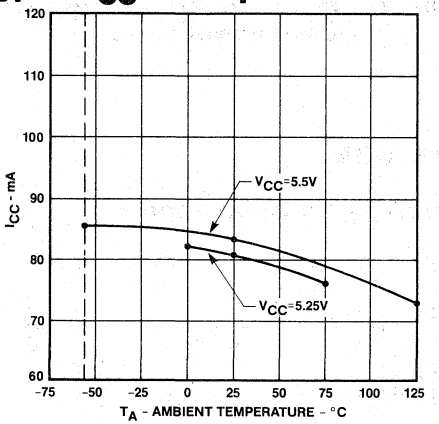


Typical T_{AA} vs Temperature

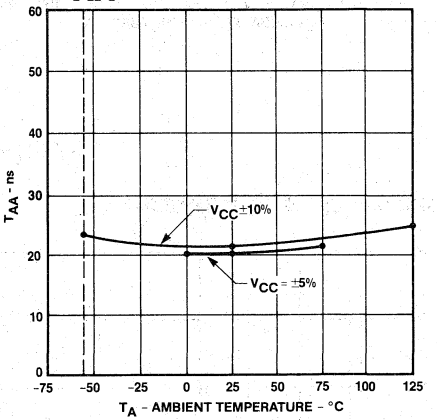


53/63S140 53/63S141/A

Typical I_{CC} vs Temperature

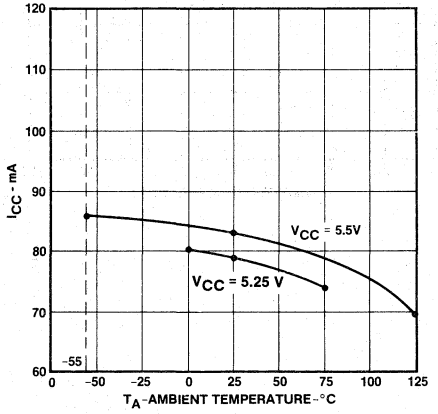


Typical T_{AA} vs Temperature

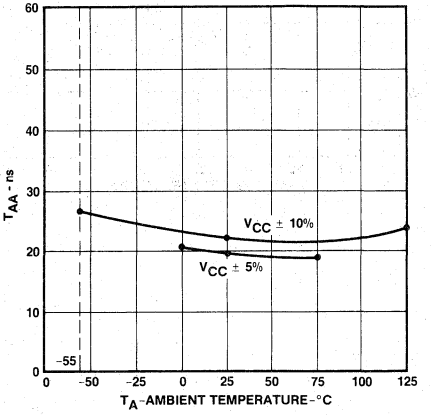


53/63S240 53/63S241/A

Typical I_{CC} vs Temperature

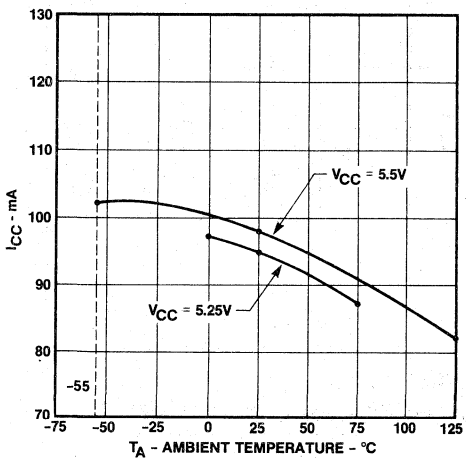


Typical T_{AA} vs Temperature

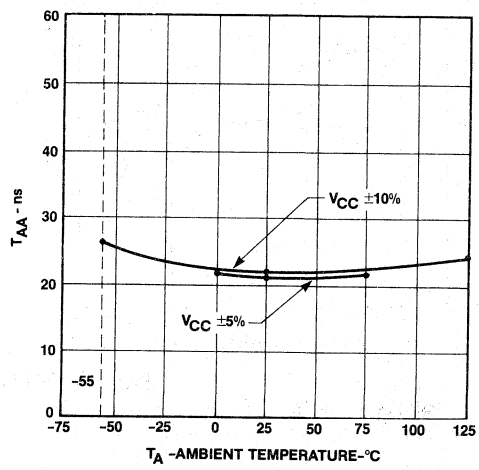


53/63S280 53/63S281/A

Typical I_{CC} vs Temperature

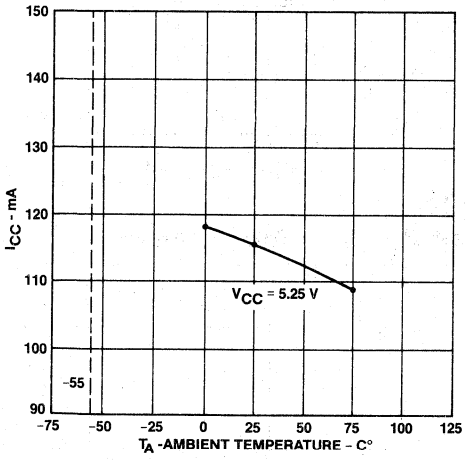


Typical T_{AA} vs Temperature

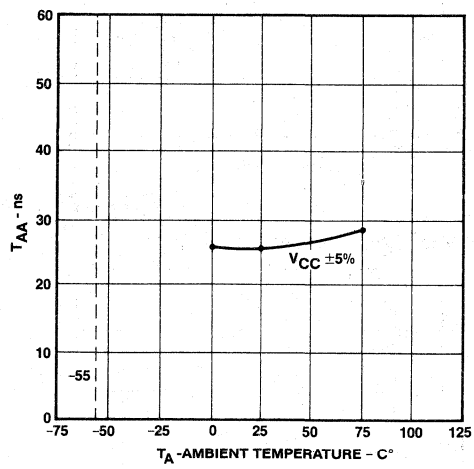


53/63S285 53/63S285A

Typical I_{CC} vs Temperature

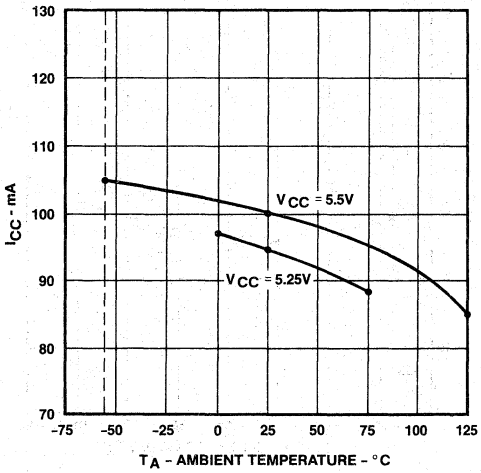


Typical T_{AA} vs Temperature

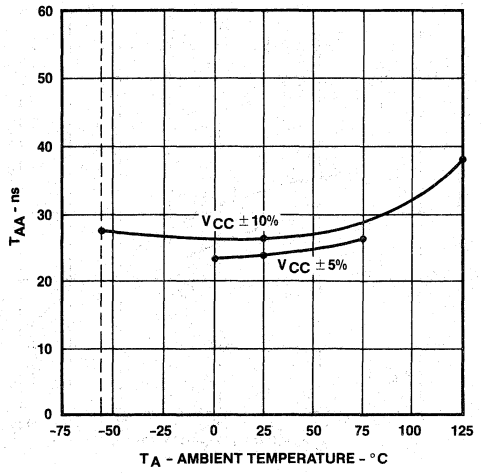


53/63S440 53/63S441A

Typical I_{CC} vs Temperature

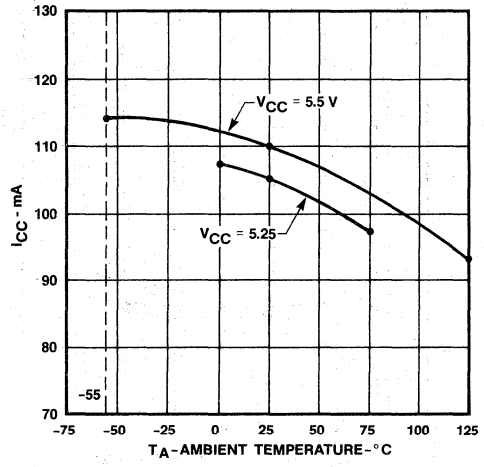


Typical T_{AA} vs Temperature

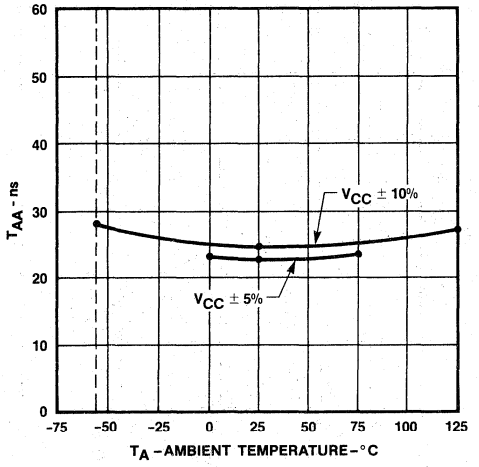


53/63S480 53/63S481A

Typical I_{CC} vs Temperature

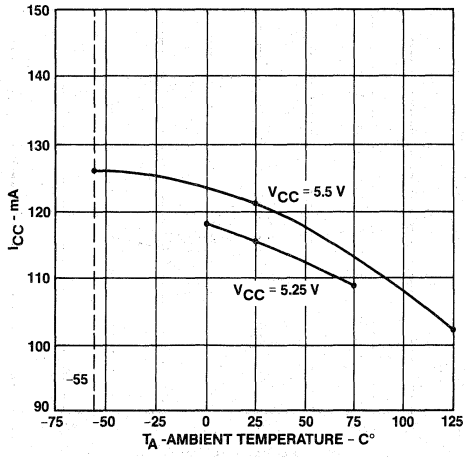


Typical T_{AA} vs Temperature

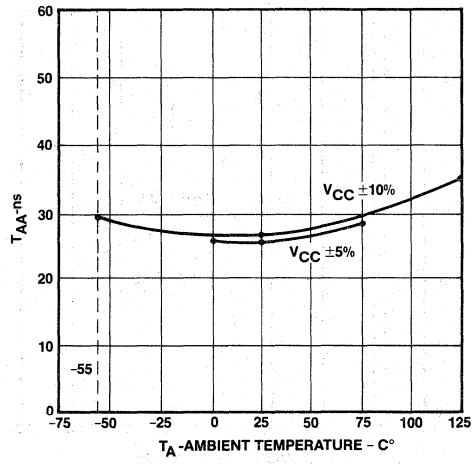


53/63S485 53/63S485A

Typical I_{CC} vs Temperature

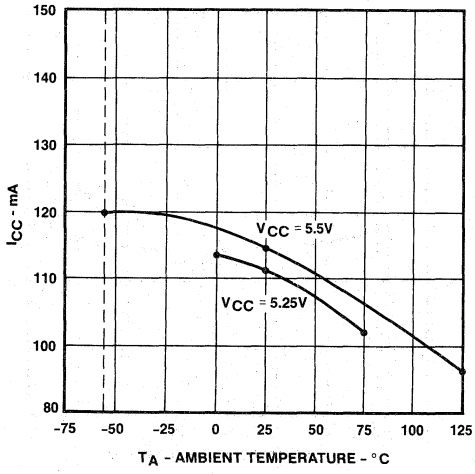


Typical T_{AA} vs Temperature

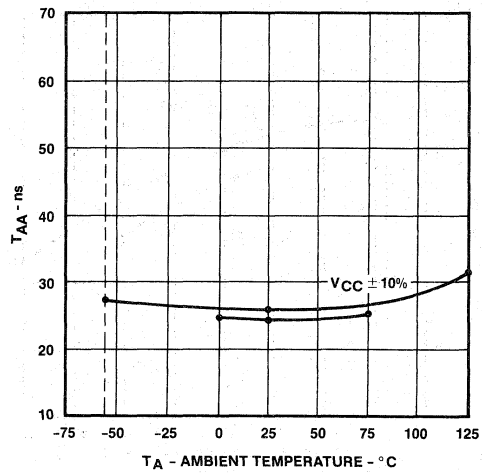


53/63S841 53/63S841A

Typical I_{CC} vs Temperature

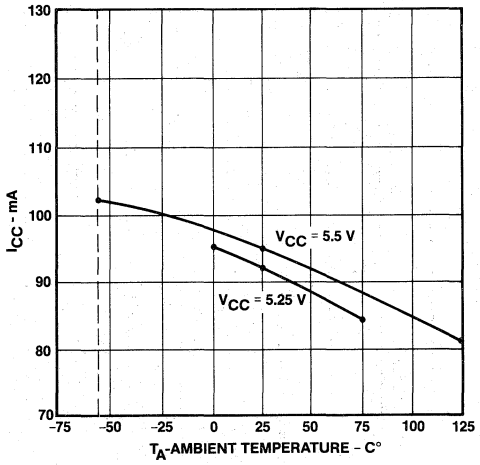


Typical T_{AA} vs Temperature

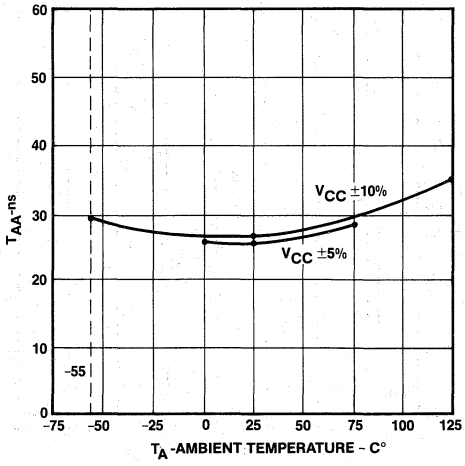


53/63S881 53/63S881A

Typical I_{CC} vs Temperature

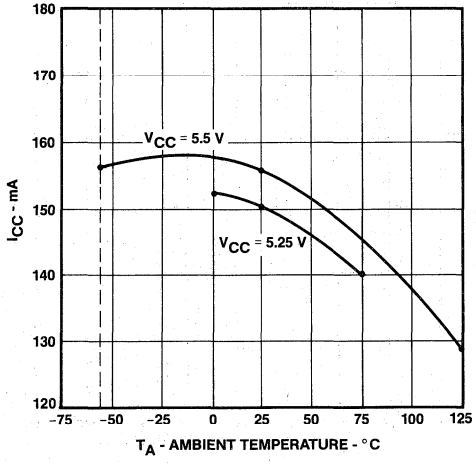


Typical T_{AA} vs Temperature

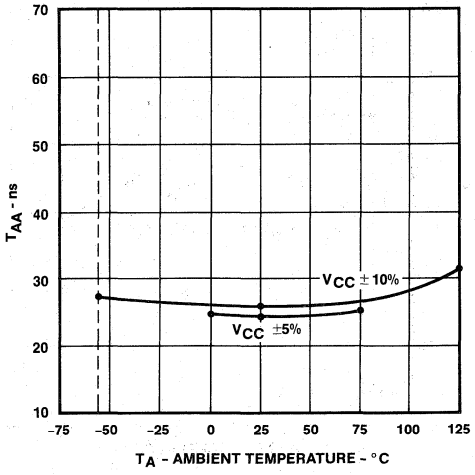


53/63S1641 53/63S1641A

Typical I_{CC} vs Temperature

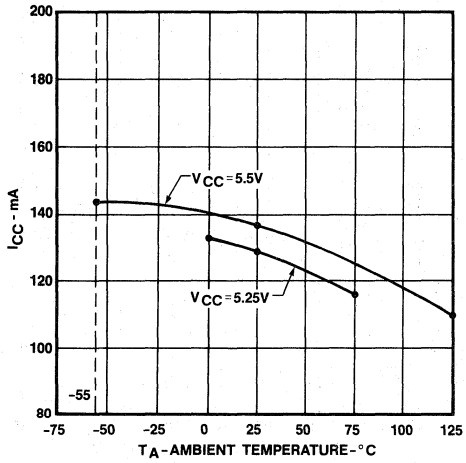


Typical T_{AA} vs Temperature

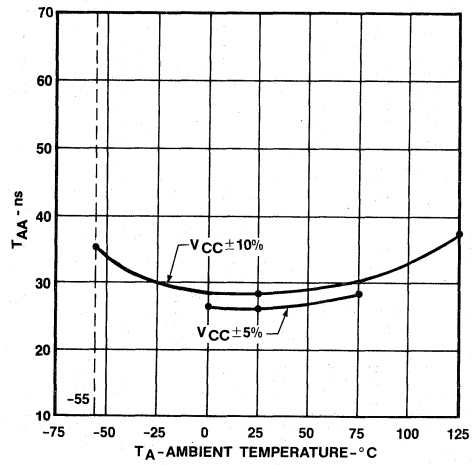


53/63S1681 53/63S1681A

Typical I_{CC} vs Temperature

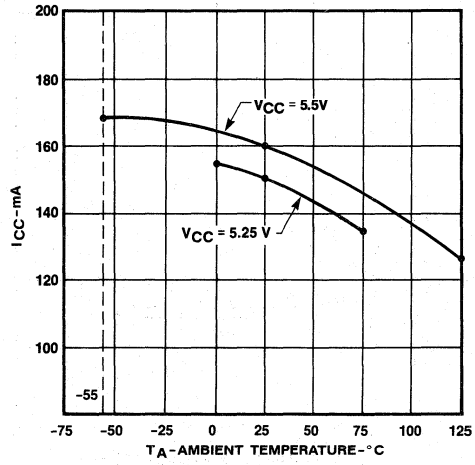


Typical T_{AA} vs Temperature

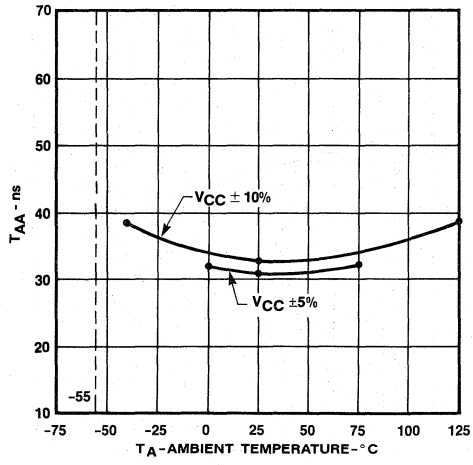


53/63S3281 53/63S3281A

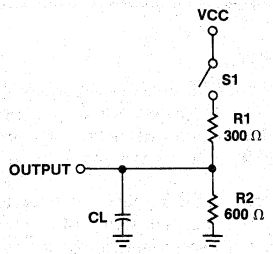
Typical I_{CC} vs Temperature



Typical T_{AA} vs Temperature



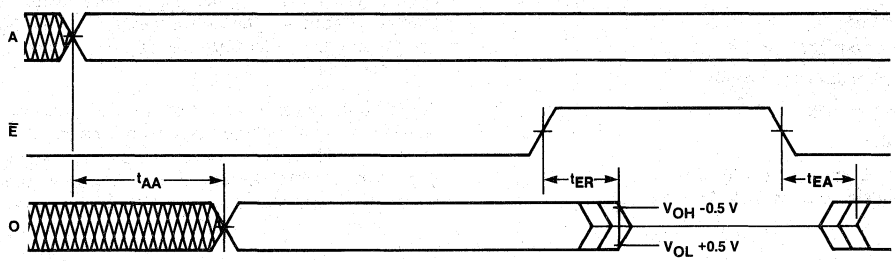
Switching Test Load



Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

Definition of Waveforms



Notes:
1. Input pulse amplitude 0 V to 3.0 V.
2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
3. Input access measured at the 1.5 V level.
4. t_{AA} is tested with switch S_1 closed. C_L = 30 pF and measured at 1.5 V output level.
5. For open collector devices, t_{EA} and t_{ER} are measured at the 1.5 V output level with S_1 closed and C_L = 30 pF. S_1 is open for high impedence to "1" test, and closed for high impedance to "0" test.
   t_{ER} is tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} -0.5 V output level; S_1 is closed for "0" to high impedance test measured at V_{OL} +0.5 V output level.

High Performance 512x8 Registered PROM

53/63RA481
53/63RA481A

Features/Benefits

- Versatile synchronous and asynchronous enables
- Asynchronous preset and clear
- Edge-triggered "D" registers
- 8-bit-wide in 24-pin SKINNYDIP® for high board density
- On-chip register simplifies system timing
- Faster cycle times
- 16 mA I_{OL} output drive capability
- Reliable titanium-tungsten fuses (Ti W), with programming yields typically greater than 98%

Applications

- Microprogram control store
- State sequencers/state machines
- Next address generation
- Mapping PROM
- Programmable Logic Element (PLE™)
  9 Inputs, 8 Registered Outputs, 512 product terms

Description

The 53/63RA481 and 53/63RA481A are 512x8 Registered PROMs with on-chip "D" type registers, versatile output enable control through synchronous and asynchronous three-state enable inputs, and asynchronous preset and clear.

Data is transferred into the output registers on the rising edge of the clock. The data will appear at the outputs provided that both the asynchronous ($\overline{E}$) and synchronous ($\overline{ES}$) enables are Low. Prior to the positive clock edge, register data are not affected by changes in addressing or synchronous enable inputs.

Memory expansion and data control is made more flexible with synchronous and asynchronous enable inputs. Outputs may be set to the high-impedance state at any time by setting $\overline{E}$ to a High or if $\overline{ES}$ is High when the rising clock edge occurs. When V_{CC} power is first applied, the synchronous enable flip-flop will be in the set condition causing the outputs to be in the high-impedance state.

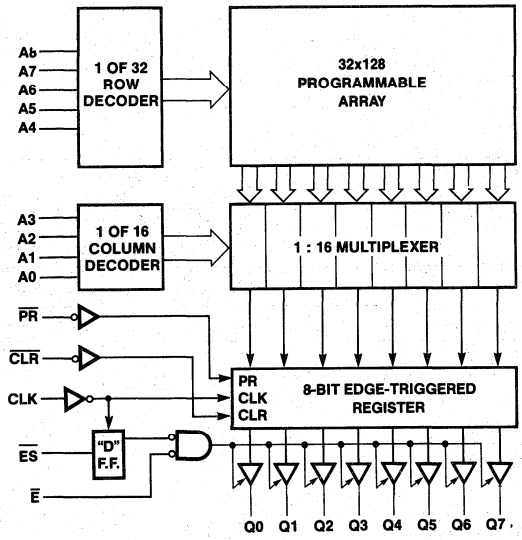
The output registers will be set to all Highs when preset is Low independent of the state of clock. The output registers will be reset to all Lows when clear is Low independent of the state of clock. Note that preset and clear are exclusive operations and cannot occur simultaneously.

Selection Guide

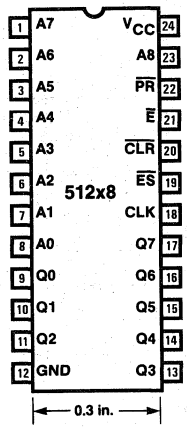
MEMORY		PACKAGE		PERFORMANCE	PART NUMBER	
SIZE	ORGANIZATION	PINS	TYPE		0°C to +75°C	-55°C to +125°C
4 K	512x8	24 (28)	NS,JS, W, (NL),(L)	Enhanced	63RA481A	53RA481A
				Standard	63RA481	53RA481

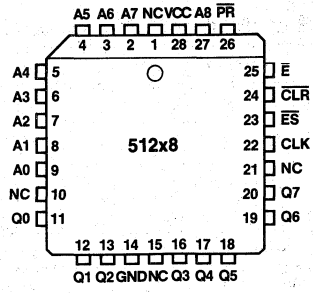
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Block Diagram



Pin Configurations





Plastic Chip Carrier

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5 V to 7 V	12 V
Input voltage	-1.5 V to 7 V	7 V
Input current	-30 mA to +5 mA	
Off-state output voltage	-0.5 V to 5.5 V	12 V
Storage temperature	-65°C to +150°C	

Operating Conditions

SYMBOL	PARAMETER	TYP†	COMMERCIAL				MILITARY				UNIT
			63RA481A		63RA481		53RA481A		53RA481		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	5.0	4.75	5.25	4.75	5.25	4.5	5.5	4.5	5.5	V
T_A	Operating free-air temperature	25	0	75	0	75	-55	125	-55	125	°C
t_w	Width of clock (High or Low)	10	20		20		20		20		ns
t_{prw} / t_{clrw}	Width of preset or clear (Low) to Output (High or Low)	10	20		20		20		20		ns
t_{prr} / t_{clrr}	Recovery from preset or clear (Low) to clock High	11	20		20		25		25		ns
t_s (A)	Setup time from address to clock	22	30		35		35		45		ns
t_s ($\overline{ES}$)	Setup time from $\overline{ES}$ to clock	7	10		10		15		15		ns
t_h (A)	Hold time from address to clock	-5	0		0		0		0		ns
t_h ($\overline{ES}$)	Hold time from $\overline{ES}$ to clock	-3	5		5		5		5		ns

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2.0			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA			-1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC}			40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16 mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	Com I_{OH} = -3.2 mA	2.4			V
			Mil I_{OH} = -2 mA				
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4 V			-40	μA
I_{OZH}			V_O = 2.4 V			40	
I_{OS}	Output short-circuit current*	V_{CC} = 5 V	V_O = 0 V	-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX.	All inputs TTL. All outputs open.		130	180	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typicals at 5.0 V V_{CC} and 25°C T_A.

Switching Characteristics Over Operating Conditions and using Standard Test Load

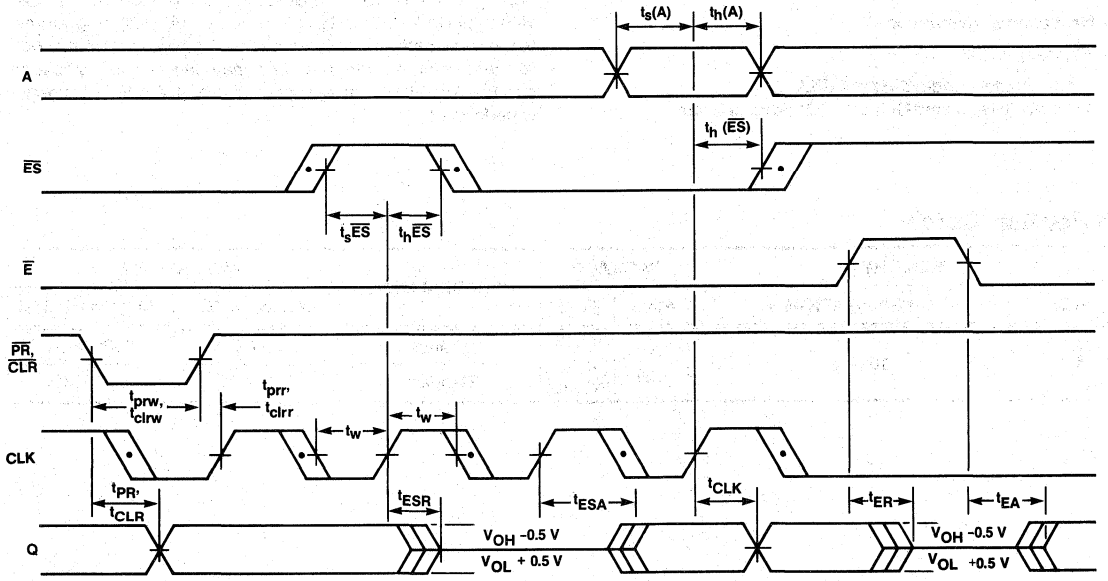
SYMBOL	PARAMETER	TYP†	COMMERCIAL		MILITARY		UNIT
			63RA481A	63RA481	53RA481A	53RA481	
			MIN MAX	MIN MAX	MIN MAX	MIN MAX	
t_{CLK}	Clock to output Delay	11	15	20	20	25	ns
t_{ESA}	Clock to output access time ($\overline{ES}$)	14	25	30	30	35	ns
t_{ESR}	Clock to output recovery time ($\overline{ES}$)	14	25	30	30	35	ns
t_{EA}	Enable to output access time ($\overline{E}$)	10	20	30	25	35	ns
t_{ER}	Disable to output recovery time ($\overline{E}$)	10	20	30	25	35	ns
t_{PR}	Preset to output delay ($\overline{PR}$)	15	25	25	25	30	ns
t_{CLR}	Clear to output delay ($\overline{CLR}$)	18	25	30	35	40	ns

† Typicals at 5.0 V V_{CC} and 25°C T_A.

Function Table

$\overline{E}$	$\overline{ES}$	CLK	$\overline{PR}$	$\overline{CLR}$	A8-A0	Q7-Q0	Operation
H	X	X	X	X	X	Z	High-Impedance
X	H	↑	X	X	X	Z	High-Impedance
L	L	X	L	H	X	H	Preset
L	L	X	H	L	X	L	Clear
L	L	X	L	L	X		Illegal Operation
L	L	↑	H	H	A	Data	Memory Access

Definition of Waveforms



Notes: 1. Input pulse amplitute 0 V to 3.0 V.

2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
3. Input access measured at the 1.5 V level.
4. Switch S_1 is closed. C_L = 30 pF and outputs measured at 1.5 V output level for all tests except t_{ESA} and t_{ESR}.
5. t_{EA} and t_{ESA} are measured at the 1.5 V output level with C_L = 30 pF. S_1 is open for high impedance to "1" test, and closed for high impedance to "0" test.

   t_{ER} and t_{ESR} are tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} -0.5 V output level; S_1 is closed for "0" to high impedance test measured at V_{OL} +0.5 V output level.

High Performance 1024x8 Registered PROM

53/63RS881 53/63RS881A

Features/Benefits

- Edge triggered "D" registers
- Synchronous and asynchronous enables
- Versatile 1:16 initialization words
- 8-Bit-wide in 24-pin SKINNYDIP® package for high board density
- Simplifies system timing
- Faster cycle times
- 16 mA I_{OL} output drive capability
- Reliable titanium-tungsten fuses (TiW), with programming yields typically greater than 98%

Applications

- Microprogram control store
- State sequencers
- Next address generation
- Mapping PROM
- Programmable Logic Element (PLE™) 10 Inputs, 8 Registered Outputs, 1024 product terms

Description

The 53/63RS881 and 53/63RS881A are 1Kx8 PROMs with on-chip "D" type registers, versatile output enable control through synchronous and asynchronous enable inputs, and flexible start up sequencing through programmable initialization.

Data is transferred into the output registers on the rising edge of the clock. Provided that the asynchronous ($\overline{E}$) and synchronous ($\overline{ES}$) enables are low, the data will appear at the outputs. Prior to the positive clock edge, register data are not affected by changes in addressing or synchronous enable inputs.

Memory expansion and data control is made flexible with synchronous and asynchronous enable inputs. Outputs may be set to the high impedance state at any time by setting $\overline{E}$ to a high or if $\overline{ES}$ is high when the rising clock edge occurs. When V_{CC} power is first applied the synchronous enable flip-flop will be in the set condition causing the outputs to be in the high impedance state.

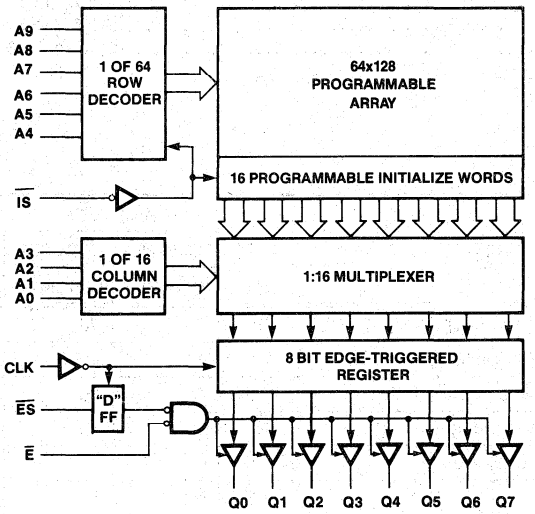
The flexible initialization feature allows start up and time out sequencing with 1:16 programmable words to be loaded into the output registers. With the synchronous INITIALIZE ($\overline{IS}$) pin low, one of the 16 column words (A3-A0) will be set in the output registers independent of the row addresses (A9-A4). The unprogrammed state of $\overline{IS}$ words are low, presenting a CLEAR with $\overline{IS}$ pin low. With all $\overline{IS}$ column words (A3-A0) programmed to the same pattern, the $\overline{IS}$ function will be independent of both row and column addressing and may be used as a single pin control. With all $\overline{IS}$ words programmed high a PRESET function is performed.

Selection Guide

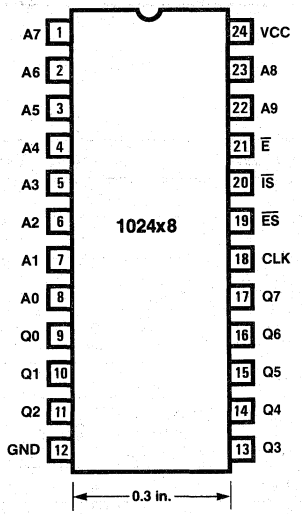
MEMORY		PACKAGE		PERFORMANCE	PART NUMBER	
SIZE	ORGANIZATION	PINS	TYPE		0°C to +75°C	-55°C to +125°C
8 K	1024x8	24 (28)	NS,JS, J,W, (NL),(L)	Enhanced	63RS881A	53RS881A
				Standard	63RS881	53RS881

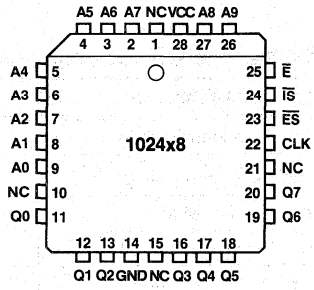
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374
Monolithic Memories

Block Diagram



Pin Configurations





Plastic Chip Carrier

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5 V to 7 V	12 V
Input voltage	-1.5 V to 7 V	7 V
Input current	-30 mA to +5 mA	
Off-state output voltage	-0.5 V to 5.5 V	12 V
Storage temperature	-65°C to +150°C	

Operating Conditions

SYMBOL	PARAMETER	TYP†	MILITARY		COMMERCIAL		UNIT
			53RS881A	53RS881	63RS881A	63RS881	
			MIN MAX	MIN MAX	MIN MAX	MIN MAX	
t_w	Width of clock (high or low)	10	20	20	20	20	ns
$t_{s(A)}$	Setup time from address to clock	25	40	45	30	35	ns
$t_{s(\overline{ES})}$	Setup time from $\overline{ES}$ to clock	8	15	15	15	15	ns
$t_{s(\overline{IS})}$	Setup time from $\overline{IS}$ to clock	20	30	35	25	30	ns
$t_{h(A)}$	Hold time address to clock	-5	0	0	0	0	ns
$t_{h(\overline{ES})}$	Hold time ($\overline{ES}$)	-3	5	5	5	5	ns
$t_{h(\overline{IS})}$	Hold time ($\overline{IS}$)	-5	0	0	0	0	ns
V_{CC}	Supply voltage	5	4.5 5.5	4.5 5.5	4.75 5.25	4.75 5.25	V
T_A	Operating free-air temperature	25	-55 125	-55 125	0 75	0 75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2.0			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA			-1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX			40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16 mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	Com I_{OH} = -3.2 mA	2.4			V
			Mil I_{OH} = -2 mA				
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4 V			-40	μA
I_{OZH}			V_O = 2.4 V			40	
I_{OS}	Output short-circuit current*	V_{CC} = 5 V	V_O = 0 V	-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX. All inputs TTL. All outputs open.			130	180	mA

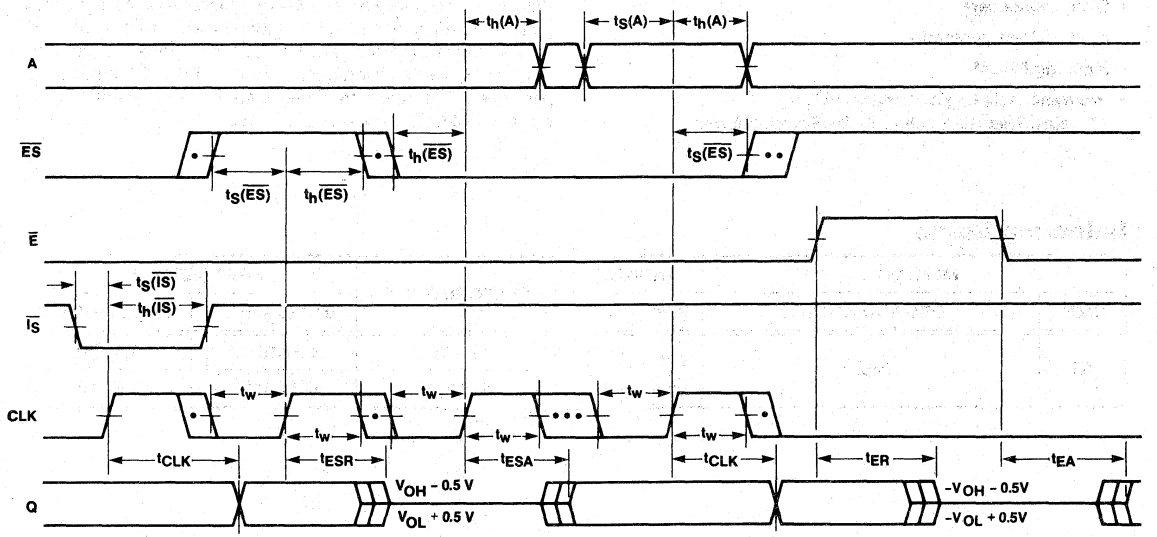
* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typicals at 5.0 V V_{CC} and 25°C T_A.

Switching Characteristics Over Operating Conditions and using Standard Test Load

SYMBOL	PARAMETER	TYP	MILITARY				COMMERCIAL				UNIT
			53RS881A		53RS881		63RS881A		63RS881		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CLK}	Clock to output Delay	10		20		25		15		20	ns
t_{ESA}	Clock to output access time ($\overline{ES}$)	18		30		35		25		30	ns
t_{ESR}	Clock to output recovery time ($\overline{ES}$)	17		30		35		25		30	ns
t_{EA}	Enable to output access time ($\overline{E}$)	18		30		35		25		30	ns
t_{ER}	Disable to output recovery time ($\overline{E}$)	17		30		35		25		30	ns

Definition of Waveforms



NOTES: 1. Input pulse amplitude 0 V to 3.0 V.

2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
3. Input access measured at the 1.5 V level.
4. t_{AA} is tested with switch S_1 closed. C_L = 30 pF and measured at 1.5 V output level.
5. t_{EA} and t_{ESA} are measured at the 1.5 V output level with C_L = 30 pF. S_1 is open for high impedance to "1" test and closed for high impedance to "0" test.

   t_{ER} and t_{EA} are measured. C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} -0.5 V output level; S_1 is closed for "0" to high impedance test measured at V_{OL} + 0.5 V output level.

2048x8 Registered PROM with Asynchronous Enable

53/63RA1681 53/63RA1681A

Features/Benefits

- Synchronous output enable
- Edge-triggered "D" registers
- Versatile 1:16 user programmable initialization words
- 8-bit-wide in 24-pin SKINNYDIP® for high board density
- Simplifies system timing
- Faster cycle times
- 16 mA I_{OL} output drive capability
- Reliable titanium-tungsten fuses (TiW), with programming yields typically greater than 98%

Applications

- Microprogram control store
- State sequencers
- Next address generation
- Mapping PROM
- Programmable Logic Element (PLE™)
  11 Inputs, 8 Registered Outputs, 2048 product terms

Description

The 53/63RA1681 and 53/63RA1681A are 2Kx8 PROMs with on-chip "D"-type registers. Output enable control through an asynchronous enable input and flexible start up sequencing through programmable initialization words.

Data is transferred into the output registers on the rising edge of the clock. Provided that the asynchronous enable ($\overline{E}$) is low, the data will appear at the outputs. Prior to the positive clock edge, register data are not affected by changes in addressing.

Memory expansion and data control is made flexible with asynchronous enable inputs. Outputs may be set to the high impedance state at any time by setting $\overline{E}$ to a HIGH.

The flexible initialization feature allows start up and time out sequencing with 1:16 programmable words to be loaded into the output registers. With the synchronous INITIALIZE ($\overline{IS}$) pin LOW, one of the 16 column words (A3-A0) will be set in the output registers independent of the row addresses (A9-A4). With all $\overline{IS}$ column words (A3-A0) programmed to the same pattern, the $\overline{IS}$ function will be independent of both row and column addressing and may be used as a single pin control. With all $\overline{IS}$ words programmed HIGH a PRESET function is performed. The unprogrammed state of $\overline{IS}$ words are LOW, presenting a CLEAR with $\overline{IS}$ pin LOW.

Selection Guide

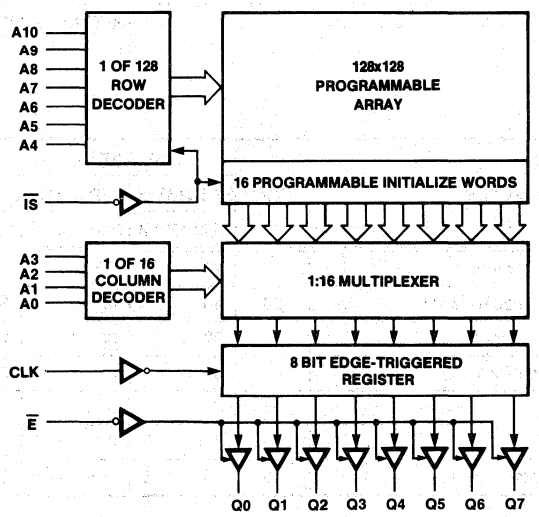
MEMORY		PACKAGE		PERFORMANCE	PART NUMBER	
SIZE	ORGANIZATION	PINS	TYPE		0°C to +75°C	-55°C to +125°C
16 K	2048x8	24 (28)	NS,JS, W, (NL),(L)	Enhanced	63RA1681A	53RA1681A
				Standard	63RA1681	53RA1681

SKINNYDIP® is a registered trademark of Monolithic Memories.
PLE™ is a trademark of Monolithic Memories.

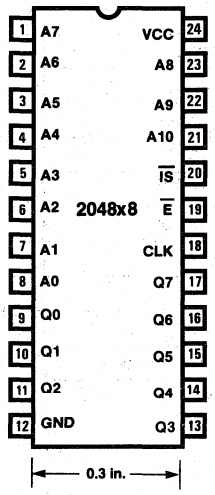
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

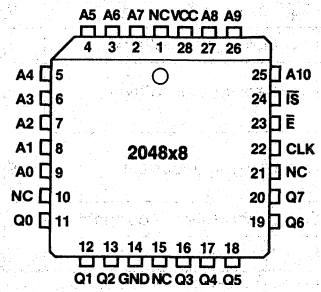
Monolithic Memories

Block Diagram



Pin Configurations





Plastic Chip Carrier

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	−0.5 V to 7 V	12 V
Input voltage	−1.5 V to 7 V	7 V
Input current	−30 mA to +5 mA	
Off-state output voltage	−0.5 V to 5.5 V	12 V
Storage temperature	−65°C to +150°C	

Operating Conditions

SYMBOL	PARAMETER	TYP†	MILITARY				COMMERCIAL				UNIT
			53RA1681A		53RA1681		63RA1681A		63RA1681		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Width of clock (high or low)	10	20		20		20		20		ns
$t_{s(A)}$	Setup time from address to clock	28	40		45		35		40		ns
$t_{s(\overline{IS})}$	Setup time from $\overline{IS}$ to clock	20	30		35		25		30		ns
$t_{h(A)}$	Hold time address to clock	−5	0		0		0		0		ns
$t_{h(\overline{IS})}$	Hold time ($\overline{IS}$)	−5	0		0		0		0		ns
V_{CC}	Supply voltage	5	4.5	5.5	4.5	5.5	4.75	5.25	4.75	5.25	V
T_A	Operating free-air temperature	25	−55	125	−55	125	0	75	0	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2.0			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA			−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX			40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16 mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	Com I_{OH} = −3.2 mA	2.4			V
			Mil I_{OH} = −2 mA				
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4 V			−40	μA
I_{OZH}			V_O = 2.4 V			40	
I_{OS}	Output short-circuit current*	V_{CC} = 5 V	V_O = 0 V	−20		−90	mA
I_{CC}	Supply current	V_{CC} = MAX. All inputs TTL. All outputs open.			140	185	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

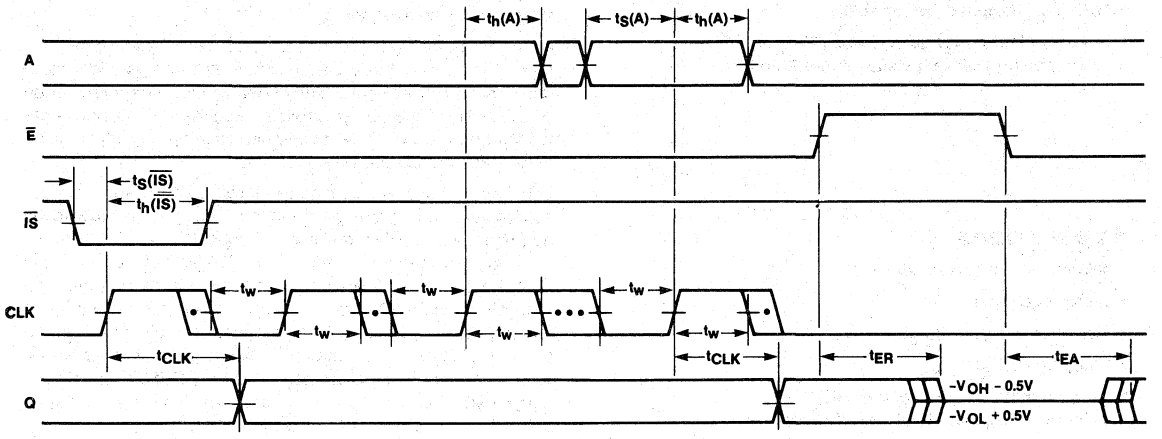
† Typicals at 5.0 V V_{CC} and 25°C T_A.

Switching Characteristics Over Operating Conditions and using Standard Test Load

SYMBOL	PARAMETER	TYP†	MILITARY				COMMERCIAL				UNIT
			53RA1681A		53RA1681		63RA1681A		63RA1681		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CLK}	Clock to output Delay	10		20		25		15		20	ns
t_{EA}	Enable to output access time ($\overline{E}$)	15		30		35		25		30	ns
t_{ER}	Disable to output recovery time ($\overline{E}$)	15		30		35		25		30	ns

† Typicals at 5.0 V V_{CC} and 25°C T_A.

Definition of Waveforms



Notes: 1. Input pulse amplitute 0 V to 3.0 V.

2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
3. Input access measured at the 1.5 V level.
4. Switch S_1 is closed. C_L = 30 pF and outputs measured at 1.5 V output level for all tests except t_{ESA} and t_{ESR}.
5. t_{EA} and t_{ESA} are measured at the 1.5 V output level with C_L = 30 pF. S_1 is open for high impedance to "1" test, and closed for high impedance to "0" test.

   t_{ER} and t_{ESR} are tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} -0.5 V output level; S_1 is closed for "0" to high impedance test measured at V_{OL} +0.5 V output level.

2048x8 Registered PROM with Synchronous Enable

53/63RS1681 53/63RS1681A

Features/Benefits

- Synchronous output enable
- Edge-triggered "D" registers
- Versatile 1:16 user programmable initialization words
- 8-bit-wide in 24-pin SKINNYDIP® for high board density
- Simplifies system timing
- Faster cycle times
- 16 mA I_{OL} output drive capability
- Reliable titanium-tungsten fuses (TiW), with programming yields typically greater than 98%

Applications

- Microprogram control store
- State sequencers
- Next address generation
- Mapping PROM
- Programmable Logic Element (PLE™)
  11 Inputs, 8 Registered Outputs, 2048 product terms

Description

The 53/63RS1681 and 53/63RS1681A are 2Kx8 PROMs with on-chip "D" type registers, versatile output enable control through synchronous enable inputs and flexible start up sequencing through programmable initialization words.

Data is transferred into the output registers on the rising edge of the clock. Provided that the synchronous ($\overline{ES}$) enable is LOW, the data will appear at the outputs. Prior to the positive clock edge, register data are not affected by changes in addressing or synchronous enable inputs.

Memory expansion and data control is made flexible with synchronous enable inputs. Outputs may be set to the high impedance state by setting $\overline{ES}$ HIGH before the rising clock edge occurs. When V_{CC} power is first applied the synchronous enable flip-flop will be in the set condition causing the outputs to be in the high impedance state.

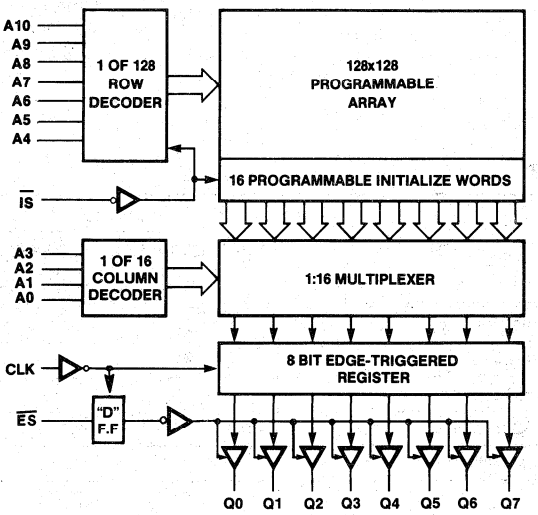
The flexible initialization feature allows start up and time out sequencing with 1:16 programmable words to be loaded into the output registers. With the synchronous INITIALIZE ($\overline{IS}$) pin LOW, one of the 16 column words (A3-A0) will be set in the output registers independent of the row addresses (A10-A4). With all $\overline{IS}$ column words (A3-A0) programmed to the same pattern, the $\overline{IS}$ function will be independent of both row and column addressing and may be used as a single pin control. With all $\overline{IS}$ words programmed HIGH a PRESET function is performed. The unprogrammed state of $\overline{IS}$ words are LOW, presenting a CLEAR with $\overline{IS}$ pin LOW.

Selection Guide

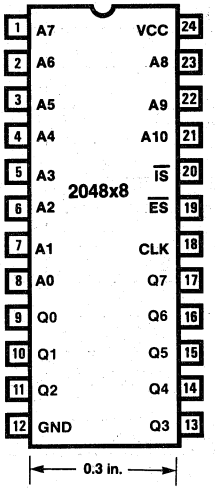
MEMORY		PACKAGE		PERFORMANCE	PART NUMBER	
SIZE	ORGANIZATION	PINS	TYPE		0°C to +75°C	-55°C to +125°C
16 K	2048x8	24 (28)	NS,JS, W, (NL),(L)	Enhanced	63RS1681A	53RS1681A
				Standard	63RS1681	53RS1681

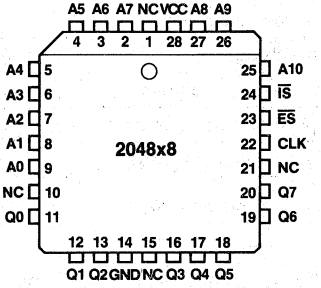
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374
Monolithic Memories

Block Diagram



Pin Configurations





Plastic Chip Carrier

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	−0.5 V to 7 V	12 V
Input voltage	−1.5 V to 7 V	7 V
Input current	−30 mA to +5 mA	
Off-state output voltage	−0.5 V to 5.5 V	12 V
Storage temperature	−65°C to +150°C	

Operating Conditions

SYMBOL	PARAMETER	TYP†	MILITARY				COMMERCIAL				UNIT
			53RS1681A		53RS1681		63RS1681A		63RS1681		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Width of clock (high or low)	10	20		20		20		20		ns
$t_{s(A)}$	Setup time from address to clock	28	40		45		35		40		ns
$t_{s(\overline{ES})}$	Setup time from $\overline{ES}$ to clock	7	15		15		15		15		ns
$t_{s(\overline{IS})}$	Setup time from $\overline{IS}$ to clock	20	30		35		25		30		ns
$t_{h(A)}$	Hold time address to clock	−5	0		0		0		0		ns
$t_{h(\overline{ES})}$	Hold time ($\overline{ES}$)	−3	5		5		5		5		ns
$t_{h(\overline{IS})}$	Hold time ($\overline{IS}$)	−5	0		0		0		0		ns
V_{CC}	Supply voltage	5	4.5	5.5	4.5	5.5	4.75	5.25	4.75	5.25	V
T_A	Operating free-air temperature	25	−55	125	−55	125	0	75	0	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2.0			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA			−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX			40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16 mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	Com I_{OH} = −3.2 mA	2.4			V
			Mil I_{OH} = −2 mA				
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4 V			−40	μA
I_{OZH}			V_O = 2.4 V			40	
I_{OS}	Output short-circuit current*	V_{CC} = 5 V	V_O = 0 V	−20		−90	mA
I_{CC}	Supply current	V_{CC} = MAX. All inputs TTL. All outputs open.			140	185	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

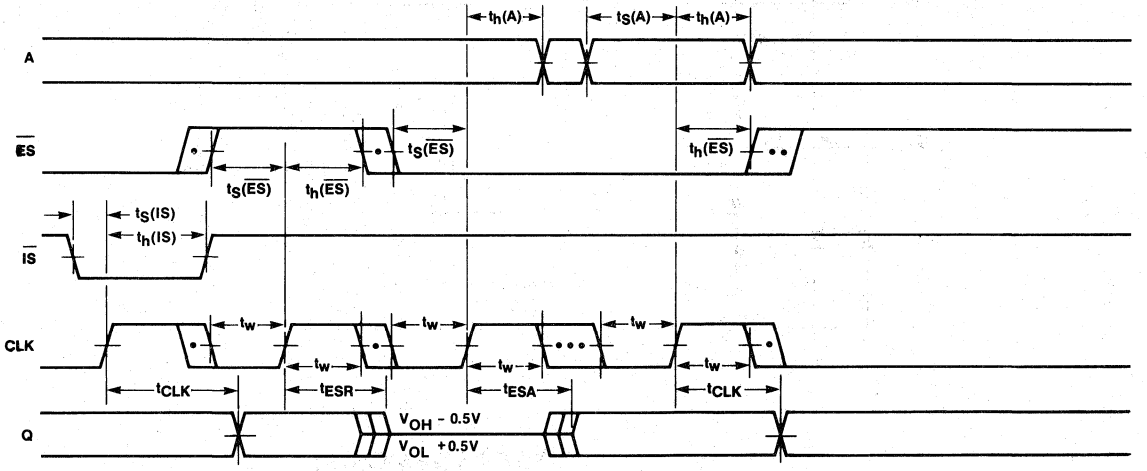
† Typicals at 5.0 V V_{CC} and 25°C T_A.

Switching Characteristics Over Operating Conditions and using Standard Test Load

SYMBOL	PARAMETER	TYP†	MILITARY				COMMERCIAL				UNIT
			53RS1681A		53RS1681		63RS1681A		63RS1681		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CLK}	Clock to output Delay	10		20		25		15		20	ns
t_{ESA}	Clock to output access time ($\overline{ES}$)	15		30		35		25		30	ns
t_{ESR}	Clock to output recovery time ($\overline{ES}$)	15		30		35		25		30	ns

† Typicals at 5.0 V V_{CC} and 25°C T_A.

Definition of Waveforms

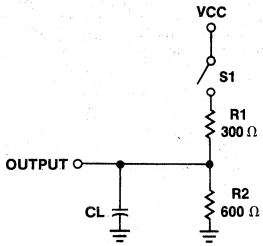


Notes: 1. Input pulse amplitute 0 V to 3.0 V.

2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
3. Input access measured at the 1.5 V level.
4. Switch S_1 is closed. C_L = 30 pF and outputs measured at 1.5 V output level for all tests except t_{ESA} and t_{ESR}.
5. t_{EA} and t_{ESA} are measured at the 1.5 V output level with C_L = 30 pF. S_1 is open for high impedance to "1" test, and closed for high impedance to "0" test.

   t_{ER} and t_{ESR} are tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} -0.5 V output level; S_1 is closed for "0" to high impedance test measured at V_{OL} +0.5 V output level.

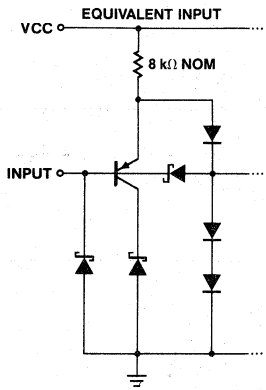
Switching Test Load

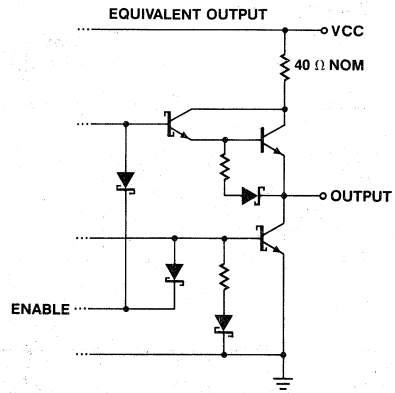


Definition of Timing Diagrams

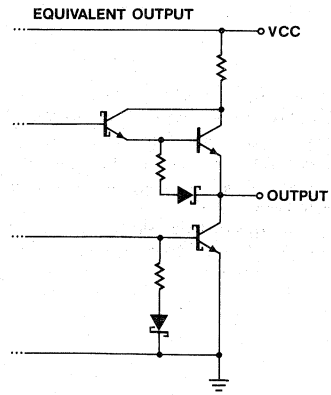
WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

Schematic of Inputs and Outputs

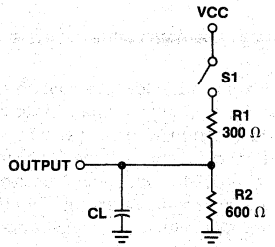




(53DA1643 Only)



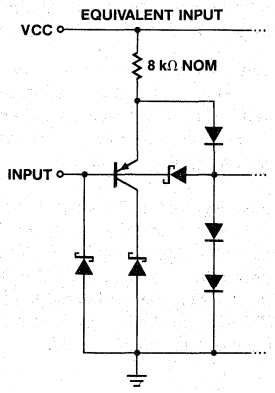
Switching Test Load

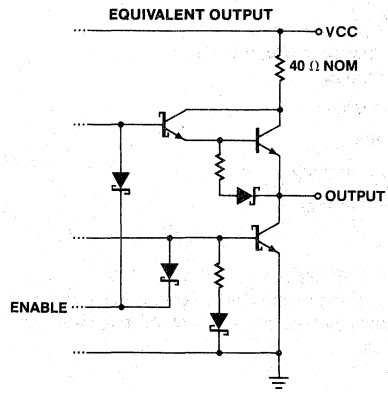


Definition of Timing Diagrams

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

Schematic of Inputs and Outputs





1024x4 Diagnostic Registered PROM

53/63DA441
53/63DA442

Enables and Output Initialization

Features/Benefits

- Programmable asynchronous output initialization
- Three-state outputs with two enables
- Provides system diagnostic testing with system controllability and observability
- Shadow register eliminates shifting hazards
- Edge-triggered "D" registers simplifies system timing
- Cascadable for wide control words used in microprogramming
- 24-pin SKINNYDIP® package saves space
- 24-mA output drive capability
- Replaces embedded diagnostic code
- Guaranteed programming yields of greater than 98%

Applications

- Microprogram control store with built-in system diagnostic testing
- Serial character generator
- Serial code converter
- Parallel in/serial out memory
- Cost-effective board testing

Description

The 53/63DA441 and 53/63DA442 are 1Kx4 PROMs with registered outputs, programmable asynchronous initialization, three-state outputs with two enables and a shadow register for diagnostic capabilities.

Shadow register diagnostics allow observation and control of the system without introducing intermediate illegal states. The output register, which can receive parallel data from either the PROM array or the shadow register is loaded on the rising edge of CLK. The shadow register, which can receive parallel data from the output register or serial data from SDI, is loaded on the rising edge of DCLK. When the output drivers are disabled, the shadow register receives its parallel data from the output bus.

During diagnostics, data loaded into the output register from the PROM array can be parallel-loaded into the shadow register and serially shifted out through SDO, allowing observation of the system. Similarly, diagnostic data can be serially shifted into the shadow register through SDI, and parallel-loaded into the output register, allowing control and test scanning to be imposed on the system. Since the output register and the shadow register are loaded by different input signals, they can be operated independently of one another. In addition, diagnostic PROMs can be cascaded to construct wide control words used in microprogramming.

When exercised, the initialization input loads the output register with a user-programmable initialization word, independent of the state of CLK. This features is a superset of preset and clear functions, and can be used to generate an arbitrary microinstruction for system reset or interrupt.

The distinguishing feature between the 53/63DA441 and 53/63DA442 is on the output enable structure. The 53/63DA441 has two asynchronous output enables, $\overline{E1}$ and $\overline{E2}$. Outputs will be enabled when both $\overline{E1}$ and $\overline{E2}$ are LOW. The 53/63DA442 has one asynchronous output enable $\overline{E}$ and one synchronous output enable $\overline{ES}$. Outputs will be enabled if $\overline{ES}$ is LOW during the last rising edge of CLK and $\overline{E}$ is LOW.

Selection Guide

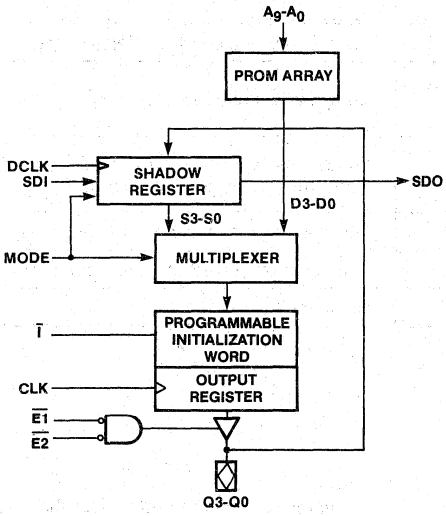
MEMORY			PACKAGE		PART NUMBER	
SIZE	ORGANIZATION	OPTIONS	PINS	TYPE	MILITARY	COMMERCIAL
4 K	1024x4	Two asynchronous enables	24 (28)	NS,JS,W, (NL),(L)	53DA441	63DA441
		One synchronous enable, one asynchronous enable			53DA442	63DA442

SKINNYDIP® is a registered trademark of Monolithic Memories

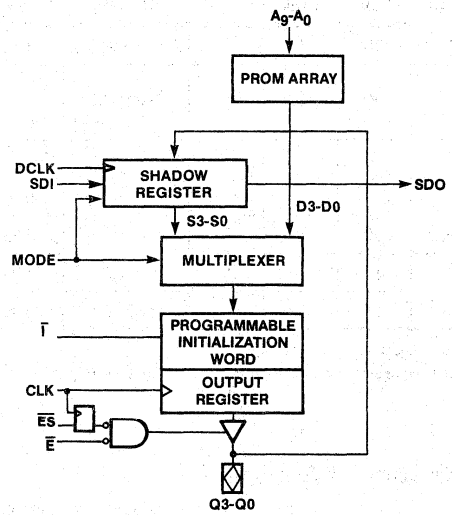
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories

Block Diagrams

53/63DA441

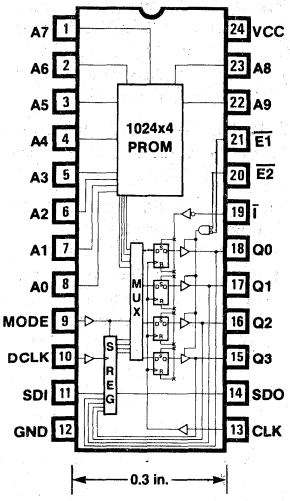


53/63DA442

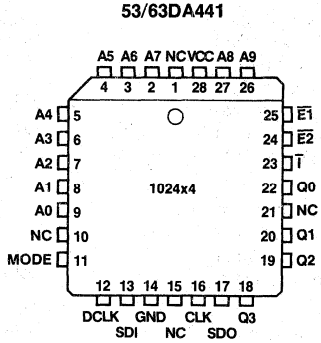


Logic Symbols

53/63DA441

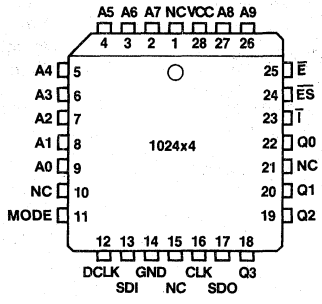


53/63DA441



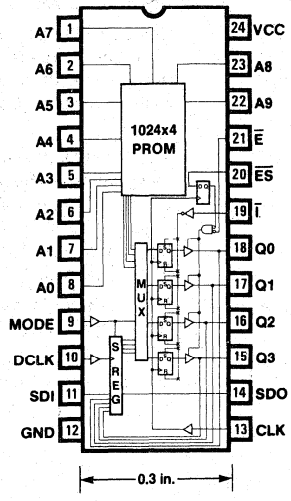
Plastic Chip Carrier

53/63DA442



Plastic Chip Carrier

53/63DA442



Function Table

INPUTS				OUTPUTS			OPERATION
MODE	SDI	CLK	DCLK	Q3-Q0	S3-S0	SDO	
L	X	↑	*	Qn ← PROM	HOLD	S3	Load output register from PROM array
L	X	*	↑	HOLD	Sn ← Sn-1 S0 ← SDI	S3	Shift shadow register data
L	X	↑	↑	Qn ← PROM	Sn ← Sn-1 S0 ← SDI	S3	Load output register from PROM array while shifting shadow register data
H	X	↑	*	Qn ← Sn	HOLD	SDI	Load output register from shadow register
H	L	*	↑	HOLD	Sn ← Qn	SDI	Load shadow register from output bus
H	H	*	↑	HOLD	HOLD	SDI	No operation†

* Clock must be steady or falling.

† Reserved operation for SN54/74S818 8-Bit Diagnostic Register.

Definition of Signals

MODE — The MODE pin controls the output register multiplexer and the shadow register. When MODE is LOW, the output register receives data from the PROM array and the shadow register is configured as a shift register with SDI as its input. When MODE is HIGH, the output register receives data from the shadow register. The shadow register is controlled by SDI as well as MODE With MODE HIGH and SDI LOW, the shadow register receives parallel data from the output bus. With MODE and SDI both HIGH, the shadow register holds its present data.

SDI — The Serial Data In pin is the input to the least-significant bit of the shadow register when operating in the shift mode. SDI is also a control input to the shadow register when it is not in the shift mode.

SDO — The Serial Data Out pin is the output from the most significant bit of the shadow register when operating in the shift mode. When the shadow register is not in the shift mode, SDO displays the logic level present at SDI, decreasing serial shift time for cascaded diagnostic PROMs.

CLK — The clock pin loads the output register on the rising edge of CLK.

DCLK — The diagnostic clock pin loads or shifts the shadow register on the rising edge of DCLK.

Q3-Q0 — Qn represents the data outputs of the output register. During a shadow register load with outputs enabled, these pins are the internal data inputs to the shadow register. With the outputs three-stated, these pins are external data inputs to the shadow register.

S3-S0 — Sn represents the internal shadow register outputs.

A9-A0 — An represents the address inputs to the PROM array.

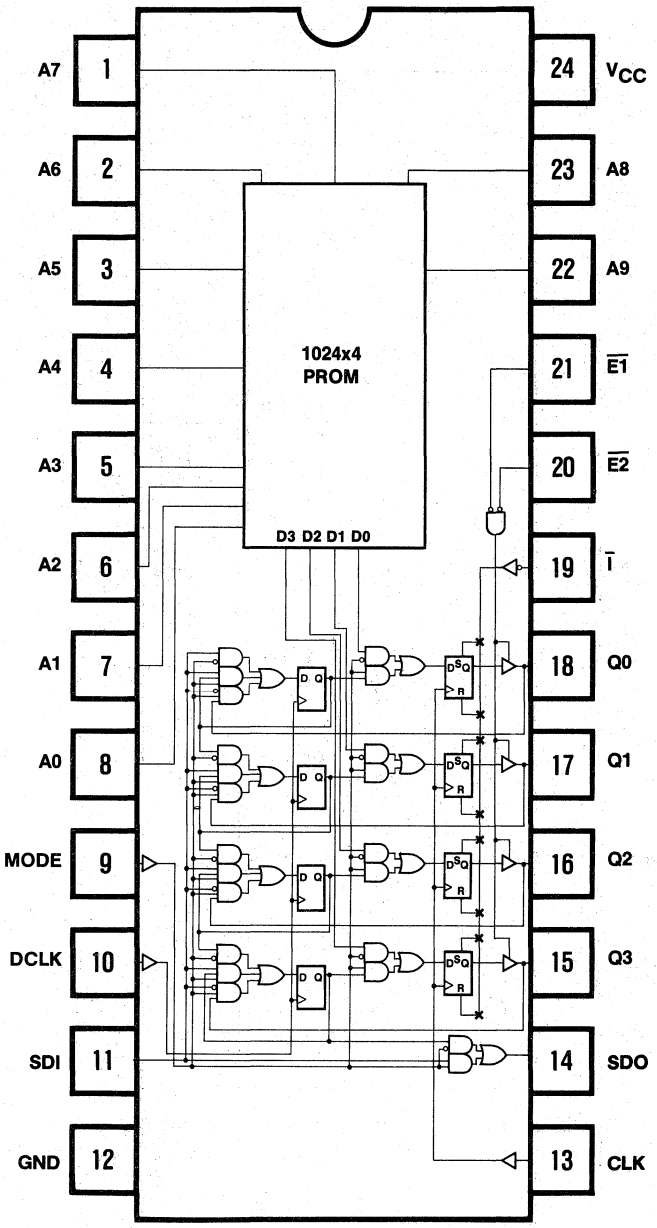
$\overline{E1}$, $\overline{E2}$, $\overline{E}$ — These Output Enable pin(s) operate independent of CLK. For 'D441, outputs are enabled if, and only if, both $\overline{E1}$ and $\overline{E2}$ are LOW. For 'D442, outputs are enabled only when $\overline{ES}$ is LOW at the last rising edge of CLK and $\overline{E}$ is LOW.

$\overline{ES}$ — Synchronous Output Enable for 'DA442 only. Outputs are enabled only when $\overline{ES}$ is LOW at the last rising edge of CLK and $\overline{E}$ is LOW.

$\overline{I}$ — The asynchronous output register initialization input pin operates independent of CLK. When $\overline{I}$ is LOW, the output register is loaded with a user-programmable initialization word. Programmable initialization is a super set of preset and clear functions, and can be used to generate any microinstruction system reset or interrupt.

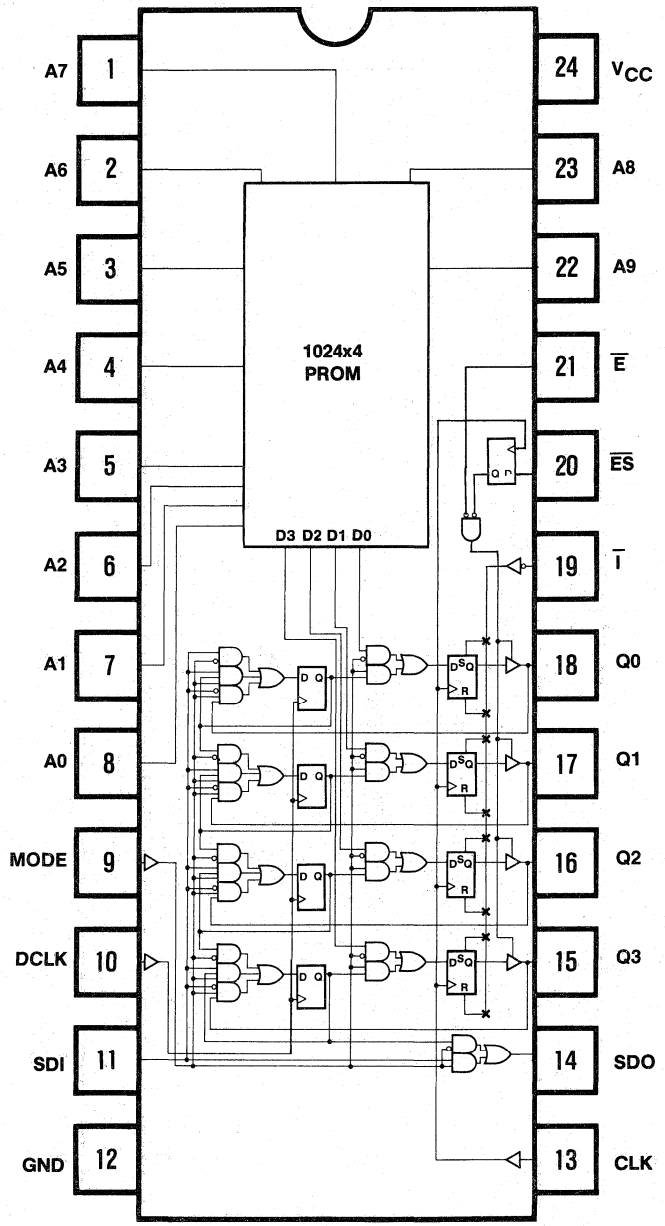
Logic Diagram

53/63DA441
1024x4 Diagnostic PROM
with Asynchronous Initialization
and Asynchronous Enables



Logic Diagram

53/63DA442
1024x4 Diagnostic PROM
with Asynchronous Initialization
and Both Asynchronous and Synchronous Enables



Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5 V to 7 V	12 V
Input voltage	-1.5 V to 7 V	7 V
Input current	-30 mA to +5 mA	
Off-state output voltage	-0.5 V to 5.5 V	12 V
Storage temperature	-65° to +150° C	

3

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	-55	25	125	0	25	75	°C
t_w	Width of CLK (HIGH or LOW)	25	10		20	10		ns
t_{su}	Setup time from address to CLK	45	25		35	25		ns
t_h	Hold time for CLK	0	-15		0	-15		ns
t_{wd}	Width of DCLK (HIGH or LOW)	35	15		25	15		ns
t_{sud}	Setup time from control inputs (SDI, MODE) to CLK, DCLK	50	20		40	20		ns
t_{hd}	Hold time for DCLK	0	-5		0	-5		ns
$t_s(\overline{ES})$	Setup time from $\overline{ES}$ to CLK ('DA442 only)	20	10		15	10		ns
$t_h(\overline{ES})$	Hold time ($\overline{ES}$) ('DA442 only)	5	0		5	0		ns
t_{iw}	Initialization pulse width (LOW)	25	10		20	10		ns
t_{ir}	Initialization recovery time	45	30		40	30		ns

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2.0			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA			-1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX			40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	Com I_{OL} = 24 mA			0.5	V
			Mil I_{OL} = 16 mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	Com I_{OH} = -3.2 mA	2.4			V
			Mil I_{OH} = -2 mA				
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4 V			-100	μA
I_{OZH}			V_O = 2.4 V			40	
I_{OS}	Output short-circuit current*	V_{CC} = MAX	V_O = 0 V	-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX. All inputs TTL. All outputs open.			130	180	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

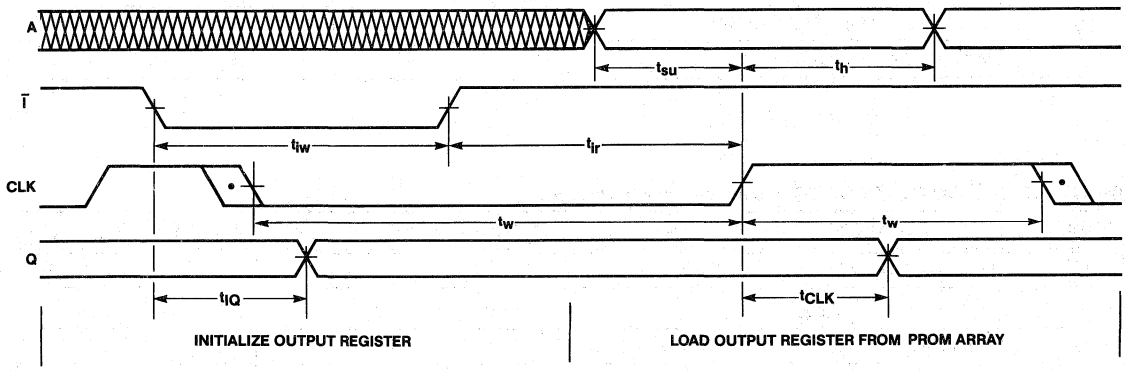
† Typicals at 5.0 V V_{CC} and 25° C T_A.

Switching Characteristics Over Operating Conditions and Using Standard Test Load

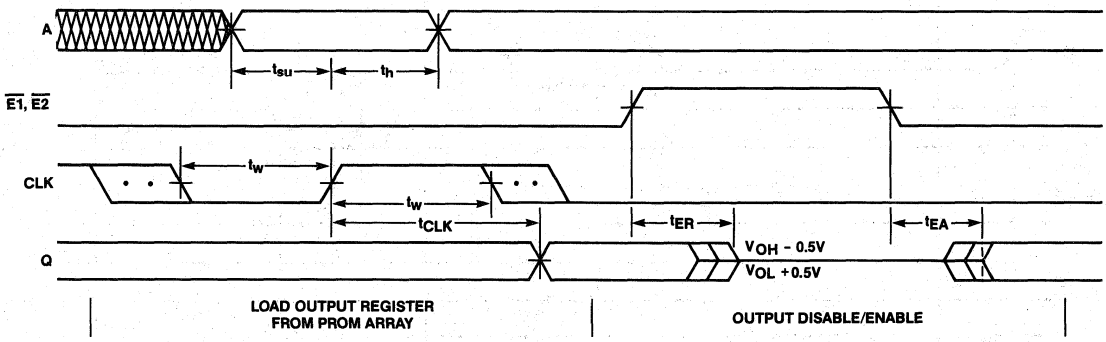
SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP†	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP†	COMMERCIAL MAX	UNIT
t_{CLK}	CLK to output		11	25		11	18	ns
t_{ER}	Disable time		14	30		14	25	ns
t_{EA}	Enable time		16	30		16	25	ns
t_{MAXD}	Maximum diagnostic clock frequency	7	20		10	20		MHz
t_{DS}	DCLK to SDO delay (MODE = LOW)		17	35		17	30	ns
t_{SS}	SDI to SDO delay (MODE = HIGH)		16	30		16	25	ns
t_{MS}	MODE to SDO delay		14	30		14	25	ns
t_{IQ}	Initialization to output delay		22	35		22	30	ns
t_{ESR}	CLK to output disable time ('DA442 only)		22	35		22	30	ns
t_{ESA}	CLK to output enable time ('DA442 only)		15	35		15	30	ns

† Typicals at 5.0 V V_{CC} and 25°C T_A.

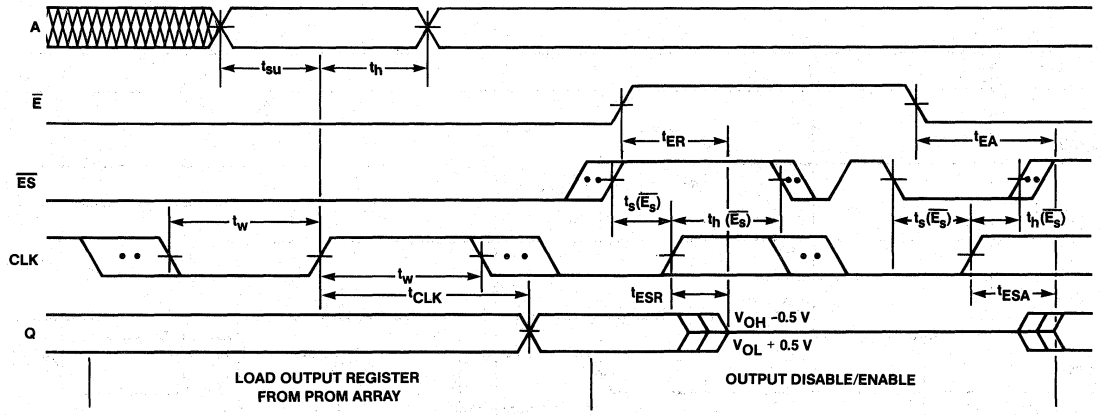
Definition of Waveforms



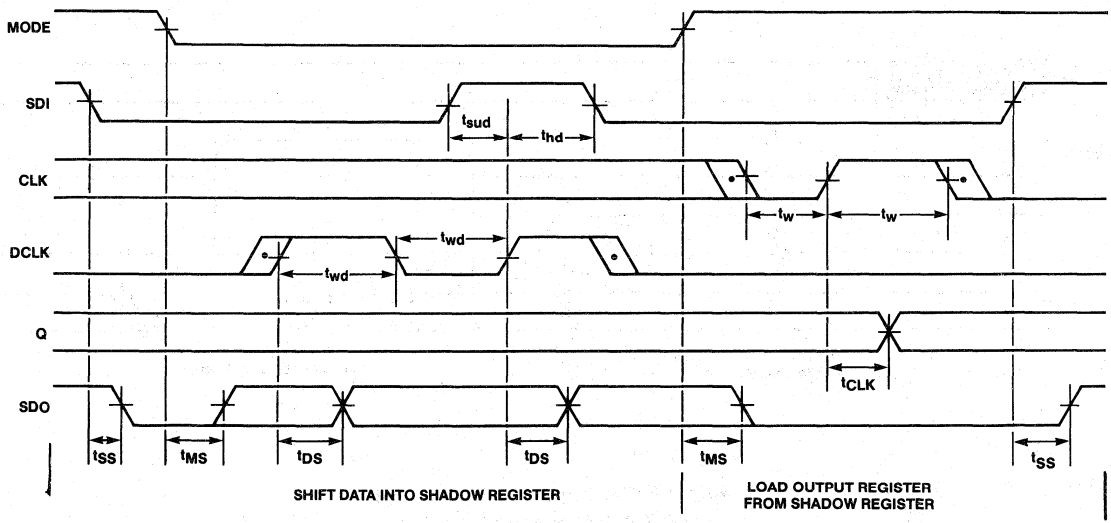
Normal PROM Operation (Mode = LOW)
(for both 53/63DA441 and 53/63DA442 with outputs enabled)



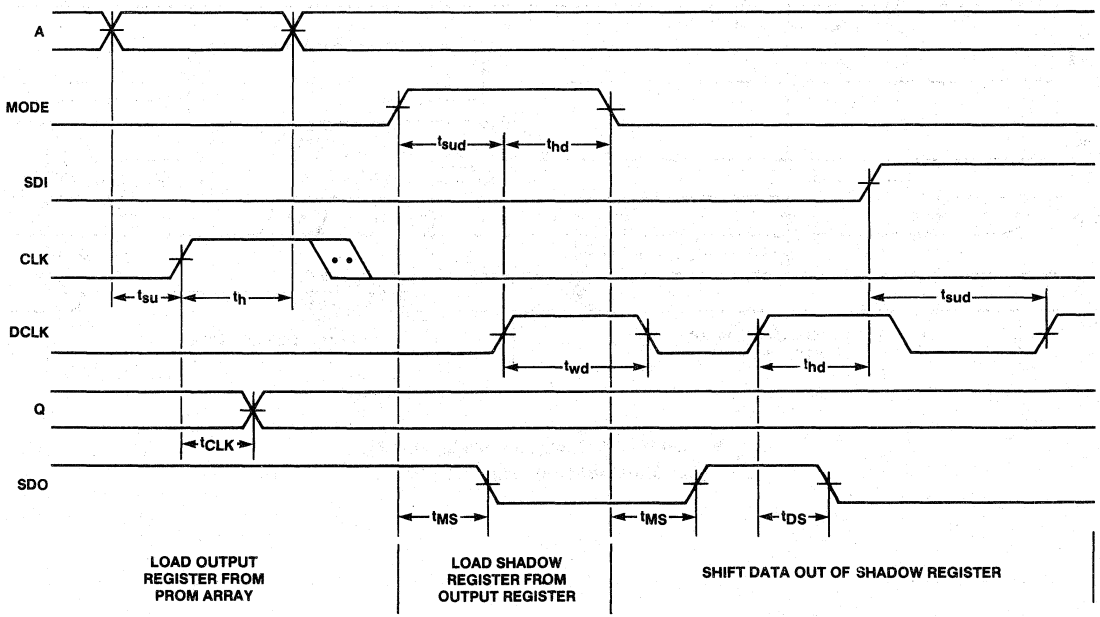
Normal PROM Operation (Mode = LOW)
(for 53/63DA441 only with $\overline{I}$ = HIGH)



Normal PROM Operation (Mode = LOW)
(for 53/63DA442 only with $\overline{I}$ = HIGH)



SYSTEM CONTROL



SYSTEM OBSERVATION

2048x4 Diagnostic Registered PROM

53DA841
63DA841

with Asynchronous Enable and Output Initialization

Features/Benefits

- Asynchronous output enable
- Programmable asynchronous output initialization
- Provides system diagnostic testing with system controllability and observability
- Shadow register eliminates shifting hazards
- Edge-triggered "D" registers simplifies system timing
- Cascadable for wide control words used in microprogramming
- 24-pin SKINNYDIP® saves space
- Reliable titanium-tungsten fuses (TiW), with programming yields typically greater than 98%
- 24-mA output drive capability
- Replaces embedded diagnostic code

Applications

- Microprogram control store with built-in system diagnostic testing
- Serial character generator
- Serial code converter
- Parallel in/serial out memory
- Cost-effective board testing

Description

The 53/63DA841 is a 2Kx4 PROM with registered three-state outputs, programmable asynchronous initialization and a shadow register for diagnostic capabilities. Shadow register diagnostics allow observation and control of the system without introducing intermediate illegal states. The output register, which can receive parallel data from either the PROM array or the shadow register is loaded on the rising edge of CLK. The shadow register, which can receive parallel data from the output register or serial data from SDI, is loaded on the rising edge of DCLK. When the output drivers are disabled, the shadow register receives its parallel data from the output bus. During diagnostics, data loaded into the output register from the PROM array can be parallel-loaded into the shadow register and serially shifted out through SDO, allowing observation of the system. Similarly, diagnostic data can be serially shifted into the shadow register through SDI, and parallel-loaded into the output register, allowing control and test scanning to be imposed on the system. Since the output register and the shadow register are loaded by different input signals, they can be operated independently of one another. In addition, diagnostic PROMs can be cascaded to construct wide control words used in microprogramming. When exercised, the Initialization input loads the register with a user-programmable initialization word, independent of the state of CLK. This feature is a superset of preset and clear functions, and can be used to generate an arbitrary microinstruction for system reset or interrupt.

Selection Guide

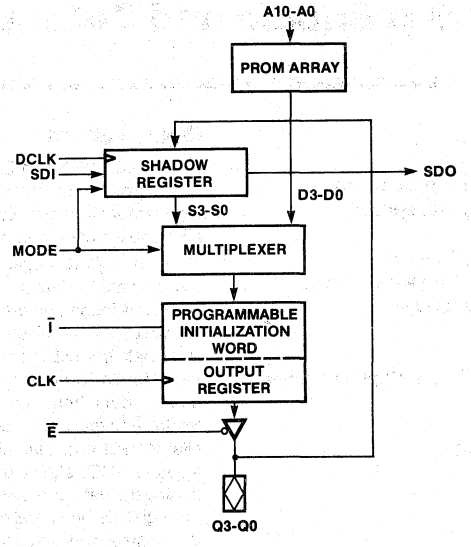
MEMORY		PACKAGE		PART NUMBER	
SIZE	ORGANIZATION	PINS	TYPE	0°C to +75°C	-55°C to +125°C
8 K	2048x4	24 (28)	NS,JS, W, (NL),(L)	63DA841	53DA841

SKINNYDIP® is a registered trademark of Monolithic Memories

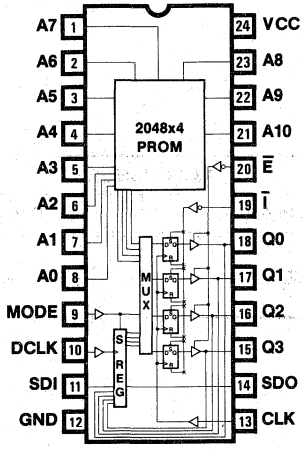
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

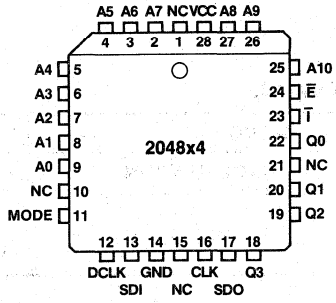
Monolithic Memories MMI

Block Diagram



Pin Configurations





Plastic Chip Carrier

Function Table

INPUTS				OUTPUTS			OPERATION
MODE	SDI	CLK	DCLK	Q3-Q0	S3-S0	SDO	
L	X	↑	*	Qn ← PROM	HOLD	S3	Load output register from PROM array
L	X	*	↑	HOLD	Sn ← Sn-1 S0 ← SDI	S3	Shift shadow register data
L	X	↑	↑	Qn ← PROM	Sn ← Sn-1 S0 ← SDI	S3	Load output register from PROM array while shifting shadow register data
H	X	↑	*	Qn ← Sn	HOLD	SDI	Load output register from shadow register
H	L	*	↑	HOLD	Sn ← Qn	SDI	Load shadow register from output bus
H	H	*	↑	HOLD	HOLD	SDI	No operation †

* Clock must be steady or falling.

† Reserved operation for SN54/74S818 8-Bit Diagnostic Register.

Definition of Signals

MODE — The MODE pin controls the output register multiplexer and the shadow register. When MODE is LOW, the output register receives data from the PROM array and the shadow register is configured as a shift register with SDI as its input. When MODE is HIGH, the output register receives data from the shadow register. The shadow register is controlled by SDI as well as MODE. With MODE HIGH and SDI LOW, the shadow register receives parallel data from the output register. With MODE and SDI both HIGH, the shadow register holds its present data.

SDI — The Serial Data In pin is the input to the least significant bit of the shadow register when operating in the shift mode. SDI is also a control input to the shadow register when it is not in the shift mode.

SDO — The Serial Data Out pin is the output from the most significant bit of the shadow register when operating in the shift mode. When the shadow register is not in the shift mode, SDO displays the logic level present at SDI, decreasing serial shift time for cascaded diagnostic PROMs.

CLK — The clock pin loads the output register on the rising edge of CLK.

DCLK — The diagnostic clock pin loads or shifts the shadow register on the rising edge of DCLK.

Q3-Q0 — Qn represents the data outputs of the output register. During a shadow register load these pins are the internal data inputs to the shadow register.

S3-S0 — Sn represents the internal shadow register outputs.

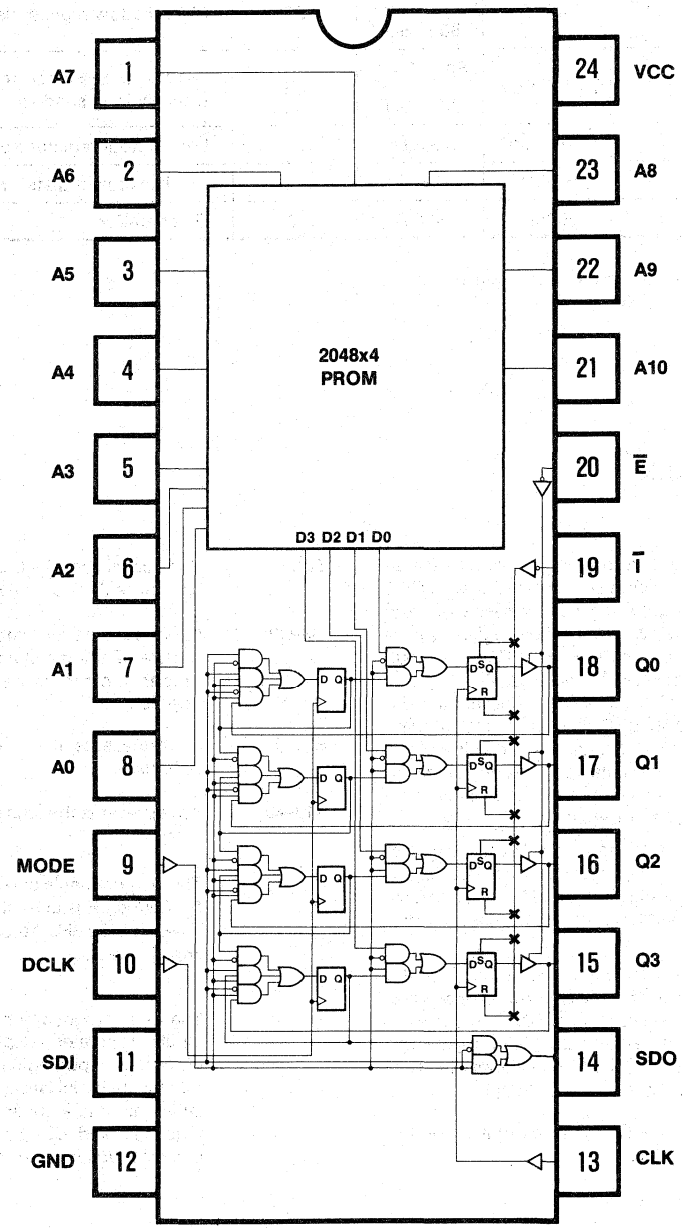
A10-A0 — An represents the address inputs to the PROM array.

$\overline{E}$ — The Output Enable pin operates independent of CLK. When $\overline{E}$ is LOW the outputs are enabled. When $\overline{E}$ is HIGH, the outputs are in the high-impedance state.

$\overline{I}$ — The asynchronous output register initialization input pin operates independent of CLK. When $\overline{I}$ is LOW, the output register is loaded with a user-programmable initialization word. Programmable initialization is a super-set of preset and clear functions, and can be used to generate any microinstruction for system reset or interrupt.

Logic Diagram

2048 x 4 Diagnostic PROM with Asynchronous Enable and Output Initialization



Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5 V to 7 V	12 V
Input voltage	-1.5 V to 7 V	7 V
Input current	-30 mA to +5 mA	
Off-state output voltage	-0.5 V to 5.5 V	12 V
Storage temperature	-65° to +150°C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP†	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP†	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	-55	25	125	0	25	75	°C
t_w	Width of CLK (HIGH or LOW)	25	10		20	10		ns
t_{su}	Set up time from address to CLK	45	27		40	27		ns
t_h	Hold time for CLK	0	-15		0	-15		ns
t_{wd}	Width of DCLK (HIGH or LOW)	45	15		40	15		ns
t_{sud}	Set up time from control inputs (SDI, MODE) to CLK, DCLK	50	20		45	20		ns
t_{hd}	Hold time for DCLK	0	-5		0	-5		ns
t_{iw}	Initialization pulse width (LOW)	25	10		20	10		ns
t_{ir}	Initialization recovery time	45	30		40	30		ns

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2.0			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA			-1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX			40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	Com I_{OL} = 24 mA			0.5	V
			Mil I_{OL} = 16 mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	Com I_{OH} = -3.2 mA	2.4			V
			Mil I_{OH} = -2 mA				
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4 V			-100	μA
I_{OZH}			V_O = 2.4 V			40	
I_{OS}	Output short-circuit current*	V_{CC} = 5 V	V_O = 0 V	-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX. All inputs TTL. All outputs open.			140	185	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

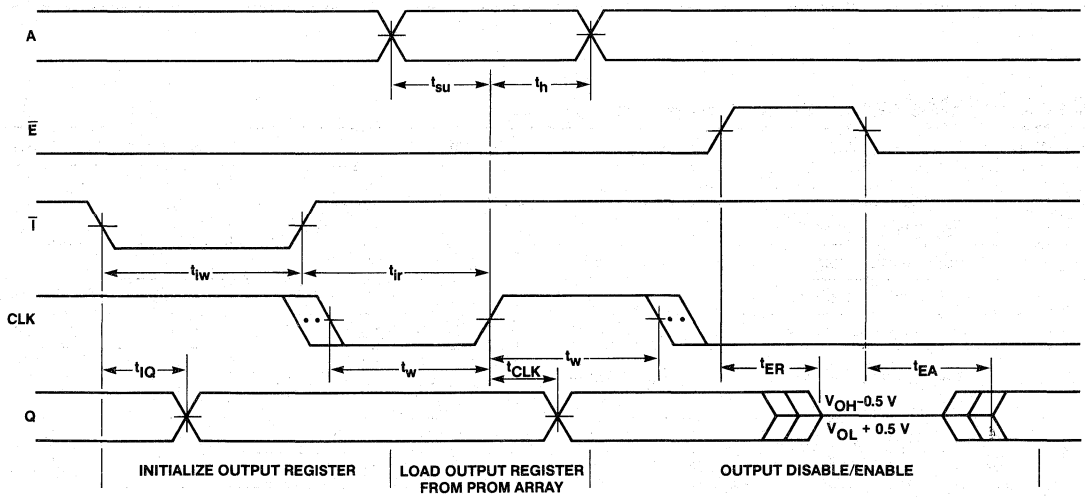
† Typicals at 5.0 V V_{CC} and 25°C T_A.

Switching Characteristics Over Operating Conditions and Using Standard Test Load

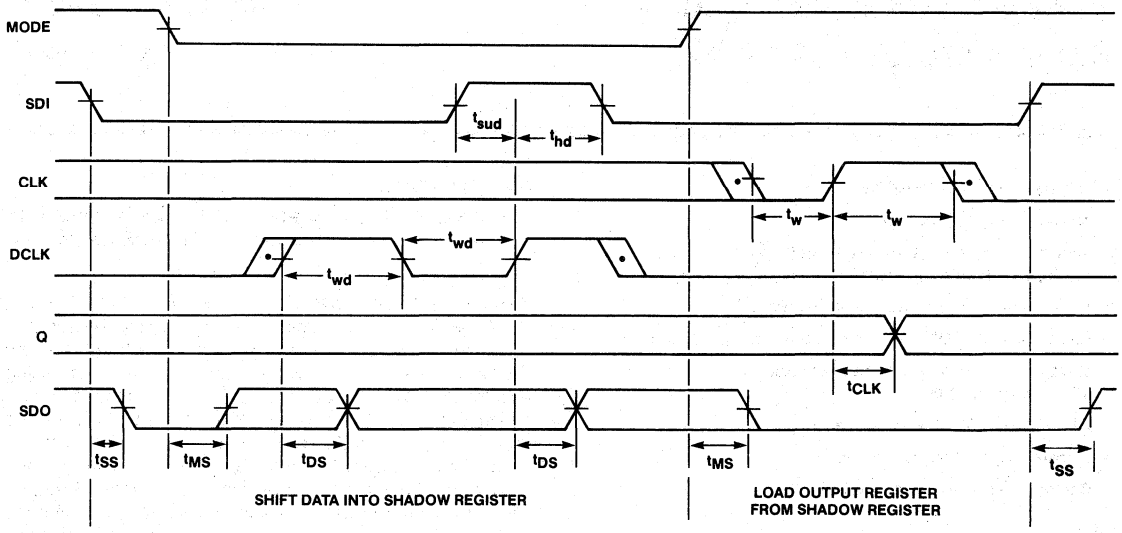
SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP†	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP†	COMMERCIAL MAX	UNIT
t_{CLK}	CLK to output		13	25		13	20	ns
t_{ER}	Enable time		16	30		16	25	ns
t_{EA}	Disable time		16	30		16	25	ns
t_{IQ}	Initialization to output delay		23	40		23	35	ns
f_{MAXD}	Maximum diagnostic clock frequency	7	18		10	18		MHz
t_{DS}	DCLK to SDO delay (MODE = LOW)		19	35		19	30	ns
t_{SS}	SDI to SDO delay (MODE = HIGH)		16	30		16	25	ns
t_{MS}	MODE to SDO delay		14	30		14	25	ns

† Typicals at 5.0 V V_{CC} and 25°C T_A.

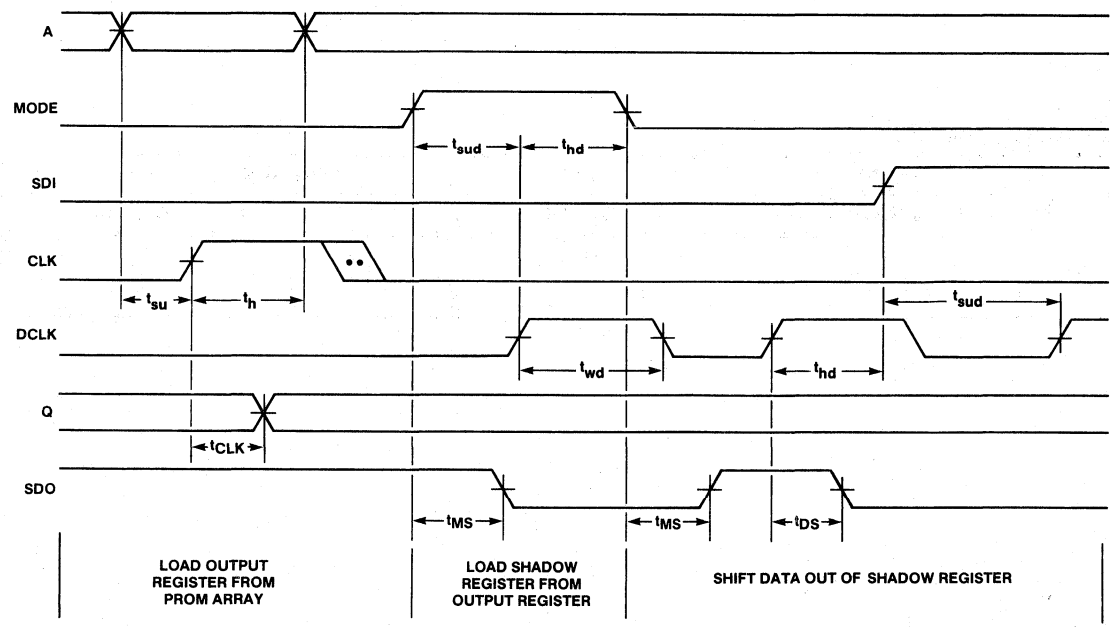
Definition of Waveforms



NORMAL PROM OPERATION (MODE = LOW)



SYSTEM CONTROL



SYSTEM OBSERVATION

4096x4 Diagnostic Registered PROM
Asynchronous Enable

53D1641
63D1641

Patent Pending

Features/Benefits

- Asynchronous output enable
- Provides system diagnostic testing for system controllability and observability
- Shadow register eliminates shifting hazards
- Edge-triggered "D" registers simplifies system timing
- Casadable for wide control words used in microprogramming
- 24-pin SKINNYDIP® saves space
- 24-mA output drive capability
- Replaces embedded diagnostic code

Applications

- Microprogram control store with built-in system diagnostic testing
- Serial character generator
- Serial code converter
- Parallel in/serial out memory
- Cost-effective board testing

Description

The 53/63D1641 is a 4Kx4 PROM with registered three-state outputs and a shadow register for diagnostic capabilities.

Shadow register diagnostics allow observation and control of the system without introducing intermediate illegal states. The output register, which can receive parallel data from either the PROM array or the shadow register, is loaded on the rising edge of CLK. The shadow register, which can receive parallel data from the output register or serial data from SDI, is loaded on the rising edge of DCLK. When the output drivers are disabled, the shadow register receives its parallel data from the output bus. During diagnostics, data loaded into the output register from the PROM array can be parallel-loaded into the shadow register and serially shifted out through SDO, allowing observation of the system. Similarly, diagnostic data can be serially shifted into the shadow register through SDI, and parallel-loaded into the output register, allowing control and test scanning to be imposed on the system. Since the output register and the shadow register are loaded by different input signals, they can be operated independent of one another. In addition, diagnostic PROMs can be cascaded to construct wide control words used in microprogramming.

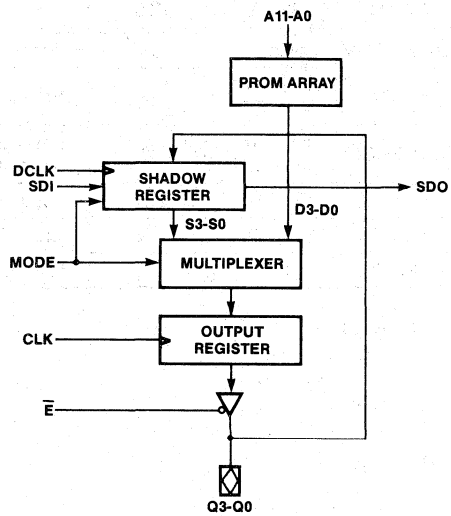
Selection Guide

MEMORY		PACKAGE		PART NUMBER	
SIZE	ORGANIZATION	PINS	TYPE	0°C to +75°C	-55°C to +125°C
16 K	4096x4	24 (28)	NS,JS, W, (NL),(L)	63D1641	53D1641

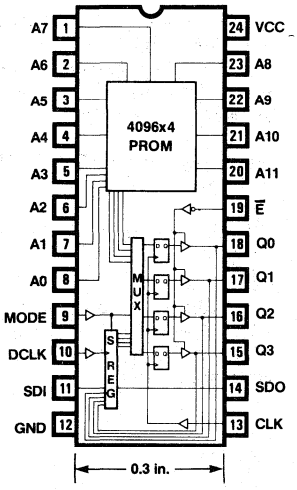
SKINNYDIP® is a registered trademark of Monolithic Memories.

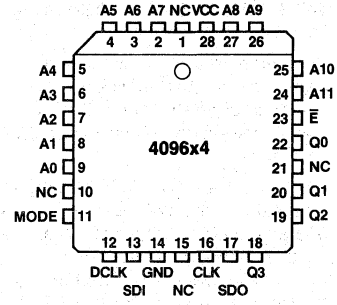
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories MMI

Block Diagram



Pin Configurations





Plastic Chip Carrier

Function Table

INPUTS				OUTPUTS			OPERATION
MODE	SDI	CLK	DCLK	Q3-Q0	S3-S0	SDO	
L	X	↑	*	Qn ← PROM	HOLD	S3	Load output register from PROM array
L	X	*	↑	HOLD	Sn ← Sn-1 S0 ← SDI	S3	Shift shadow register data
L	X	↑	↑	Qn ← PROM	Sn ← Sn-1 S0 ← SDI	S3	Load output register from PROM array while shifting shadow register data
H	X	↑	*	Qn ← Sn	HOLD	SDI	Load output register from shadow register
H	L	*	↑	HOLD	Sn ← Qn	SDI	Load shadow register from output bus
H	H	*	↑	HOLD	HOLD	SDI	No operation†

* Clock must be steady or falling.

† Reserved operation for SN54/74S818 8-Bit Diagnostic Register.

Definition of Signals

MODE — The MODE pin controls the output register multiplexer and the shadow register. When MODE is LOW, the output register receives data from the PROM array and the shadow register is configured as a shift register with SDI as its input. When MODE is HIGH, the output register receives data from the shadow register. The shadow register is controlled by SDI as well as MODE. With MODE HIGH and SDI LOW, the shadow register receives parallel data from the output bus. With MODE and SDI both HIGH, the shadow register holds its present data.

SDI — The Serial Data In pin is the input to the least significant bit of the shadow register when operating in the shift mode. SDI is also a control input to the shadow register when it is not in the shift mode.

SDO — The Serial Data Out pin is the output from the most significant bit of the shadow register when operating in the shift mode. When the shadow register is not in the shift mode, SDO displays the logic level present at SDI, decreasing serial shift time for cascaded diagnostic PROMs.

CLK — The CLOCK pin loads the output register on the rising edge of CLK.

DCLK — The diagnostic clock pin loads or shifts the shadow register on the rising edge of DCLK.

Q3-Q0 — Qn represents the data outputs of the output register. During a shadow register load with outputs enabled these pins are the internal data inputs to the shadow register. With the outputs three-stated these pins are external data inputs to the shadow register.

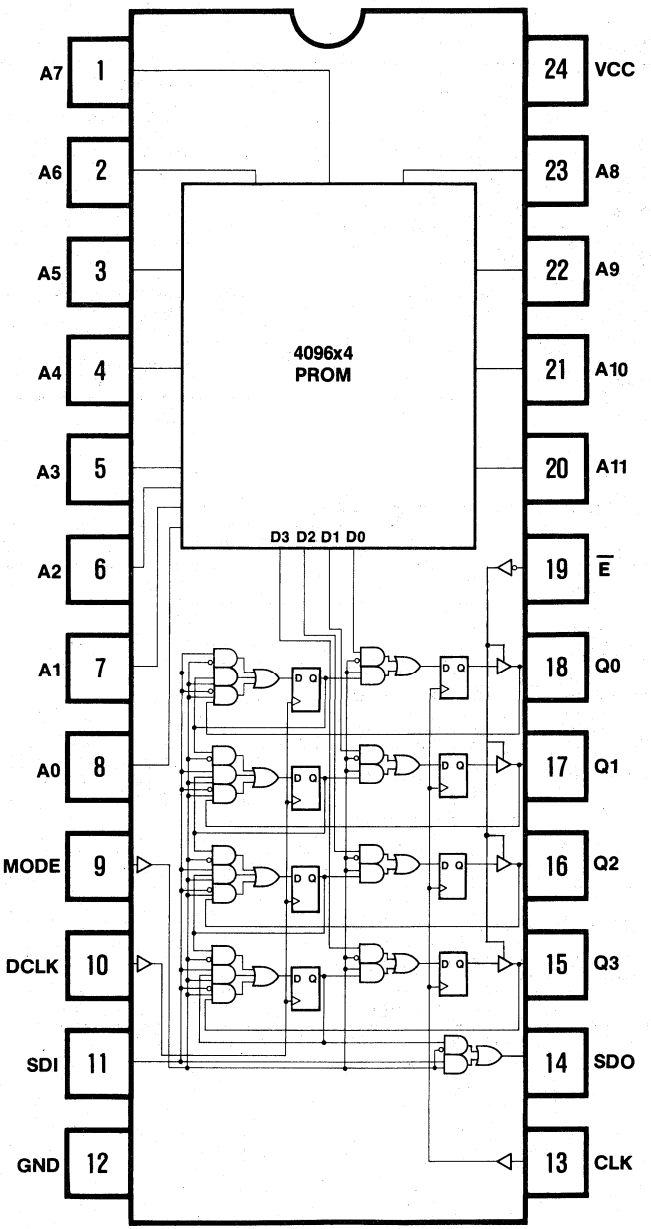
S3-S0 — Sn represents the internal shadow register outputs.

A11-A0 — An represents the address inputs to the PROM array.

$\overline{E}$ — The Output Enable pin operates independent of CLK. When $\overline{E}$ is LOW the outputs are enabled. When $\overline{E}$ is HIGH, the outputs are in the high impedance state.

Logic Diagram

4096x4 Diagnostic PROM with Asynchronous Enable



Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	−0.5 V to 7 V	12 V
Input voltage	−1.5 V to 7 V	7 V
Input Current	−30 mA to +5 mA	
Off-state output voltage	−0.5 V to 5.5 V	12 V
Storage temperature	−65° to +150°C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP†	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP†	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature	−55	25	125	0	25	75	°C
t_w	Width of CLK (HIGH or LOW)	25	10		20	10		ns
t_{su}	Set up time from address to CLK	45	25		40	25		ns
t_h	Hold time for CLK	0	−15		0	−15		ns
t_{wd}	Width of DCLK (HIGH or LOW)	45	15		40	15		ns
t_{sud}	Set up time from control inputs (SDI, MODE) to CLK, DCLK	50	20		45	20		ns
t_{hd}	Hold time for DCLK	0	−5		0	−5		ns

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2.0			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA			−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX			40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	Com I_{OL} = 24 mA			0.5	V
			Mil I_{OL} = 16 mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	Com I_{OH} = −3.2 mA	2.4			V
			Mil I_{OH} = −2 mA				
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4 V			−100	μA
I_{OZH}			V_O = 2.4 V			40	
I_{OS}	Output short-circuit current*	V_{CC} = 5 V	V_O = 0 V	−20		−90	mA
I_{CC}	Supply current	V_{CC} = MAX. All inputs TTL. All outputs open.			140	190	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typicals at 5.0 V V_{CC} and 25°C T_A.

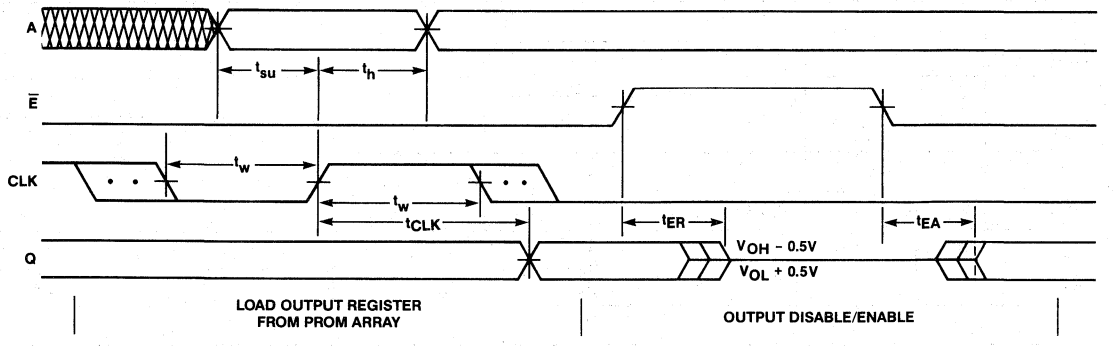
Switching Characteristics Over Operating Conditions and Using Standard Test Load

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP†	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP†	COMMERCIAL MAX	UNIT
t_{CLK}	CLK to output		11	25		11	20	ns
t_{ER}	Disable time		16	30		16	25	ns
t_{EA}	Enable time		16	30		16	25	ns
f_{MAXD}	Maximum diagnostic clock frequency	7	18		10	18		MHz
t_{DS}	DCLK to SDO delay (MODE = LOW)		17	35		17	30	ns
t_{SS}	SDI to SDO delay (MODE = HIGH)		16	30		16	25	ns
t_{MS}	MODE to SDO delay		14	30		14	25	ns

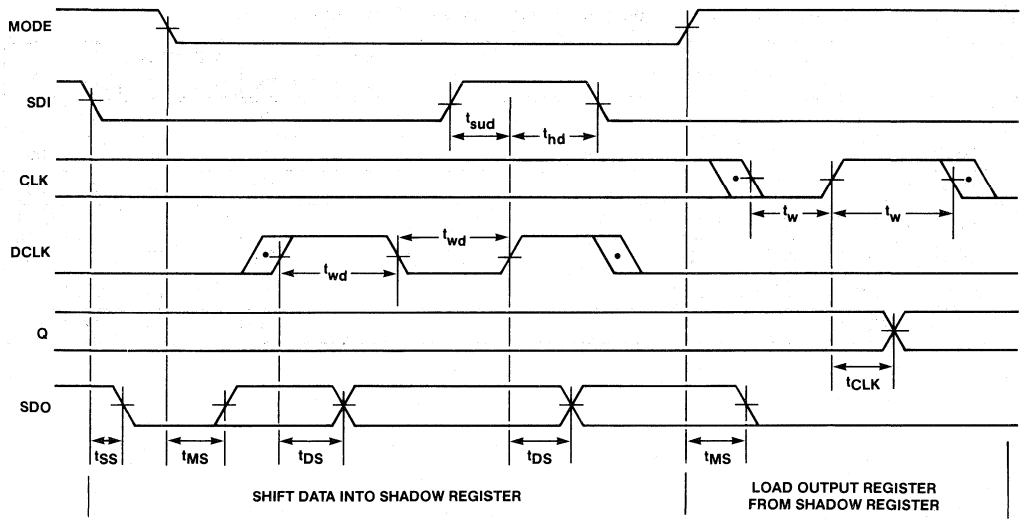
† Typicals at 5.0 V V_{CC} and 25°C T_A.

3

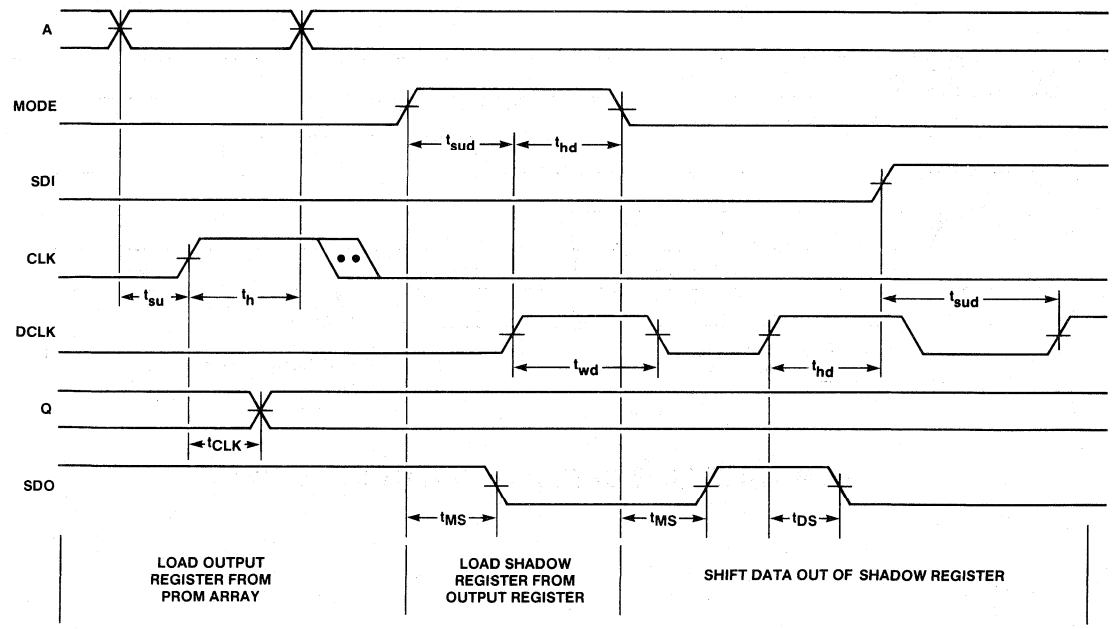
Definition of Waveforms



NORMAL PROM OPERATION (MODE = LOW)



SYSTEM CONTROL



SYSTEM OBSERVATION

4096x4 Diagnostic Registered PROM

53DA1643
63DA1643

Output Initialization

Features/Benefits

- Programmable asynchronous output initialization
- Provides system diagnostic testing with system controllability and observability
- Shadow register eliminates shifting hazards
- Edge-triggered "D" registers simplifies system timing
- Cascadable for wide control words used in microprogramming
- 24-pin SKINNYDIP® saves space
- 24-mA output drive capability
- Replaces embedded diagnostic code

Applications

- Microprogram control store with built-in system diagnostic testing
- Serial character generator
- Serial code converter
- Parallel in/serial out memory
- Cost-effective board testing

Description

The 53/63DA1643 is a 4Kx4 PROM with registered outputs, programmable asynchronous initialization, and a shadow register for diagnostic capabilities. Shadow register diagnostics allow observation and control of the system without introducing intermediate illegal states. The output register, which can receive parallel data from either the PROM array or the shadow register is loaded on the rising edge of CLK. The shadow register, which can receive parallel data from the output register or serial data from SDI, is loaded on the rising edge of DCLK. During diagnostics, data loaded into the output register from the PROM array can be parallel-loaded into the shadow register and serially shifted out through SDO, allowing observation of the system. Similarly, diagnostic data can be serially shifted into the shadow register through SDI, and parallel-loaded into the output register, allowing control and test scanning to be imposed on the system. Since the output register and the shadow register are loaded by different input signals, they can be operated independently of one another. In addition, diagnostic PROMs can be cascaded to construct wide control words used in microprogramming. When exercised, the Initialization input loads the output register with a user-programmable initialization word, independent of the state of CLK. This feature is a superset of preset and clear functions, and can be used to generate an arbitrary microinstruction for system reset or interrupt

Selection Guide

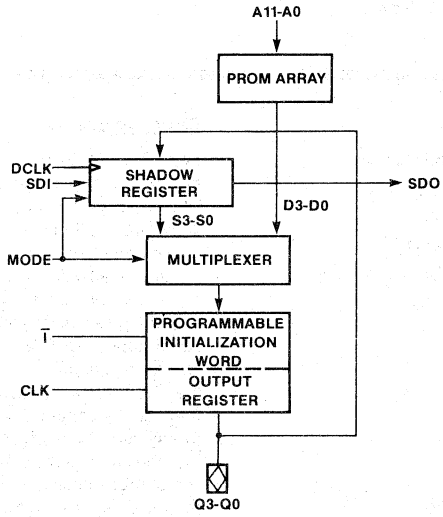
MEMORY		PACKAGE		PART NUMBER	
SIZE	ORGANIZATION	PINS	TYPE	0°C to +75°C	-55°C to +125°C
16 K	4096x4	24 (28)	NS,JS, W, (NL),(L)	63DA1643	53DA1643

SKINNYDIP® is a registered trademark of Monolithic Memories.

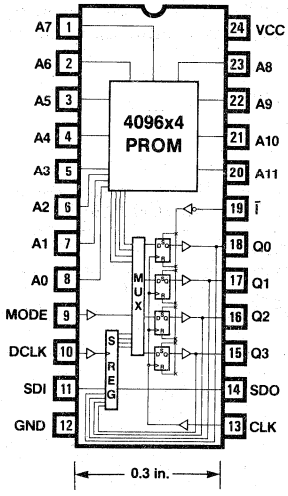
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

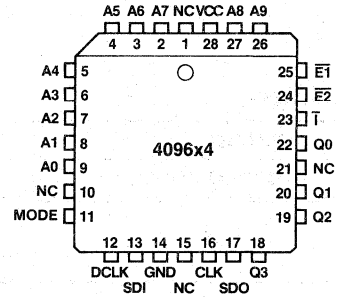
Monolithic Memories MMI

Block Diagram



Pin Configurations





Plastic Chip Carrier

Function Table

INPUTS				OUTPUTS			OPERATION
MODE	SDI	CLK	DCLK	Q3-Q0	S3-S0	SDO	
L	X	↑	*	Qn ← PROM	HOLD	S3	Load output register from PROM array
L	X	*	↑	HOLD	Sn ← Sn-1 S0 ← SDI	S3	Shift shadow register data
L	X	↑	↑	Qn ← PROM	Sn ← Sn-1 S0 ← SDI	S3	Load output register from PROM array while shifting shadow register data
H	X	↑	*	Qn ← Sn	HOLD	SDI	Load output register from shadow register
H	L	*	↑	HOLD	Sn ← Qn	SDI	Load shadow register from output bus
H	H	*	↑	HOLD	HOLD	SDI	No operation†

* Clock must be steady or falling.

† Reserved operation for SN54/74S818 8-Bit Diagnostic Register.

3

Definition of Signals

MODE — The MODE pin controls the output register multiplexer and the shadow register. When MODE is LOW, the output register receives data from the PROM array and the shadow register is configured as a shift register with SDI as its input. When MODE is HIGH, the output register receives data from the shadow register. The shadow register is controlled by SDI as well as MODE. With MODE HIGH and SDI LOW, the shadow register receives parallel data from the output register. With MODE and SDI both HIGH, the shadow register holds its present data.

SDI — The Serial Data In pin is the input to the least significant bit of the shadow register when operating in the shift mode. SDI is also a control input to the shadow register when it is not in the shift mode.

SDO — The Serial Data Out pin is the output from the most significant bit of the shadow register when operating in the shift mode. When the shadow register is not in the shift mode, SDO displays the logic level present at SDI, decreasing serial shift time for cascaded diagnostic PROMs.

CLK — The clock pin loads the output register on the rising edge of CLK.

DCLK — The diagnostic clock pin loads or shifts the shadow register on the rising edge of DCLK.

Q3-Q0 — Qn represents the data outputs of the output register. During a shadow register load these pins are the internal data inputs to the shadow register.

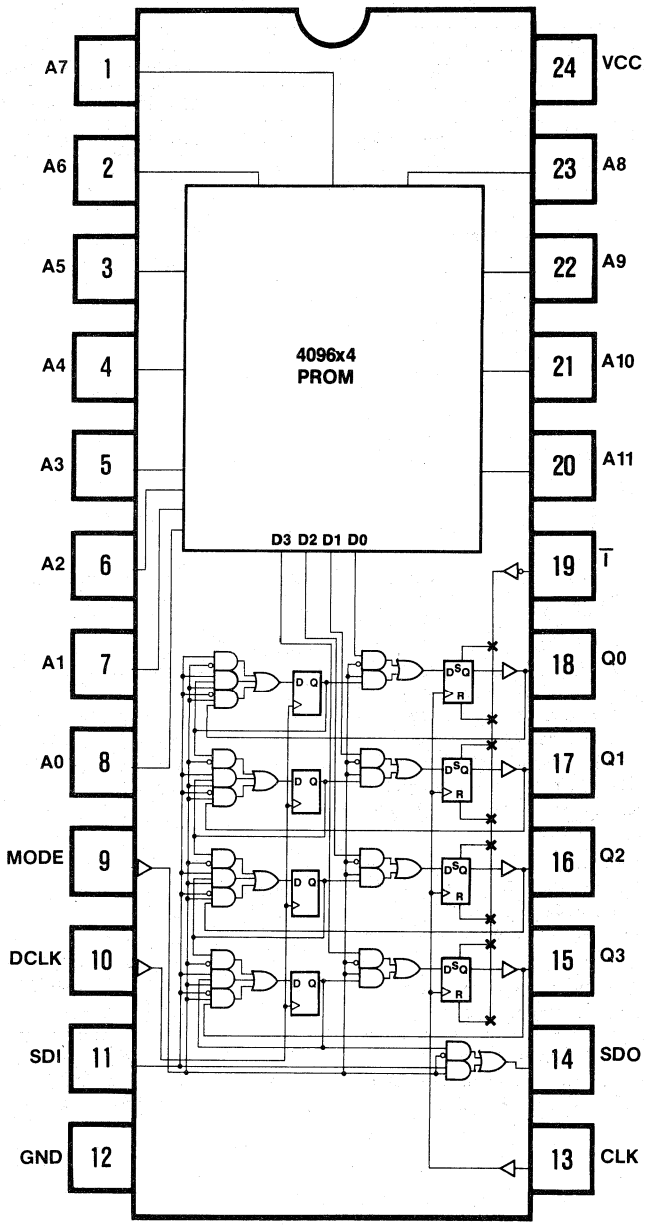
S3-S0 — Sn represents the internal shadow register outputs.

A11-A0 — An represents the address inputs to the PROM array.

$\overline{I}$ — The asynchronous output register initialization input pin operates independent of CLK. When $\overline{I}$ is LOW, the output register is loaded with a user programmable initialization word. Programmable initialization is a super set of preset and clear functions, and can be used to generate any microinstruction for system reset or interrupt.

Logic Diagram

4096x4 Diagnostic PROM
with Asynchronous Initialization



Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5 V to 7 V	12 V
Input voltage	-1.5 V to 7 V	7 V
Input current	-30 mA to +5 mA	
Off-state output voltage	-0.5 V to 5.5 V	12 V
Storage temperature	-65° to +150°C	

3

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP†	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP†	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	-55	25	125	0	25	75	°C
t_w	Width of CLK (HIGH or LOW)	25	10		20	10		ns
t_{su}	Set up time from address to CLK	45	25		40	25		ns
t_h	Hold time for CLK	0	-15		0	-15		ns
t_{wd}	Width of DCLK (HIGH or LOW)	45	15		40	15		ns
t_{sud}	Set up time from control inputs (SDI, MODE) to CLK, DCLK	50	20		45	20		ns
t_{hd}	Hold time for DCLK	0	-5		0	-5		ns
t_{iw}	Initialization pulse width (LOW)	25	10		20	10		ns
t_{ir}	Initialization recovery time	45	25		40	25		ns

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2.0			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA			-1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX			40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	Com I_{OL} = 24 mA			0.5	V
			Mil I_{OL} = 16 mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	Com I_{OH} = -3.2 mA	2.4			V
			Mil I_{OH} = -2 mA				
I_{OS}	Output short-circuit current*	V_{CC} = MAX	V_O = 0 V	-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX. All inputs TTL. All outputs open.			140	190	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

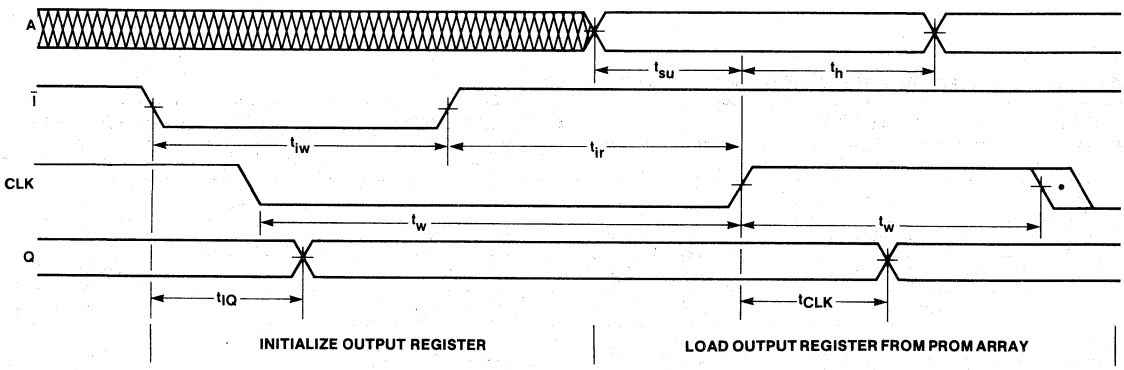
† Typicals at 5.0 V V_{CC} and 25°C T_A.

Switching Characteristics Over Operating Conditions and Using Standard Test Load

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP†	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP†	COMMERCIAL MAX	UNIT
t_{CLK}	CLK to output		11	25		11	20	ns
t_{IQ}	Initialization to output delay		23	40		23	35	ns
f_{MAXD}	Maximum diagnostic clock frequency	7	18		10	18		MHz
t_{DS}	DCLK to SDO delay (MODE = LOW)		17	35		17	30	ns
t_{SS}	SDI to SDO delay (MODE = HIGH)		16	30		16	25	ns
t_{MS}	MODE to SDO delay		14	30		14	25	ns

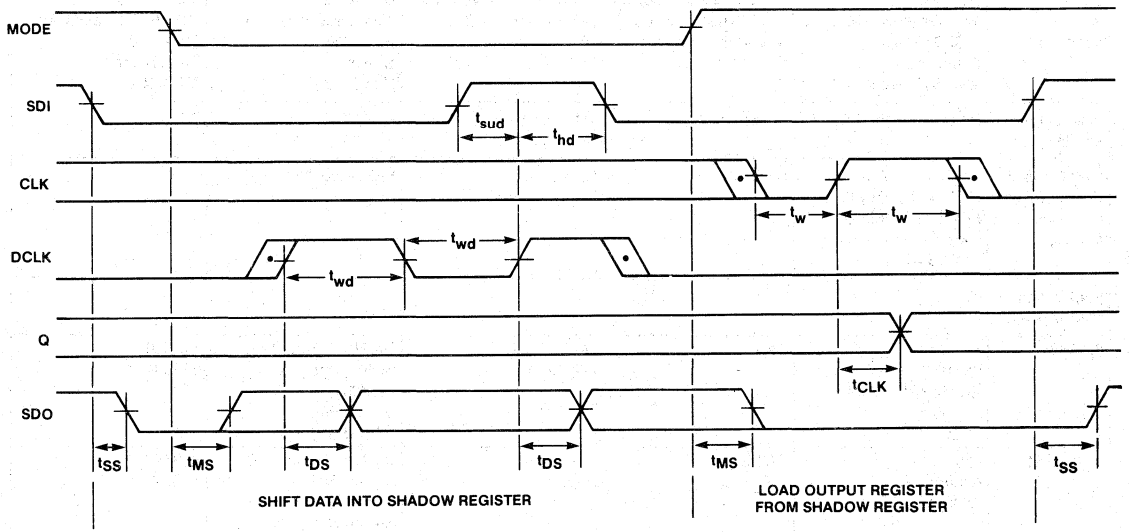
† Typicals at 5.0 V V_{CC} and 25°C T_A.

Definition of Waveforms

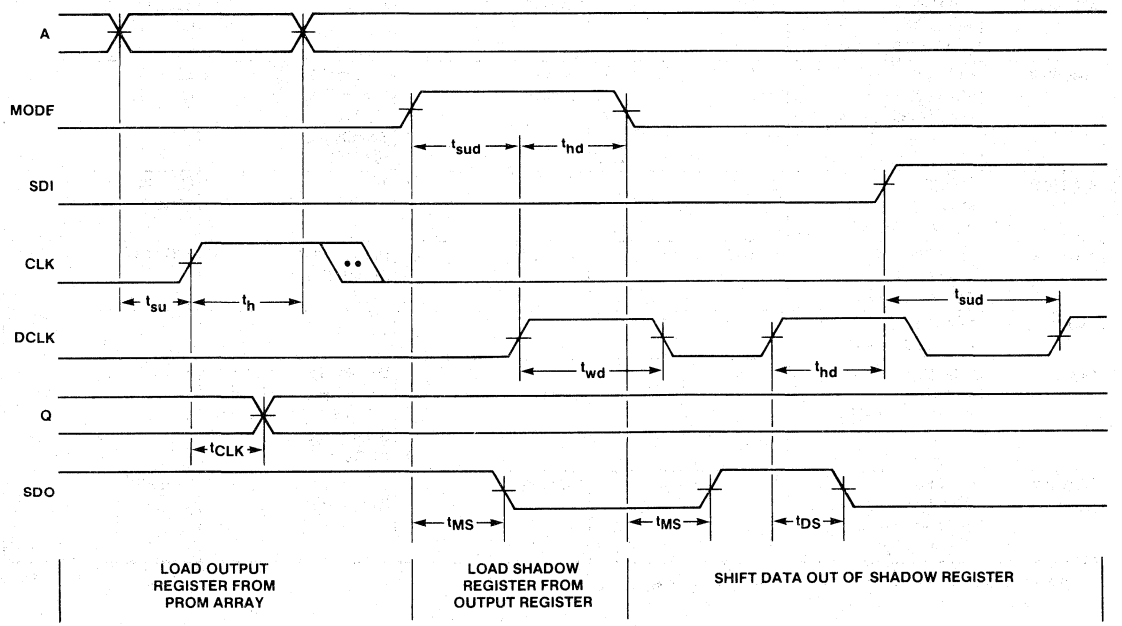


NORMAL PROM OPERATION (MODE = LOW)

Definition of Waveforms



SYSTEM CONTROL



SYSTEM OBSERVATION

Monolithic Memories PROM Programmer Reference Chart

Source and Location	Data I/O Corp. 10525 Willows Rd. N.E. P.O. Box 97046 Redmond WA 98073-9746	Kontron Electronics Inc. 1230 Charleston Rd. Mountain View CA 94039	Stag Microsystems Inc. 528-5 Weddell Dr. Sunnyvale CA 94089	Digelec Inc. 1602 Lawrence Ave. Suite 113 Ocean NJ 07712	Varix Corp. 1210 E. Campbell Rd. Suite 100 Richardson TX 75081
Programmer Model(s)	Model 19/29A/29B	Model MPP-80S	Model PPX Model PPZ	UP803	OMNI
MMI Generic Bipolar PROM Personality Module	UniPak Rev 10 UniPak II Rev 07 (Not all PROMs are supported by earlier UniPak revisions)	MOD16	Zm 2000	FAM Mod. No. 12	
Socket Adapter(s) and Device Code					
63S080/81	F18 P02 Model 22A - Adapter 351A-064	SA3	AM110-2 Code 21	DA No. 2 Pinout 1A Switch Pos. 0-7 (63S080) Switch Pos. 0-6 (63S081)	63S080 63S081
63S140/41	F18 P01 Model 22A - Adapter 351A-064	SA4-2	AM130-2 Code 21	DA No. 1 Pinout 1B Switch Pos. 0-7 (63S140) Switch Pos. 0-6 (63S141)	63S140 63S141
63S240/41	F18 P03 Model 22A - Adapter 351A-064	SA4-1	AM130-3 Code 21	DA No. 1 Pinout 1D Switch Pos. 2-15 (63S240) Switch Pos. 2-14 (63S241)	63S240 63S241
63S280/81	F18 P08 Model 22A - Adapter 351A-064	SA6-1	Code 21	†	63S280 63S281
63S440/41	F18 P05 Model 22A - Adapter 351A-064	SA4	AM140-2 Code 21	DA No. 3 Pinout 1E Switch Pos. 0-7 (63S440) Switch Pos. 0-6 (63S441)	63S440 63S441
63S480/81	F18 P09 Model 22A - Adapter 351A-064	SA6	Code 21	†	63S480 63S481
63RA481	FEC P65 Model 22A - Adapter 351A-074	SA31-2	Code 21	Pinout 1H Switch Pos. 5-14	63RA481
63DA441/42	FAA PAC Adapter 351A-073	†	†	†	†
63S841	F18 P06 Model 22A - Adapter 351A-064	SA4-4	AM 140-3 Code 21	DA No. 3 Pinout 1L Switch Pos. 5-15 (63S840) Switch Pos. 5-14 (63S841)	63S841
63RS881	F18 P86 Model 22A - Adapter 351A-074 (300 mil pkg)	†	Code 21	DA No. 64 Switch Pos. 0-12	63RS881

† Contact manufacturer for availability and programming information.

Monolithic Memories PROM Programmer Reference Chart

Source and Location	Data I/O Corp. 10525 Willows Rd. N.E. P.O. Box 97046 Redmond WA 98073-9746	Kontron Electronics Inc. 1230 Charleston Rd. Mountain View CA 94039	Stag Microsystems Inc. 528-5 Weddell Dr. Sunnyvale CA 94089	Digelec Inc. 1602 Lawrence Ave. Suite 113 Ocean NJ 07712	Varix Corp. 1210 E. Campbell Rd. Suite 100 Richardson TX 75081
Programmer Model(s)	Model 19/29A/29B	Model MPP-80S	Model PPX Model PPZ	UP803	OMNI
MMI Generic Bipolar PROM Personality Module	UniPak Rev 10 UniPak II Rev 07 (Not all PROMs are supported by earlier UniPak revisions)	MOD16	Zm 2000	FAM Mod. No. 12	
Socket Adapter(s) and Device Code					
63DA841	FAA PAD Adapter 351A-073	†	†	†	†
63S1641	F18 P53 Model 22A - Adapter 351A-064	SA20	AM 120-6 Code 21	DA No. 70 Switch Pos. 4-12	63S1641
63S1681	F18 P21	SA5-4	AM 100-5 Code 21	DA No. 7	63S1681
63RA1681 **63RS1681**	F18 PA3	†	Code 21	DA No. 64	63RA1681 63RS1681
63D1641	FB2 P80 Adapter 351A-073	†	Code 21	†	63D1641
63DA1643	FAA P87 Adapter 351A-073	†	†	†	†
63S3281	F18 P63	†	Code 21	DA No. 64 Pinout 47 Switch Pos. 0-4	63S3281

† Contact manufacturer for availability and programming information.


IMPORTANT.
NOTES

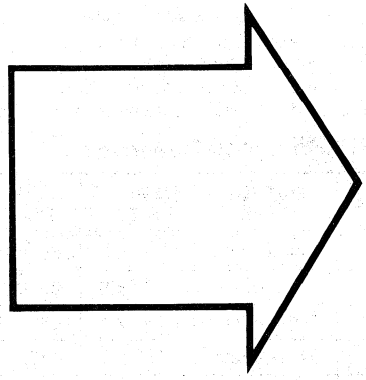


Table of Contents

PLE DEVICES

PLE to PROM Cross Reference

TEMP. RANGE	PLE NUMBER	INPUTS	OUTPUTS	OUTPUT TYPE	MEMORY SIZE	PROM NUMBER	PACKAGE
Com.	PLE5P8C	5	8	Three-State	32 x 8	63S081	16N,J,(20),(NL)
	PLE5P8AC	5	8	Three-State	32 x 8	63S081A	16N,J,(20),(NL)
	PLE8P4C	8	4	Three-State	256 x 4	63S141A	16N,J,(20),(NL)
	PLE8P8C	8	8	Three-State	256 x 8	63S281A	20N,J,NL
	PLE9P4C	9	4	Three-State	512 x 4	63S241A	16N,J,(20),(NL)
	PLE9P8C	9	8	Three-State	512 x 8	63S481A	20N,J,NL
	PLE10P4C	10	4	Three-State	1024 x 4	63S441A	18N,J,(20),(NL)
	PLE10P8C	10	8	Three-State	1024 x 8	63S881A	24N,J,NS,JS,(28),(NL)
	PLE11P4C	11	4	Three-State	2048 x 4	63S841A	18N,J,(20),(NL)
	PLE11P8C	11	8	Three-State	2048 x 8	63S1681A	24N,J,NS,JS,(28),(NL)
	PLE12P4C	12	4	Three-State	4096 x 4	63S1641A	20N,J,NL
	PLE12P8C	12	8	Three-State	4096 x 8	63S3281A	24N,J,(28),(NL)
	PLE9R8C	9	8	Register	512 x 8	63RA481A	24NS,JS,(28),(NL)
	PLE10R8C	10	8	Register	1024 x 8	63RS881A	24NS,JS,(28),(NL)
	PLE11RA8C	11	8	Register	2048 x 8	63RA1681A	24NS,JS,(28),(NL)
	PLE11RS8C	11	8	Register	2048 x 8	63RS1681A	24NS,JS,(28),(NL)
Mil.	PLE5P8M	5	8	Three-State	32 x 8	53S081	16J,W,(20),(L)
	PLE8P4M	8	4	Three-State	256 x 4	53S141A	16J,W,(20),(L)
	PLE8P8M	8	8	Three-State	256 x 8	53S281A	20J,W,L
	PLE9P4M	9	4	Three-State	512 x 4	53S241A	16J,W,(20),(L)
	PLE9P8M	9	8	Three-State	512 x 8	53S481A	20J,F,L
	PLE10P4M	10	4	Three-State	1024 x 4	53S441A	18J,W,(20),(L)
	PLE10P8M	10	8	Three-State	1024x8	53S881A	24JS,J,W,(28),(L)
	PLE11P4M	11	4	Three-State	2048 x 4	53S841A	18J,W,(28),(L),(20),(L)*
	PLE11P8M	11	8	Three-State	2048 x 8	53S1681A	24JS,J,W,(28),(L)
	PLE12P4M	12	4	Three-State	4096 x 4	53S1641A	20J
	PLE12P8M	12	8	Three-State	4096 x 8	53S3281A	24J,W,(28),(L)
	PLE9R8M	9	8	Register	512 x 8	53RA481A	24JS,W,(28),(L)
	PLE10R8M	10	8	Register	1024 x 8	53RS881A	24JS,J,W,(28),(L)
	PLE11RA8M	11	8	Register	2048 x 8	53RA1681A	24JS,W,(28),(L)
	PLE11RS8M	11	8	Register	2048 x 8	53RS1681A	24JS,W,(28),(L)

* The PLE11P4M is available in a 20- or 28-pin Leadless Chip Carrier

Programmable Logic Element
PLE™ Circuit Family

Features/Benefits

- Programmable replacement for conventional TTL logic
- Reduces IC inventories and simplifies their control
- Expedites and simplifies prototyping and board layout
- Saves space with 0.3-inch SKINNYDIP® packages (except PLE 12P8)
- Programmed on standard PROM programmers
- Test and simulation made simple with PLEASM™ software
- Low-current PNP inputs
- Three-state outputs
- Reliable TiW fuses guarantee >98% programming yield

Ordering Information

PLE5P8 A C N STD

PREFIX
PLE = Programmable Logic Element

NUMBER OF INPUTS

OUTPUT TYPE
P = Non Registered
R = Registered
RA = Registered Asynchronous Enable
RS = Registered Synchronous Enable

NUMBER OF OUTPUTS

PERFORMANCE
Blank = Standard
A = Enhanced

TEMPERATURE CODE
C = 0°C to +75°C
M = −55°C to +125°C

PACKAGE TYPE
N = Plastic DIP
NS = Plastic SKINNYDIP
J = Ceramic DIP
JS = Ceramic SKINNYDIP
F = Ceramic Solder Seal Flat Pack
L = Leadless Chip Carrier
NL = Plastic Leaded Chip Carrier
W = Cerpack

PROCESSING
STD = Standard
XXXX = Mil-Std-883, Class B

4

PLE Circuit Selection Guide

PART NUMBER	INPUTS	OUTPUTS	PRODUCT TERMS	OUTPUT REGISTERS	t_{PD} (ns) MAX*
PLE5P8	5	8	32		25
PLE5P8A	5	8	32		15
PLE8P4	8	4	256		30
PLE8P8	8	8	256		28
PLE9P4	9	4	512		35
PLE9P8	9	8	512		30
PLE10P4	10	4	1024		35
PLE10P8	10	8	1024		30
PLE11P4	11	4	2048		35
PLE11P8	11	8	2048		35
PLE12P4	12	4	4096		35
PLE12P8	12	8	4096		35
PLE9R8	9	8	512	8	15
PLE10R8	10	8	1024	8	15
PLE11RA8	11	8	2048	8	15
PLE11RS8	11	8	2048	8	15

* Clock to output time for registered outputs.

Note: Commercial limits specified.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376
TWX: 910-338-2374
Monolithic Memories MMI

PLE Means Programmable Logic Element

Joining the world of IdeaLogic™ is a new generation of High-speed PROMs which the designer can use as *Programmable Logic Elements*. The combination of PLE circuits as logic elements with PAL devices can greatly enhance system speed while providing almost unlimited design freedom.

Basically, PLE circuits are ideal when a large number of product terms is required. On the other hand, a PAL device is best suited for situations when many inputs are needed.

The PLE circuit transfer function is the familiar OR of products, Like the PAL device, the PAE circuit has a single array of fusible links. Unlike the PAL device, the PLE circuits have a programmable OR array driven by a fixed AND array (the PAL device is a programmed AND array driving a fixed OR array).

PRODUCT TERM AND INPUT LINES

	PLE	PAL
Product Terms	32 to 4096	1 to 16
Input Lines	5 to 12	6 to 64

The PLE family features common electrical parameters and programming algorithm, low-current PNP inputs, full Schottky clamping and three-state outputs.

The entire PLE family is programmed on conventional PROM programmers with the appropriate personality cards and socket adapters.

Registered PLE Circuits

The registered PLE circuits have on-chip "D" type registers, versatile output enable control through synchronous and asynchronous enable inputs, and flexible start-up sequencing through programmable initialization.

Data is transferred into the output registers on the rising edge of the clock. Provided that the asynchronous ($\overline{E}$) and synchronous ($\overline{ES}$) enables are Low, the data will appear at the outputs. Prior to the positive clock edge, register data are not affected by changes in addressing or synchronous enable inputs.

Data control is made flexible with synchronous and asynchronous enable inputs. Outputs may be set to the high-impedance state at any time by setting $\overline{E}$ to a High or if $\overline{ES}$ is High when the rising clock edge occurs. When V_{CC} power is first applied the synchronous enable flip-flop will be in the set condition causing the outputs to be in the high-impedance state.

A flexible initialization feature allows start-up and time-out sequencing with 1:16 programmable words to be loaded into the output registers. With the synchronous INITIALIZE ($\overline{IS}$) pin Low, one of the 16 initialize words, addressed through pins 5,6,7 and 8 will be set in the output registers independent of all other input pins. The unprogrammed state of $\overline{IS}$ words are Low, presenting a CLEAR with $\overline{IS}$ pin Low. With all $\overline{IS}$ column words (A3-AO) programmed to the same pattern, the $\overline{IS}$ function will be independent of both row and column addressing and may be used as a single pin control. With all $\overline{IS}$ words programmed High a PRESET function is performed.

The PLE9R8 has asynchronous PRESET and CLEAR functions. With the chip enabled, a Low on the $\overline{PR}$ input will cause all outputs to be set to the High state. When the $\overline{CLR}$ input is set Low the output registers are reset and all outputs will be set to the Low state. The $\overline{PR}$ and $\overline{CLR}$ functions are common to all output registers and independent of all other data input states.

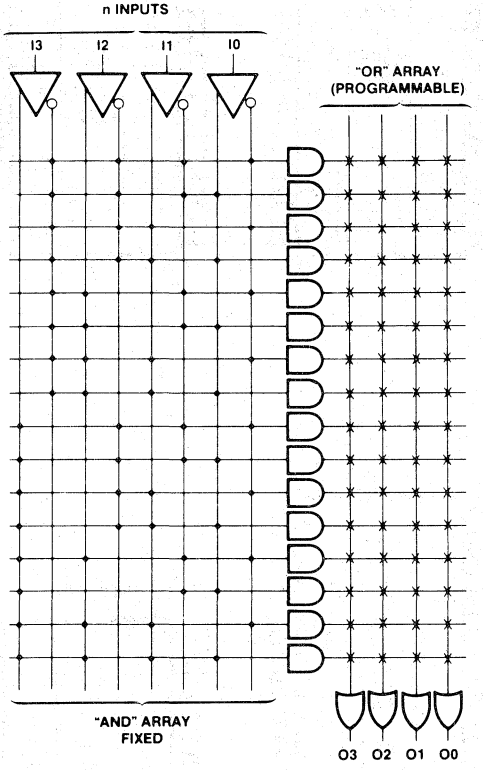
	AND	OR	OUTPUT OPTIONS
PLE	Fixed	Prog	TS, Registered Outputs, Fusible Polarity
FPLA	Prog	Prog	TS, OC, Fusible Polarity
FPGA	Prog	Prog	TS, OC, Fusible Polarity
FPLS	Prog	Prog	TS, Registered Feedback I/O
PAL	Prog	Fixed	TS, Registered Feedback I/O Fusible Polarity

PLEASM™ Software

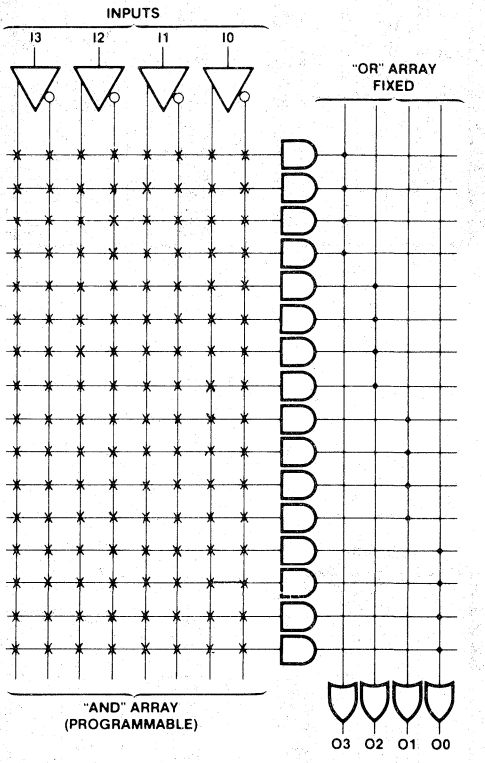
Software that makes programmable logic easy.
Monolithic Memories has developed a software tool to assist in designing and programming PROMs as PLE circuits. This package called "PLEASM" (PLE Assembler) is available for several computers including the VAX/VMS and IBM PC/DOS. PLEASM software converts design equation (Boolean and arithmetic) into truth tables and formats compatible with PROM programmers. A simulator is also provided to test a design using a Function Table before actually programming the PLE circuit.

PLEASM software may be requested through the Monolithic Memories IdeaLogic Exchange.

PLE (PROM)



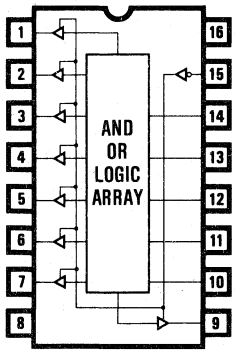
PAL Device



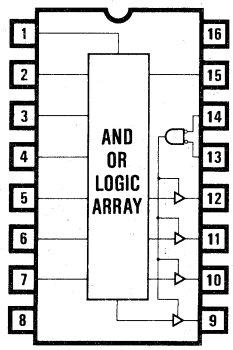
Note: • = Hardwired connection
X = Programmable fuse with a diode

Logic Symbols

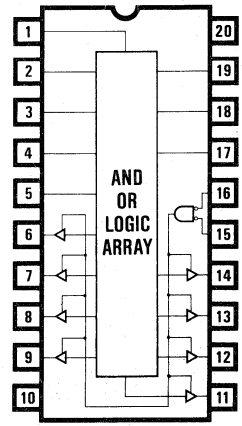
PLE5P8/A



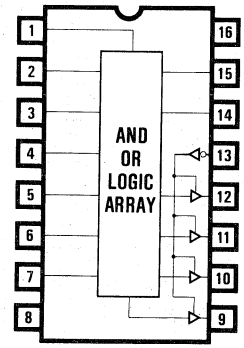
PLE8P4



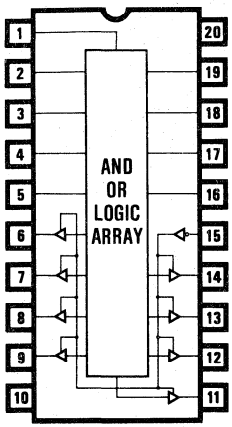
PLE8P8



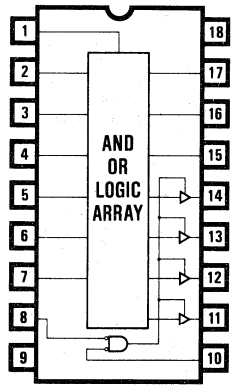
PLE9P4



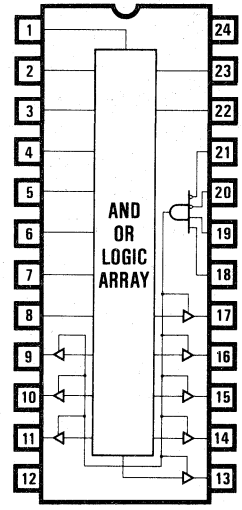
PLE9P8



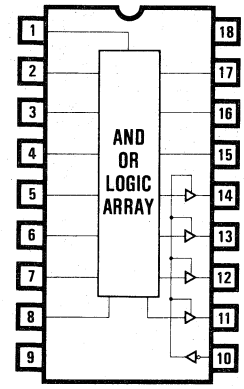
PLE10P4



PLE10P8

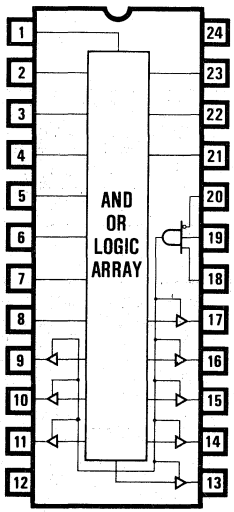


PLE11P4

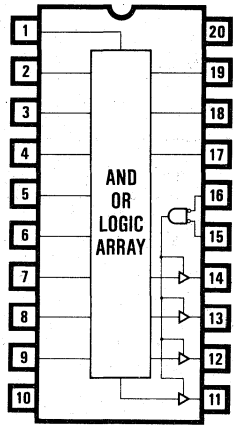


Logic Symbols

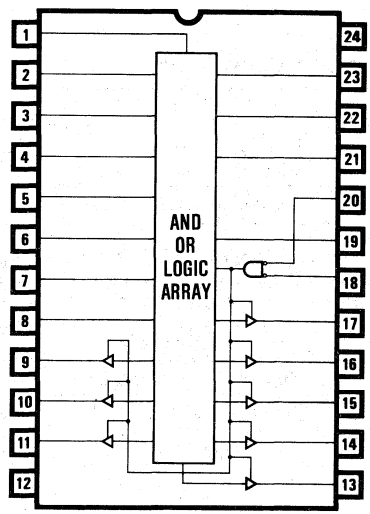
PLE11P8



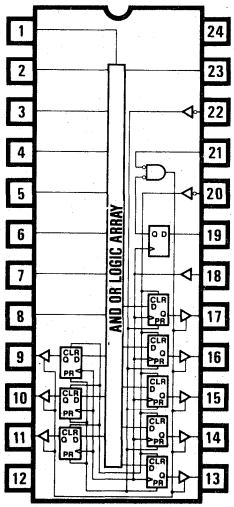
PLE12P4



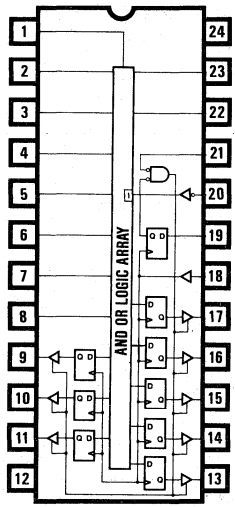
PLE12P8



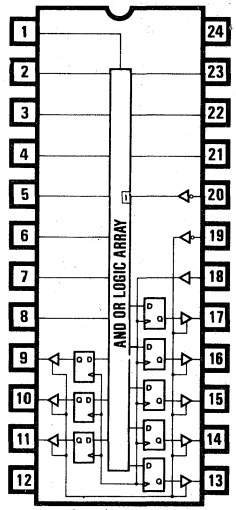
PLE9R8



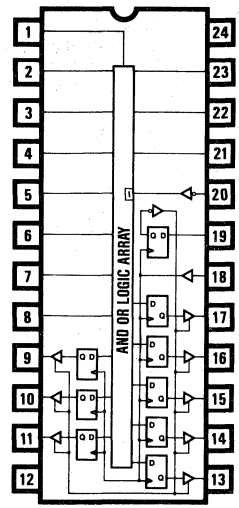
PLE10R8



PLE11RA8



PLE11RS8



* Initialize Pin.

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5 V to 7 V	12 V
Input voltage	-1.5 V to 7 V	7 V
Off-state output voltage	-0.5 V to 5.5 V	12 V
Storage temperature	-65° to +150°C	

Operating Conditions

SYMBOL	PARAMETER	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	MILITARY MIN	MILITARY NOM	MILITARY MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	4.5	5	5.5	V
T_A	Operating free-air temperature	0	25	75	-55	25	125	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA				-1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V				-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC}				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16 mA	Com			0.45	V
				Mil			0.5	
V_{OH}	High-level output voltage	V_{CC} = MIN	Com I_{OH} = -3.2 mA		2.4			V
			Mil I_{OH} = -2 mA					
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4 V				-40	μA
I_{OZH}			V_O = 2.4 V				40	
I_{OS}	Output short-circuit current*	V_{CC} = 5 V	V_O = 0 V		-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX All inputs grounded; all outputs open	5P8			90	125	mA
			5P8A			90	125	
			8P4			80	130	
			8P8			90	140	
			9P4			80	130	
			9P8			104	155	
			10P4			95	140	
			10P8			92	160	
			11P4			110	150	
			11P8			135	185	
			12P4			130	175	
			12P8			150	190	
		V_{CC} = MAX All inputs TTL; all outputs open	9R8			130	180	
			10R8			130	180	
			11RA8			140	185	
			11RS8			140	185	

† Typicals at 5.0 V V_{CC} and 25°C T_A.

Switching Characteristics Over Commercial Operating Conditions

DEVICE TYPE	t_{PD} (ns) PROPAGATION DELAY MAX	t_{PZX} AND t_{PXZ} (ns) INPUT TO OUTPUT ENABLE/DISABLE TIME MAX
5P8AC	15	20
5P8C	25	20
8P4C	30	20
8P8C	28	25
9P4C	35	20
9P8C	30	25
10P4C	35	25
10P8C	30	25
11P4C	35	25
11P8C	35	25
12P4C	35	25
12P8C	35	30

Switching Characteristics Over Military Operating Conditions

DEVICE TYPE	t_{PD} (ns) PROPAGATION DELAY MAX	t_{PZX} AND t_{PXZ} (ns) INPUT TO OUTPUT ENABLE/DISABLE TIME MAX
5P8M	35	30
8P4M	40	30
8P8M	40	30
9P4M	45	30
9P8M	40	30
10P4M	50	30
10P8M	45	30
11P4M	50	30
11P8M	50	30
12P4M	50	30
12P8M	40	35

Operating Conditions

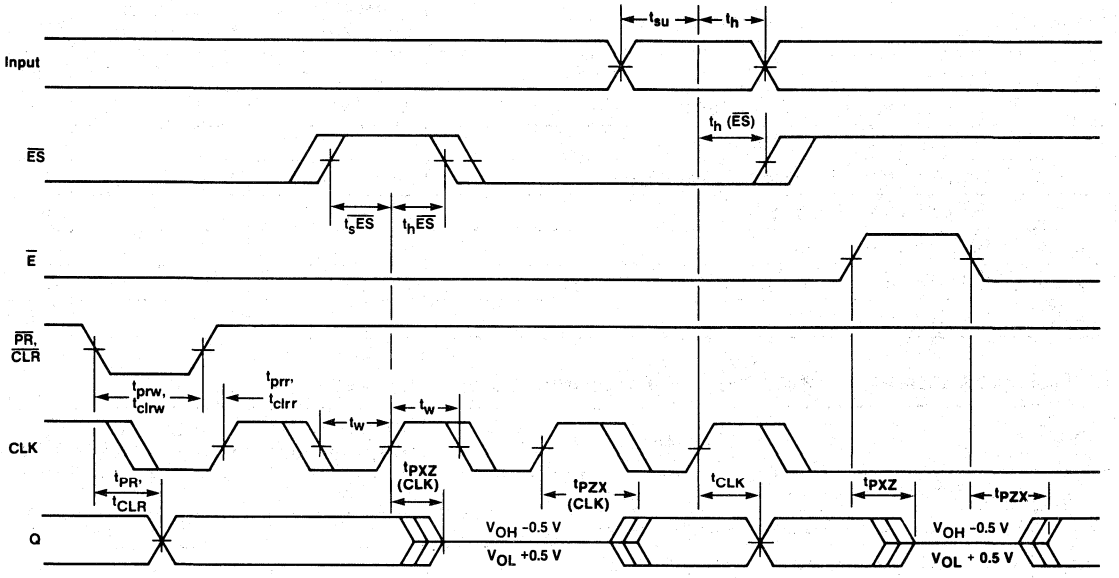
SYMBOL	PARAMETER	COMMERCIAL MIN	COMMERCIAL TYP*	COMMERCIAL MAX	MILITARY MIN	MILITARY TYP*	MILITARY MAX	UNIT
t_w	Width of clock (High or Low)	20	10		20	10		ns
t_{prw} t_{clrw}	Width of preset or clear (Low) to Output (High or Low)	20	10		20	10		ns
t_{prr} t_{clrr}	Recovery from preset or clear (Low) to clock High	20	11		25	11		ns
t_{su}	Setup time from input to clock	30	22		35	22		ns
$t_{s(\overline{ES})}$	Setup time from $\overline{ES}$ to clock	10	7		15	7		ns
t_h	Hold time from input to clock	0	-5		0	-5		ns
$t_{h(\overline{ES})}$	Hold time from $\overline{ES}$ to clock	5	-3		5	-3		ns

Switching Characteristics Over Operating Conditions and using Standard Test Load

SYMBOL	PARAMETER	COMMERCIAL MIN	COMMERCIAL TYP*	COMMERCIAL MAX	MILITARY MIN	MILITARY TYP*	MILITARY MAX	UNIT
t_{CLK}	Clock to output delay		11	15		11	20	ns
t_{PR}	Preset to output delay		15	25		15	25	ns
t_{CLR}	Clear to output delay		18	25		18	35	ns
t_{PZX} (CLK)	Clock to output enable time		14	25		14	30	ns
t_{PXZ} (CLK)	Clock to output disable time		14	25		14	30	ns
t_{PZX}	Input to output enable time		10	20		10	25	ns
t_{PXZ}	Input to output disable time		10	20		10	25	ns

† Typicals at 5.0 V V_{CC} and 25°C T_A.

Definition of Waveforms



NOTES: 1. Input pulse amplitude 0 V to 3.0 V.

2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
3. Input access measured at the 1.5 V level.
4. Switch S_1 is closed. C_L = 30 pF and outputs measured at 1.5 V level for all tests except t_{PXZ} and t_{PZX}.
5. t_{PZX} and $t_{PZX(CLK)}$ are measured at the 1.5 V output level with C_L = 30 pF. S_1 is open for high impedance to "1" test and closed for high impedance to "0" test.

   t_{PXZ} and $t_{PXZ(CLK)}$ are tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH}-0.5 V output level; S_1 is closed for "0" to high impedance test measured at V_{OL}+0.5 V output level.

Operating Conditions

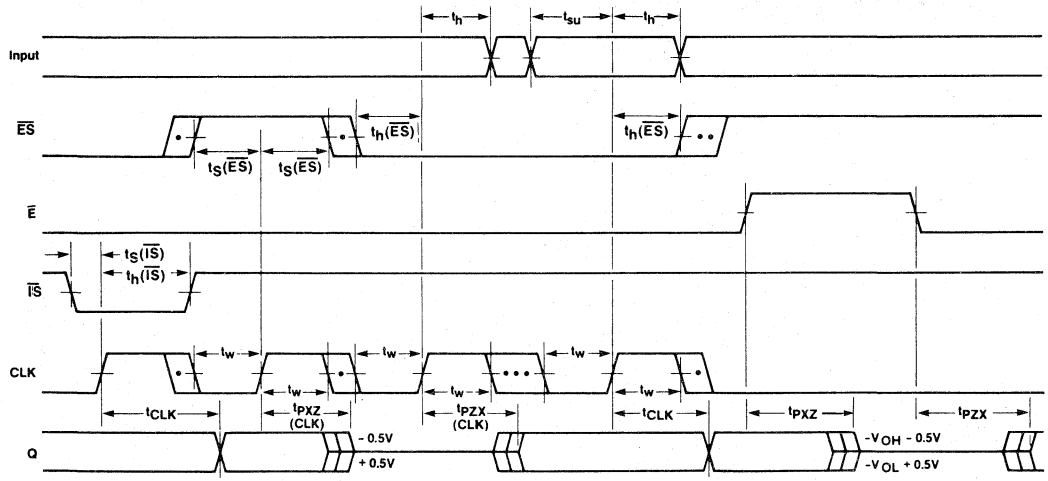
SYMBOL	PARAMETER	COMMERCIAL MIN	TYP*	MAX	MILITARY MIN	TYP*	MAX	UNIT
t_w	Width of clock (High or Low)	20	10		20	10		ns
t_{su}	Setup time from input to clock (10R8)	30	25		40	25		ns
t_{su}	Setup time from input to clock (11RA8, 11RS8)	35	28		40	28		ns
t_s ($\overline{ES}$)	Setup time from $\overline{ES}$ to clock (except 11RA8)	15	7		15	8		ns
t_s ($\overline{IS}$)	Setup time from $\overline{IS}$ to clock	25	20		30	20		ns
t_h	Hold time input to clock	0	-5		0	-5		ns
t_h ($\overline{ES}$)	Hold time ($\overline{ES}$) (except 11RA8)	5	-3		5	-3		ns
t_h ($\overline{IS}$)	Hold time ($\overline{IS}$)	0	-5		0	-5		ns

Switching Characteristics Over Operating Conditions and using Standard Test Load

SYMBOL	PARAMETER	COMMERCIAL MIN	TYP*	MAX	MILITARY MIN	TYP*	MAX	UNIT
t_{CLK}	Clock to output delay		10	15		10	20	ns
t_{PZX} (CLK)	Clock to output enable time (except 11RA8)		17	25		18	30	ns
t_{PXZ} (CLK)	Clock to output disable time (except 11RA8)		17	25		18	30	ns
t_{PZX}	Input to output enable time (except 11RS8)		17	25		17	30	ns
t_{PXZ}	Input to output disable time (except 11RS8)		17	25		17	30	ns

* Typicals at 5.0 V V_{CC} and 25°C T_A.

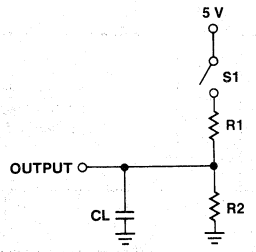
Definition of Waveforms



NOTES:
1. Input pulse amplitude 0 V to 3.0 V.
2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
3. Input access measured at the 1.5 V level.
4. Switch S_1 is closed. C_L = 30 pF and outputs measured at 1.5 V level for all tests except t_{PZX} and t_{PXZ}.
5. t_{PZX} and $t_{PZX(CLK)}$ are measured at the 1.5 V output level with C_L = 30 pF. S_1 is open for high impedance to "1" test and closed for high impedance to "0" test.

   t_{PXZ} and $t_{PXZ(CLK)}$ are tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH}-0.5 V output level; S_1 is closed for "0" to high impedance test measured at V_{OL}+0.5 V output level.

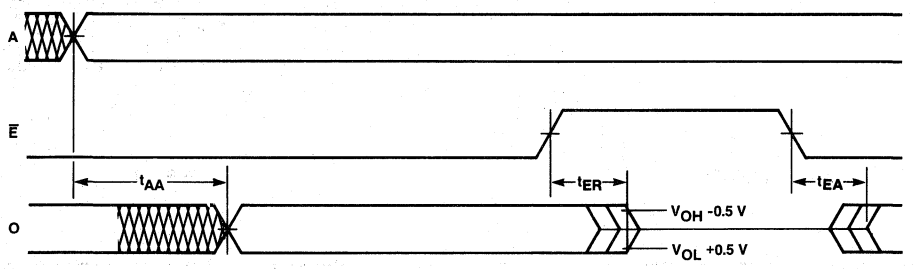
Switching Test Load



Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

Definition of Waveforms



NOTES: Apply to electrical and switching characteristics.

Typical at 5.0 V V_{CC} and 25°C T_A.

Measurements are absolute voltages with respect to the ground pin on the device and includes all overshoots due to system and/or tester noise. In all PLE devices unused inputs must be tied to either ground or V_{CC}. The series resistor required for unused inputs on standard TTL is NOT required for PLE devices, thus using less parts.

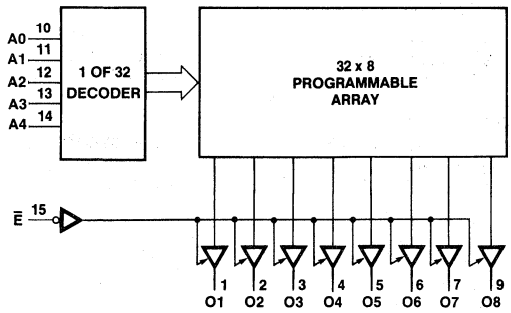
*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

For commercial operating range R_1 = 200 Ω, R_2 = 390 Ω. For military operating range R_1 = 300 Ω, R_2 = 600 Ω.

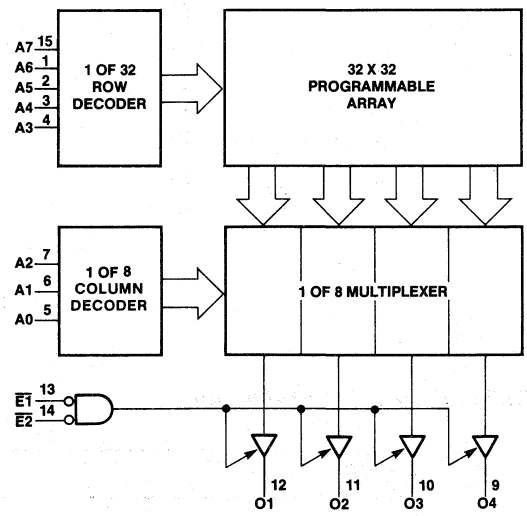
1. Input pulse amplitude 0 V to 3.0 V.
2. Input rise and fall times 2-5 ns from 0.8 to 2.0 V.
3. Input access measured at the 1.5 V level.
4. Data delay is tested with switch S_1 closed. C_L = 30 pF and measured at 1.5 V output level.
5. t_{PZX} is measured at the 1.5 V ouput level with C_L = 30 pF. S_1 is open for high-impedance to "1" test and closed for high-impedance to "0" test. t_{PXZ} is measured C_L = 5 pF. S_1 is open for "1" to high-impedance test, measured at V_{OH} −0.5 V output level; S_1 is closed for "0" to high-impedance test measured at V_{OL} +0.5 V output level.

Block Diagrams

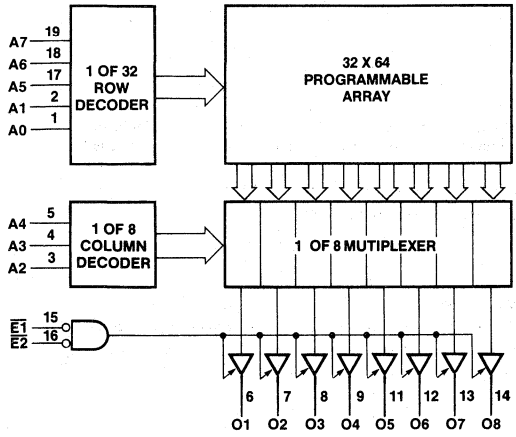
PLE5P8/A



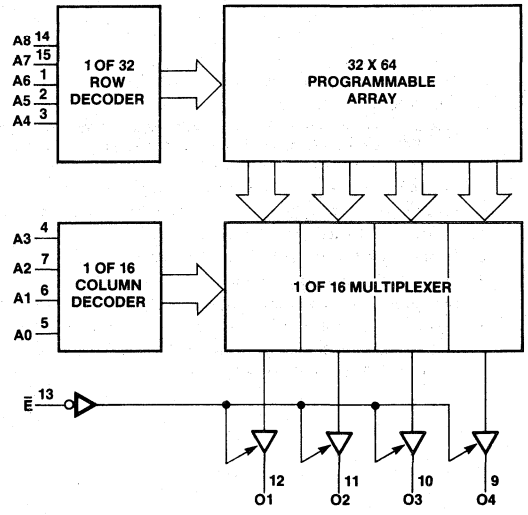
PLE8P4



PLE8P8

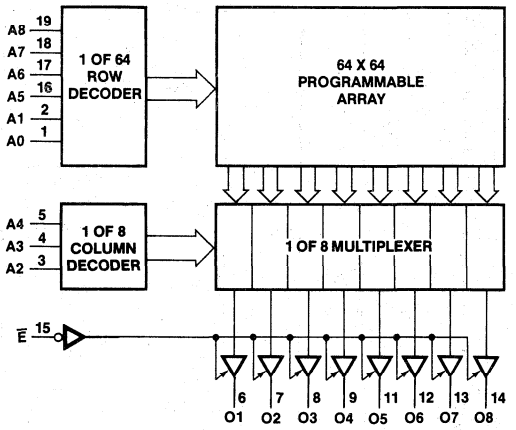


PLE9P4

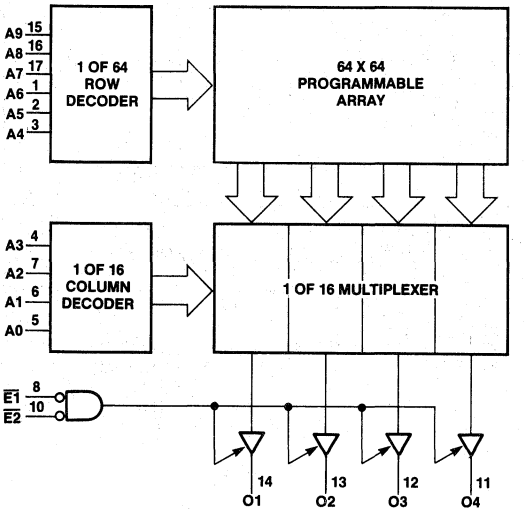


Block Diagrams

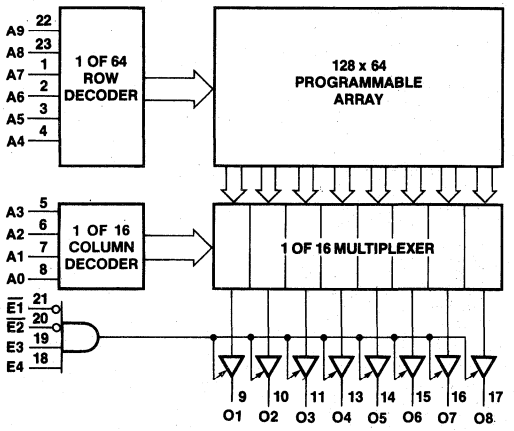
PLE9P8



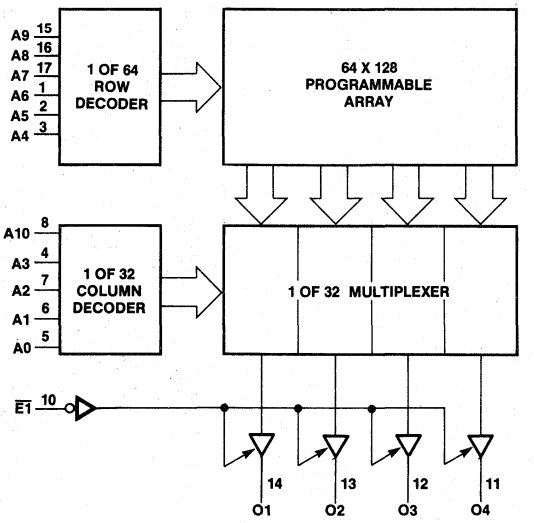
PLE10P4



PLE10P8

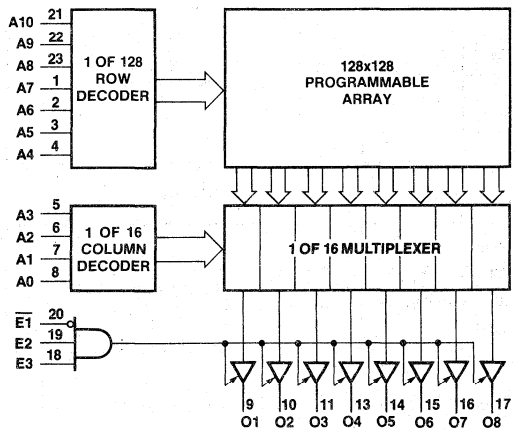


PLE11P4

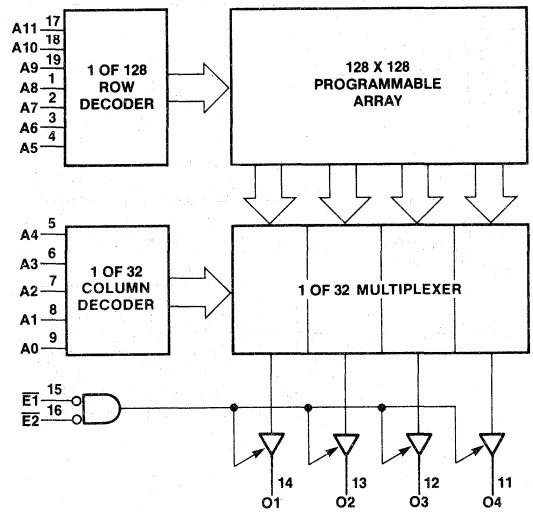


Block Diagrams

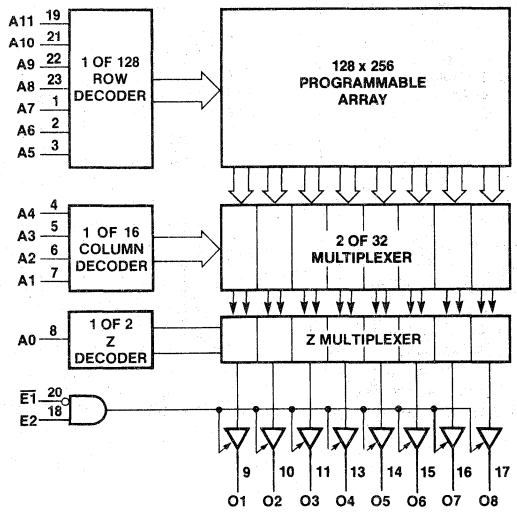
PLE11P8



PLE12P4

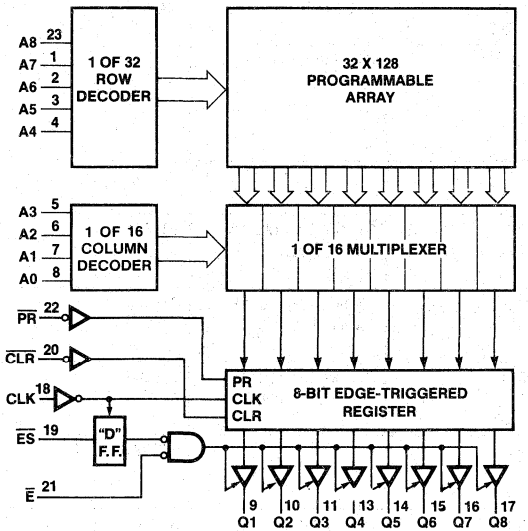


PLE12P8

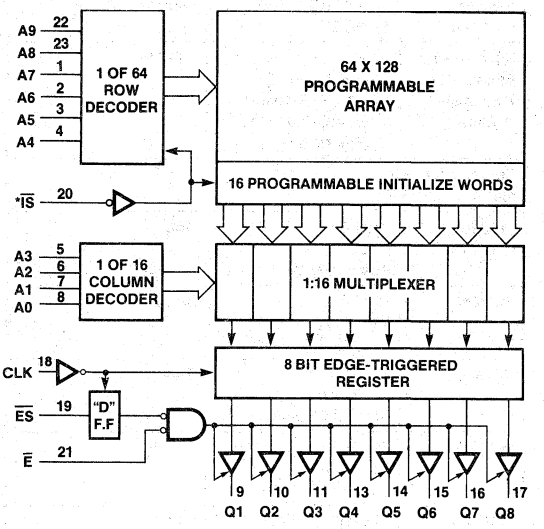


Block Diagrams

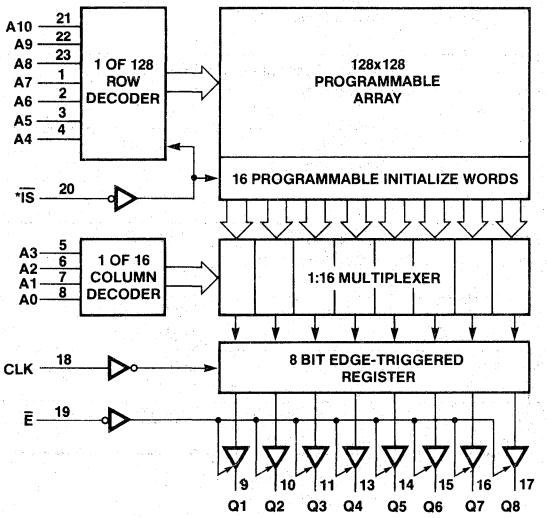
PLE9R8



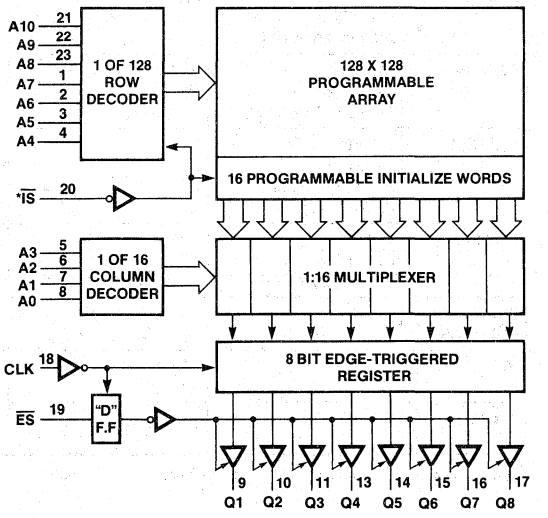
PLE10R8



PLE11RA8



PLE11RS8



*$\overline{IS}$ selects 1:16 programmable initialization words.

Monolithic Memories PLE Programmer Reference Chart

SOURCE AND LOCATION	Data I/O Corp. 10525 Willows Rd. N.E. P.O. Box 97046 Redmond WA 98073-9746	Kontron Electronics Inc. 1230 Charleston Rd. Mountain View CA 94039-7230	Stag Microsystems Inc. 528-5 Weddell Dr. Sunnyvale CA 94089	Digelec Inc. 1602 Lawrence Ave. Suite 113 Ocean NJ 07712	Varix Corp. 1210 E. Campbell Rd. Suite 100 Richardson TX 75081
Programmer Model(s)	Model 19/29A/29B Model 22	Model MMP-80S	Model PPX Model PPZ	UP803	OMNI
MMI Generic Bipolar PLE Personality Module	UniPak Rev 10 UniPak II Rev 07 (Not all PLE devices are supported by earlier UniPak revisions)	MOD16	Zm 2000	FAM Mod. No. 12	
Socket Adapter(s) and Device Code					
PLE5P8/ PLE5P8A	F18 P02 Model 22A- Adapter 351A-064	SA3	AM110-2 Code 21	DA No. 2 Pinout 1A Switch Pos. 0-6	63S081
PLE8P4	F18 P01 Model 22A- Adapter 351A-064	SA4-2	AM130-2 Code 21	DA No. 1 Pinout 1B Switch Pos. 0-6	63S141
PLE9P4	F18 P03 Model 22A- Adapter 351A-064	SA4-1	AM130-3 Code 21	DA No. 1 Pinout 1D Switch Pos. 2-14	63S241
PLE8P8	F18 P08 Model 22A- Adapter 351A-064	SA6-1	Code 21	†	63S281
PLE10P4	F18 P05 Model 22A- Adapter 351A-064	SA4	AM140-2 Code 21	DA No. 3 Pinout 1E Switch Pos. 0-6	63S441
PLE9P8	F18 P08 Model 22A- Adapter 351A-064	SA6	Code 21	†	63S481
PLE9R8	FEC P65 Model 22A- Adapter 351A-074	SA31-2	Code 21	Pinout 1H Switch Pos. 5-14	63RA481
PLE11P4	F18 P06 Model 22A- Adapter 351A-064	SA4-4	AM140-3 Code 21	DA No. 3 Pinout 1L Switch 5-14	63S841
PLE10R8	F18 P86 Model 22A- Adapter 351A-074 (300 mil pkg)	†	Code 21	DA No. 64† Switch Pos. 0-12	63RS881
PLE12P4	F18 P53 Model 22A- Adapter 351A-064	SA20	AM120-6 Code 21	DA No. 70 Switch Pos. 4-12	63S1641
PLE11RA8 PLE11RS8	F18 PA3	†	Code 21	DA No. 64	63RA1681 63RS1681
PLE11P8	F18P21	SA5-4	AM100-5 Code 21	DA No. 7	63S1681
PLE12P8	F18P63	†	Code 21	DA No. 64 Pinout 47 Switch Pos. 0-4	63S3281

† Contact manufacturer for availability and programming information.

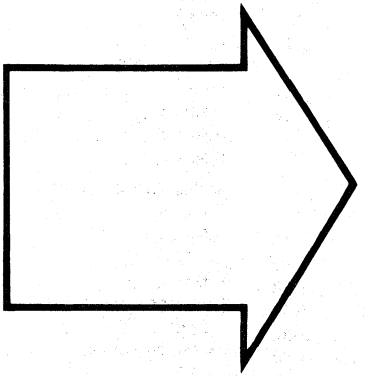
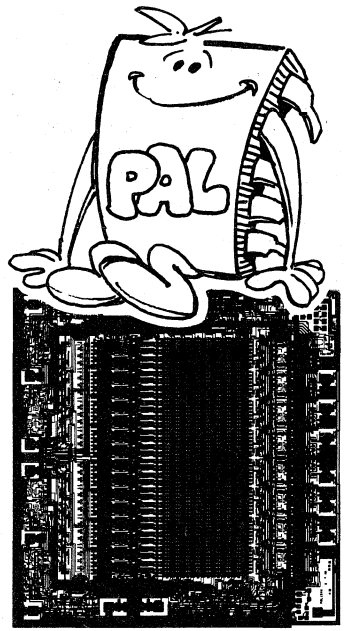


Table of Contents

Table of Contents

5



The PAL® Device Concept

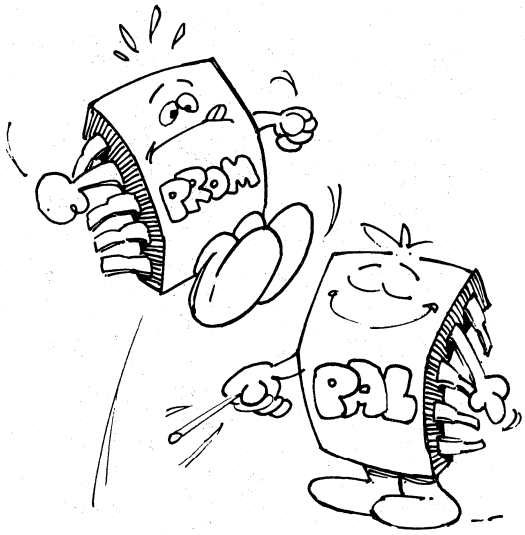
Monolithic Memories' family of PAL devices gives designers a powerful tool with unique capabilities for use in new and existing logic designs. The PAL device saves time and money by solving many of the system partitioning and interface problems brought about by increases in semiconductor device technology.

Rapid advances in large scale integration technology have led to larger and larger standard logic functions; single I.C.s now perform functions that formerly required complete circuit cards. While LSI offers many advantages, advances have been made at the expense of device flexibility. Most LSI devices still require large numbers of SSI/MSI devices for interfacing with user systems. Designers are still forced to turn to random logic for many applications.

The designer is confronted with another problem when a product is designed. Often the function is well defined and could derive significant benefits from fabrication as an integrated circuit. However, the design cycle for a custom circuit is long and the costs can be very high. This makes the risk significant enough to deter most users. The technology to support maximum flexibility combined with fast turnaround on custom logic has simply not been available. Monolithic Memories offers the programmable solution.

The PAL device family offers a fresh approach to using fuse programmable logic. PAL circuits are a conceptually unified group of devices which combine programmable flexibility with high speed and an extensive selection of interface options. PAL devices can lower inventory, cut design cycles and provide high complexity with maximum flexibility. These features, combined with lower package count and high reliability, truly make the PAL device a circuit designer's best friend.

The PAL Device—Teaching Old PROMs New Tricks



Monolithic Memories developed the modern PROM and introduced many of the architectures and techniques now regarded as industry standards. As the world's largest PROM manufacturer, Monolithic Memories has the proven technology and high volume production capability required to manufacture and support the PAL device.

The PAL device is an extension of the fusible link technology pioneered by Monolithic Memories for use in bipolar PROMs. The fusible link PROM first gave the digital systems designer the power to "write on silicon". In a few seconds he was able to transform a blank PROM from a general purpose device into one containing a custom algorithm, microprogram, or Boolean transfer function. This opened up new horizons for the use of PROMs in computer control stores, character generators, data storage tables and many other applications. The wide acceptance of this technology is clearly demonstrated by today's multi-million dollar PROM market.

The key to the PROM's success is that it allows the designer to customize the chip quickly and easily to fit his unique requirements. The PAL device extends this programmable flexibility by utilizing proven fusible link technology to implement logic functions. By using PAL circuits the designer can quickly and effectively implement custom logic varying in complexity from random gates to complex arithmetic functions.

ANDs and ORs

The PAL device implements the familiar sum-of-products logic by using a programmable AND array whose output terms feed a fixed OR array. Since the sum-of-products form can express any Boolean transfer function, the PAL circuit uses are only limited by the number of terms available in the AND - OR arrays. PAL devices come in different sizes to allow for effective logic optimization.

Figure 1 shows the basic PAL device structure for a two-input, one-output logic segment. The general logic equation for this segment is:

$$\text{Output} = (I_1+\overline{f_1})(\overline{I_1}+\overline{f_2})(I_2+\overline{f_3})(\overline{I_2}+\overline{f_4}) +$$
$$(I_1+\overline{f_5})(\overline{I_1}+\overline{f_6})(I_2+\overline{f_7})\ (\overline{I_2}+\overline{f_8})$$

where the "f" terms represent the state of the fusible links in the PAL device AND array. An unblown link represents a logic 1. Thus:

fuse blown, f = 0

fuse intact, f = 1

An unprogrammed PAL device has all fuses intact.

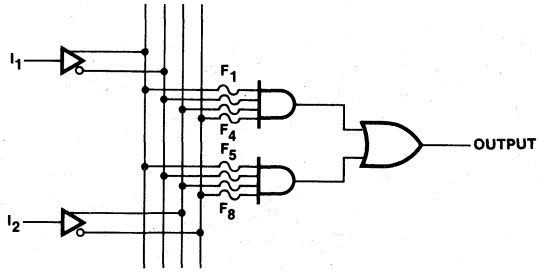


Figure 1

PAL Device Notation

Logic equations, while convenient for small functions, rapidly become cumbersome in large systems. To reduce possible confusion, complex logic networks are generally defined by logic diagrams and truth tables. Figure 2 shows the logic convention adopted to keep PAL device logic easy to understand and use, in the figure, an "x" represents an intact fuse used to perform the logic AND function. (Note: the input terms on the common line with the x's are not connected together.) The logic symbology shown in Figure 2 has been informally adopted by integrated circuit manufacturers because it clearly establishes a one-to-one correspondence between the chip layout and the logic diagram. It also allows the logic diagram and truth table to be combined into a compact and easy to read form, thereby serving as a convenient shorthand for PAL circuits. The two-input, one-output example from Figure 1, redrawn using the new logic convention, is shown in Figure 3.

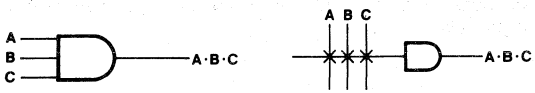


Figure 2

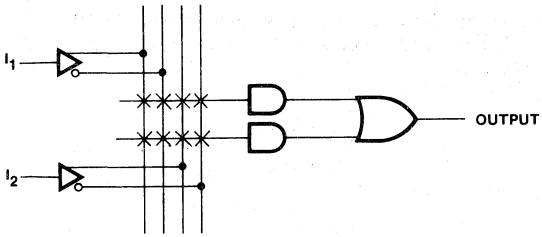


Figure 3

As a simple PAL device example, consider the implementation of the transfer function:

$$\text{Output} = I_1\overline{I_2} + \overline{I_1}I_2$$

The normal combinatorial logic diagram for this function is shown in Figure 4, with the PAL device logic equivalent shown in Figure 5.

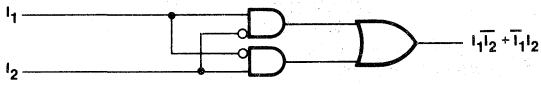


Figure 4

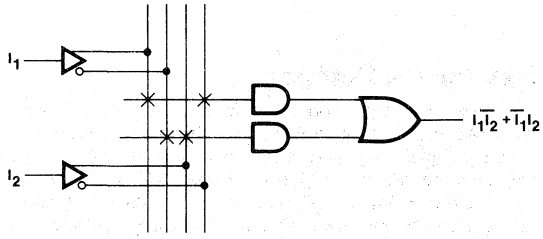


Figure 5

Using this logic convention it is now possible to compare the PAL device structure to the structure of the more familiar PROM and PLA. The basic logic structure of a PROM consists of a fixed AND array whose outputs feed a programmable OR array (Figure 6). PROMs are low-cost, easy to program, and available in a variety of sizes and organizations. They are most commonly

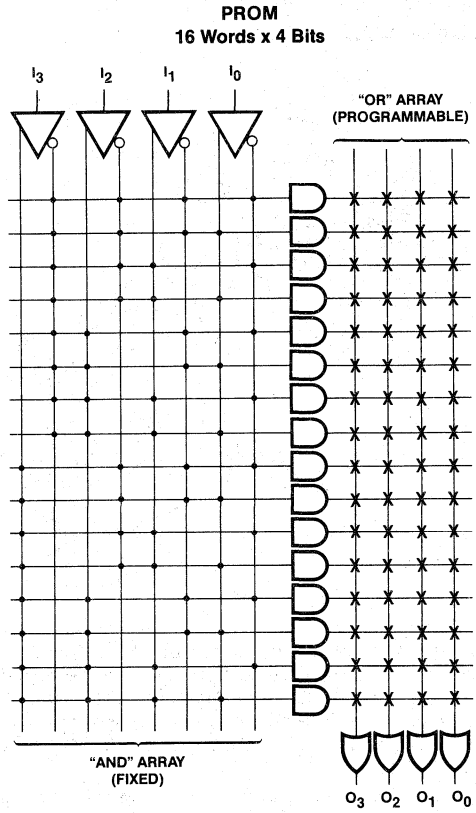


Figure 6

used to store computer programs and data. In these applications the fixed input is a computer memory address; the output is the contents of that memory location.

The basic logic structure of the PLA consists of a programmable AND array whose outputs feed a programmable OR array (Figure 7). Since the designer has complete control over all inputs and outputs, the PLA provides the ultimate flexibility for implementing logic functions. They are used in a wide variety of applications. However, this generality can make PLAs expensive, quite formidable to understand, and costly to program.

The basic logic structure of the PAL device, as mentioned earlier, consists of a programmable AND array whose outputs feed a fixed OR array (Figure 8). The PAL device combines much of the flexibility of the PLA with the low cost and easy programmability of the PROM. Table 1 summarizes the characteristics of the PROM, PLA, and PAL device logic families.

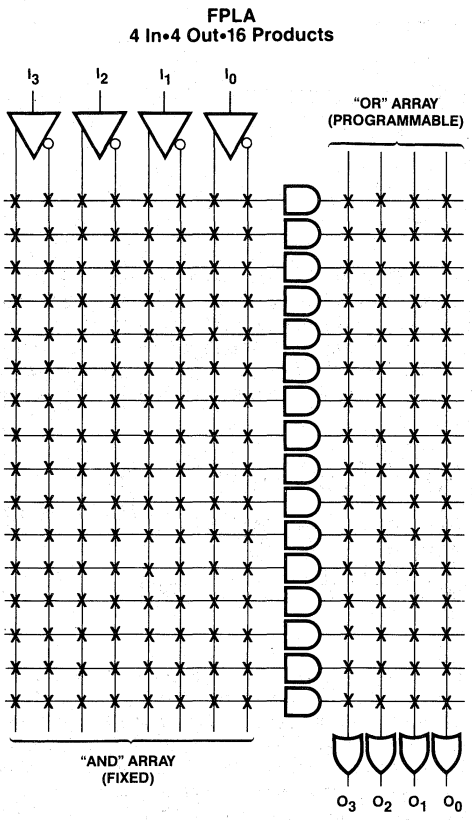


Figure 7

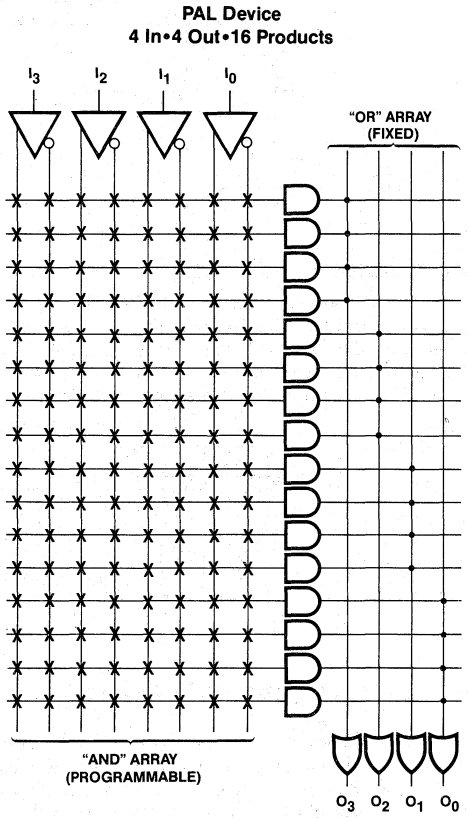


Figure 8

	AND	OR	OUTPUT OPTIONS
PROM	Fixed	Prog	TS,OC
FPLA	Prog	Prog	TS, OC, Prog. Polarity
FPGA	Prog	None	TS, OC, Prog. Polarity
FPLS	Prog	Prog	TS, Registered Feedback, I/O
PAL Device	Prog	Fixed	TS, Registered Feedback, I/O Prog. Polarity

PAL Device Circuits For Every Task

The members of the PAL device family and their characteristics are summarized in the PAL device menu. They are designed to cover the spectrum of logic functions at reduced cost and lower package count. This allows the designer to select the PAL device that best fits his application. PAL device units come in the following basic configurations:

Logic Arrays

PAL device logic arrays are available in sizes from 6x16 (6 input terms, 16 output terms) to 64x32, with both active high and active low output configurations available (ref. PAL device menu). This wide variety of input/output formats allows the PAL device to replace many different sized blocks of combinatorial logic with single packages.

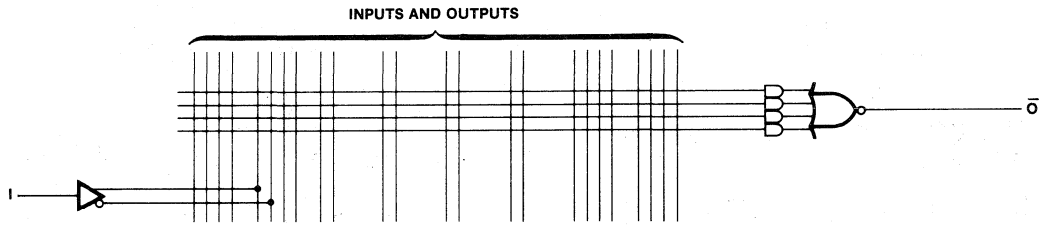


Figure 9

Programmable I/O

A feature of the high-end members of the PAL device family is programmable input/output. This allows the product terms to directly control the outputs of the PAL device (Figure 10). One product term is used to enable the three-state buffer, which in turn gates the summation term to the output pin. The output is also fed back into the PAL device array as an input. Thus the PAL device drives the I/O pin when the three-state gate is enabled; the I/O pin is an input to the PAL device array when the three-state gate is disabled. This feature can be used to allocate available pins for I/O functions or to provide bi-directional output pins for operations such as shifting and rotating serial data.

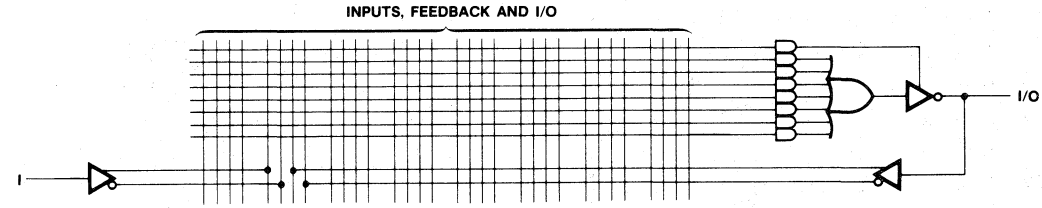


Figure 10

Registered Outputs with Feedback

Another feature of the high end members of the PAL device family is registered data outputs with registered feedback. Each product term is stored into a D-type output flip-flop on the rising edge of the system clock (Figure 11). The Q output of the flip-flop can then be gated to the output pin by enabling the active low three-state buffer.

In addition to being available for transmission, the Q output is fed back into the PAL device array as an input term. This feedback allows the PAL device to "remember" the previous state, and it can alter its function based upon that state. This allows the designer to configure the PAL device as a state sequencer which can be programmed to execute such elementary functions as count up, count down, skip, shift, and branch. These functions can be executed by the registered PAL device at rates of up to 40 MHz.

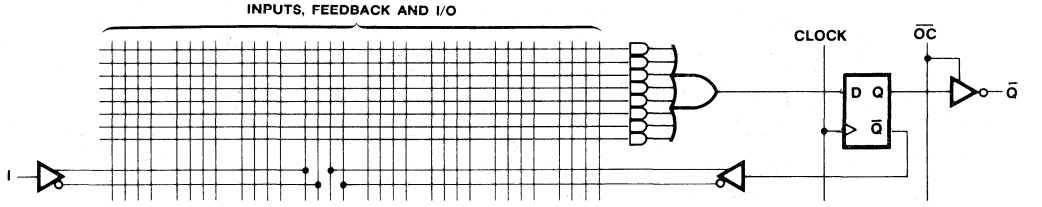


Figure 11

XOR PAL Devices

These PAL devices feature an exclusive-OR (XOR) function. The sum of products is segmented into two sums which are then exclusive ORed at the input of the D-type flip-flop (Figure 12). All of the features of the Registered PAL devices are included in the XOR PAL unit. The XOR function provides an easy implementation of the HOLD operation used in counters and other state sequencers.

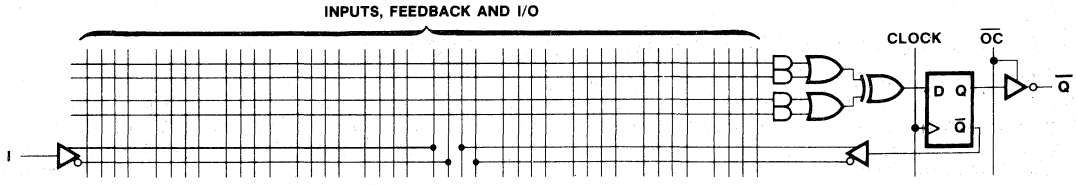


Figure 12

Arithmetic Gated Feedback

The arithmetic functions (add, subtract, greater than, and less than) are implemented by addition of gated feedback to the features of the XOR PAL device. The XOR at the input of the D-type flip-flop allows carrys from previous operations to be XORed with two variable sums generated by the PAL device array. The flip-flop Q output is fed back to be gated with input terms A (Figure 13). This gated feedback provides any one of the sixteen possible Boolean combinations which are mapped in the Karnaugh map (Figure 15). Figure 14 shows how the PAL device array can be programmed to perform these sixteen operations. These features provide for versatile operations on two variables and facilitate the parallel generation of carrys necessary for fast arithmetic operations.

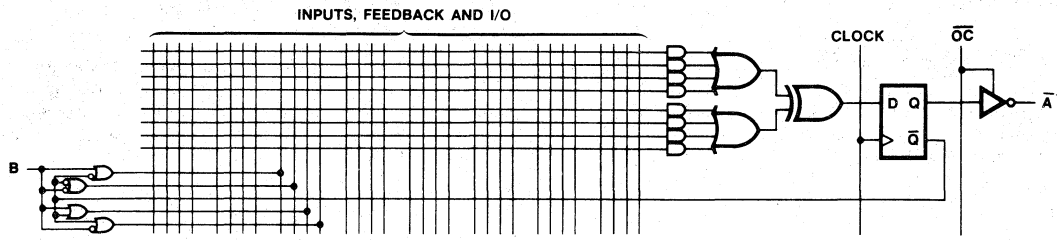


Figure 13

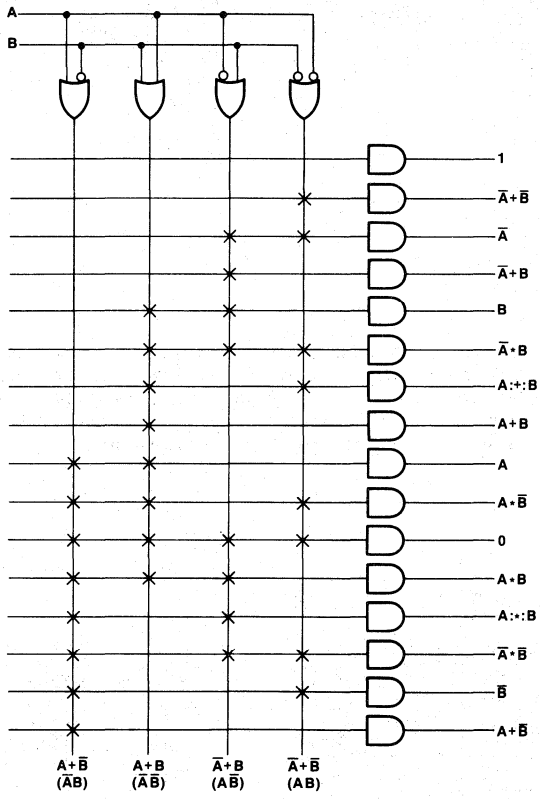


Figure 14

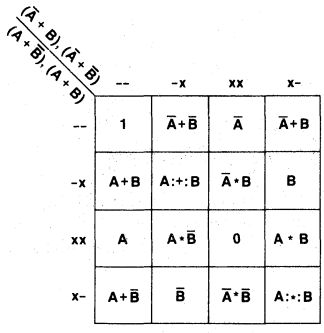


Figure 15

Programmable Output Polarity

The outputs can be programmed either active-low or active-high. This is represented by the exclusive-or gates shown in Figure 13, PAL20RA10 Logic Diagram. When the output polarity fuse is blown, the lower input to the exclusive-or gate is high, so the output is active-high. Similarly, when the output polarity fuse is intact, the output is active-low. The programmable output polarity feature allows the user a higher degree of flexibility when writing equations.

Programmable Clock

One of the product lines in each group is connected to the clock. This provides the user with the additional flexibility of a programmable clock, so each output can be clocked independently of all the others. (See Figure 16)

Programmable Set and Reset

Two product lines are dedicated to asynchronous set and reset. If the set product line is high, the register output becomes a logic 1. If the reset product line is high, the register output becomes a logic 0. The operation of the programmable set and reset overrides the clock. (See Figure 16)

Individually Programmable Register Bypass

If both the set and reset product lines are high, the sum-of-products bypasses the register and appears immediately at the output, thus making the output combinatorial. This allows each output to be configured in the registered or combinatorial mode. (See Figure 16)

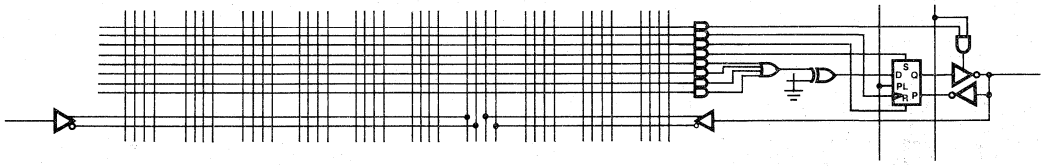


Figure 16

Product Term Sharing

The basic configuration is sixteen product terms shared between two output cells. For a typical output pair, each product term can be used by either output; but, since product term sharing is exclusive, a product term can be used by only one output, not both. If equations call for an output pair to use the same product term, two product terms are generated, one for each output. This should be taken into account when writing equations. PAL assemblers configure product terms automatically.

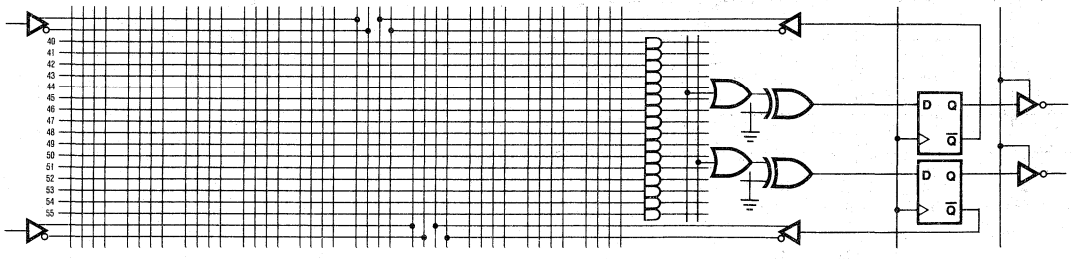


Figure 17

PAL Device Programming

PAL devices can be programmed in most standard PROM programmers with the addition of a PAL device personality card. For details on programming equipment, see the PAL Device Programmer Reference Guide in this databook.

PALASM (PAL Device Assembler)

PALASM is the software used to define, simulate, build, and test PAL device units. PALASM accepts the PAL device Design Specification as an input file. It verifies the design against an optional function table and generates the fuse plot which is used to program the PAL devices. PALASM is available upon request for many computers.

HAL (Hard Array Logic) Device

The HAL device family is the mask programmed version of a PAL device. The HAL device is to a PAL device just as a ROM is to a PROM. A standard wafer is fabricated as far as the metal mask. Then a custom metal mask is used to fabricate aluminum links for a HAL device instead of the programmable TiW fuses used in a PAL device.

PAL Device Technology

PAL circuits are manufactured using the proven TTL Schottky bipolar TiW fuse process to make fusible-link PROMs. An NPN emitter follower array forms the programmable AND array. PNP inputs provide high impedance inputs (0.25 mA max) to the array. All outputs are standard TTL drivers with internal active pull-up transistors.

PAL Device Data Security

The circuitry used for programming and logic verification can be used at any time to determine the logic pattern stored in the PAL device array. For security, the PAL device has a "last fuse" which can be blown to disable the verification logic. This provides a significant deterrent to potential copiers, and it can be used to protect proprietary designs.

* Patent pending

PAL Device Part Numbers

The PAL device part number is unique in that the part number code also defines the part's logic operation. The PAL device numbering system is shown in Figure 17. For example, a PAL 14L4CN would be a 14-input term, 4-output term, active-low PAL device with a commercial temperature range packaged in a 20-pin plastic DIP.

The electronic dice game is simply constructed using a free running oscillator whose output is used to drive two asynchronous modulo six counters. When the user "rolls" the dice (presses a button), the current state of the counters is decoded and latched into a display resembling the pattern seen on an ordinary pair of dice.

A conventional logic diagram for the dice game is shown in Figure 16. It is implemented using standard TTL, SSI and MSI parts, with a total I.C. count of eight: six quad gate packages and two quad D-latches. Looks like a nice clean logic design, right? Wrong!!

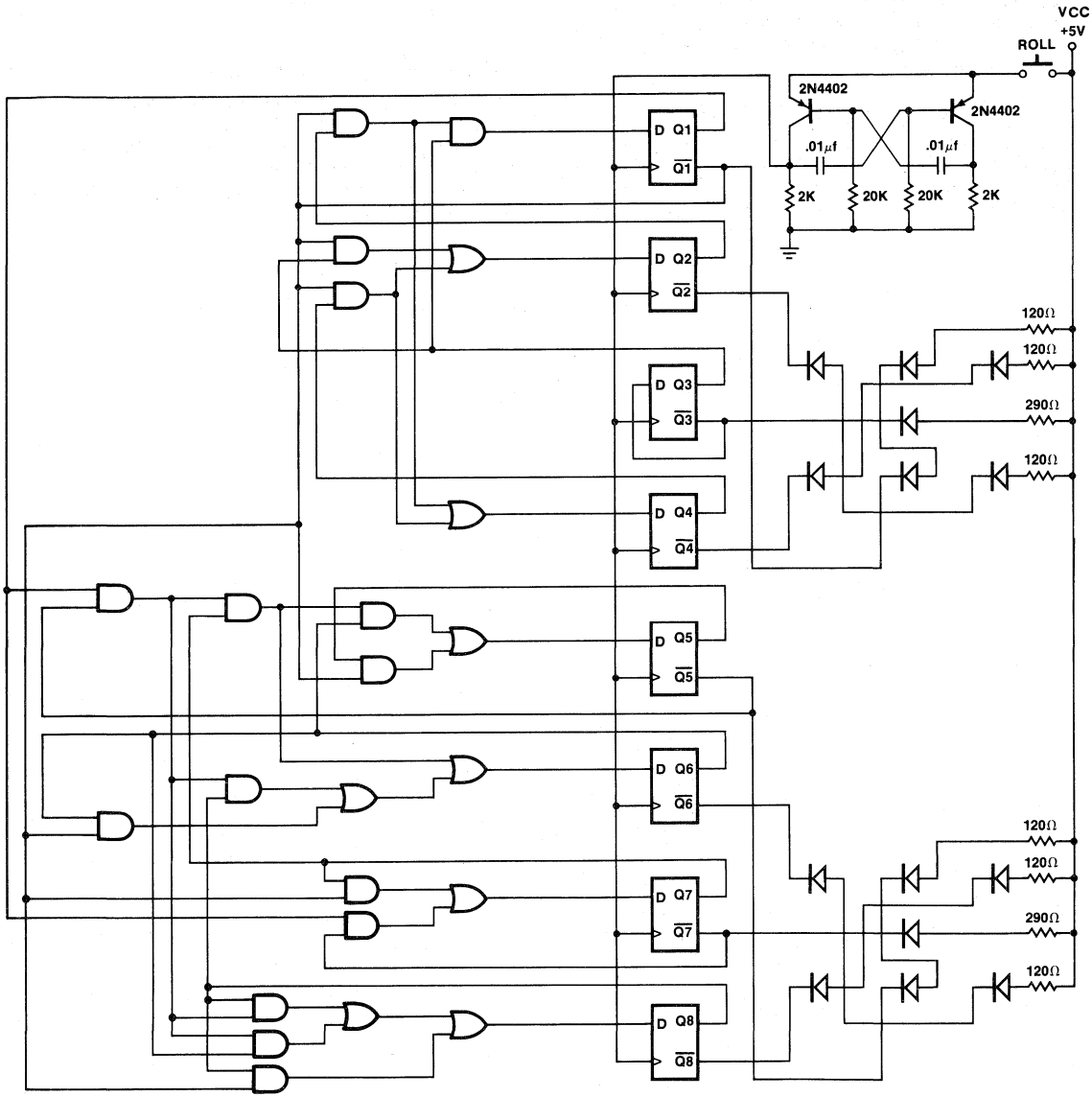
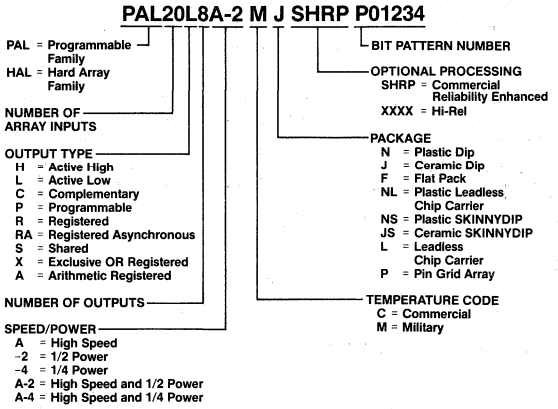


Figure 16



PAL Device Logic Symbols

The logic symbols for each of the individual PAL devices gives a concise functional description of the PAL device logic function. This symbol makes a convenient reference when selecting the PAL device that best fits a specific application. Figure 18 shows the logic symbol for a PAL10H8 array.

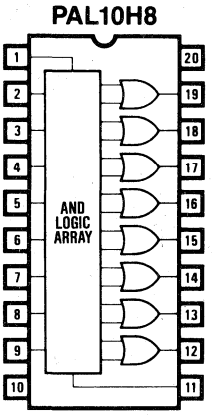


Figure 18

A PAL Device Example

As an example of how the PAL device enables the designer to reduce costs and simplify logic design, consider the design of a simple, high-volume consumer product: an electronic dice game. This type of product will be produced in extremely high volume, so it is essential that every possible production cost be minimized.

PAL Device Goes to the Casino

A brief examination of Figure 16 reveals two basic facts: first, the circuit contains mostly simple, combinatorial logic, and second, it uses a clocked state transition sequence. Remembering that the PAL device family contains ample provision for these features, the PAL device catalog is consulted. The PAL16R8 has all the required functions, and the entire logic content of the circuit can be programmed into a single PAL device shown in Figure 19.

In this example, the PAL device effected an eight-to-one package count reduction and a significant cost savings. This is typical of the power and cost-effective performance that the PAL device family brings to logic design.

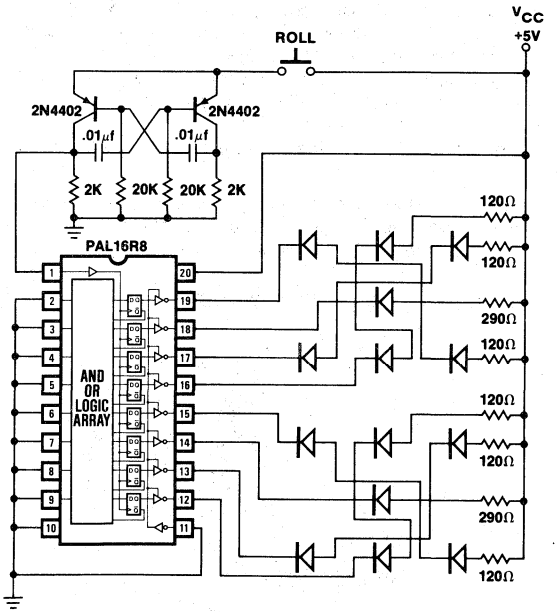
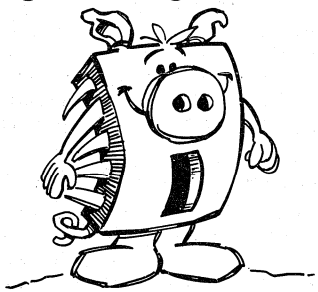


Figure 19

Advantages of Using PAL Devices



The PAL device has a unique place in the world of logic design. Not only does it offer many advantages over conventional logic, it also provides many features not found anywhere else. Among the benefits of the PAL device family:

- Programmable replacement for conventional TTL logic.
- Reduces IC inventories substantially and simplifies their control.
- Reduces chip count by at least 4 to 1.
- Expedites and simplifies prototyping and board layout.
- Saves space with 20-pin and 24-pin SKINNYDIP packages, and surface-mount PLCC packages.
- High speed: 15 ns maximum propagation delay, on B series.
- Programmed on standard PROM programmers.
- Programmable three-state outputs.
- Special feature eliminates possibility of copying by competitors.

All of these features combine together to lower product development costs and increase product cost effectiveness. The bottom line is that PAL devices save money.

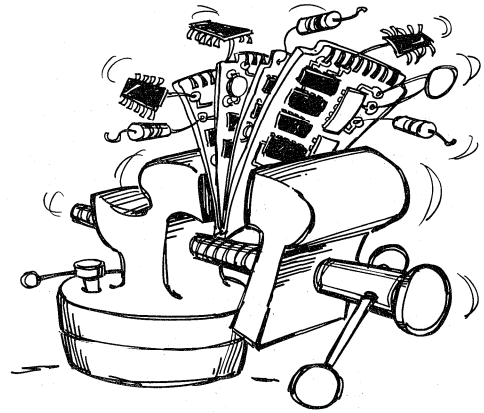
Direct Logic Replacement

In both new and existing designs, the PAL device can be used to replace various logic functions. This allows the designer to optimize a circuit in many ways never before possible. The PAL device is particularly effective when used to provide interfaces required by many LSI functions. The combination of PAL device flexibility and LSI function density makes a powerful team.

Design Flexibility

The PAL device offers the systems logic designer a whole new world of options. Until now, the decision on logic system implementation was usually between SSI/MSI logic functions on one hand and microprocessors on the other. In many cases the function required is too awkward to implement the first way and too simple to justify the second. Now the PAL device offers the designer high functional density, high speed, and low cost. Even better, PAL devices come in a variety of sizes and functions, thereby further increasing the designer's options.

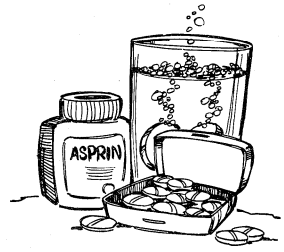
Space Efficiency



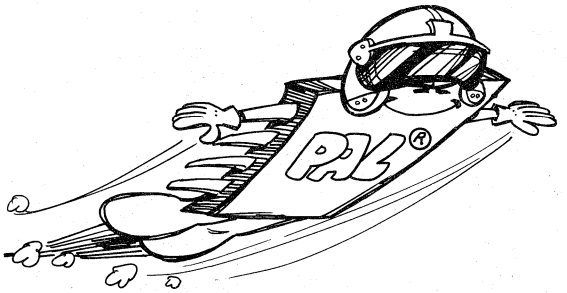
By allowing designers to replace many simple logic functions with single packages, the PAL device allows more compact P.C. board layouts. The PAL device space-saving 20-pin and 24-pin SKINNYDIP packages help to reduce board area further while simplifying board layout and fabrication. this means that many multi-card systems can now be reduced to one or two cards, and that can make the difference between a profitable success or an expensive disaster.

Smaller Inventory

The PAL device family can be used to replace up to 90% of the conventional TTL family. This considerably lowers both shelving and inventory cataloging requirements. In addition, small custom modifications to the standard functions are easy for PAL device users, but not so easy for standard TTL users.



High Speed



The PAL device family runs faster than or equal to the best of bipolar logic circuits. This makes the PAL device the ideal choice for most logical operations or control sequence which requires a medium complexity and high speed. Also, in many microcomputer systems, the PAL device can be used to handle high-speed data interfaces that are not feasible for the microprocessor alone. This can be used to significantly extend the capabilities of the low-cost, low-speed NMOS microprocessors into areas formerly requiring high-cost bipolar microprocessors.

Easy Programming

The members of the PAL device family can be quickly and easily programmed using standard PROM programmers. This allows designers to use PAL devices with a minimum investment in special equipment. Many types of programmable logic, such as the FPLA, require an expensive, dedicated programmer.

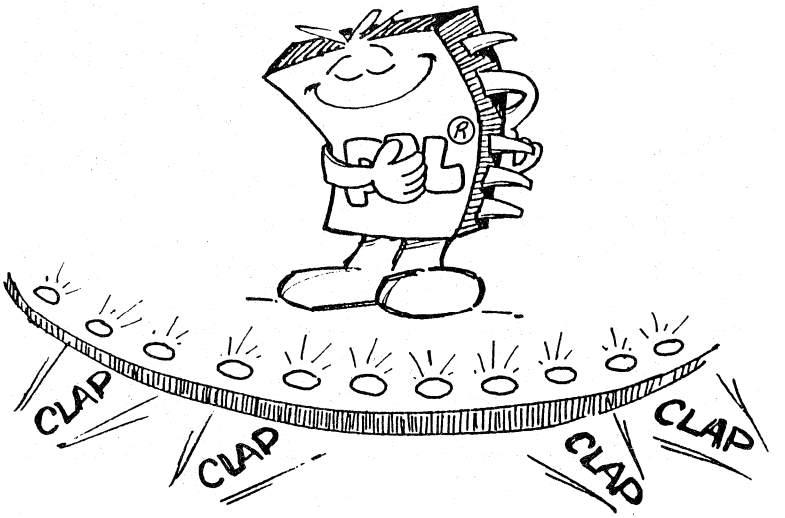
Secure Data

The PAL device verification logic can be completely disabled by blowing out a special "last link". This prevents the unauthorized copying of valuable data, and makes the PAL device perfect for use in any application where data integrity must be carefully guarded.

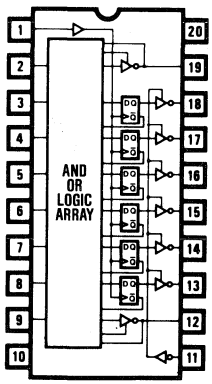
Summary

The PAL device family of logic devices offers logic designers new options in the implementation of sequential and combinatorial logic designs. The family is fast, compact, flexible, and easy to use in both new and existing designs. It promises to reduce costs in most areas of design and production with a corresponding increase in product profitability.

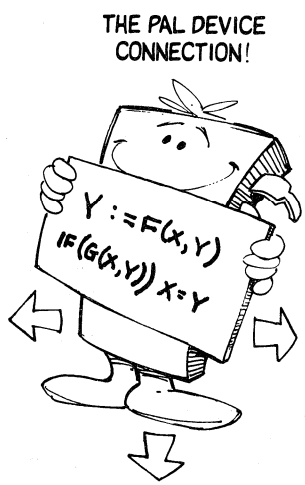
A Great Performer!

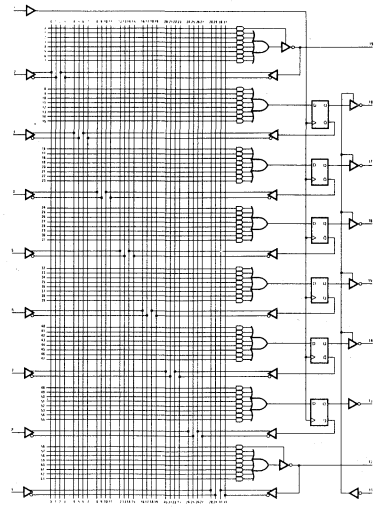


PAL16R6

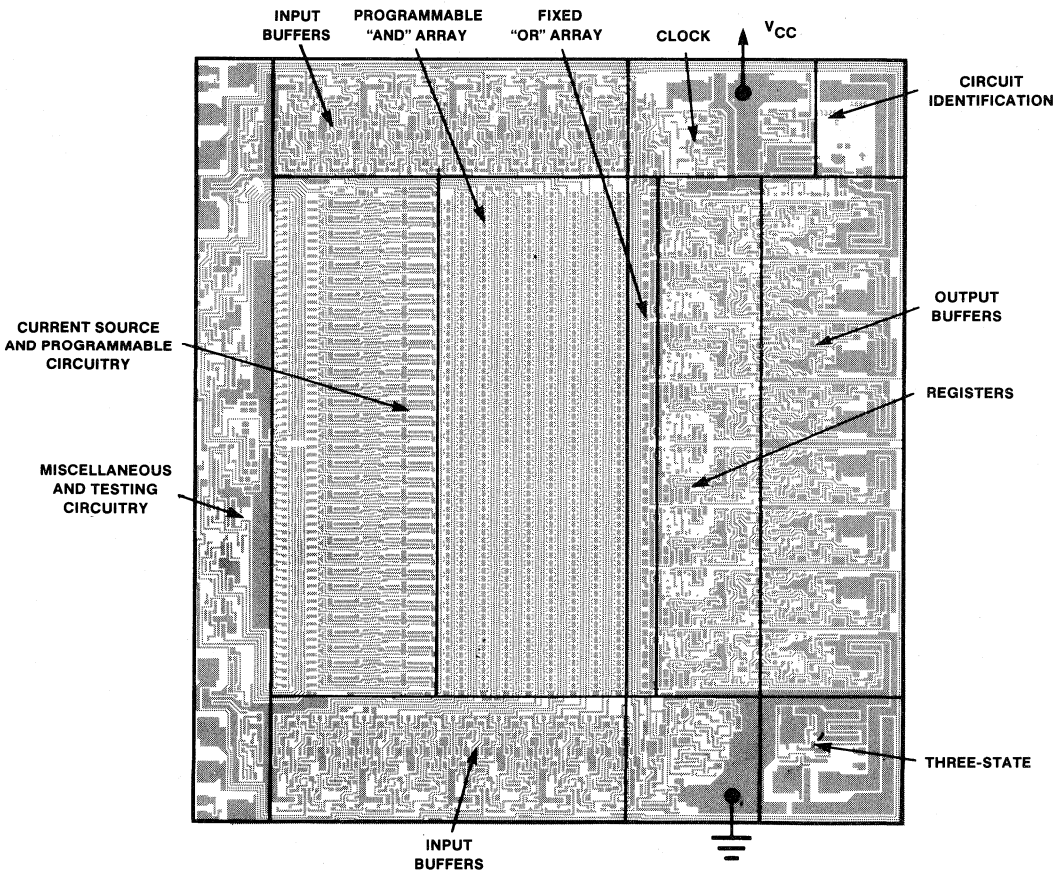


PAL16R6 Logic Symbols





PAL16R6 Logic Diagram



PAL 16R6 Metalization

PAL® (Programmable Array Logic) Devices
HAL® (Hard Array Logic) Devices

Features/Benefits

- **Reduces SSI/MSI chip count greater than 5 to 1**
- **Saves space with SKINNYDIP® packages**
- **Reduces IC inventories substantially**
- **Expedites and simplifies prototyping and board layout**
- **PALASM®2 silicon compiler provides easy design entry**
- **Security fuse reduces possibility of copying by competitors**

Description

The PAL device family utilizes an advanced Schottky TTL process and the Bipolar PROM fusible link technology to provide user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at reduced chip count.

The HAL device family utilizes standard Low-Power Schottky TTL process and automated mask pattern generation directly from logic equations to provide a semi-custom gate array for replacing conventional SSI/MSI gates and flip-flops at reduced chip count.

The PAL device lets the systems engineer "design his own chip" by blowing fusible links to configure AND and OR gates to perform his desired logic function. Complex interconnections which previously required time-consuming layout are thus "lifted" from PC board etch and placed on silicon where they can be easily modified during prototype check-out or production.

The PAL/HAL device transfer function is the familiar sum of products. Like the PROM, the PAL device has a single array of fusible links. Unlike the PROM, the PAL device is a programmable AND array driving a fixed OR array (the PROM is a fixed AND array driving a programmable OR array).

In addition the PAL/HAL device provides these options:

- **Variable input/output pin ratio**
- **Programmable three-state outputs**
- **Registers with feedback**
- **Arithmetic capability**
- **Exclusive-OR gates**

Unused input pins should be tied directly to V_{CC} or GND. Product terms with all fuses blown assume the logical high state, and product terms connected to both true and complement of any single input assume the logical low state. Registers consist of D-type flip-flops which are loaded on the low-to-high transition of the clock. PAL/HAL device Logic Diagrams are shown with all fuses blown, enabling the designer to use the diagrams as coding sheets. PALASM software automatically generates a similar diagram, called the fuse plot.

The entire PAL device family is programmed using inexpensive conventional PROM programmers with appropriate personality and socket adapter cards. Once the PAL device is programmed and verified, two additonal fuses may be blown to defeat verification. This feature gives the user a proprietary circuit which is very difficult to copy.

To design a HAL, the user first programs and debugs a PAL device using PALASM and the "PAL DEVICE DESIGN SPECIFICATION" standard format. This specification is submitted to Monolithic Memories where it is computer-processed and assigned a bit pattern number, e.g., H01234.

Monolithic Memories will provide a PAL device sample for customer qualification. The user then submits a purchase order for a HAL of the specified bit pattern number, e.g., HAL18L4 H01234. For details on ordering HAL devices, please refer to the brochure, *ProPAL, HAL, and ZHAL Devices: The Logical Solutions for Volume Programmable Logic,* available from Monolithic Memories.

Register Bypass (MegaPAL Devices)

Outputs within a bank must either be all registered or all combinatorial. Whether or not a bank of registers is bypassed depends on how the outputs are defined in the equations. A colon followed by an equal sign [:=] specifies a registered output with feedback which is updated after the low-to-high transition of the clock. An equal sign [=] defines a combinatorial output which bypasses the register. Registers are bypassed in banks of eight. Bypassing a bank of registers eliminates the feedback lines for those outputs.

Output Polarity

Output polarity is defined by comparison of the pin list and the equations. If the logic sense of a specific output in the pin list is different from the logic sense of that output as defined by its equation, the output is inverted or active low polarity. If the logic sense of a specific output in the pin list is the same as the logic sense of that output as defined by its equation, the output is active high polarity. Note that the P, RA, RS, and MegaPAL devices have programmable output polarity.

Product Term Sharing (RS, MegaPAL Devices)

The basic configuration is sixteen product terms shared between two output cells. For a typical output pair, each product term can be used by either output; but, since product term sharing is exclusive, a product term can be used by only one output, not both. If equations call for an output pair to use the same product term, two product terms are generated, one for each output. This should be taken into account when writing equations. PAL device assemblers configure product terms automatically.

Product Term Editing

A unique feature of product term sharing is the ability to edit the design after the device has been programmed. Without this feature, a new PAL device had to be programmed if the user needed to change his design. Product term editing allows the user to delete an unwanted product term and reprogram a previously unused product term to the desired fuse pattern. This feature is made possible by the product term sharing architecture. Since each product term can be routed to either output in a given pair by selecting one of two steering fuses, it is possible to blow both of the steering fuses thereby completely disabling that product term. Once disabled, that product term is powered down, saving typically 0.25 mA. The desired change may now be programmed into one of the previously unused product terms corresponding to that output pair. Additional edits can be made as long as there are unused product terms for the output in question.

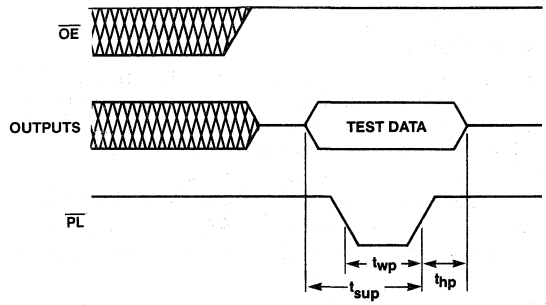
PRESET Feature (PAL64R32 only)

Register banks of eight may be PRESET to all highs on the outputs by setting the PRESET pin (PS) to a Low level. Note from the Logic Diagram that when the state of an output is High, the state of the register is Low due to the inverting tri-state buffer.

TTL-Level Preload Features (RA, MegaPAL Devices)

Preload pins have been added to enable the testability of each state in state-machine design. Typically, for a modulo-n counter or a state machine there are many unreachable states for the registers. These states, and the logic which controls them are untestable without a way to "set-in" the desired starting state of the registers. In addition, long test sequences are sometimes needed to test a state machine simply to reach those starting states which are legal. Since complete logic verification is needed to ensure the proper exit from "illegal" or unused states, a way to enter these states must be provided. The ability to preload a given bank of registers is provided in this device.

To use the preload feature, several steps must be followed. First, a high level on an assertive-low output enable pin disables the outputs for that bank of registers. Next, the data to be loaded is presented at the output pins. This data is then loaded into the register by placing a low level on the PRELOAD pin. PRELOAD is asynchronous with respect to the clock.



Programmable Set and Reset (RA Family only)

In each SMAC, two product lines are dedicated to asynchronous set and reset. If the set product line is high, the register output becomes a logic 1. If the reset product line is high, the register output becomes a logic 0. The operation of the programmable set and reset overrides the clock. Note that set and reset are in reference to the register, independent of polarity.

Individually Programmable Register Bypass (RA Family only)

If both the set and reset product lines are high, the sum-of-products bypasses the register and appears immediately at the output, thus making the output combinatorial. This allows each output to be configured in the registered or combinatorial mode.

Programmable Clock (RA Family only)

One of the product lines in each group is connected to the clock. This provides the user with the additional flexibility of a programmable clock, so each output can be clocked independently of all the others.

Monolithic Memories PAL® Device Menu

FAMILY	PART NUMBER	PACKAGE	DESCRIPTION			MAXIMUM	
			INPUTS	OUTPUTS		t_{PD}* ns	I_{CC} mA
				COMBINATORIAL	REGISTERED		
Small 20 Combinatorial	PAL10H8	20N, J, NL, F, L	10	8	—	35	90
	PAL12H6		12	6	—	35	
	PAL14H4		14	4	—	35	
	PAL16H2		16	2	—	35	
	PAL16C1		16	2	—	40	
	PAL10L8		10	8	—	35	
	PAL12L6		12	6	—	35	
	PAL14L4		14	4	—	35	
	PAL16L2		16	2	—	35	
Small 20-2 Combinatorial	PAL10H8-2	20N, J, NL, F, L	10	8	—	60	45
	PAL12H6-2		12	6	—		
	PAL14H4-2		14	4	—		
	PAL16H2-2		16	2	—		
	PAL16C1-2		16	2	—		
	PAL10L8-2		10	8	—		
	PAL12L6-2		12	6	—		
	PAL14L4-2		14	4	—		
	PAL16L2-2		16	2	—		
Medium 20 Standard	PAL16L8	20N, J, NL	16	8	—	35	180
	PAL16R8		16	—	8		
	PAL16R6		16	2	6		
	PAL16R4		16	4	4		
Medium 20A Standard	PAL16L8A	20N, J, NL, W, L	16	8	—	25	180
	PAL16R8A		16	—	8		
	PAL16R6A		16	2	6		
	PAL16R4A		16	4	4		
Medium 20A-2 Standard	PAL16L8A-2	20N, J, NL, F, L	16	8	—	35	90
	PAL16R8A-2		16	—	8		
	PAL16R6A-2		16	2	6		
	PAL16R4A-2		16	4	4		
Medium 20A-4 Standard	PAL16L8A-4	20N, J, NL, F, L	16	8	—	55	50
	PAL16R8A-4		16	—	8		
	PAL16R6A-4		16	2	6		
	PAL16R4A-4		16	4	4		
Medium 20B Standard	PAL16L8B	20N, J, NL, W, L	16	8	—	15	180
	PAL16R8B		16	—	8		
	PAL16R6B		16	2	6		
	PAL16R4B		16	4	4		
Medium 20B-2 Standard	PAL16L8B-2	20N, J, NL, W, L	16	8	—	25	90
	PAL16R8B-2		16	—	8		
	PAL16R6B-2		16	2	6		
	PAL16R4B-2		16	4	4		
Medium 20B-4 Standard	PAL16L8B-4	20N, J, NL, W, L	16	8	—	35	55
	PAL16R8B-4		16	—	8		
	PAL16R6B-4		16	2	6		
	PAL16R4B-4		16	4	4		
Medium 20AP Programmable Polarity	PAL16P8A	20N, J, NL	16	8	—	25/30**	180
	PAL16RP8A		16	—	8		
	PAL16RP6A		16	2	6		
	PAL16RP4A		16	4	4		
Large 20 Arithmetic	PAL16X4	20N, J, NL, F, L	16	4	4	40	225
	PAL16A4		16	4	4		240
Large 20RA Asynchronous	PAL16RA8	20N, J, NL	16	—	8	30/35**	170

* Minimum commercial t_{SU} for devices with all registered outputs.

** Polarity fuse programmed (active High).

N = Plastic DIP
NS = Plastic SKINNYDIP
J = Ceramic DIP
JS = Ceramic SKINNYDIP
NL = Plastic Leaded Chip Carrier (PLCC)
P = Pin Grid Array
L = Leadless Chip Carrier (LCC)
W = Cerpack
F = Ceramic Solder Seal Flat Pack

Monolithic Memories PAL® Device Menu

PAL Circuit Series 24

FAMILY	PART NUMBER	PACKAGE	DESCRIPTION			MAXIMUM	
			INPUTS	OUTPUTS		t_{PD}* ns	I_{CC} mA
				COMBINATORIAL	REGISTERED		
Small 24 Combinatorial	PAL12L10	24NS, JS, W, 28NL, 28L	10	10	—	40	100
	PAL14L8		14	8	—		
	PAL16L6		16	6	—		
	PAL18L4		18	4	—		
	PAL20L2		20	2	—		
	PAL20C1		20	2	—		
Small 24A Decoder	PAL6L16A	24NS,JS, 28NL	6	16	—	25	90
	PAL8L14A		8	14	—		
Medium 24A Standard	PAL20L8A	24NS, JS, W, 28NL, 28L	20	8	—	25	210
	PAL20R8A		20	—	8		
	PAL20R6A		20	2	6		
	PAL20R4A		20	4	4		
Medium 24A-2 Standard	PAL20L8A-2	24NS, JS, W, 28NL, 28L	20	8	—	35	105
	PAL20R8A-2		20	—	8		
	PAL20R6A-2		20	2	6		
	PAL20R4A-2		20	4	4		
Medium 24B Standard	PAL20L8B	24NS, JS, W, 28NL, 28L	20	8	—	15	210
	PAL20R8B		20	—	8		
	PAL20R6B		20	2	6		
	PAL20R4B		20	4	4		
Medium 24X Exclusive OR	PAL20L10	24NS, JS, W, 28NL, 28L	20	10	—	50	165
	PAL20X10		20	—	10		180
	PAL20X8		20	2	8		180
	PAL20X4		20	4	4		180
Medium 24XA Exclusive OR	PAL20L10A	24NS, JS, W, 28NL, 28L	20	10	—	30	165
	PAL20X10A		20	—	10		180
	PAL20X8A		20	2	8		180
	PAL20X4A		20	6	4		180
Large 24RS Shared Product Terms	PAL20S10	24NS, JS, W, 28NL, 28L	20	10	—	35/40**	240
	PAL20RS10		20	—	10	35	240
	PAL20RS8		20	2	8	35/40**	240
	PAL20RS4		20	6	4	35/40**	240
Large 24RA Asynchronous	PAL20RA10	24NS, JS, W, 28NL, 28L	20	—	10	30/35**	200

PAL Circuit Series MegaPAL™

FAMILY	PART NUMBER	PACKAGE	DESCRIPTION		MAXIMUM	
			INPUTS	REGISTERED OUTPUTS	t_{PD}* ns	I_{CC} mA
1500 Gates	PAL32R16	40N, J, 44NL, 44L	32	16	40/45**	280
5000 Gates	PAL64R32	88P, 84L	64	32	50/55**	640

* Minimum commercial t_{SU} for devices with all registered outputs.

** Polarity fuse programmed (active high).

f_{MAX} Parameters

The parameter f_{MAX} is the maximum speed at which the PAL device is guaranteed to operate. Because flexibility inherent to PAL devices allows a choice of clocked flip-flop designs, for the convenience of the user, f_{MAX} for the B-speed devices is specified to address two major classes of synchronous designs.

The simplest type of synchronous design can be described as a data path application. In this case, data is presented to the data terminal of the flip-flop and clocked through; no feedback is employed (Figure 1). Under these conditions, the frequency of operation is limited by the greater of the data setup time (t_{su}) or the minimum clock period (t_W high + t_W low). This parameter is designated f_{MAX} (no feedback).

For synchronous sequential designs, i.e., state machines, where logical feedback is required, inputs to flip-flop data terminals originate from the device input pins or flip-flop outputs via the internal feeback paths (Figure 2). Under these conditions, f_{MAX} is defined as the reciprocal of (t_{su} + t_{CLK}) and is designated f_{MAX} (feedback).

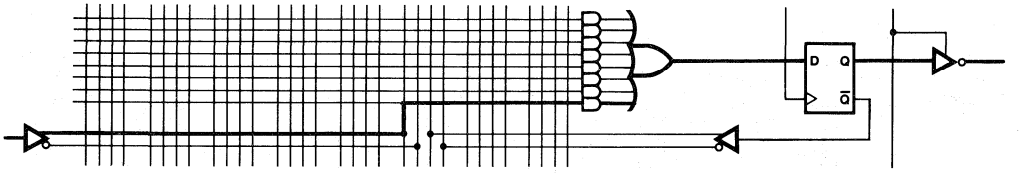


Figure 1. No Feedback

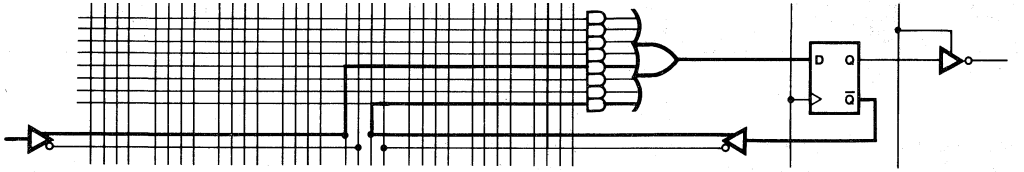
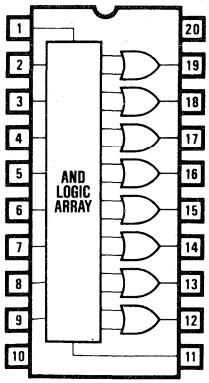
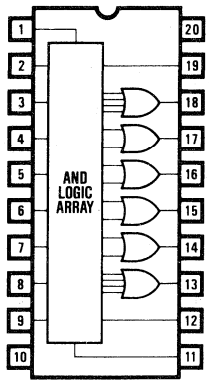


Figure 2. Feedback

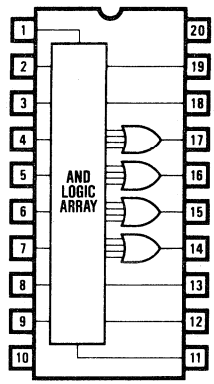
10H8/-2



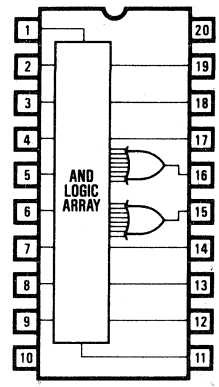
12H6/-2



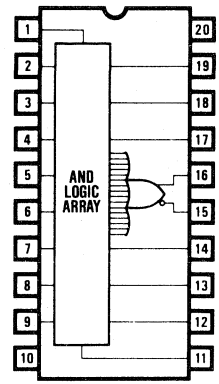
14H4/-2



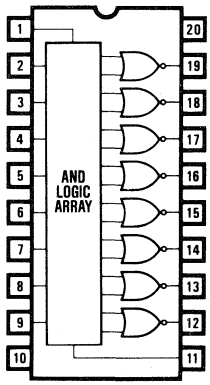
16H2/-2



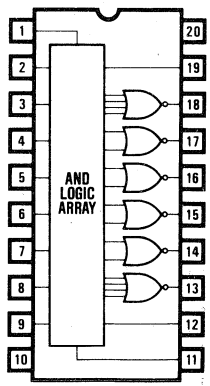
16C1/-2



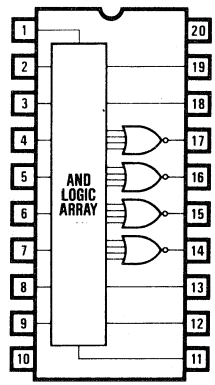
10L8/-2



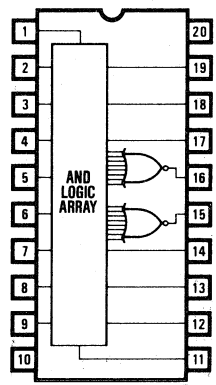
12L6/-2



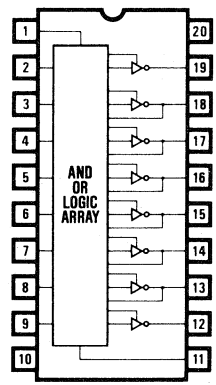
14L4/-2



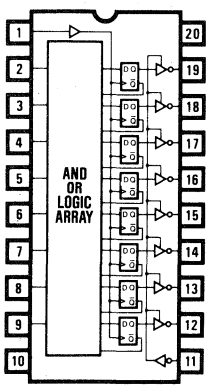
16L2/-2



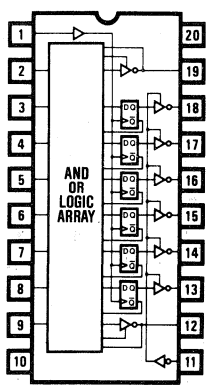
16L8/B/B-2/B-4
A/A-2/A-4



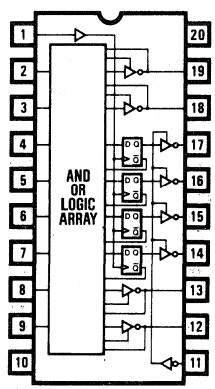
16R8/B/B-2/B-4
A/A-2/A-4



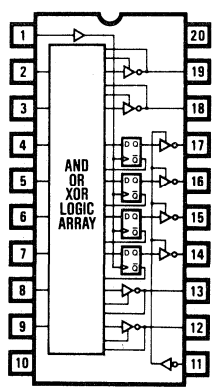
16R6/B/B-2/B-4
A/A-2/A-4



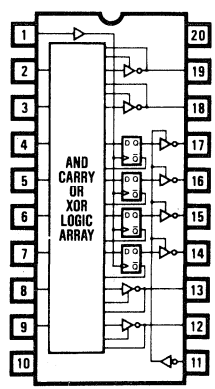
16R4/B/B-2/B-4
A/A-2/A-4



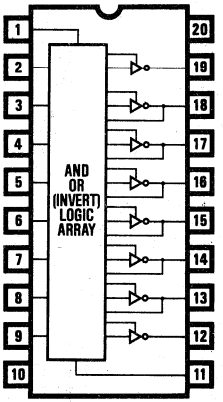
16X4



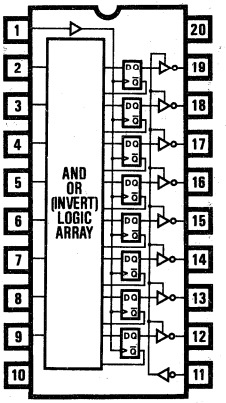
16A4



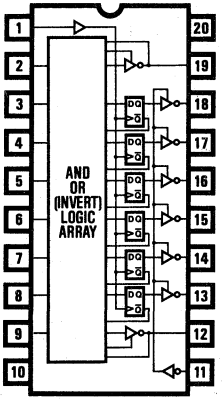
16P8A



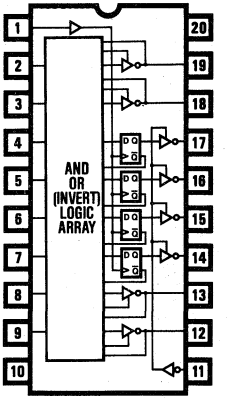
16RP8A



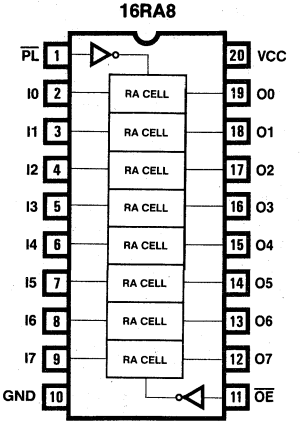
16RP6A



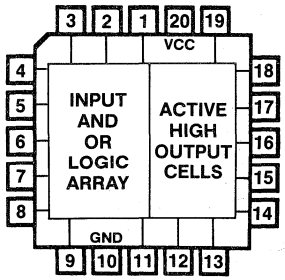
16RP4A



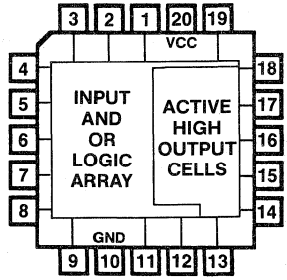
16RA8



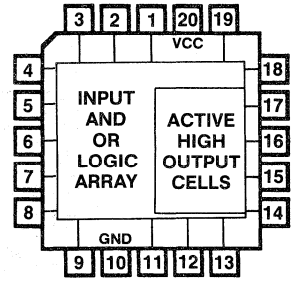
10H8/-2



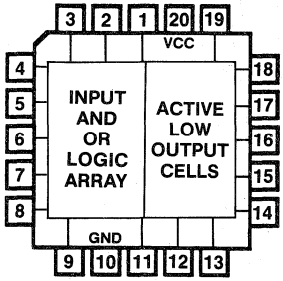
12H6/-2



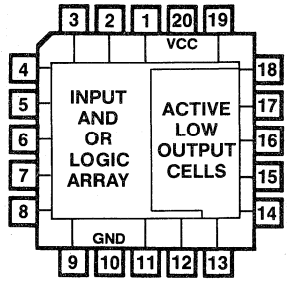
14H4/-2



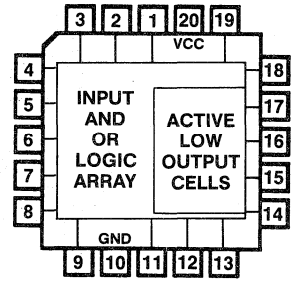
10L8/-2



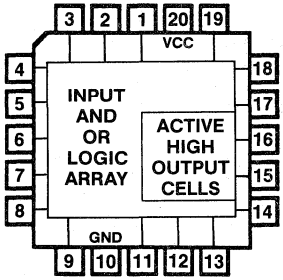
12L6/-2



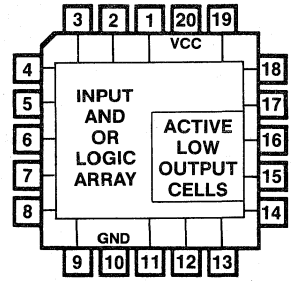
14L4/-2



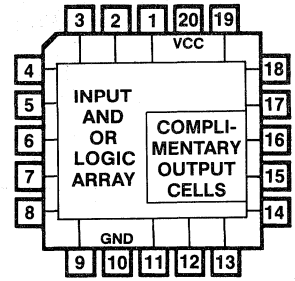
16H2/-2



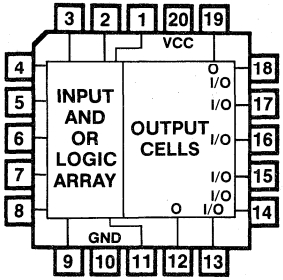
16L2/-2



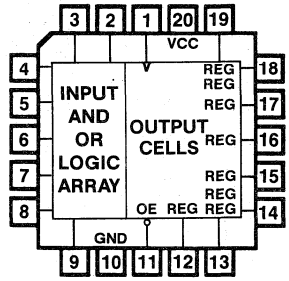
16C1/-2



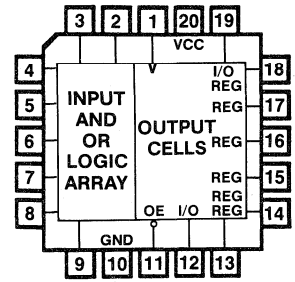
16L8/B/B-2/B-4
A/A-2/A-4



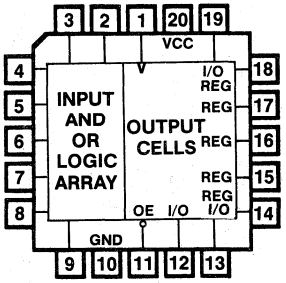
16R8/B/B-2/B-4
A/A-2/A-4



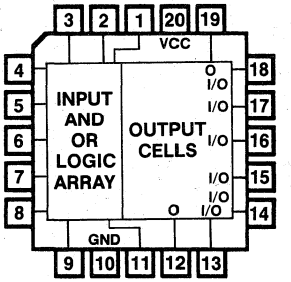
16R6/B/B-2/B-4
A/A-2/A-4



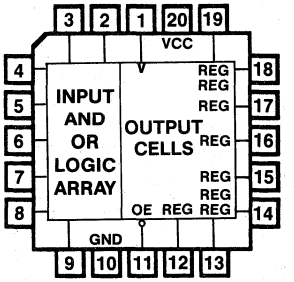
16R4/B/B-2/B-4
A/A-2/A-4



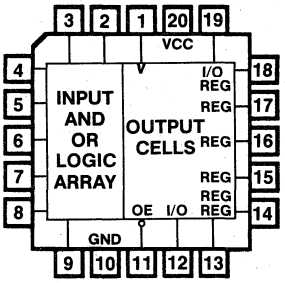
16P8A



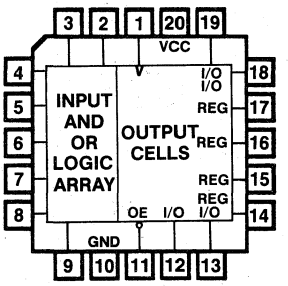
16RP8A



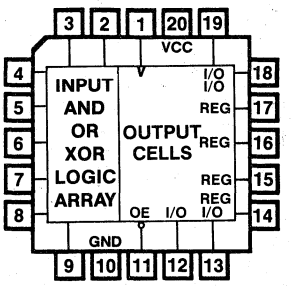
16RP6A



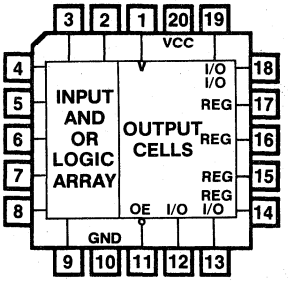
16RP4A



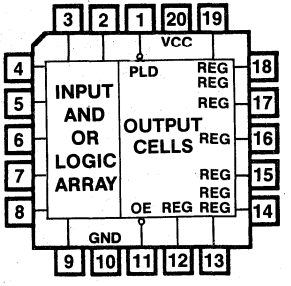
16X4



16A4

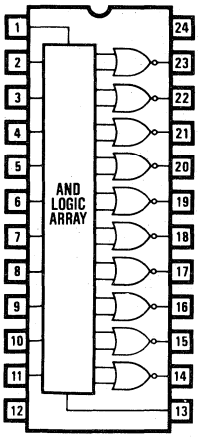


16RA8

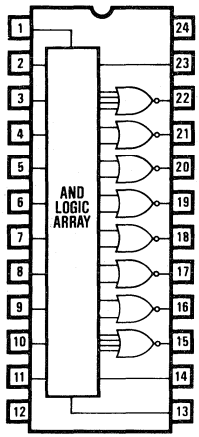


5

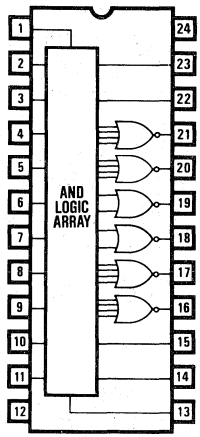
12L10



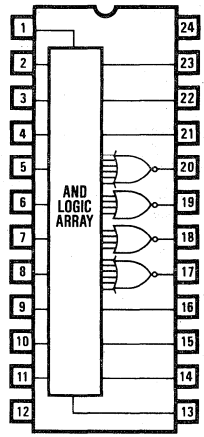
14L8



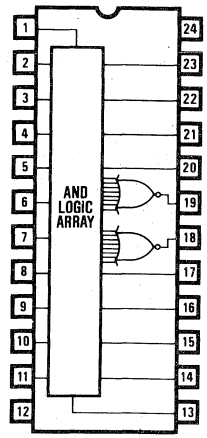
16L6



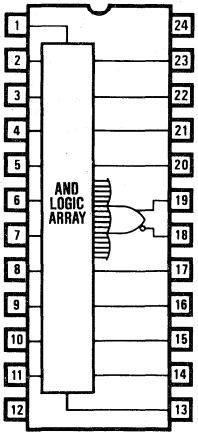
18L4



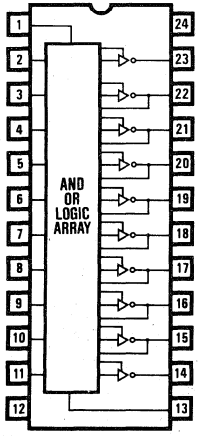
20L2



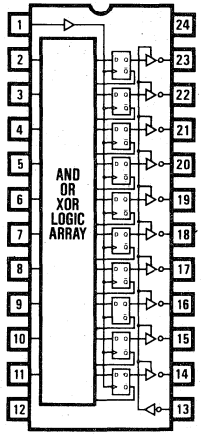
20C1



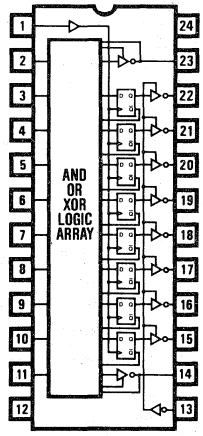
20L10/A



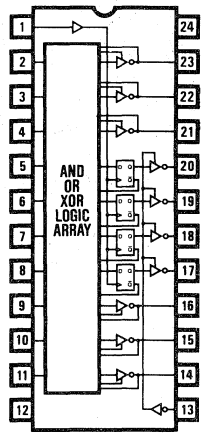
20X10/A



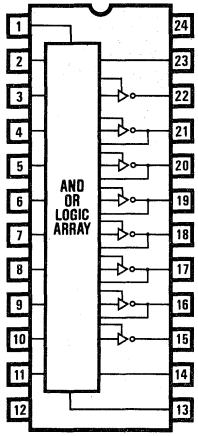
20X8/A



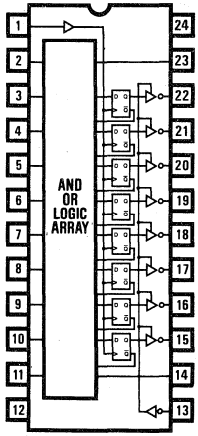
20X4/A



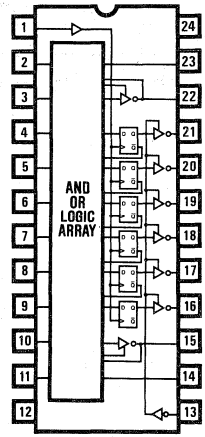
20L8A/A-2/B



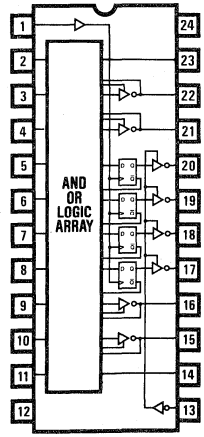
20R8A/A-2/B

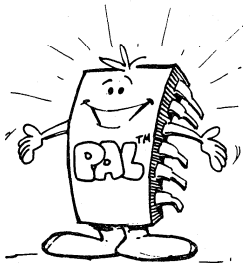


20R6A/A-2/B

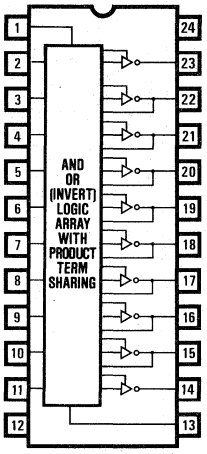


20R4A/A-2/B

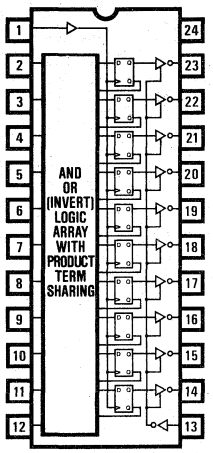




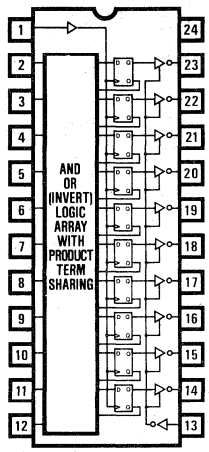
20S10



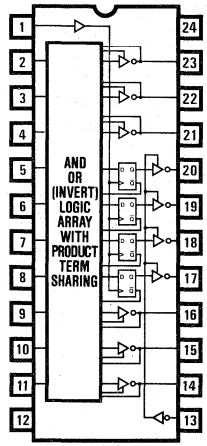
20RS10



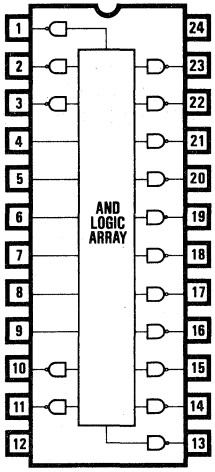
20RS8



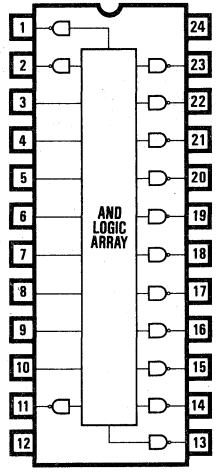
20RS4



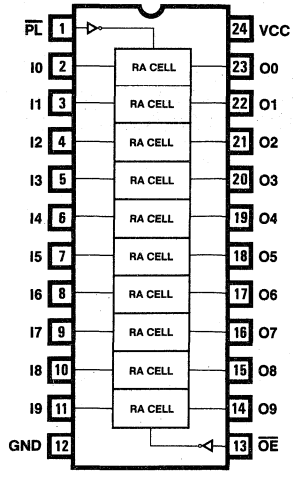
6L16A



8L14A

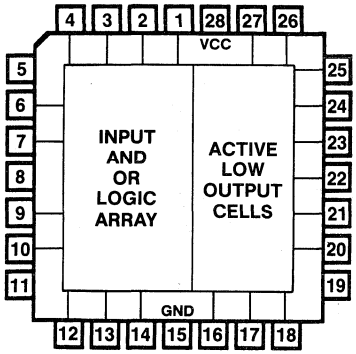


20RA10

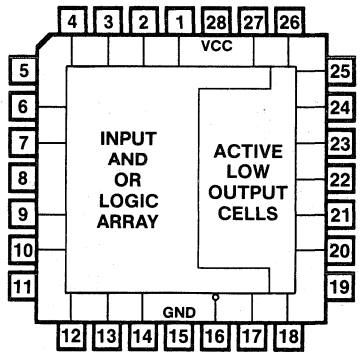


5

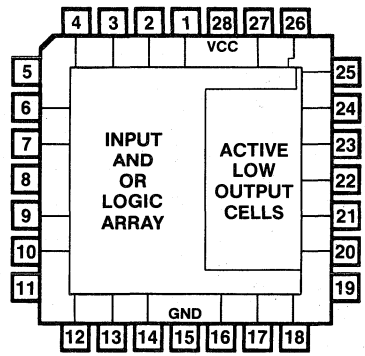
12L10



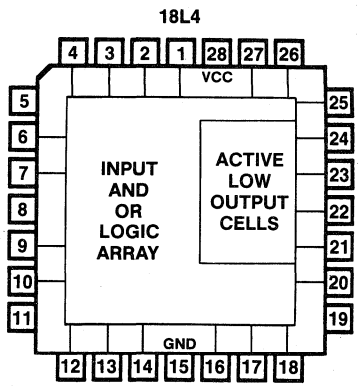
14L8



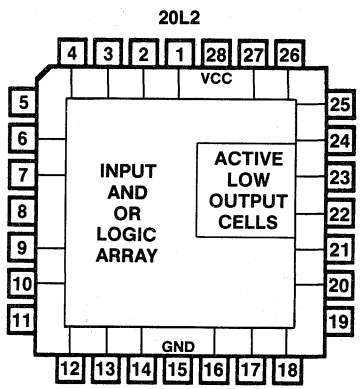
16L6



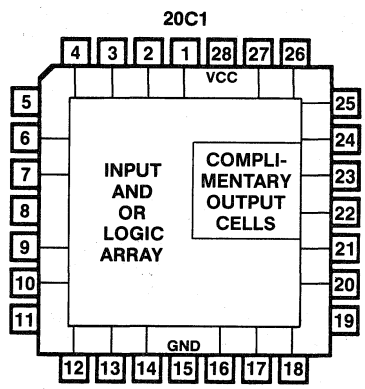
18L4



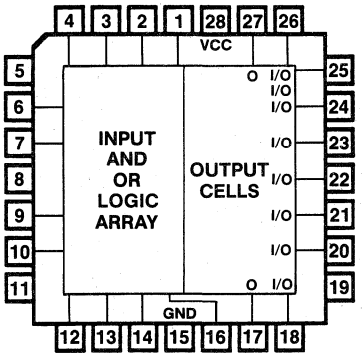
20L2



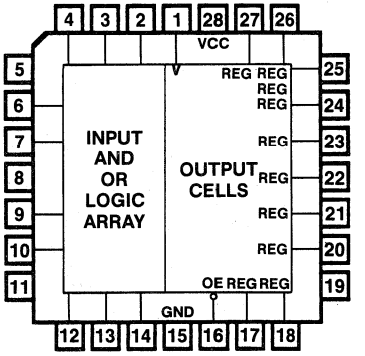
20C1



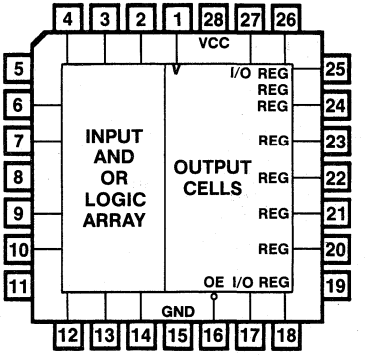
20L10/A



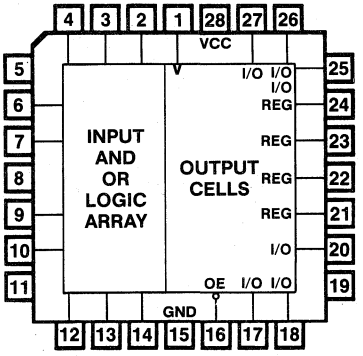
20X10/A



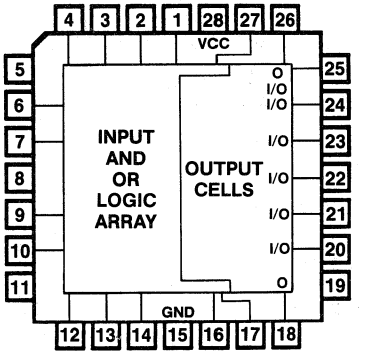
20X8/A



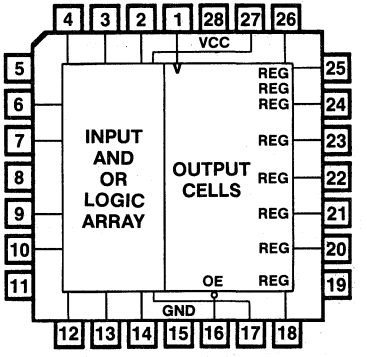
20X4/A



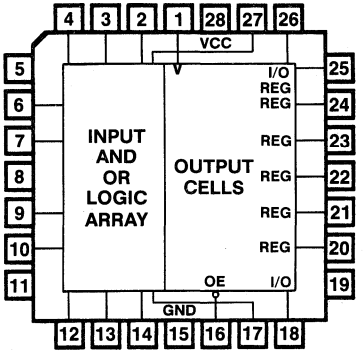
20L8A/A-2/B



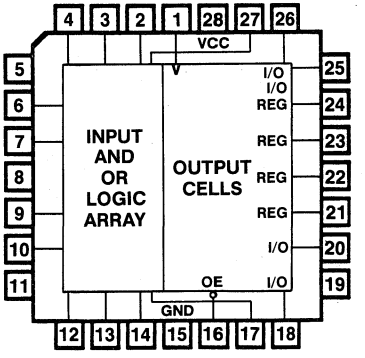
20R8A/A-2/B



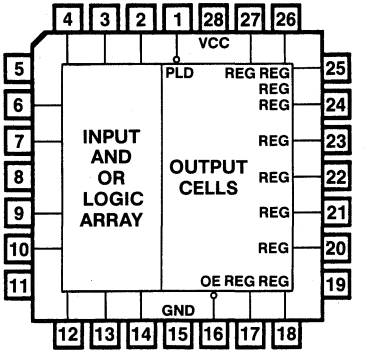
20R6A/A-2/B



20R4A/A-2/B

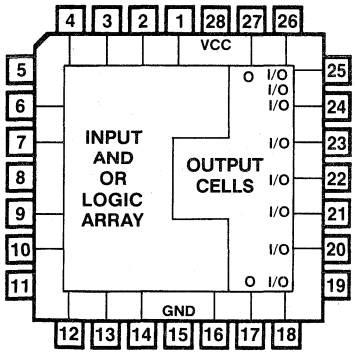


20RA10

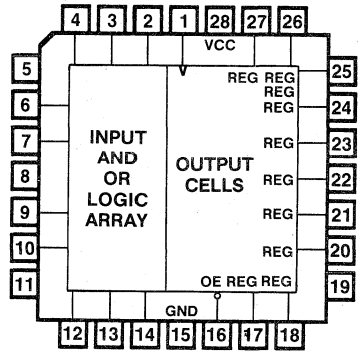


5

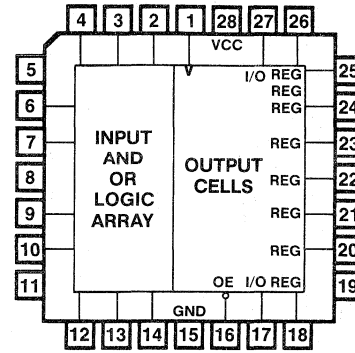
20S10



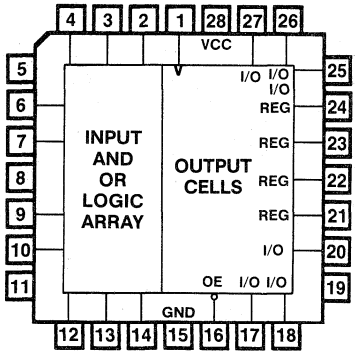
20RS10



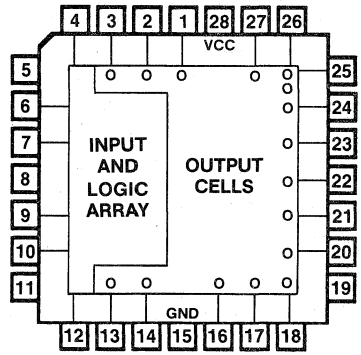
20RS8



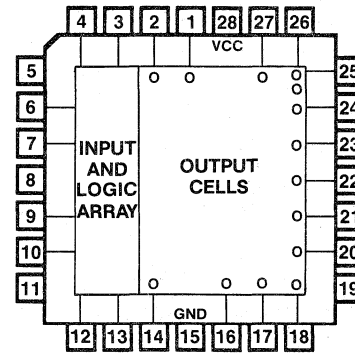
20RS4



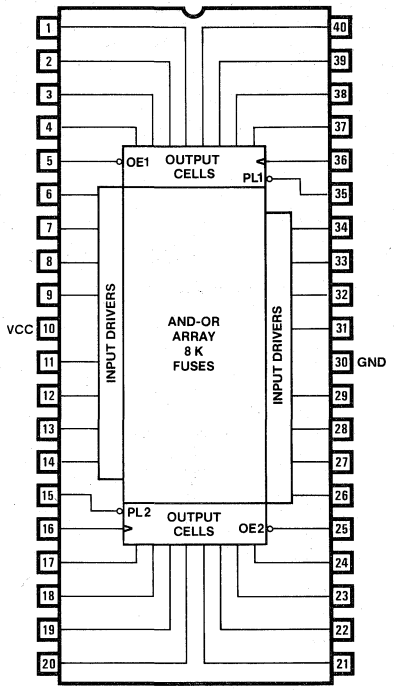
6L16A



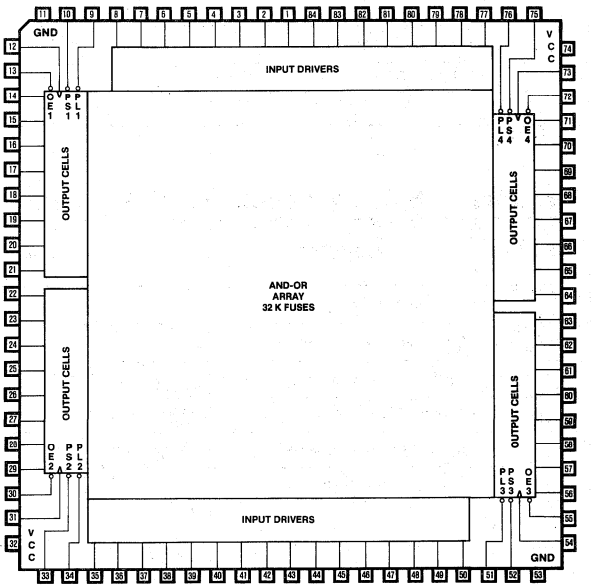
8L14A



32R16

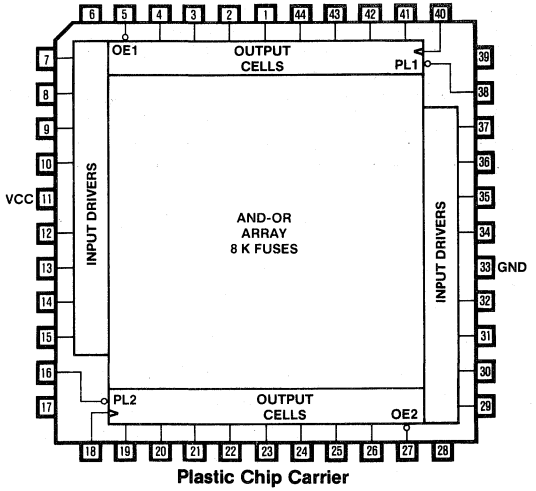


64R32



Plastic Chip Carrier

32R16



Plastic Chip Carrier

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55			0		75	°C
T_C	Operating case temperature			125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = −18mA		−0.8	−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX		V_I = 0.4V		−0.02	−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL	I_{OL} = 8mA		0.3	0.5	V
			COM	I_{OL} = 8mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL	I_{OH} = −2mA	2.4	2.8		V
			COM	I_{OH} = −3.2mA				
I_{OS}	Output short-circuit current**	V_{CC} = 5V		V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX				55	90	mA

Switching Characteristics

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Input or feedback to output	Except 16C1	R1 = 560Ω, R2 = 1.1kΩ		25	45		25	35	ns
		16C1			25	45		25	40	

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	–55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = –18mA			–0.8	–1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V			–0.02	–0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4V				25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	Mil	I_{OL} = 4mA		0.3	0.5	V
			Com	I_{OL} = 4mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	Mil	I_{OH} = –1mA	2.4	2.8		V
			Com	I_{OH} = –1mA				
I_{OS}	Output short-circuit current**	V_{CC} = 5V		V_O = 0V	–30	–70	–130	mA
I_{CC}	Supply current	V_{CC} = MAX				30	45	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Input or feedback to output	R1 = 1.12kΩ R2 = 2.2kΩ		45	80		45	60	ns

Operating Conditions

SYMBOL	PARAMETER		MILITARY 16X4/A4 ONLY MIN	TYP	MAX	COMMERCIAL MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	25	10		25	10		ns
		High	25	10		25	10		
t_{su}	Set up time from input or feedback to clock	16R8, 16R6, 16R4	45	25		35	25		ns
		16X4, 16A4	55	30		45	30		
t_h	Hold time		0	−15		0	−15		ns
T_A	Operating free-air temperature		−55			0		75	°C
T_C	Operating case temperature				125				°C

Electrical Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage					0.8	V
V_{IH}*	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA		−0.8	−1.5	V
I_{IL}†	Low-level input current	V_{CC} = MAX	V_I = 0.4 V		−0.02	−0.25	mA
I_{IH}†	High-level input current	V_{CC} = MAX	V_I = 2.4 V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	Mil 16X4/A4 only I_{OL} = 12 mA		0.3	0.5	V
			Com I_{OL} = 24 mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	Mil 16X4/A4 only I_{OH} = −2 mA	2.4	2.8		V
			Com I_{OH} = −3.2 mA				
I_{OZL}†	Off-state output current	V_{CC} = MAX	V_O = 0.4 V			−100	μA
I_{OZH}†			V_O = 2.4 V			100	μA
I_{OS}**	Output short-circuit current	V_{CC} = 5 V	V_O = 0 V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX	16R4, 16R6, 16R8, 16L8		120	180	mA
			16X4		160	225	
			16A4		170	240	

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY 16X4/A4 ONLY MIN	TYP	MAX	COMMERCIAL MIN	TYP	MAX	UNIT
t_{PD}	Input or feedback to output	16R6, 16R4, 16L8	R_1 = 200 Ω, R_2 = 390 Ω					25	35	ns
		16X4, 16A4			30	45		30	40	
t_{CLK}	Clock to output or feedback				15	25		15	25	ns
t_{PZX}	Pin 11 to output enable except 16L8				15	25		15	25	ns
t_{PXZ}	Pin 11 to output disable except 16L8				15	25		15	25	ns
t_{PZX}	Input to output enable	16R6, 16R4, 16L8						25	35	ns
		16X4, 16A4			30	45		30	40	
t_{PXZ}	Input to output disable	16R6, 16R4, 16L8						25	35	ns
		16X4, 16A4			30	45		30	40	
f_{MAX}	Maximum frequency	16R8, 16R6, 16R4					16	25		MHz
		16X4, 16A4		12	22		14	22		

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	20	10		15	10		ns
		High	20	10		15	10		
t_{su}	Set up time from input or feedback to clock	16R8A, 16R6A, 16R4A	30	15		25	15		ns
t_h	Hold time		0	-10		0	-10		ns
T_A	Operating free-air temperature		-55			0		75	°C
T_C	Operating case temperature				125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18mA			-0.8	-1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX	V_I = 0.4V			-0.02	-0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX	V_I = 2.4V				25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	Mil	I_{OL} = 12mA		0.3	0.5	V
			Com	I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	Mil	I_{OH} = -2mA	2.4	2.8		V
			Com	I_{OH} = -3.2mA				
I_{OZL}	Off-state output current †	V_{CC} = MAX		V_O = 0.4V			-100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current**	V_{CC} = 5V		V_O = 0V	-30	-70	-130	mA
I_{CC}	Supply current	V_{CC} = MAX				120	180	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feedback to output	16R6A, 16R4A, 16L8A	R_1 = 200 Ω, R_2 = 390 Ω		15	30		15	25	ns
t_{CLK}	Clock to output or feedback				10	20		10	15	ns
t_{PZX}	Pin 11 to output enable except 16L8A				10	25		10	20	ns
t_{PXZ}	Pin 11 to output disable except 16L8A				11	25		11	20	ns
t_{PZX}	Input to output enable	16R6A, 16R4A, 16L8A			10	30		10	25	ns
t_{PXZ}	Input to output disable	16R6A, 16R4A, 16L8A			13	30		13	25	ns
f_{MAX}	Maximum frequency	16R8A, 16R6A, 16R4A		20	40		28.5	40		MHz

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	25	10		25	10		ns
		High	25	10		25	10		
t_{su}	Set up time from input or feedback to clock	16R6A-2 16R4A-2 16R8A-2	50	25		35	25		ns
t_h	Hold time		0	-15		0	-15		ns
T_A	Operating free-air temperature		-55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18mA			-0.8	-1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX	V_I = 0.4V			-0.02	-0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX	V_I = 2.4V				25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	Mil	I_{OL} = 12mA		0.3	0.5	V
			Com	I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	Mil	I_{OH} = -2mA	2.4	2.8		V
			Com	I_{OH} = -3.2mA				
I_{OZL}	Off-state output current †	V_{CC} = MAX		V_O = 0.4V			-100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current**	V_{CC} = 5V		V_O = 0V	-30	-70	-130	mA
I_{CC}	Supply current	V_{CC} = MAX				60	90	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feedback to output	16L8A-2 16R6A-2 16R4A-2	R_1 = 200Ω, R_2 = 390Ω		25	50		25	35	ns
t_{CLK}	Clock to output or feedback				15	25		15	25	ns
$t_{PXZ/ZX}$	Pin 11 to output disable/enable except 16L8A-2				15	25		15	25	ns
t_{PZX}	Input to output enable	16L8A-2 16R6A-2 16R4A-2			25	45		25	35	ns
t_{PXZ}	Input to output disable	16L8A-2 16R6A-2 16R4A-2			25	45		25	35	ns
f_{MAX}	Maximum frequency	16R8A-2 16R6A-2 16R4A-2		14	25		16	25		MHz

Operating Conditions

SYMBOL	PARAMETER			MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage			4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock		Low	40	20		30	20		ns
			High	40	20		30	20		
t_{su}	Set up time from input or feedback to clock	16R8A-4 16R6A-4 16R4A-4		90	45		60	45		ns
t_h	Hold time			0	-15		0	-15		ns
T_A	Operating free-air temperature			-55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = -18mA		-0.8	-1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX		V_I = 0.4V		-0.02	-0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	Mil	I_{OL} = 4mA		0.3	0.5	V
			Com	I_{OL} = 8mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	Mil	I_{OH} = -1mA	2.4	2.8		V
			Com	I_{OH} = -1 mA				
I_{OZL}	Off-state output current†	V_{CC} = MAX		V_O = 0.4V			-100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current**	V_{CC} = 5V		V_O = 0V	-30	-70	-130	mA
I_{CC}	Supply current	V_{CC} = MAX				30	50	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feedback to output	16R6A-4 16R4A-4 16L8A-4	R_1 = 800Ω, R_2 = 1.56kΩ		35	75		35	55	ns
t_{CLK}	Clock to output or feedback				20	45		20	35	ns
$t_{PXZ/ZX}$	Pin 11 to output disable/enable—except 16L8A-4				15	40		15	30	ns
t_{PZX}	Input to output enable	16R6A-4 16R4A-4 16L8A-4			30	65		30	50	ns
t_{PXZ}	Input to output disable	16R6A-4 16R4A-4 16L8A-4			30	65		30	50	ns
f_{MAX}	Maximum frequency	16R8A-4 16R6A-4 16R4A-4		8	18		11	18		MHz

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
t_w	Width of clock	Low	10	6		ns
		High	10	5		
t_{su}	Setup time from input or feedback to clock	16R8B 16R6B 16R4B	15	10		ns
t_h	Hold time		0	−10		ns
T_A	Operating free-air temperature		0	25	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		COMMERCIAL MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage					0.8	V
V_{IH}*	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA		−0.8	−1.5	V
I_{IL}†	Low-level input current	V_{CC} = MAX	V_I = 0.4 V		−0.02	−0.25	mA
I_{IH}†	High-level input current	V_{CC} = MAX	V_I = 2.4 V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 24 mA		0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = −3.2 mA	2.4	2.8		V
I_{OZL}†	Off-state output current	V_{CC} = MAX	V_O = 0.4 V			−100	μA
I_{OZH}†			V_O = 2.4 V			100	μA
I_{OS}**	Output short-circuit current	V_{CC} = 5 V	V_O = 0 V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX			120	180	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	COMMERCIAL MIN	TYP	MAX	UNIT
t_{PD}	16L8B, 16R4B, 16R6B input or feedback to output		Commercial R_1 = 200 Ω R_2 = 360 Ω		12	15	ns
t_{CLK}	Clock to output or feedback except 16L8B				8	12	ns
t_{PZX}	Pin 11 to output enable except 16L8B				10	15	ns
t_{PXZ}	Pin 11 to output disable except 16L8B				10	15	ns
t_{PZX}	Input to output enable	16R6B, 16R4B, and 16L8B			12	22	ns
t_{PXZ}	Input to output disable	16R6B, 16R4B, and 16L8B			12	20	ns
f_{MAX}	16R8B, 16R6B, 16R4B Maximum frequency	Feedback		37	45		MHz
		No feedback		50	55		

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
t_w	Width of clock	Low	15	10		ns
		High	15	10		
t_{su}	Setup time from input or feedback to clock	16R8B-2 16R6B-2 16R4B-2	25	15		ns
t_h	Hold time		0	−10		ns
T_A	Operating free-air temperature		0	25	75	°C

5

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}*	Low-level input voltage					0.8	V
V_{IH}*	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA		−0.8	−1.5	V
I_{IL}†	Low-level input current	V_{CC} = MAX	V_I = 0.4 V		−0.02	−0.25	mA
I_{IH}†	High-level input current	V_{CC} = MAX	V_I = 2.4 V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 24 mA		0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = −3.2 mA	2.4	2.8		V
I_{OZL}†	Off-state output current	V_{CC} = MAX	V_O = 0.4 V			−100	μA
I_{OZH}†			V_O = 2.4 V			100	μA
I_{OS}**	Output short-circuit current	V_{CC} = 5 V	V_O = 0 V	−30	−100	−250	mA
I_{CC}	Supply current	V_{CC} = MAX			60	90	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feedback to output 16L8B-2, 16R4B-2, and 16R6B-2	Commercial R_1 = 200 Ω R_2 = 390 Ω		17	25	ns
t_{CLK}	Clock to output or feedback except 16L8B-2			10	15	ns
t_{PZX}	Pin 11 to output enable except 16L8B-2			10	20	ns
t_{PXZ}	Pin 11 to output disable except 16L8B-2			11	20	ns
t_{PZX}	Input to output enable 16R6B-2, 16R4B-2, and 16L8B-2			10	25	ns
t_{PXZ}	Input to output disable 16R6B-2, 16R4B-2, and 16L8B-2			13	25	ns
f_{MAX}	Maximum frequency 16R8B-2, 16R6B-2, and 16R4B-2		28.5	40		MHz

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
t_w	Width of clock	Low	25	10		ns
		High	25	10		
t_{su}	Setup time from input or feedback to clock	16R8B-4 16R6B-4 16R4B-4	35	25		ns
t_h	Hold time		0	−10		ns
T_A	Operating free-air temperature		0	25	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}*	Low-level input voltage					0.8	V
V_{IH}*	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA		−0.8	−1.5	V
I_{IL}†	Low-level input current	V_{CC} = MAX	V_I = 0.4 V		−0.02	−0.25	mA
I_{IH}†	High-level input current	V_{CC} = MAX	V_I = 2.4 V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 8 mA		0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = −1 mA	2.4	2.8		V
I_{OZL}†	Off-state output current	V_{CC} = MAX	V_O = 0.4 V			−100	μA
I_{OZH}†			V_O = 2.4 V			100	μA
I_{OS}**	Output short-circuit current	V_{CC} = 5 V	V_O = 0 V	−30	−100	−250	mA
I_{CC}	Supply current	V_{CC} = MAX			30	55	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feedback to output 16L8B-4, 16R4B-4, and 16R6B-4	R_1 = 800 Ω R_2 = 1.56K Ω		25	35	ns
t_{CLK}	Clock to output or feedback except 16L8B-4			15	25	ns
t_{PZX}	Pin 11 to output enable except 16L8B-4			15	25	ns
t_{PXZ}	Pin 11 to output disable except 16L8B-4			15	25	ns
t_{PZX}	Input to output enable 16R6B-4, 16R4B-4, and 16L8B-4			25	35	ns
t_{PXZ}	Input to output disable 16R6B-4, 16R4B-4, and 16L8B-4			25	35	ns
f_{MAX}	Maximum frequency 16R8B-4, 16R6B-4, and 16R4B-4		16	25		MHz

Operating Conditions

SYMBOL	PARAMETER			COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage			4.75	5	5.25	V
t_w	Width of clock	Low		20	14		ns
		High		10	6		
t_{su}	Setup time from input or feedback to clock	16RP8A 16RP6A 16RP4A	Polarity fuse intact	25	15		ns
			Polarity fuse blown	30	20		
t_h	Hold time			0	−10		ns
T_A	Operating free-air temperature			0		75	°C
T_C	Operating case temperature						°C

5

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage					0.8	V
V_{IH}*	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA		−0.8	−1.5	V
I_{IL}†	Low-level input current	V_{CC} = MAX	V_I = 0.4 V		−0.02	−0.25	mA
I_{IH}†	High-level input current	V_{CC} = MAX	V_I = 2.4 V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 24 mA		0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = −3.2 mA	2.4	2.8		V
I_{OZL}†	Off-state output current	V_{CC} = MAX	V_O = 0.4 V			−100	μA
I_{OZH}†			V_O = 2.4 V			100	μA
I_{OS}**	Output short-circuit current	V_{CC} = 5 V	V_O = 0 V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX			120	180	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feedback to output 16P8A, 16RP6A, 16RP4A	Polarity fuse intact	R_1 = 200 Ω R_2 = 390 KΩ		15	25	ns
		Polarity fuse blown			20	30	
t_{CLK}	Clock to output or feedback				10	15	ns
t_{PZX}	Pin 11 to output enable except 16P8A				10	20	ns
t_{PXZ}	Pin 11 to output disable except 16P8A				11	20	ns
t_{PZX}	Input to output enable	16RP6A, 16RP4A, and 16P8A			10	25	ns
t_{PXZ}	Input to output disable	16RP6A, 16RP4A, and 16P8A			13	25	ns
f_{MAX}	Maximum frequency 16RP8A, 16RP6A, 16RP4A	Polarity fuse intact		28.5	40		MHz
		Polarity fuse blown		25	33		

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
t_w	Width of clock		20	13		ns
t_{wp}	Preload pulse width		35	15		ns
t_{su}	Setup time for input or feedback to clock		20	10		ns
t_{sup}	Preload setup time		25	5		ns
t_h	Hold time	Polarity fuse intact	10	-2		ns
		Polarity fuse blown	0	-6		
t_{hp}	Preload hold time		25	5		ns
T_A	Operating free-air temperature		0		75	°C
T_C	Operating case temperature					°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA		-0.8	-1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V		-0.02	-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4 V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 8 mA		0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = -3.2 mA	2.4	2.8		V
I_{OZ}	Off-state output current	V_{CC} = MAX	V_O = 2.4 V/V_O = 0.4 V	-100		100	μA
I_{OS}	Output short-circuit current	V_{CC} = 5 V	V_O = 0 V	-30	-70	-130	mA
I_{CC}	Supply current	V_{CC} = MAX			135	170	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feedback to output	Polarity fuse intact	R_1 = 560 Ω, R_2 = 1.1 KΩ		20	30	ns
		Polarity fuse blown			25	35	
t_{CLK}	Clock to output or feedback			10	17	30	ns
t_S	Input to asynchronous set				22	35	ns
t_R	Input to asynchronous reset				27	40	ns
t_{PZX}	Pin 11 to output enable				10	20	ns
t_{PXZ}	Pin 11 to output disable				10	20	ns
t_{PZX}	Input to output enable				18	30	ns
t_{PXZ}	Input to output disable				15	30	ns
f_{MAX}	Maximum frequency			20	35		MHz

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	–55			0		75	°C
T_C	Operating case temperature			125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = –18mA		–0.8	–1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX		V_I = 0.4V		–0.02	–0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL	I_{OL} = 8mA		0.3	0.5	V
			COM	I_{OL} = 8mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL	I_{OH} = –2mA	2.4	2.8		V
			COM	I_{OH} = –3.2mA				
I_{OS}	Output short-circuit current**	V_{CC} = 5V		V_O = 0V	–30	–70	–130	mA
I_{CC}	Supply current	V_{CC} = MAX				60	100	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Input or feedback to output	R1 = 560Ω R2 = 1.1kΩ		25	45		25	40	ns

Operating Conditions

SYMBOL	PARAMETER	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
T_A	Operating free-air temperature	0	25	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage					0.8	V
V_{IH}*	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA		−0.8	−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V		−0.02	−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4 V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 8 mA		0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = −3.2 mA	2.4	2.8		V
I_{OS} **	Output short-circuit current	V_{CC} = 5 V	V_O = 0 V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX			60	90	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input to output propagation delay	R1 = 560 Ω R2 = 1.1 KΩ		15	25	ns

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	20	7		15	7		ns
		High	20	7		15	7		
t_{su}	Set up time from input or feedback to clock	20R8A 20R6A 20R4A	30	15		25	15		ns
t_h	Hold time		0	-10		0	-10		ns
T_A	Operating free-air temperature		-55			0		75	°C
T_C	Operating case temperature				125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18mA			-0.8	-1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX	V_I = 0.4V			-0.02	-0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX	V_I = 2.4V				25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	Mil	I_{OL} = 12mA		0.3	0.5	V
			Com	I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	Mil	I_{OH} = -2mA	2.4	2.8		V
			Com	I_{OH} = -3.2mA				
I_{OZL}	Off-state output current †	V_{CC} = MAX		V_O = 0.4V			-100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current**	V_{CC} = 5V		V_O = 0V	-30	-90	-130	mA
I_{CC}	Supply current	V_{CC} = MAX				160	210	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feedback to output	20R6A 20R4A 20L8A	R_1 = 200Ω, R_2 = 390Ω		15	30		15	25	ns
t_{CLK}	Clock to output or feedback				10	20		10	15	ns
t_{PZX}	Pin 13 to output enable except 20L8A				10	25		10	20	ns
t_{PXZ}	Pin 13 to output disable except 20L8A				11	25		11	20	ns
t_{PZX}	Input to output enable	20R6A 20R4A 20L8A			10	30		10	25	ns
t_{PXZ}	Input to output disable	20R6A 20R4A 20L8A			13	30		13	25	ns
f_{MAX}	Maximum frequency	20R8A 20R6A 20R4A		20	40		28.5	40		MHz

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
t_w	Width of clock	Low	25	10		ns
		High	25	10		
t_{su}	Setup time from input or feedback to clock	20R8A-2, 20R6A-2, 20R4A-2	35	25		ns
t_h	Hold time		0	−15		ns
T_A	Operating free-air temperature		0	25	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage					0.8	V
V_{IH}*	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA		−0.8	−1.5	V
I_{IL}†	Low-level input current	V_{CC} = MAX	V_I = 0.4 V		−0.02	−0.25	mA
I_{IH}†	High-level input current	V_{CC} = MAX	V_I = 2.4 V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 24 mA		0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = −3.2 mA	2.4	2.8		V
I_{OZL}†	Off-state output current	V_{CC} = MAX	V_O = 0.4 V			−100	μA
I_{OZH}†			V_O = 2.4 V			100	μA
I_{OS}**	Output short-circuit current	V_{CC} = 5 V	V_O = 0 V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX			80	105	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feedback to output 20L8A-2 20R6A-2 20R4A-2	Commercial R_1 = 200 Ω R_2 = 390 Ω		25	50		25	35	ns
t_{CLK}	Clock to output or feedback except 20L8A-2			15	25		15	25	ns
$t_{PXZ/ZX}$	Pin 13 to output disable/enable except 20L8A-2			15	25		15	25	ns
t_{PZX}	Input to output enable 20L8A-2 20R6A-2 20R4A-2			25	45		25	35	ns
t_{PXZ}	Input to output disable 20L8A-2 20R6A-2 20R4A-2			25	45		25	35	ns
f_{MAX}	Maximum frequency 20R8A-2 20R6A-2 20R4A-2		14	19		16	19		MHz

Operating Conditions

SYMBOL	PARAMETER			COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage			4.75	5	5.25	V
t_w	Width of clock	Low	20R8B, 20R6B, 20R4B	10	6		ns
		High		12	8		
t_{su}	Setup time from input or feedback to clock			15	10		ns
t_h	Hold time			0	−10		ns
T_A	Operating free-air temperature			0	25	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}*	Low-level input voltage					0.8	V
V_{IH}*	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA		−0.8	−1.5	V
I_{IL}†	Low-level input current	V_{CC} = MAX	V_I = 0.4 V		−0.02	−0.25	mA
I_{IH}†	High-level input current	V_{CC} = MAX	V_I = 2.4 V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 24 mA		0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = −3.2 mA	2.4	2.8		V
I_{OZL}†	Off-state output current	V_{CC} = MAX	V_O = 0.4 V			−100	μA
I_{OZH}†			V_O = 2.4 V			100	μA
I_{OS}**	Output short-circuit current	V_{CC} = 5 V	V_O = 0 V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX			140	210	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feedback to output 20L8B, 20R6B, 20R4B		Commercial R_1 = 200 Ω R_2 = 390 Ω		12	15	ns
t_{CLK}	Clock to output or feedback except 20L8B				8	12	ns
t_{PZX}	Pin 13 to output enable except 20L8B				10	15	ns
t_{PXZ}	Pin 13 to output disable except 20L8B				8	12	ns
t_{PZX}	Input to output enable 20R6B, 20R4B, 20L8B				12	18	ns
t_{PXZ}	Input to output disable 20R6B, 20R4B, 20L8B				12	15	ns
f_{MAX}	Maximum frequency 20R8B, 20R6B, 20R4B	Feedback		37	40		MHz
		No feedback		45	50		

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	40	20		35	20		ns
		High	30	10		25	10		
t_{su}	Set up time from input or feedback to clock	20X10, 20X8, 20X4	60	38		50	38		ns
t_h	Hold time		0	−15		0	−15		ns
T_A	Operating free-air temperature		−55			0		75	°C
T_C	Operating case temperature				125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−0.8	−1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX	V_I = 0.4V			−0.02	−0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX	V_I = 2.4V				25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	Mil	I_{OL} = 12mA		0.3	0.5	V
			Com	I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	Mil	I_{OH} = −2mA	2.4	2.8		V
			Com	I_{OH} = −3.2mA				
I_{OZL}	Off-state output current †	V_{CC} = MAX		V_O = 0.4V			−100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current**	V_{CC} = 5V		V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX	20X10	20X8 20X4		120	180	mA
I_{CC}	Supply current	V_{CC} = MAX	20L10			90	165	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feedback to output 20X8, 20X4, 20LID	R_1 = 200 Ω, R_2 = 390 Ω		35	60		35	50	ns
t_{CLK}	Clock to output or feedback except 20L10			20	35		20	30	ns
$t_{PXZ/ZX}$	Pin 13 to output disable/enable except 20L10			20	45		20	35	ns
t_{PZX}	Input to output enable except 20X10			35	55		35	45	ns
t_{PXZ}	Input to output disable except 20X10			35	55		35	45	ns
f_{MAX}	Maximum frequency 20X10, 20X8, 20X4		10.5	16		12.5	16		MHz

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
t_w	Width of clock	Low	25	15		ns
		High	15	7		
t_{su}	Setup time from input or feedback to clock	20X10A 20X8A 20X4A	30	20		ns
t_h	Hold time		0	−15		ns
T_A	Operating free-air temperature		0	25	75	°C

5

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage					0.8	V
V_{IH}*	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA		−0.8	−1.5	V
I_{IL}†	Low-level input current	V_{CC} = MAX	V_I = 0.4 V		−0.02	−0.25	mA
I_{IH}†	High-level input current	V_{CC} = MAX	V_I = 2.4 V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 24 mA		0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = −3.2 mA	2.4	2.8		V
I_{OZL}†	Off-state output current	V_{CC} = MAX	V_O = 0.4 V			−100	μA
I_{OZH}†			V_O = 2.4 V			100	μA
I_{OS}**	Output short-circuit current	V_{CC} = 5 V	V_O = 0 V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX	20X10A,20X8A,20X4A		140	180	mA
			20L10A		115	165	

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feedback to output 20L10A, 20X8A, and 20X4A		Commercial R_1 = 200 Ω R_2 = 360 Ω		23	30	ns
t_{CLK}	Clock to output or feedback				10	15	ns
t_{PZX}	Pin 13 to output enable except 20L10A				11	20	ns
t_{PXZ}	Pin 13 to output disable except 20L10A				10	20	ns
t_{PZX}	Input to output enable	20X8A, 20X4A, and 20L10A			19	30	ns
t_{PXZ}	Input to output disable	20X8A, 20X4A, and 20L10A			15	30	ns
f_{MAX}	Maximum frequency	20X10A, 20X8A, and 20X4A		22.2	32		MHz

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	20	10		15	10		ns
		High	20	10		15	10		
t_{su}	Setup time from input or feedback to clock	20RS10, 20RS8, 20RS4	40	25		35	25		ns
t_h	Hold time		0	−10		0	−10		ns
T_A	Operating free-air temperature		−55			0		75	°C
T_C	Operating case temperature				125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA			−0.8	−1.5	V
I_{IL}†	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			−0.02	−0.25	mA
I_{IH}†	High-level input current	V_{CC} = MAX	V_I = 2.4 V				25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	Mil	I_{OL} = 12 mA		0.3	0.5	V
			Com	I_{OL} = 24 mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	Mil	I_{OH} = −2 mA	2.4	2.8		V
			Com	I_{OH} = −3.2 mA				
I_{OZL}†	Off-state output current	V_{CC} = MAX		V_O = 0.4 V			−100	μA
I_{OZH}†				V_O = 2.4 mA			100	
I_{OS}**	Output short-circuit current	V_{CC} = 5 V		V_O = 0 V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX				175	240	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feedback to output 20S10, 20RS8, 20RS4	Polarity fuse intact	Commercial R_1 = 200 Ω R_2 = 390 KΩ		25	40		25	35	ns
		Polarity fuse blown			30	45		30	40	
t_{CLK}	Clock to output or feedback				12	20		12	17	ns
t_{PZX}	Pin 13 to output enable except 20S10				10	25		10	20	ns
t_{PXZ}	Pin 13 to output disable except 20S10				11	25		11	20	ns
t_{PZX}	Input to output enable	20S10, 20RS8, 20RS4			25	35		25	35	ns
t_{PXZ}	Input to output disable	20S10, 20RS8 20RP4	Military R_1 = 390 Ω R_2 = 750 Ω		13	30		13	25	ns
f_{MAX}	Maximum frequency	20RS10, 20RS8, 20RS4		18	28		20	28		MHz

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	25	13		20	13		ns
		High	25	13		20	13		
t_{wp}	Preload pulse width		45	15		35	15		ns
t_{su}	Setup time for input or feedback to clock		25	10		20	10		ns
t_{sup}	Preload setup time		30	5		25	5		ns
t_h	Hold time	Polarity fuse intact	10	-2		10	-2		ns
		Polarity fuse blown	0	-6		0	-6		
t_{hp}	Preload hold time		30	5		25	5		ns
T_A	Operating free-air temperature		-55			0		75	°C
T_C	Operating case temperature				125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage					0.8	V
V_{IH}*	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA		-0.8	-1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V		-0.02	-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4 V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 8 mA		0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH}: Mil-2 mA Com-3.2 mA	2.4	2.8		V
I_{OZ}	Off-state output current	V_{CC} = MAX	V_O = 2.4 V/V_O = 0.4 V	-100		100	μA
I_{OS}**	Output short-circuit current	V_{CC} = 5 V	V_O = 0 V	-30	-70	-130	mA
I_{CC}	Supply current	V_{CC} = MAX			155	200	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feedback to output	Polarity fuse intact	R_1 = 560 Ω, R_2 = 1.1 KΩ		20	35		20	30	ns
		Polarity fuse blown			25	40		25	35	
t_{CLK}	Clock to output or feedback			10	17	35	10	17	30	ns
t_S	Input to asynchronous set				22	40		22	35	ns
t_R	Input to asynchronous reset				27	45		27	40	ns
t_{PZX}	Pin 13 to output enable				10	25		10	20	ns
t_{PXZ}	Pin 13 to output disable				10	25		10	20	ns
t_{PZX}	Input to output enable				18	35		18	30	ns
t_{PXZ}	Input to output disable				15	35		15	30	ns
f_{MAX}	Maximum frequency			16	35		20	35		MHz

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	25			20			ns
		High	25			20			
t_{wp}	Preload pulse width		45			35			ns
t_{su}	Setup time for input to clock	Polarity fuse intact	50			40			ns
		Polarity fuse blown	50			40			
t_{sup}	Preload setup time		30			25			ns
t_h	Hold time		0		-10	0		-10	ns
t_{hp}	Preload hold time		10			5			ns
T_A	Operating free-air temperature		-55			0		75	°C
T_C	Operating case temperature				125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA			-0.8	-1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			-0.02	-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4 V				25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	Mil	I_{OL} = 8 mA		0.3	0.5	V
			Com	I_{OL} = 8 mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	Mil	I_{OH} = -2 mA	2.4	2.8		V
			Com	I_{OH} = -3.2 mA				
I_{OZL}	Off-state output current	V_{CC} = MAX		V_O = 0.4 V			-100	μA
I_{OZH}				V_O = 2.4 V			100	μA
I_{OS}**	Output short-circuit current	V_{CC} = MAX		V_O = 0 V	-30	-70	-130	mA
I_{CC}	Supply current	V_{CC} = MAX				200	280	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input to output	Polarity fuse intact	R_1 = 560 Ω, R_2 = 1.1 KΩ			50			40	ns
		Polarity fuse blown				55			45	
t_{CLK}	Clock to output or feedback					30			25	ns
t_{PZX}	Output enable					25			20	ns
t_{PXZ}	Output disable					25			20	ns
f_{MAX}	Maximum frequency			14			16			MHz

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
t_w	Width of clock	Low	20			ns
		High	20			
t_{su}	Setup time from input to clock	Polarity fuse intact	40			ns
		Polarity fuse blown	40			
t_h	Hold time		0	-10		ns
T_A	Operating free-air temperature		0		75	°C
T_C	Operating case temperature					°C

5

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		COMMERCIAL MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage					0.8	V
V_{IH}*	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA		-0.8	-1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V		-0.02	-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4 V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 8 mA		0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = -0.4 mA	2.4	2.8		V
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4 V			-100	μA
I_{OZH}			V_O = 2.4 V			100	μA
I_{OS}**	Output short-circuit current	V_{CC} = 5 V	V_O = 0 V	-10	-40	-60	mA
I_{CC}	Supply current	V_{CC} = MAX			400	640	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	COMMERCIAL MIN	TYP	MAX	UNIT
t_{PD}	Input to output	Polarity fuse intact	R_1 = 560 Ω, R_2 = 1.1 KΩ			50	ns
		Polarity fuse blown				55	
t_{CLK}	Clock to output or feedback					22	ns
t_{PZX}	Output enable					30	ns
t_{PXZ}	Output disable					30	ns
t_{PRH}	Preset to output					35	ns
f_{MAX}	Maximum frequency			16	20		MHz

Testing Conditions

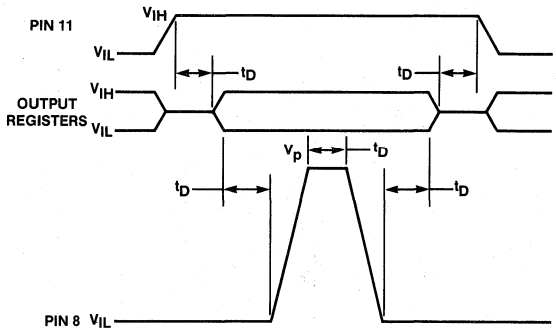
SYMBOL	PARAMETER	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{wp}	Preload pulse width	35			ns
t_{sup}	Preload setup time	50			ns
t_{hp}	Preload hold time	5			ns
t_{PRW}	Preset pulse width	25			ns
t_{PRR}	Preset recovery time	35			ns

Output Register PRELOAD

The PRELOAD function allows the register to be loaded from data placed on the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for PRELOAD is as follows:

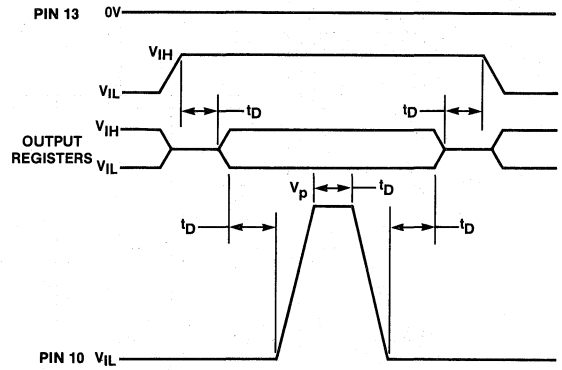
Series 20PA

1. Raise V_{CC} to 4.5 V.
2. Disable output registers by setting pin 11 to V_{IH}.
3. Apply V_{IL}/V_{IH} to all registered output pins.
4. Pulse pin 8 to V_p, then back to 0 V.
5. Remove V_{IL}/V_{IH} from all output registers.
6. Lower pin 11 to V_{IL} to enable the output registers.
7. Verify for V_{OL}/V_{OH} at all registered output pins.



Series 24RS/24XA

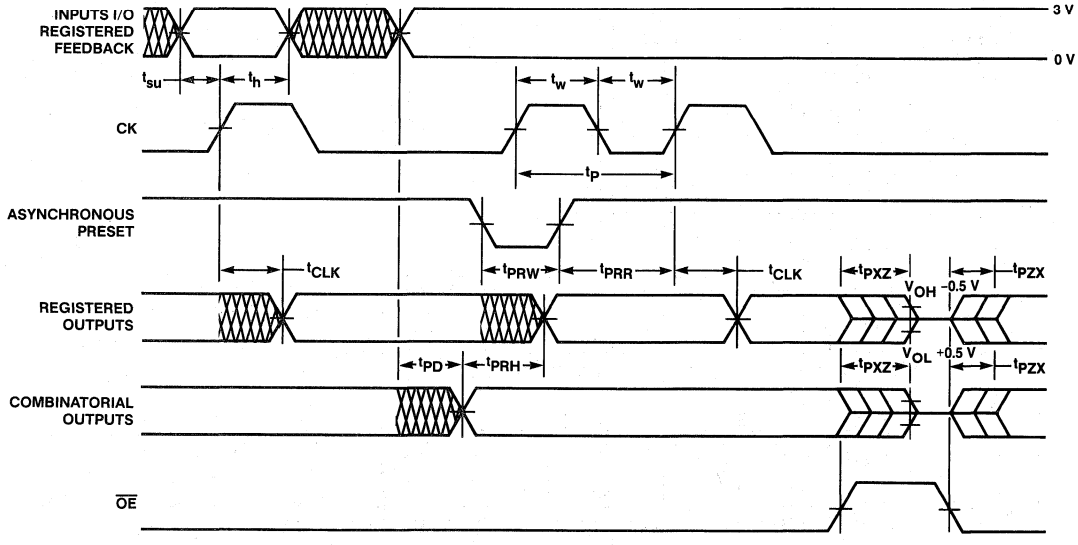
1. Raise V_{CC} to 4.5 V.
2. Disable output registers by setting pin 13 to V_{IH}.
3. Apply V_{IL}/V_{IH} to all registered output pins.
4. Pulse pin 10 to V_p, then back to 0 V.
5. Remove V_{IL}/V_{IH} from all output registers.
6. Lower pin 13 to V_{IL} to enable the output registers.
7. Verify for V_{OL}/V_{OH} at all registered output pins.



Power-Up RESET

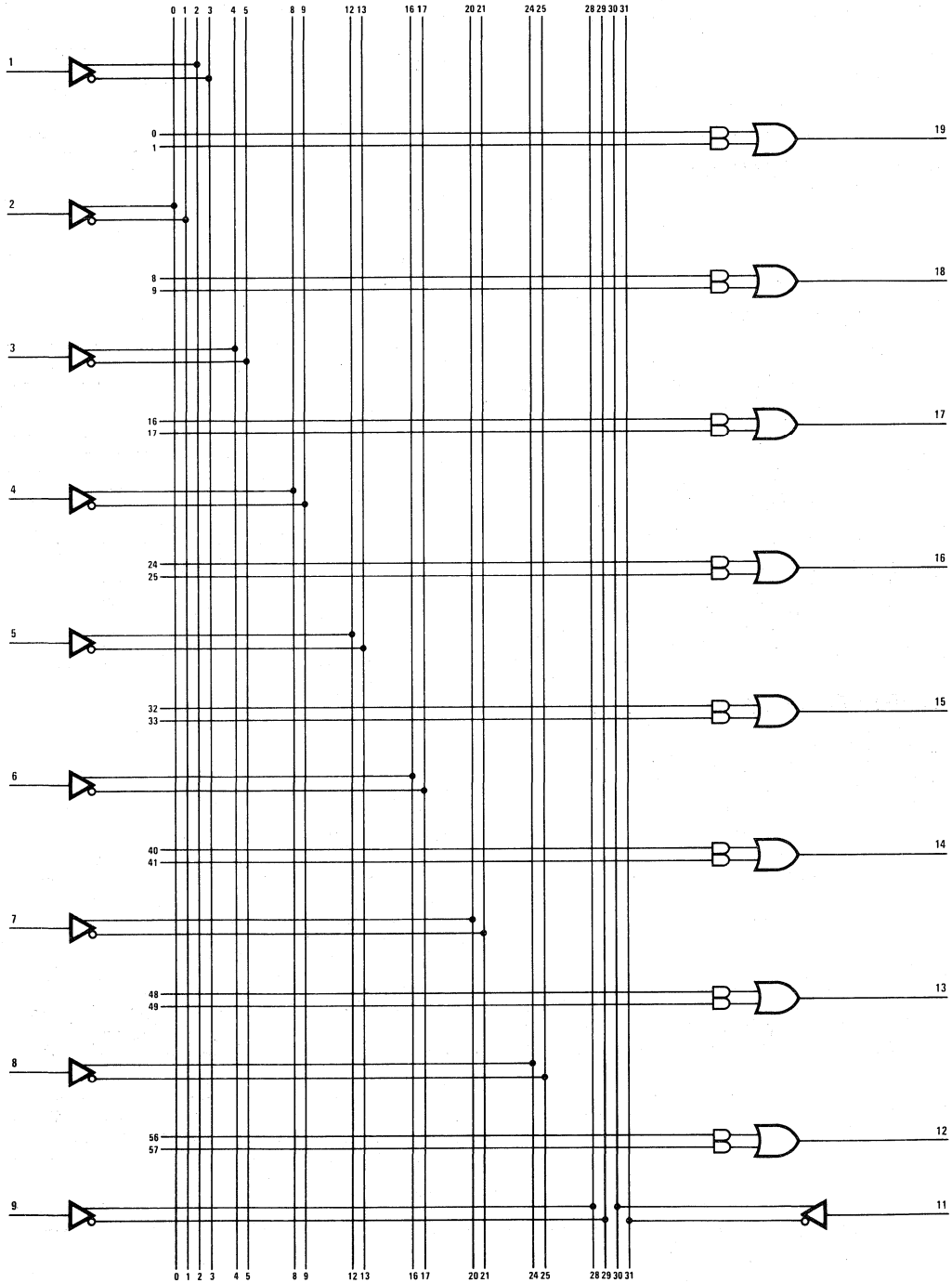
All devices with this PRELOAD feature also have power-up RESET. All registers power up to a logic high for predictable system initialization.

Switching Waveforms

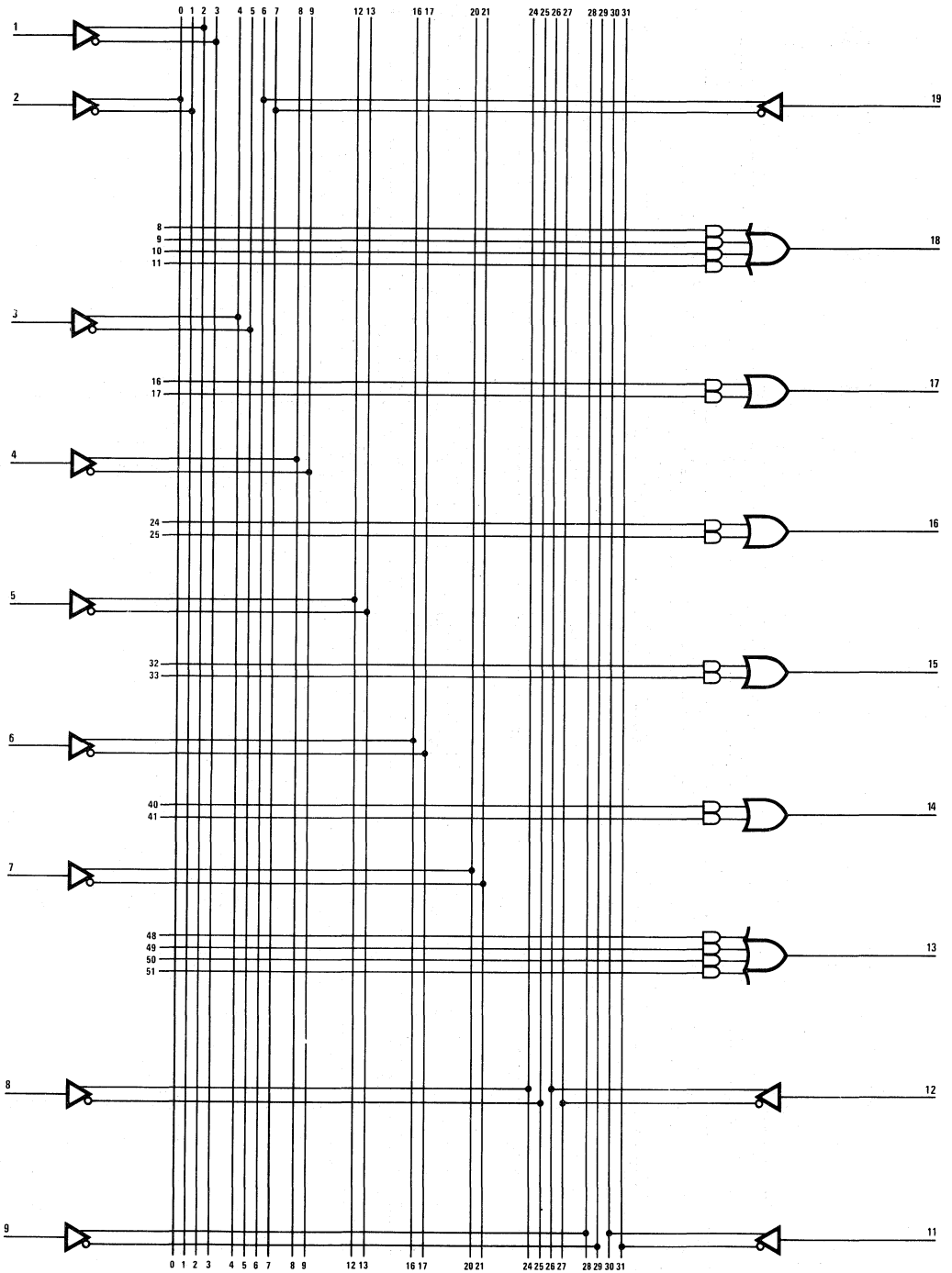


Notes: 1. Input pulse amplitude 0 V to 3.0 V.
2. Input access measured at the 1.5 V level.

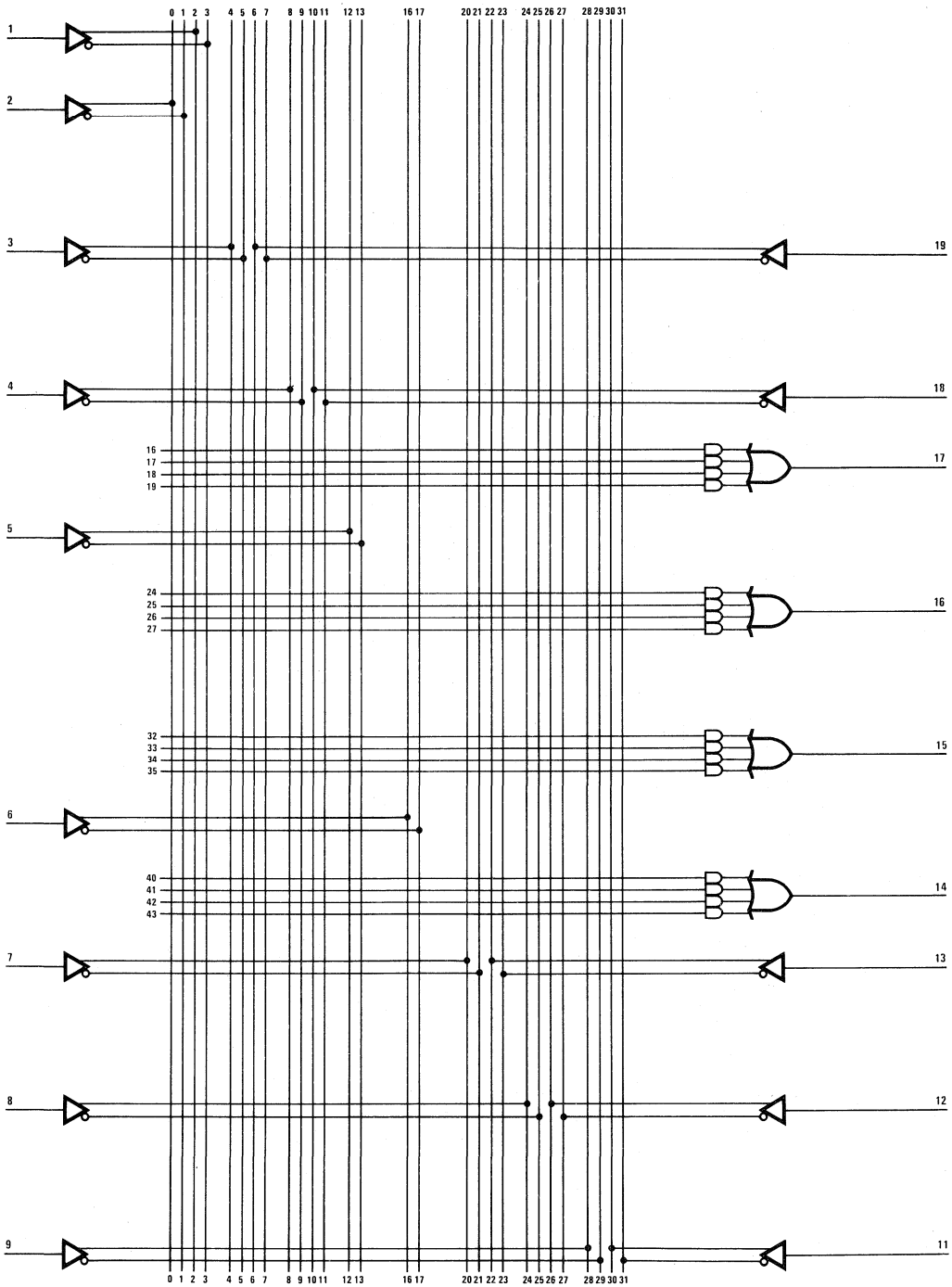
10H8


0 1 2 3 4 5 8 9 12 13 16 17 20 21 24 25 28 29 30 31
1
0
1
19
2
8
9
18
3
16
17
17
4
24
25
16
5
32
33
15
6
40
41
14
7
48
49
13
8
56
57
12
9
11

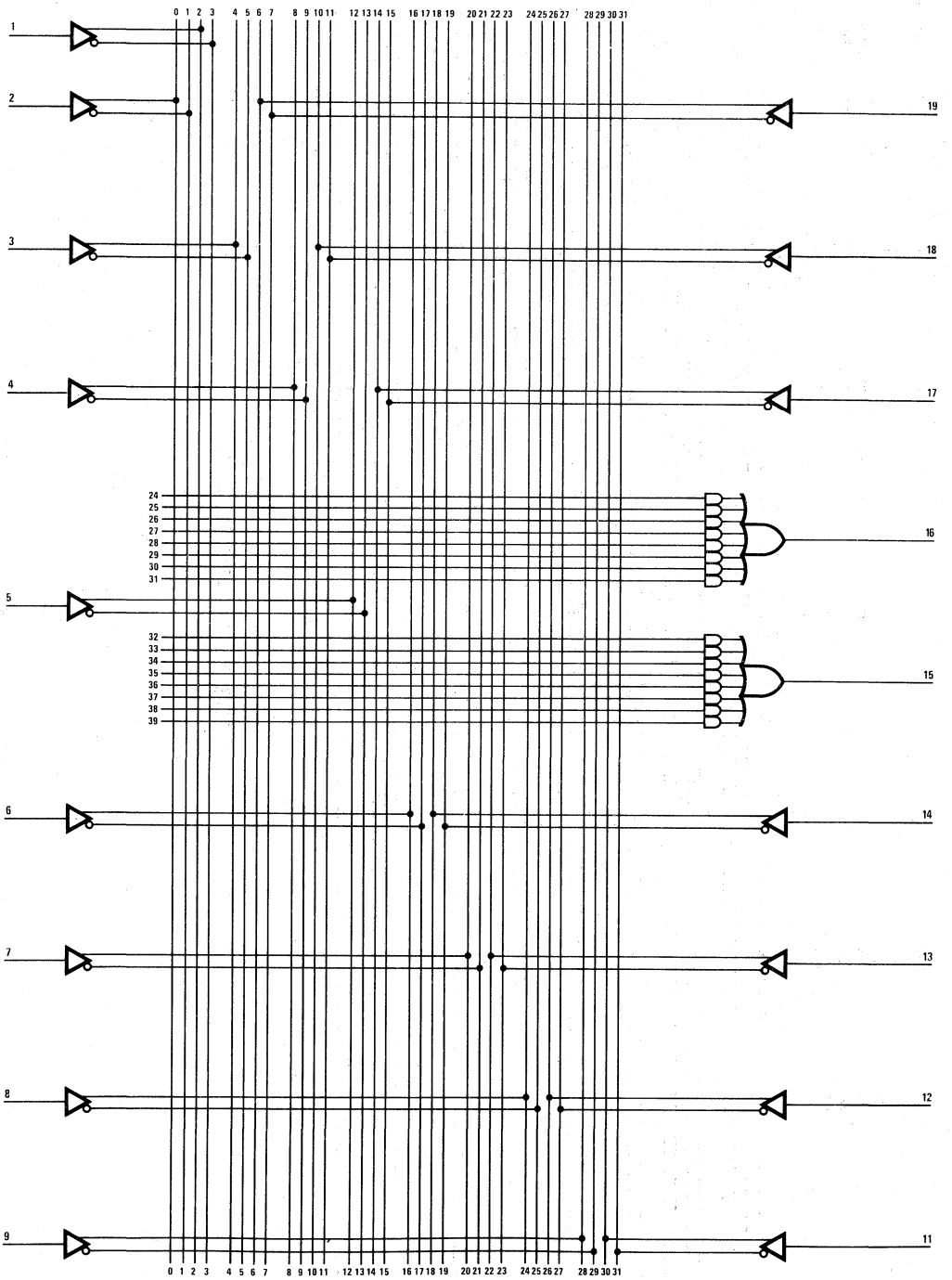
12H6


0 1 2 3 4 5 6 7 8 9 12 13 16 17 20 21 24 25 26 27 28 29 30 31
1
2
19
8
9
10
11
18
3
16
17
17
4
24
25
16
5
32
33
15
6
40
41
14
7
48
49
50
51
13
8
12
9
11

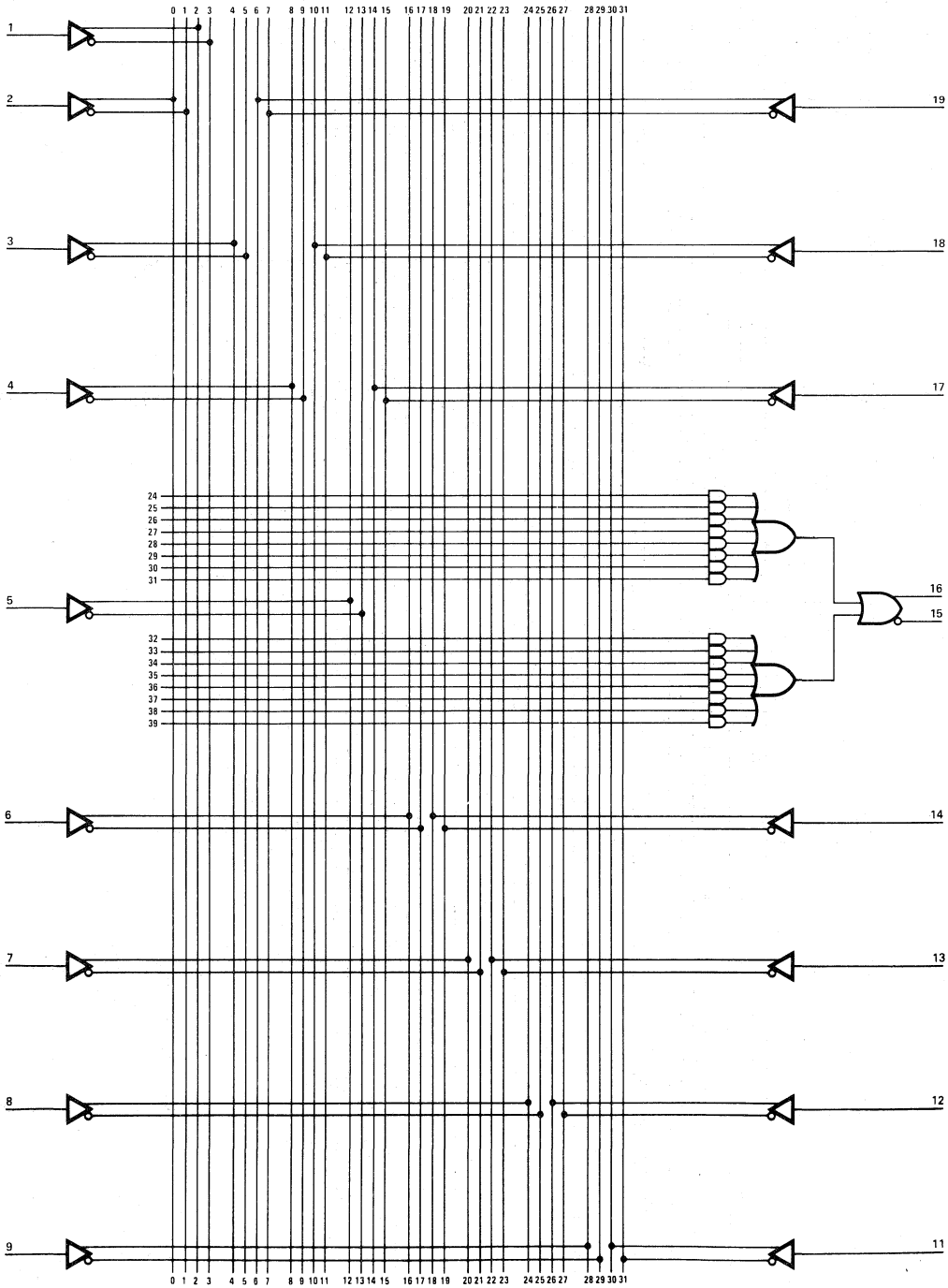
14H4


0 1 2 3 4 5 6 7 8 9 10 11 12 13 16 17 20 21 22 23 24 25 26 27 28 29 30 31
1
2
3
4
5
6
7
8
9
19
18
17
16
15
14
13
12
11
16 17 18 19
24 25 26 27
32 33 34 35
40 41 42 43

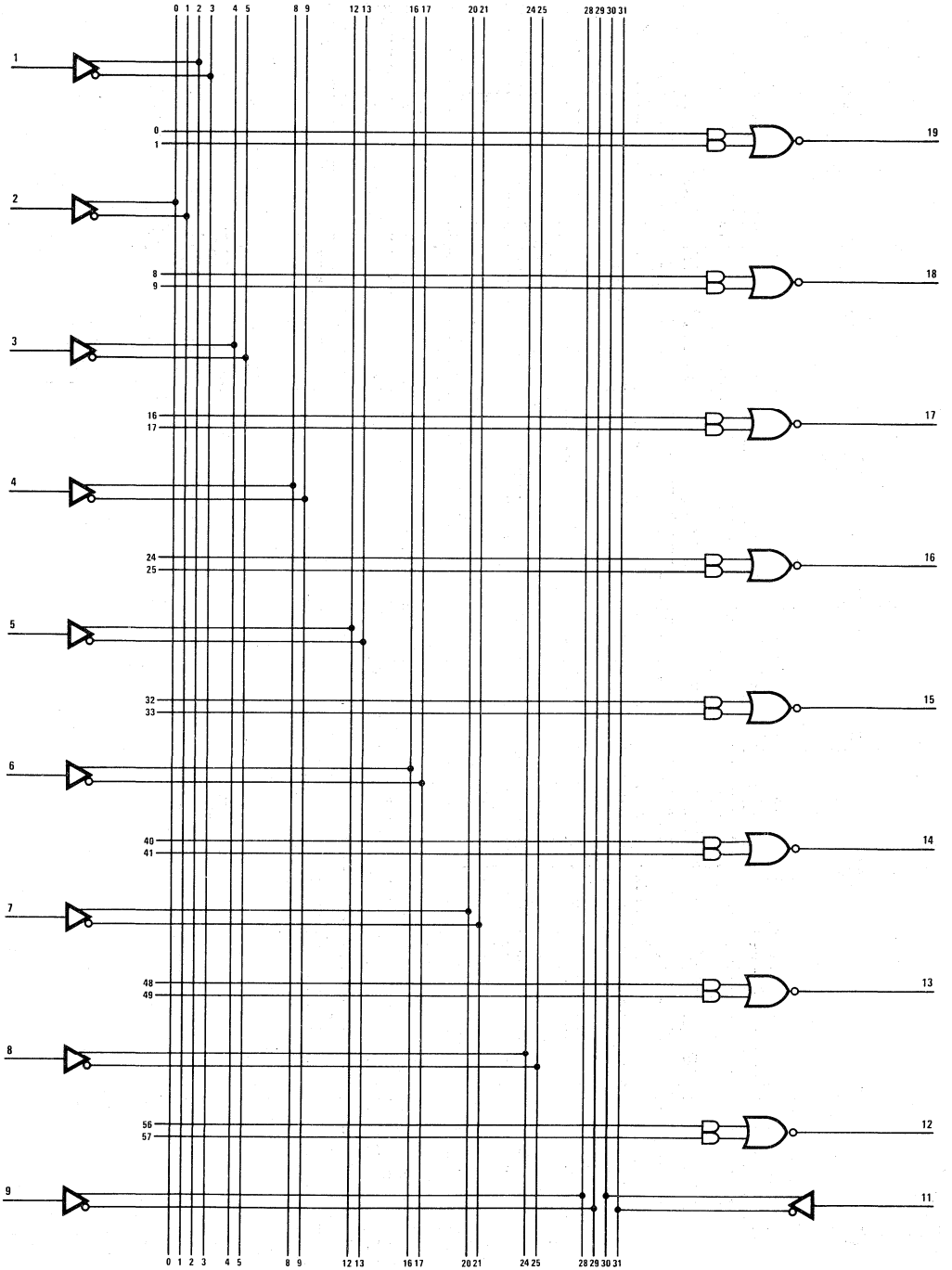
16H2


0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
1
2
3
4
5
6
7
8
9
19
18
17
16
15
14
13
12
11
24 25 26 27 28 29 30 31
32 33 34 35 36 37 38 39

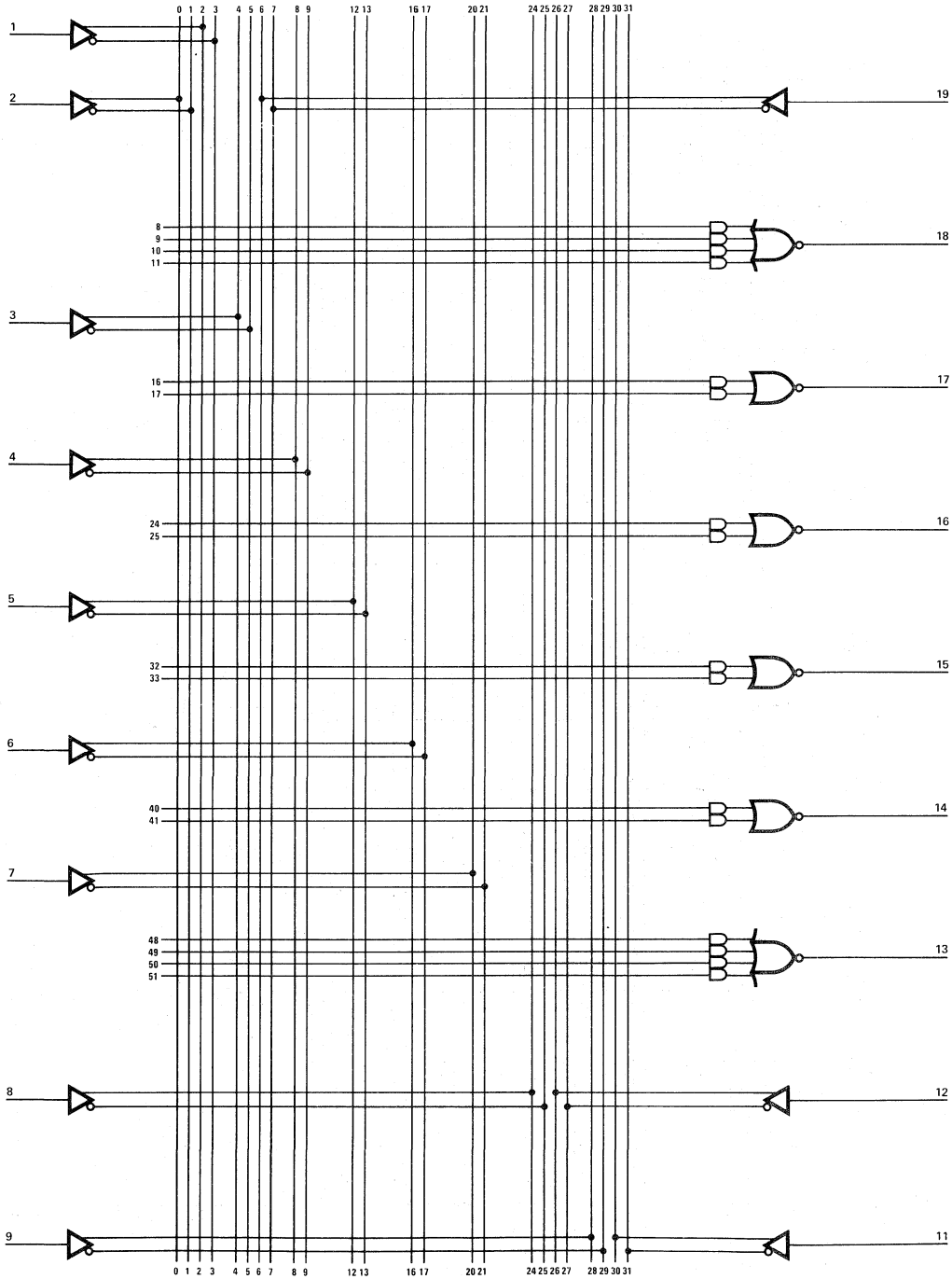
16C1


0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
1
2
3
4
5
6
7
8
9
19
18
17
16
15
14
13
12
11
24 25 26 27 28 29 30 31
32 33 34 35 36 37 38 39

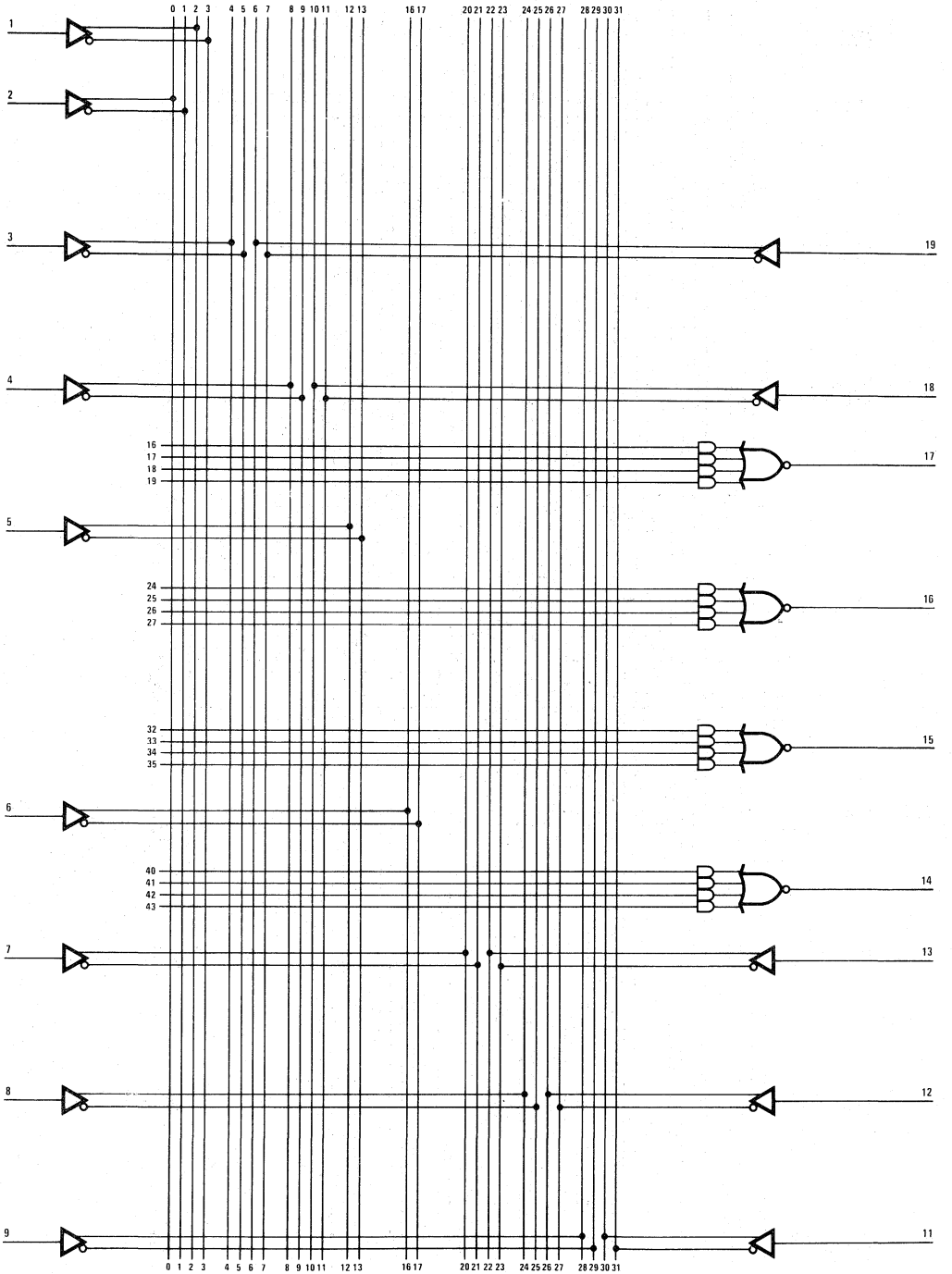
10L8


0 1 2 3 4 5 8 9 12 13 16 17 20 21 24 25 28 29 30 31
1
2
3
4
5
6
7
8
9
0
1
8
9
16
17
24
25
32
33
40
41
48
49
56
57
19
18
17
16
15
14
13
12
11

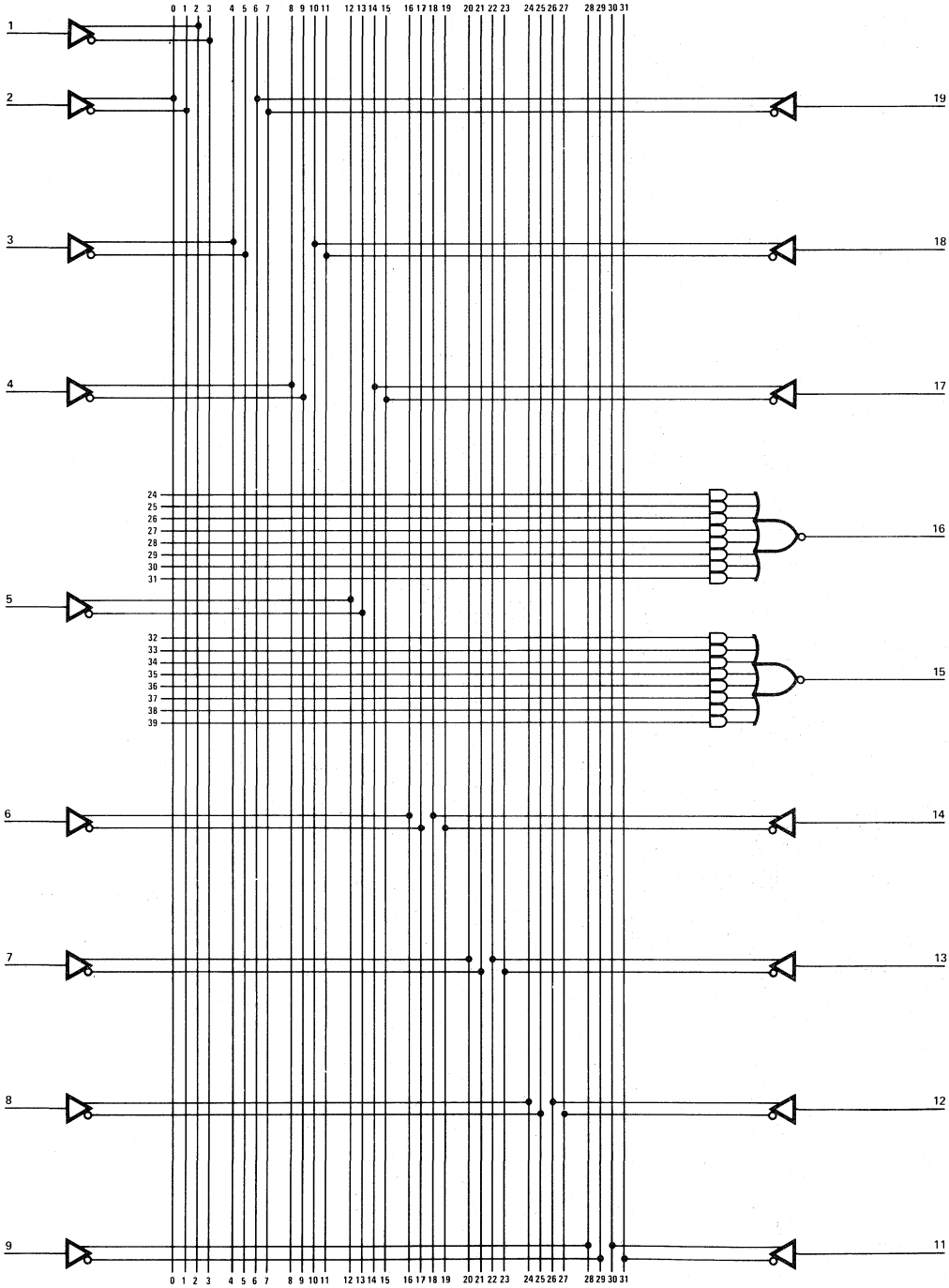
12L6


0 1 2 3 4 5 6 7 8 9 12 13 16 17 20 21 24 25 26 27 28 29 30 31
1
2
19
8
9
10
11
18
3
16
17
17
4
24
25
16
5
32
33
15
6
40
41
14
7
48
49
50
51
13
8
12
9
11

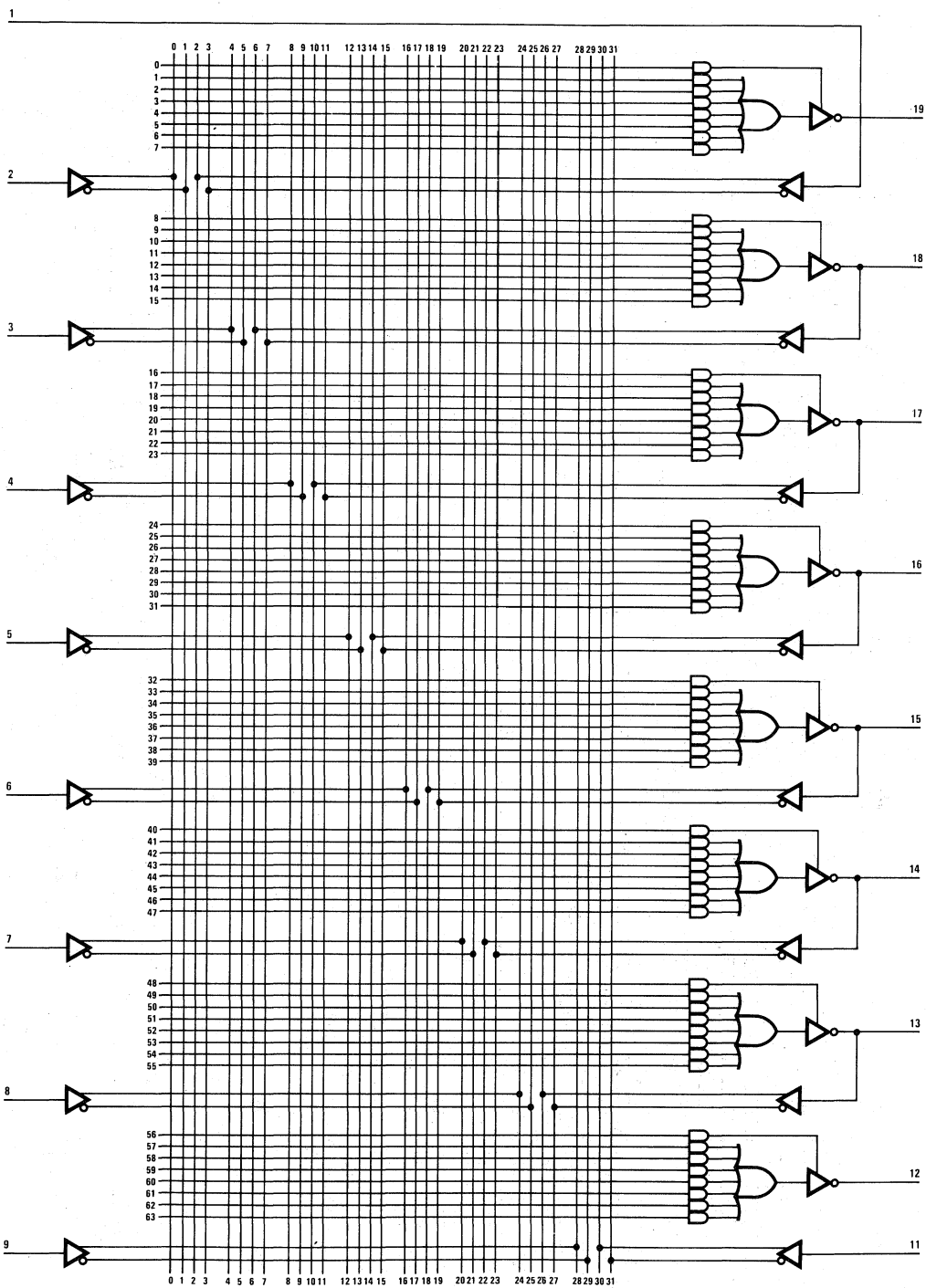
14L4


0 1 2 3 4 5 6 7 8 9 10 11 12 13 16 17 20 21 22 23 24 25 26 27 28 29 30 31
1
2
3
4
5
6
7
8
9
19
18
17
16
15
14
13
12
11
16 17 18 19
24 25 26 27
32 33 34 35
40 41 42 43

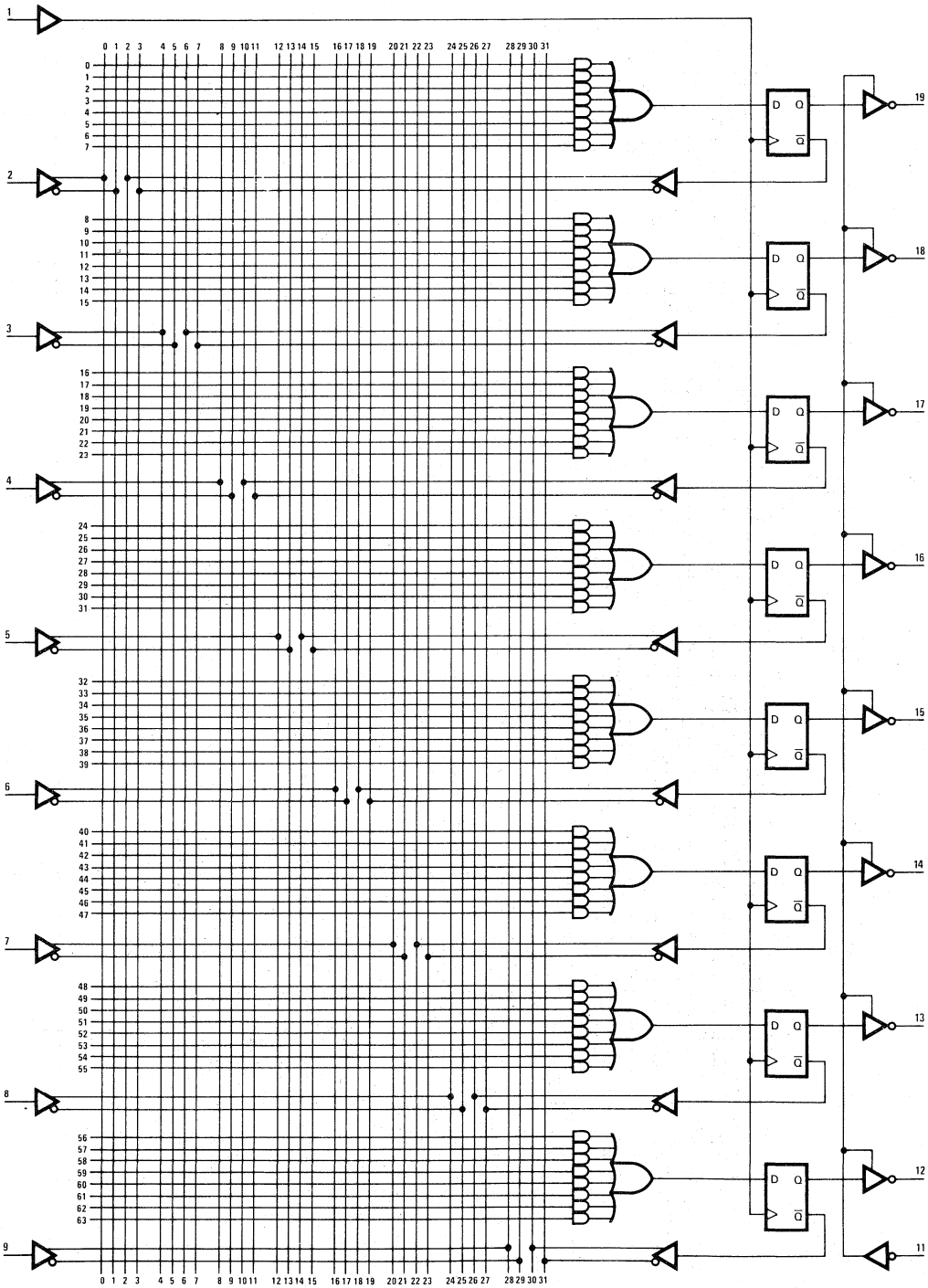
16L2


0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
1
2
3
4
5
6
7
8
9
19
18
17
16
15
14
13
12
11
24 25 26 27 28 29 30 31
32 33 34 35 36 37 38 39

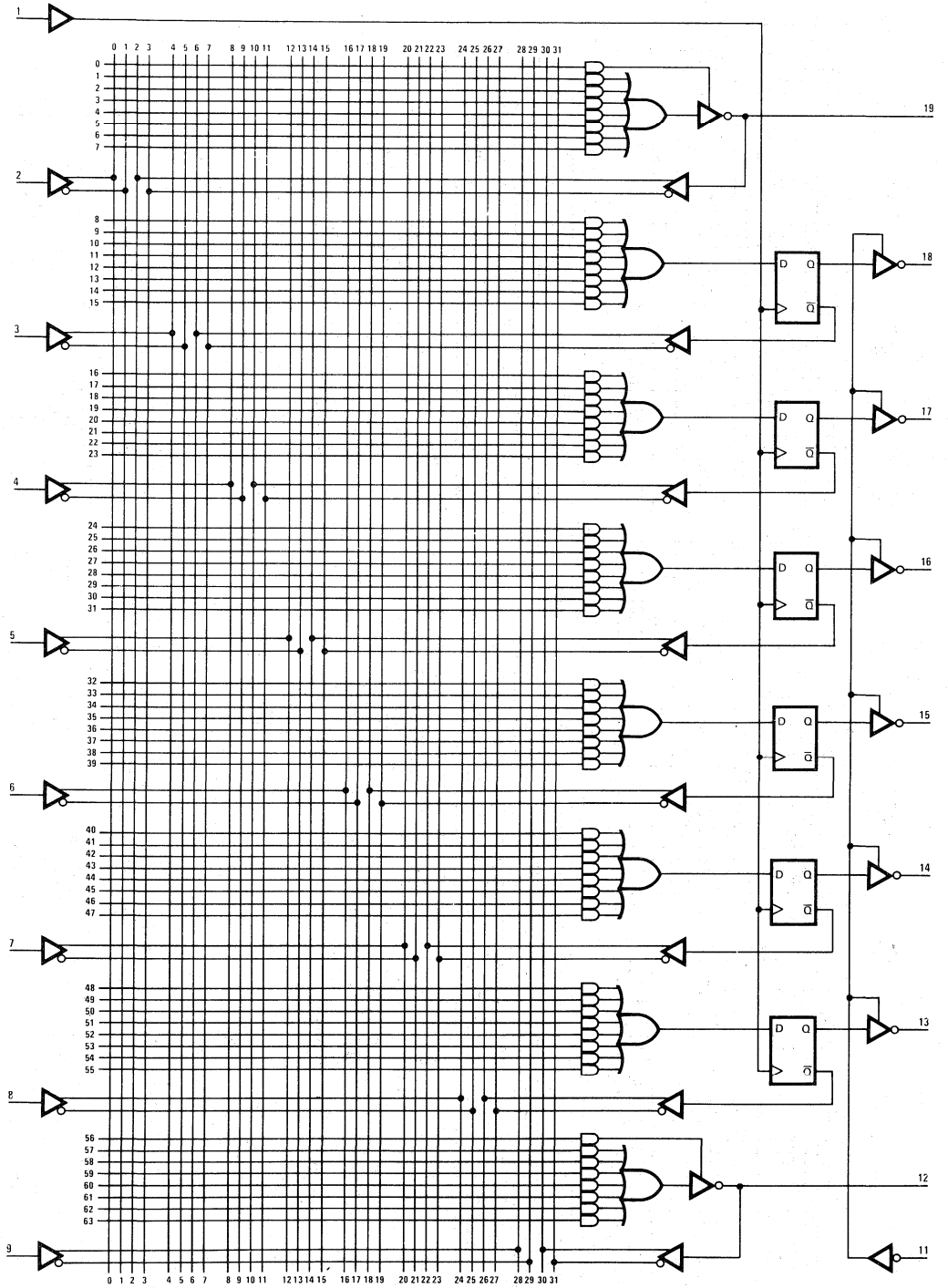
16L8


1
2
3
4
5
6
7
8
9
19
18
17
16
15
14
13
12
11
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
0 1 2 3 4 5 6 7
8 9 10 11 12 13 14 15
16 17 18 19 20 21 22 23
24 25 26 27 28 29 30 31
32 33 34 35 36 37 38 39
40 41 42 43 44 45 46 47
48 49 50 51 52 53 54 55
56 57 58 59 60 61 62 63

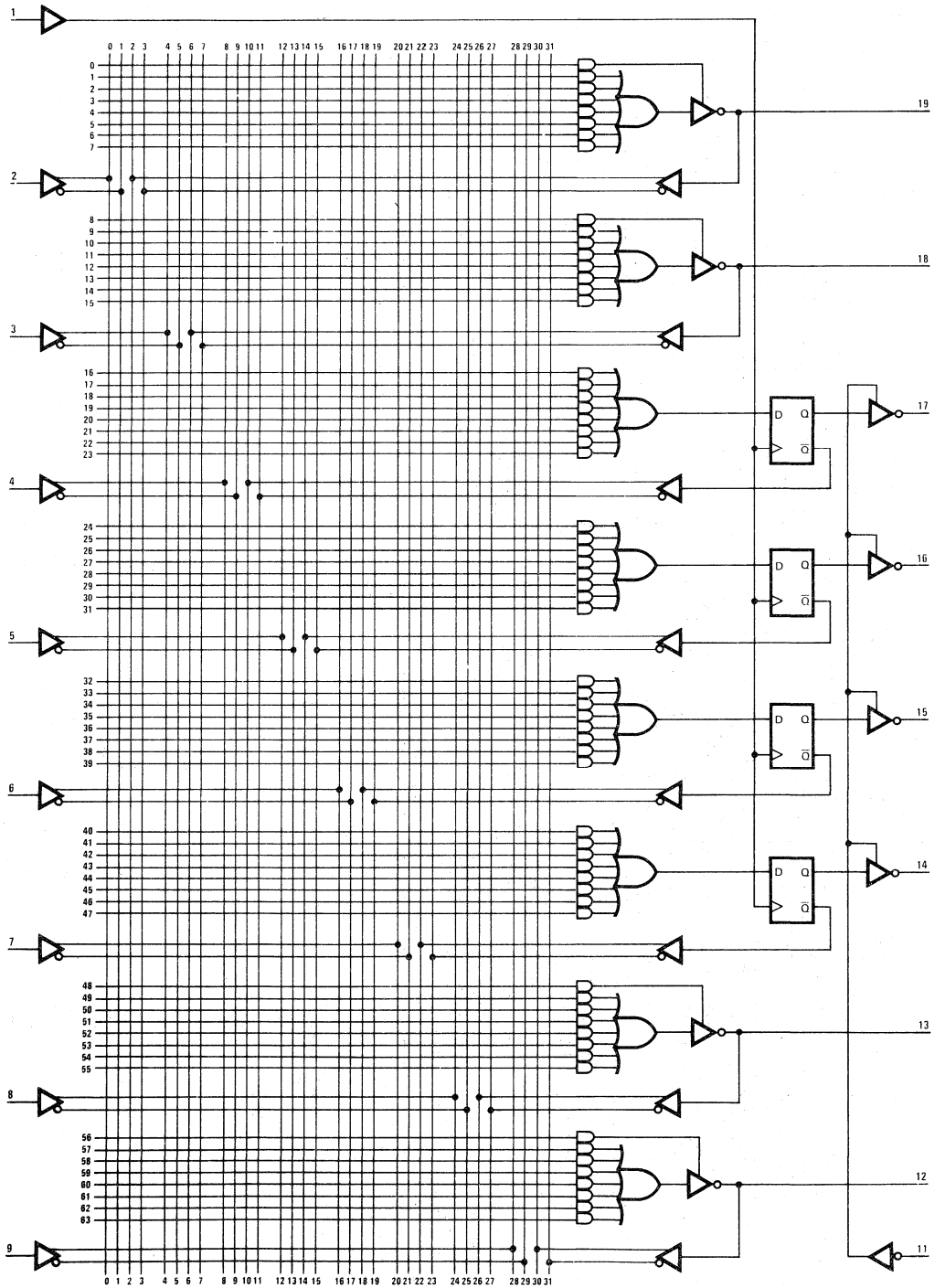
16R8


1
2
3
4
5
6
7
8
9
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
0 1 2 3 4 5 6 7
8 9 10 11 12 13 14 15
16 17 18 19 20 21 22 23
24 25 26 27 28 29 30 31
32 33 34 35 36 37 38 39
40 41 42 43 44 45 46 47
48 49 50 51 52 53 54 55
56 57 58 59 60 61 62 63
D Q
CI
19
18
17
16
15
14
13
12
11

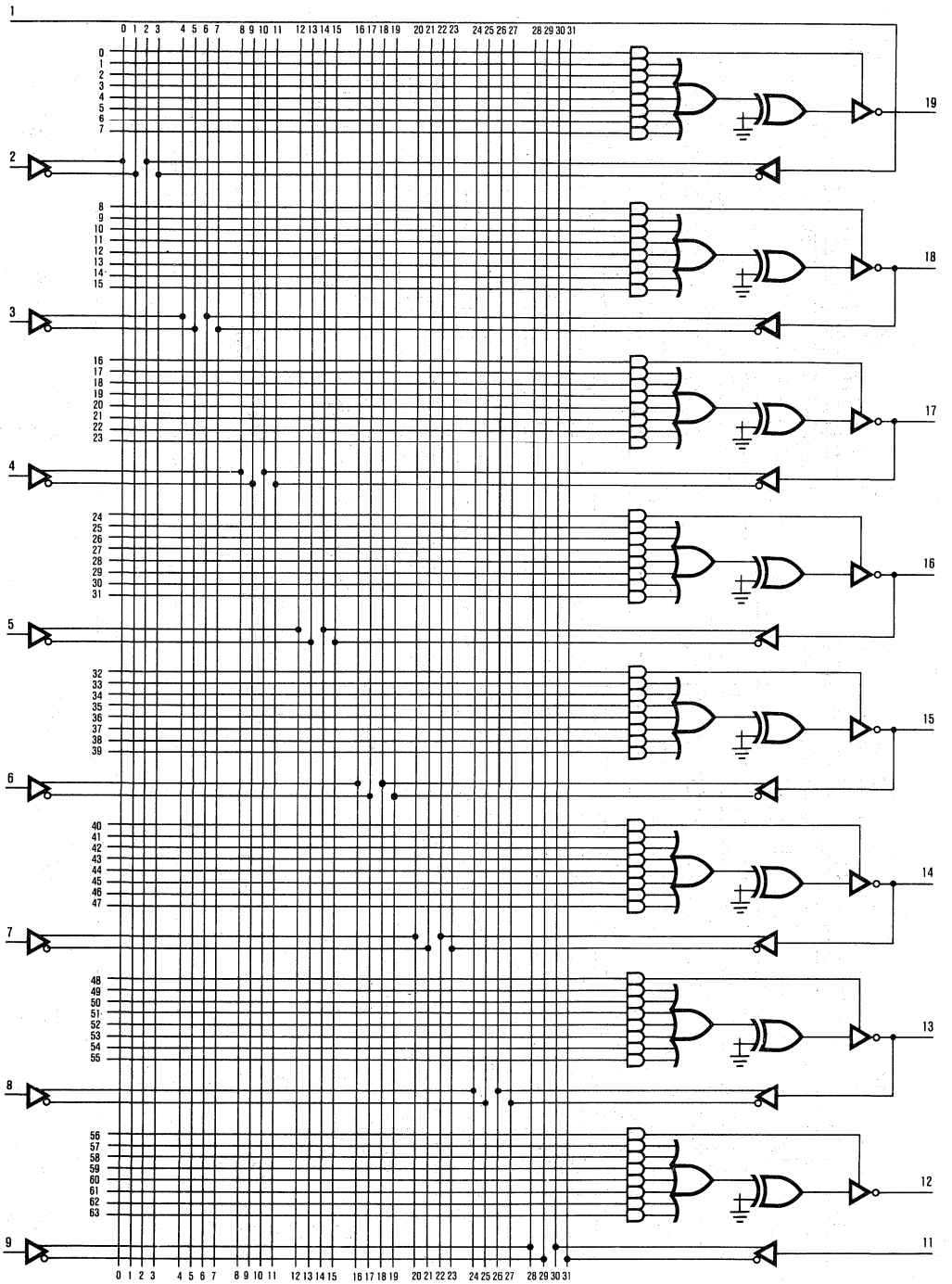
16R6


1
2
3
4
5
6
7
8
9
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
0 1 2 3 4 5 6 7
8 9 10 11 12 13 14 15
16 17 18 19 20 21 22 23
24 25 26 27 28 29 30 31
32 33 34 35 36 37 38 39
40 41 42 43 44 45 46 47
48 49 50 51 52 53 54 55
56 57 58 59 60 61 62 63
D Q
Q
19
18
17
16
15
14
13
12
11

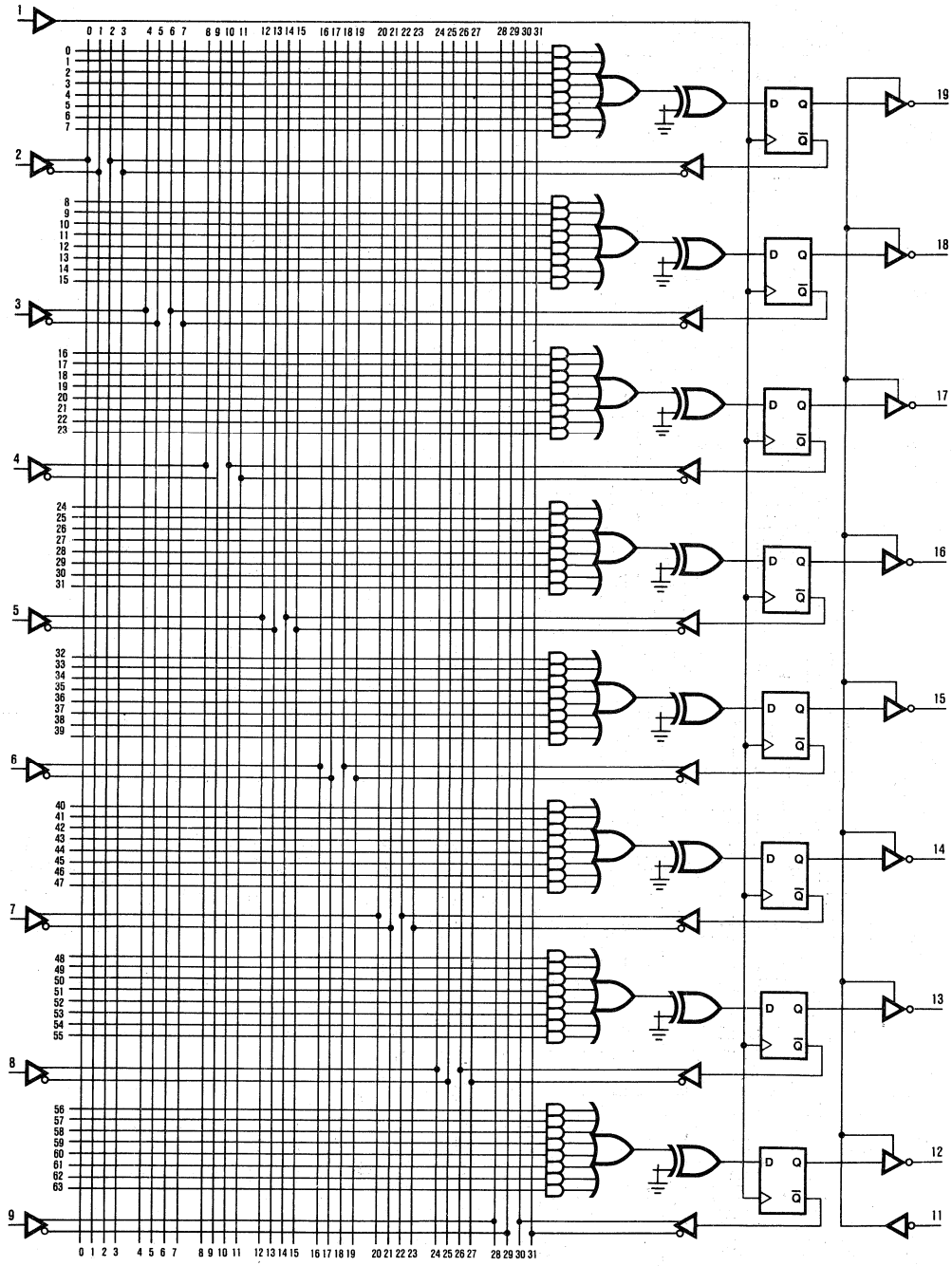
16R4


1
2
3
4
5
6
7
8
9
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
0 1 2 3 4 5 6 7
8 9 10 11 12 13 14 15
16 17 18 19 20 21 22 23
24 25 26 27 28 29 30 31
32 33 34 35 36 37 38 39
40 41 42 43 44 45 46 47
48 49 50 51 52 53 54 55
56 57 58 59 60 61 62 63
D Q
Q̄
19
18
17
16
15
14
13
12
11

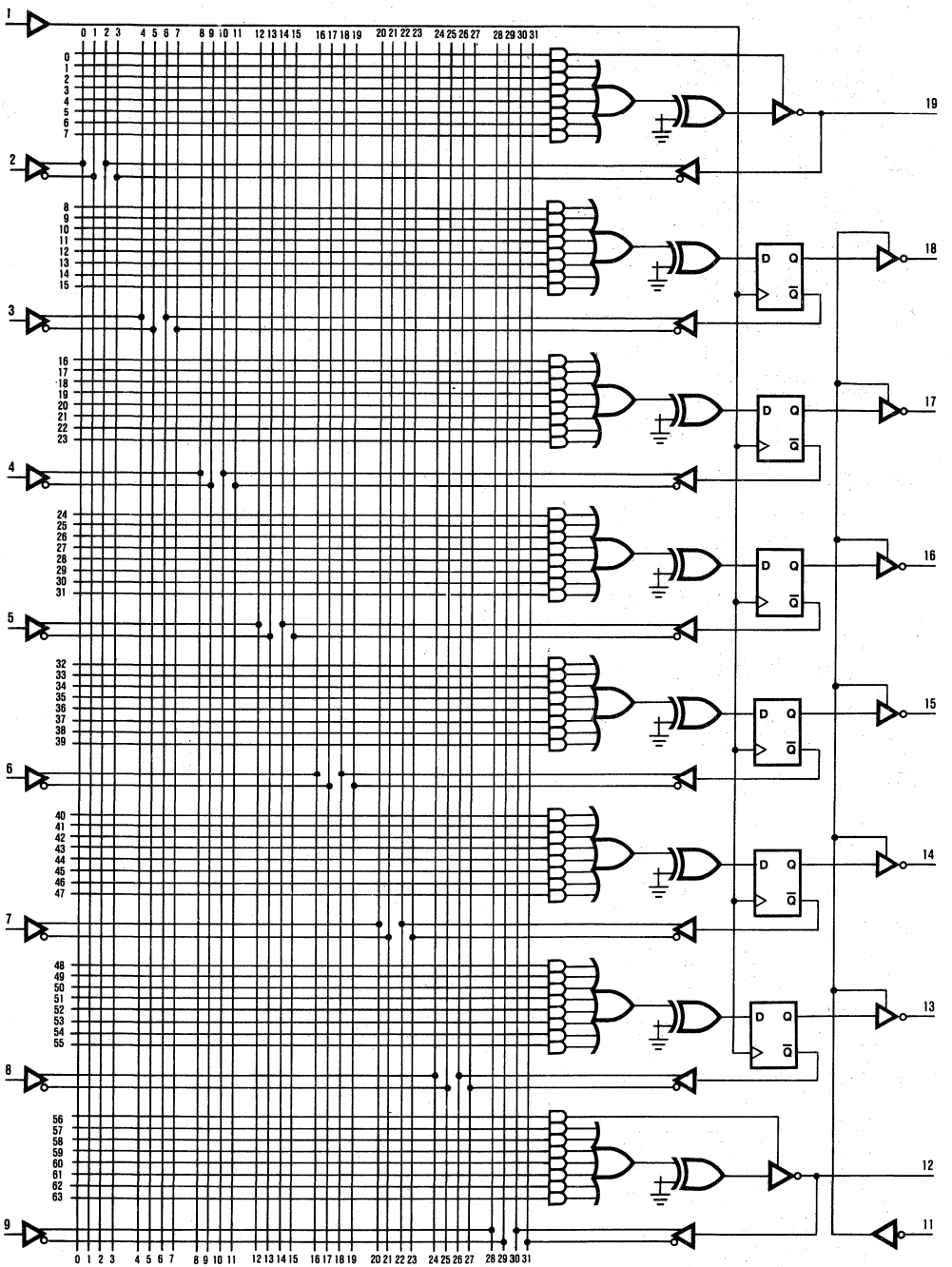
16P8


1
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
0 1 2 3 4 5 6 7
2
8 9 10 11 12 13 14 15
3
16 17 18 19 20 21 22 23
4
24 25 26 27 28 29 30 31
5
32 33 34 35 36 37 38 39
6
40 41 42 43 44 45 46 47
7
48 49 50 51 52 53 54 55
8
56 57 58 59 60 61 62 63
9
19
18
17
16
15
14
13
12
11

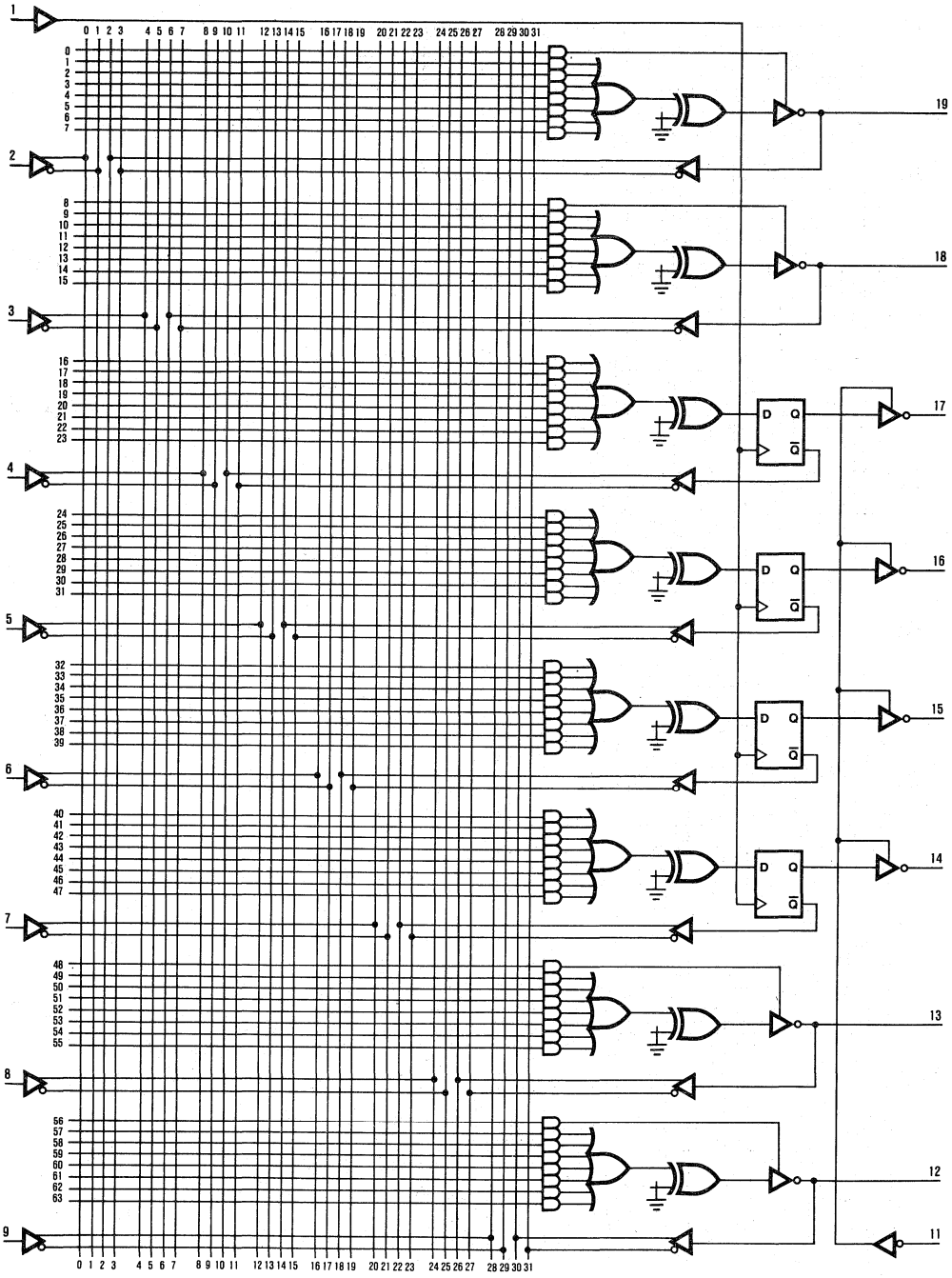
16RP8


1
2
3
4
5
6
7
8
9
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
0 1 2 3 4 5 6 7
8 9 10 11 12 13 14 15
16 17 18 19 20 21 22 23
24 25 26 27 28 29 30 31
32 33 34 35 36 37 38 39
40 41 42 43 44 45 46 47
48 49 50 51 52 53 54 55
56 57 58 59 60 61 62 63
D Q
Q
19
18
17
16
15
14
13
12
11

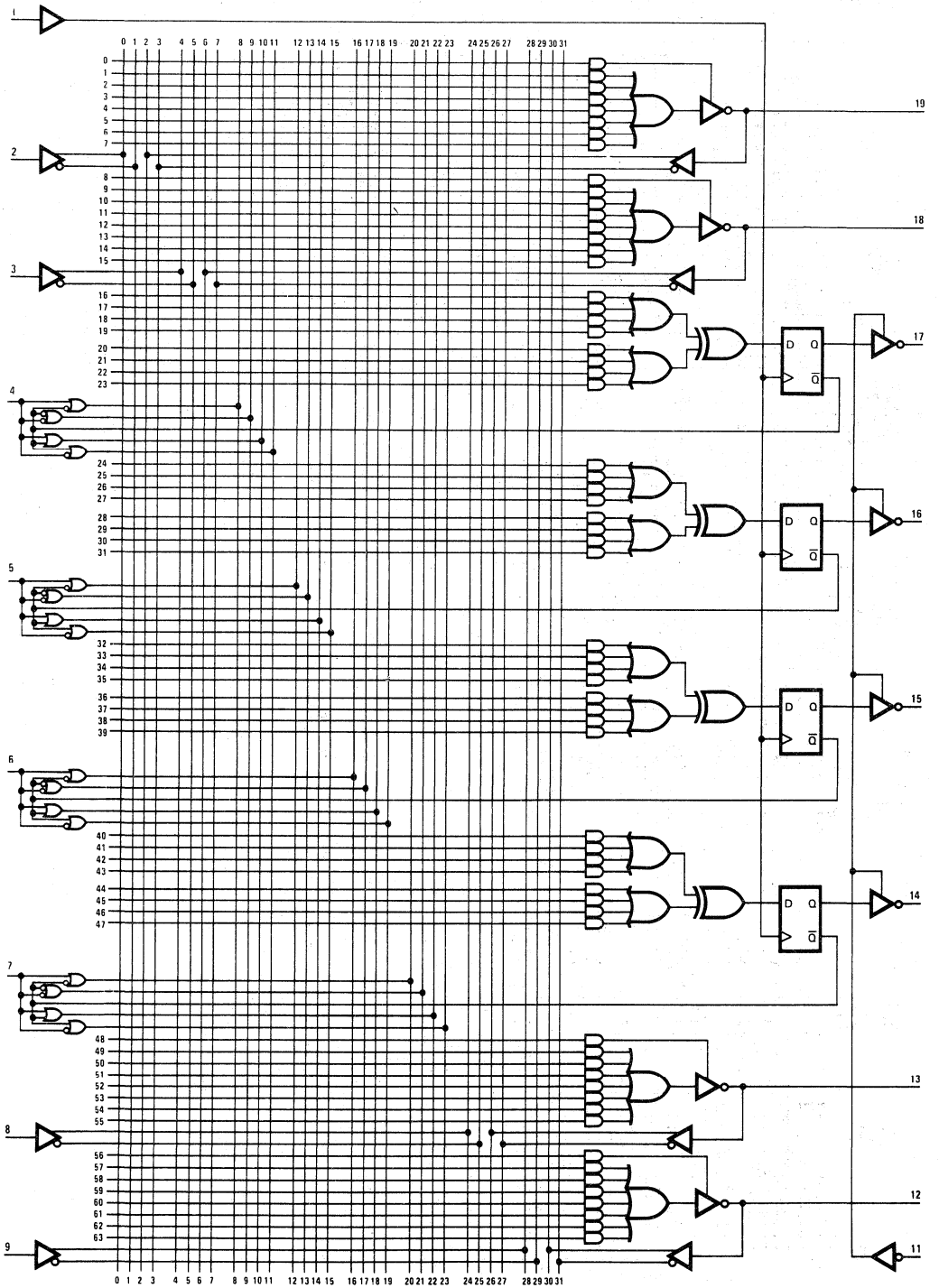
16RP6


1
2
3
4
5
6
7
8
9
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
0 1 2 3 4 5 6 7
8 9 10 11 12 13 14 15
16 17 18 19 20 21 22 23
24 25 26 27 28 29 30 31
32 33 34 35 36 37 38 39
40 41 42 43 44 45 46 47
48 49 50 51 52 53 54 55
56 57 58 59 60 61 62 63
D Q
Q
19
18
17
16
15
14
13
12
11

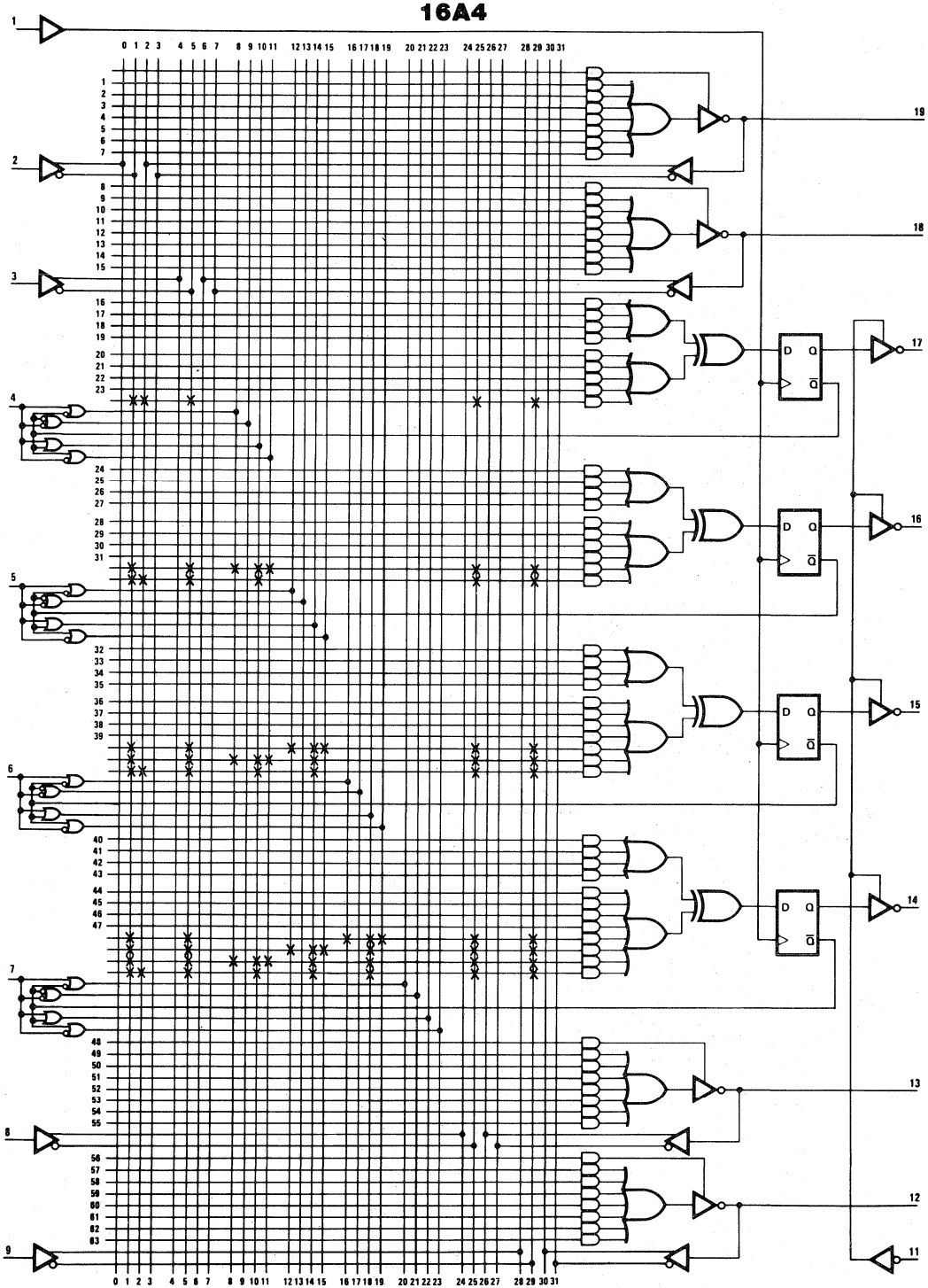
16RP4


1
2
3
4
5
6
7
8
9
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
0 1 2 3 4 5 6 7
8 9 10 11 12 13 14 15
16 17 18 19 20 21 22 23
24 25 26 27 28 29 30 31
32 33 34 35 36 37 38 39
40 41 42 43 44 45 46 47
48 49 50 51 52 53 54 55
56 57 58 59 60 61 62 63
D Q
Q
19
18
17
16
15
14
13
12
11

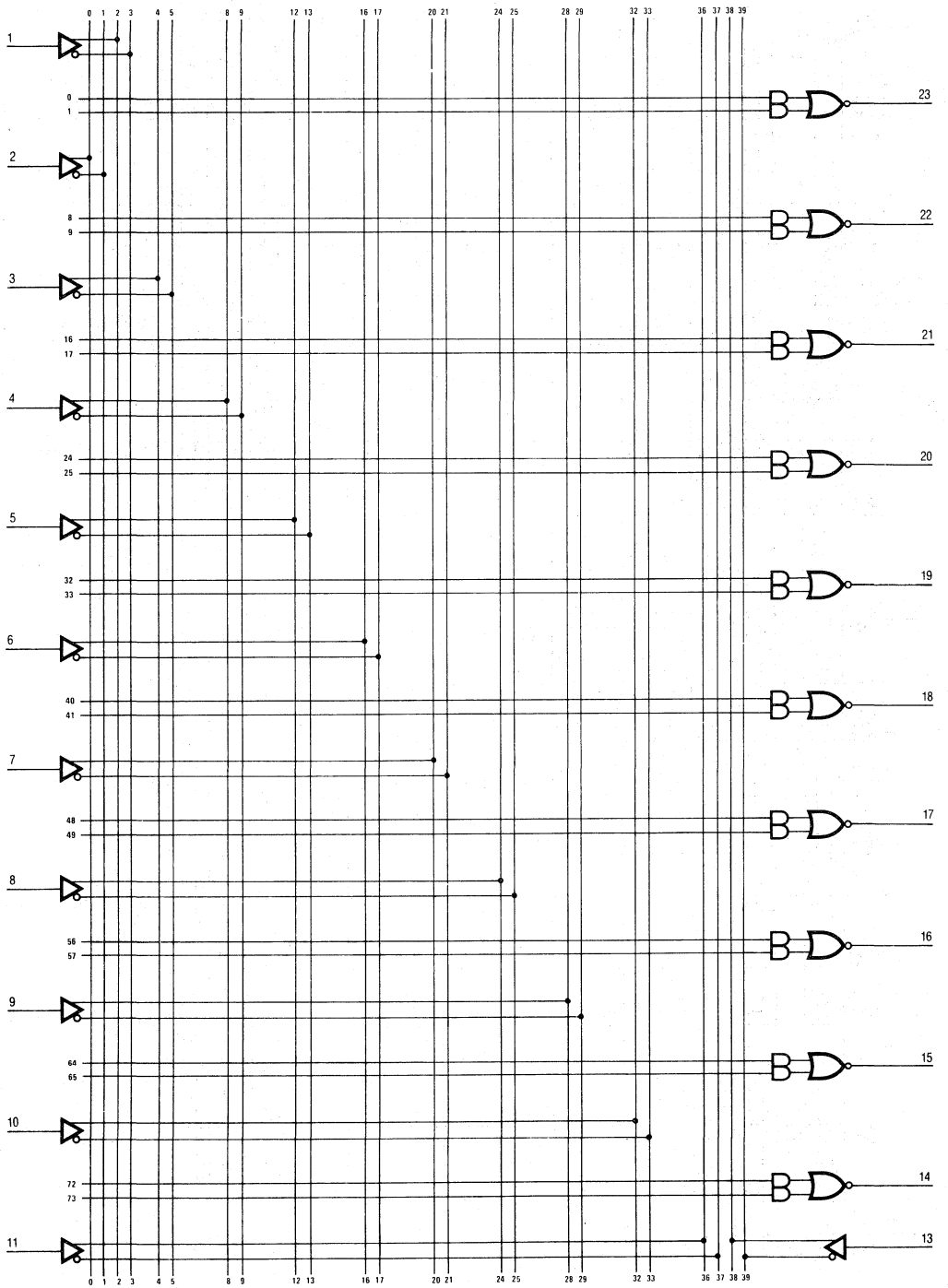
16X4


1
2
3
4
5
6
7
8
9
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
19
18
17
16
15
14
13
12
11
D Q
Q̄

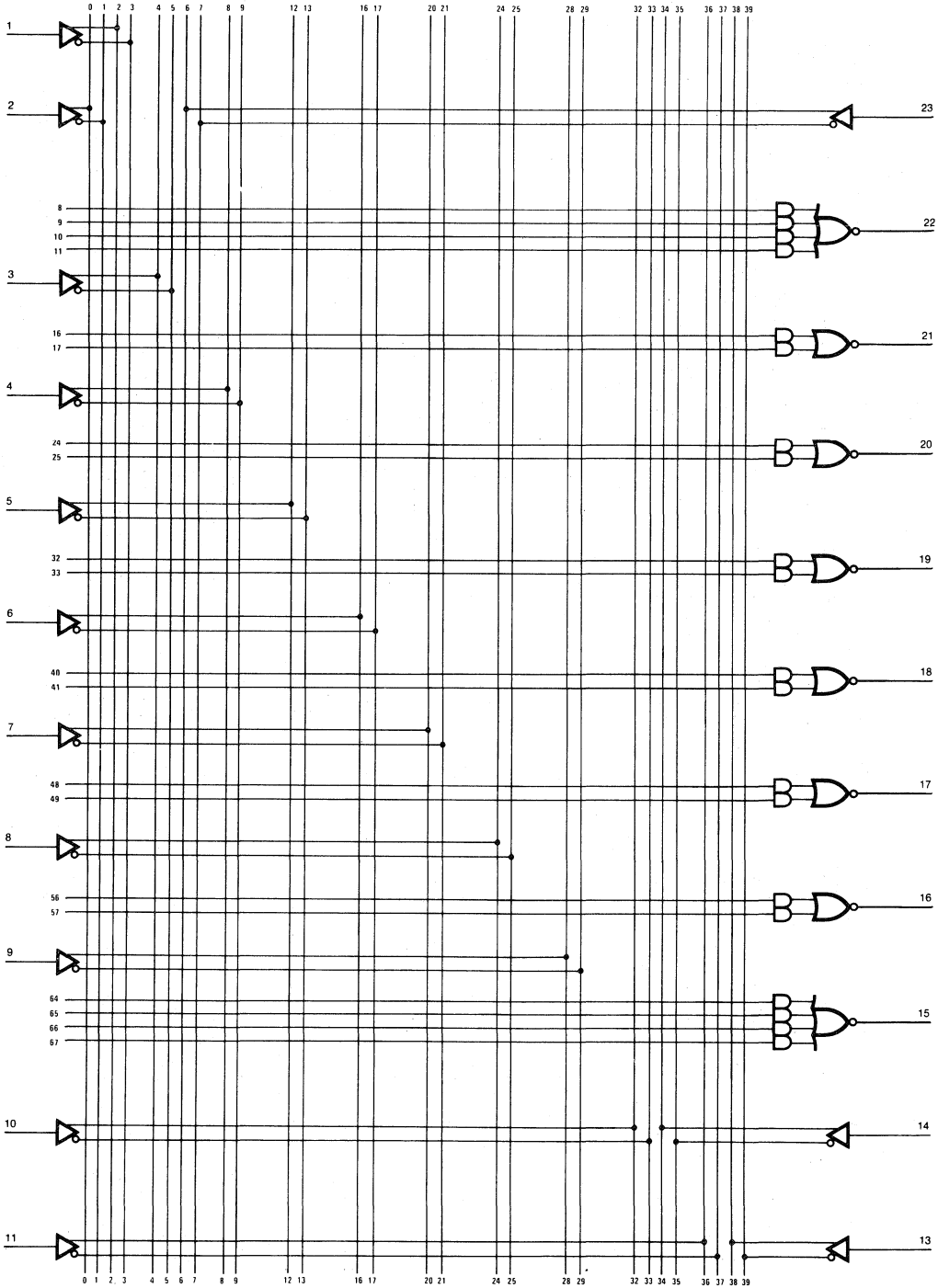
16A4


1
2
3
4
5
6
7
8
9
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63
D Q Q̄
19
18
17
16
15
14
13
12
11

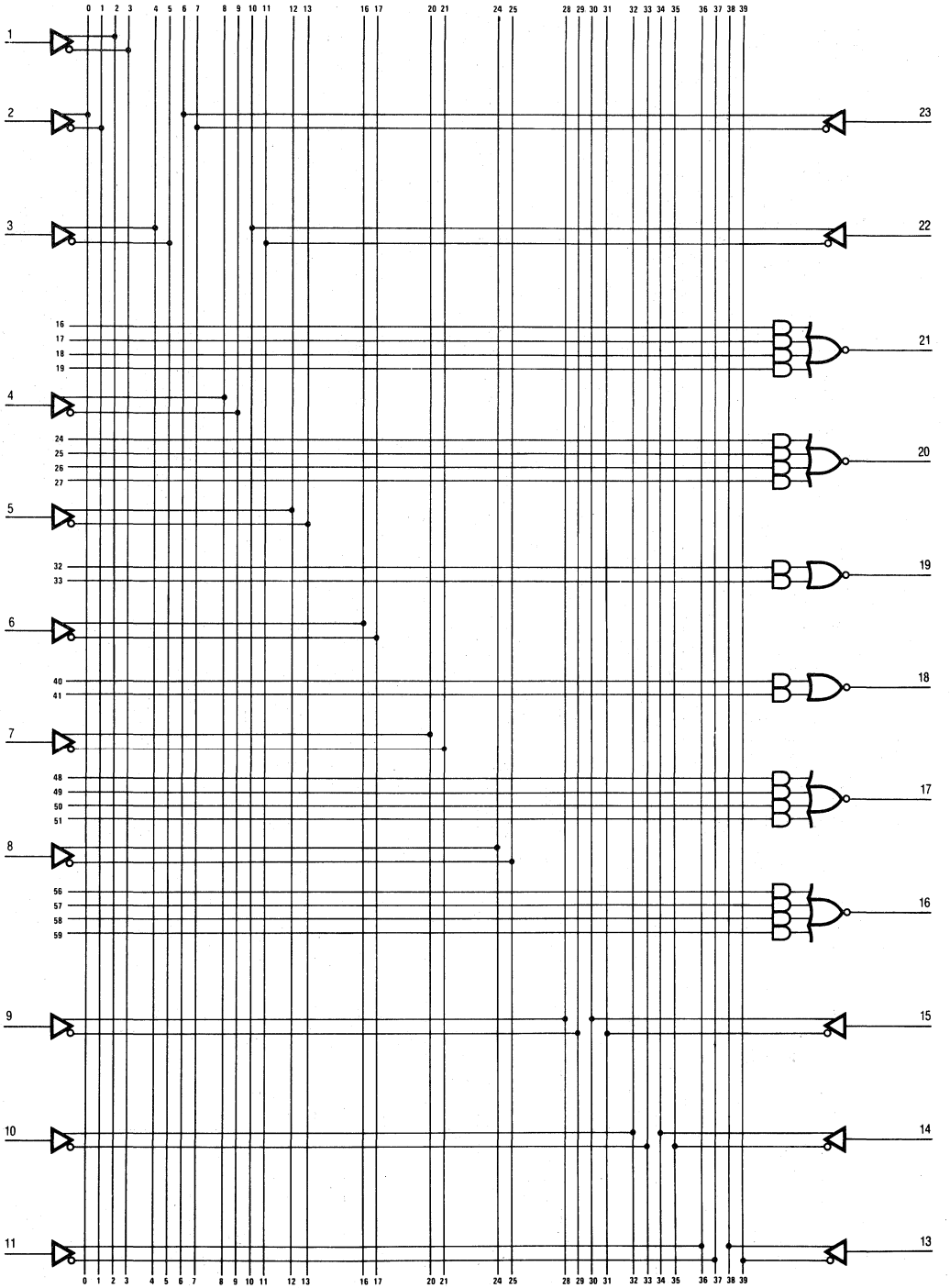
12L10


0 1 2 3 4 5 8 9 12 13 16 17 20 21 24 25 28 29 32 33 36 37 38 39
1
0
1
2
8
9
3
16
17
4
24
25
5
32
33
6
40
41
7
48
49
8
56
57
9
64
65
10
72
73
11
23
22
21
20
19
18
17
16
15
14
13

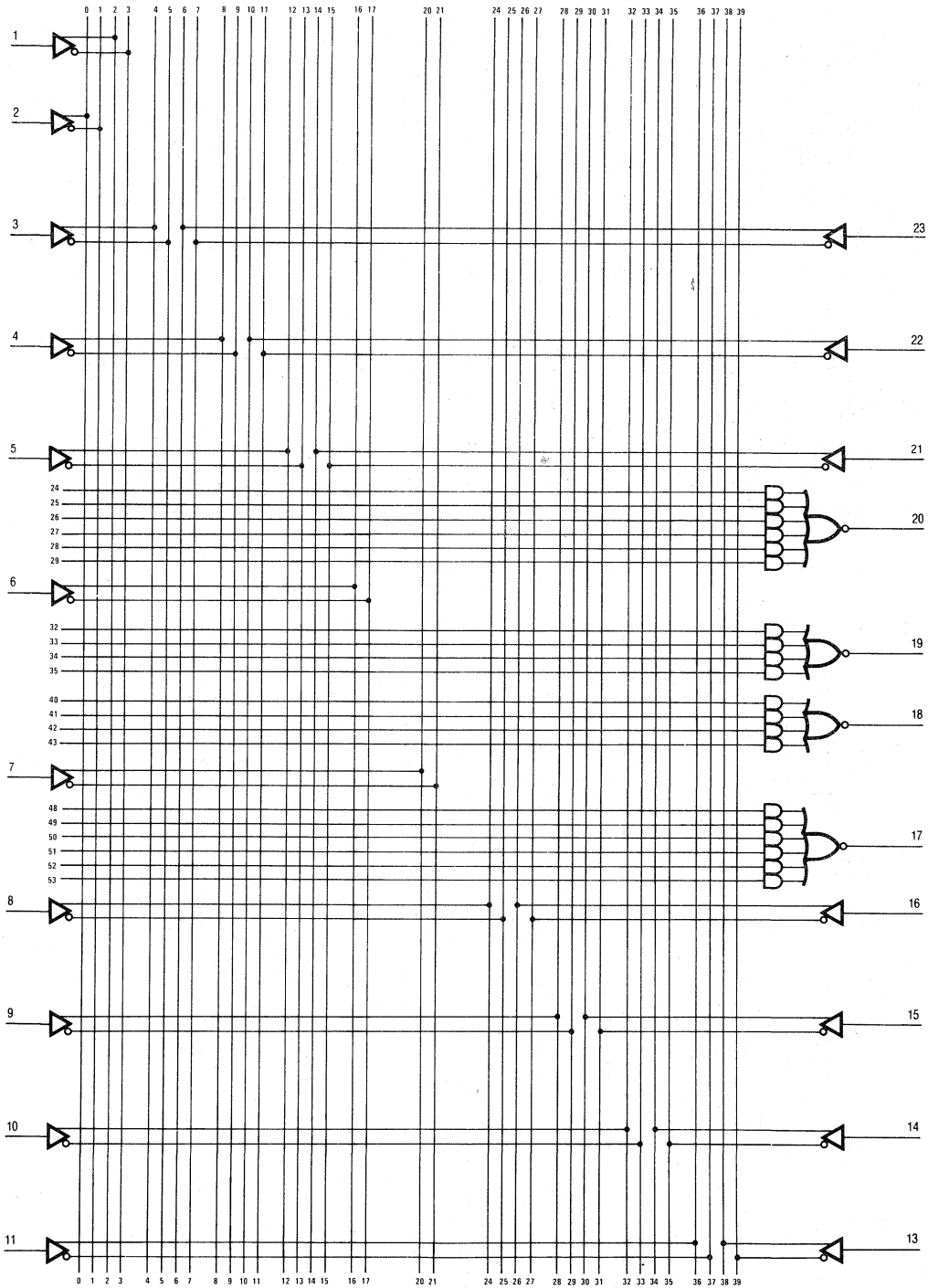
14L8


0 1 2 3
4 5 6 7
8 9
12 13
16 17
20 21
24 25
28 29
32 33 34 35
36 37 38 39
1
2
3
4
5
6
7
8
9
10
11
8
9
10
11
16
17
24
25
32
33
40
41
48
49
56
57
64
65
66
67
23
22
21
20
19
18
17
16
15
14
13

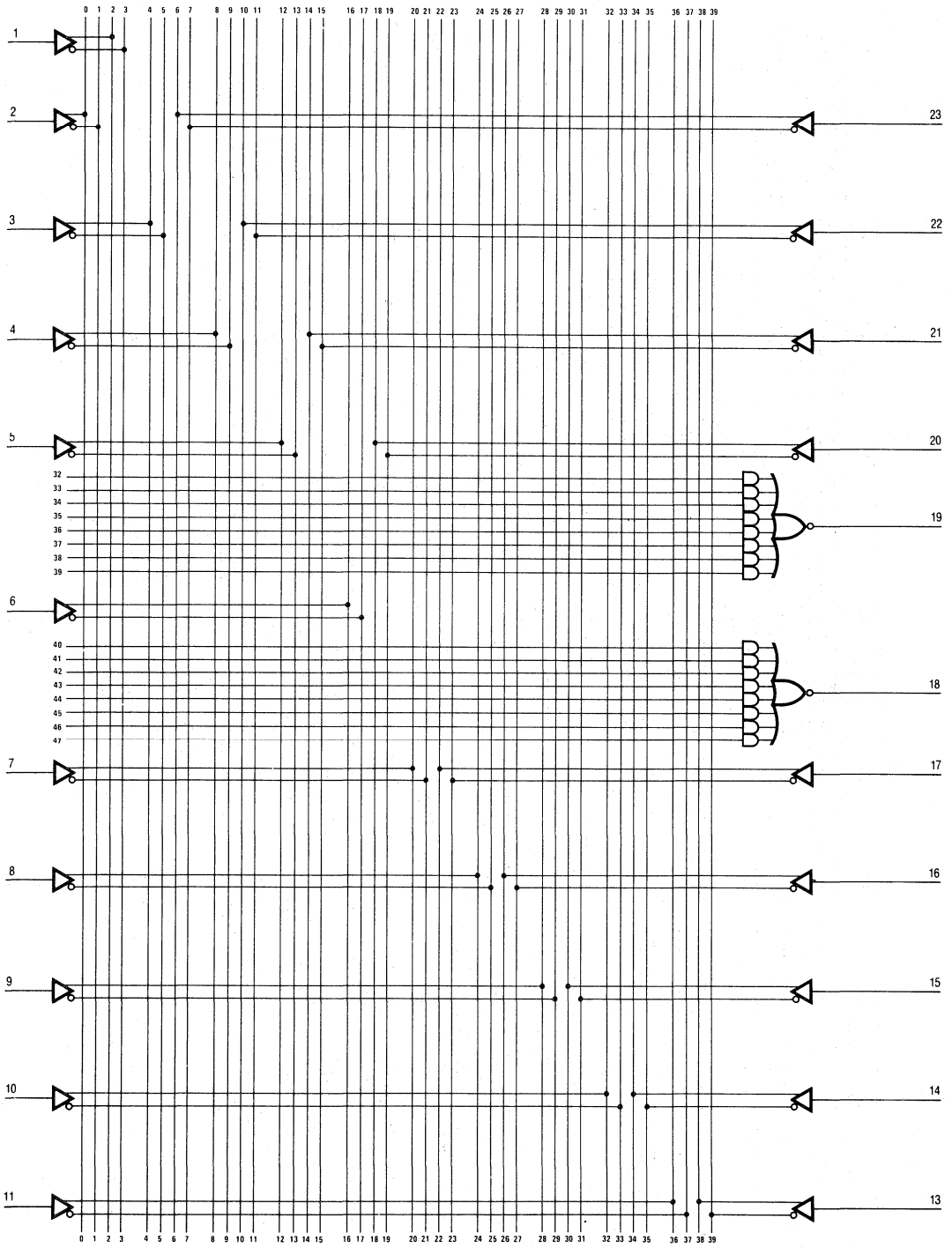
16L6


0 1 2 3 4 5 6 7 8 9 10 11 12 13 16 17 20 21 24 25 28 29 30 31 32 33 34 35 36 37 38 39
1
2
3
4
5
6
7
8
9
10
11
16 17 18 19
24 25 26 27
32 33
40 41
48 49 50 51
56 57 58 59
23
22
21
20
19
18
17
16
15
14
13

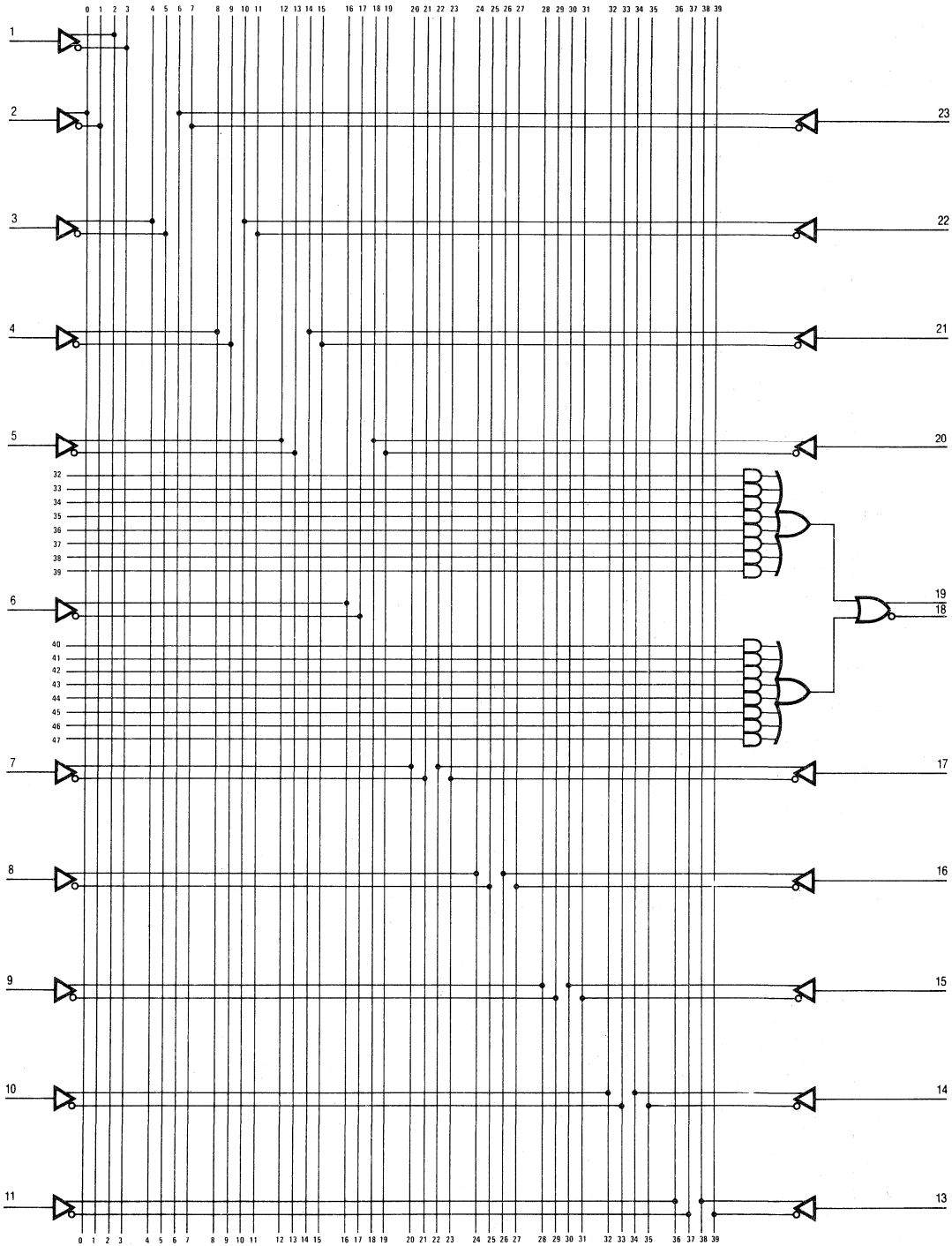
18L4


0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 20 21 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39
1
2
3
4
5
6
7
8
9
10
11
23
22
21
20
19
18
17
16
15
14
13
24 25 26 27 28 29
32 33 34 35
40 41 42 43
48 49 50 51 52 53

20L2

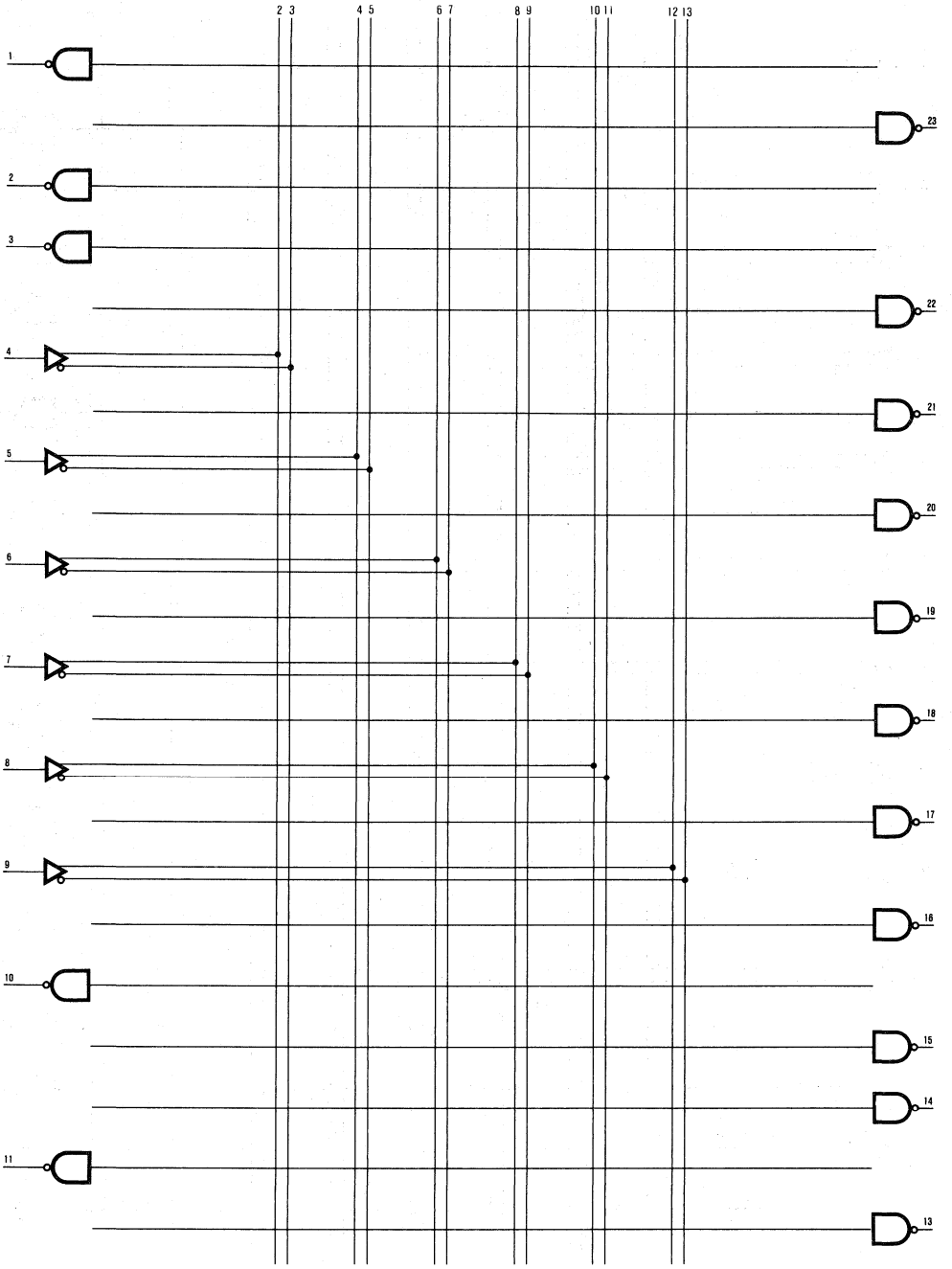

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39
1
2
3
4
5
6
7
8
9
10
11
23
22
21
20
19
18
17
16
15
14
13
32 33 34 35 36 37 38 39
40 41 42 43 44 45 46 47

20C1


0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39
1
2
3
4
5
6
7
8
9
10
11
23
22
21
20
19
18
17
16
15
14
13
32 33 34 35 36 37 38 39
40 41 42 43 44 45 46 47

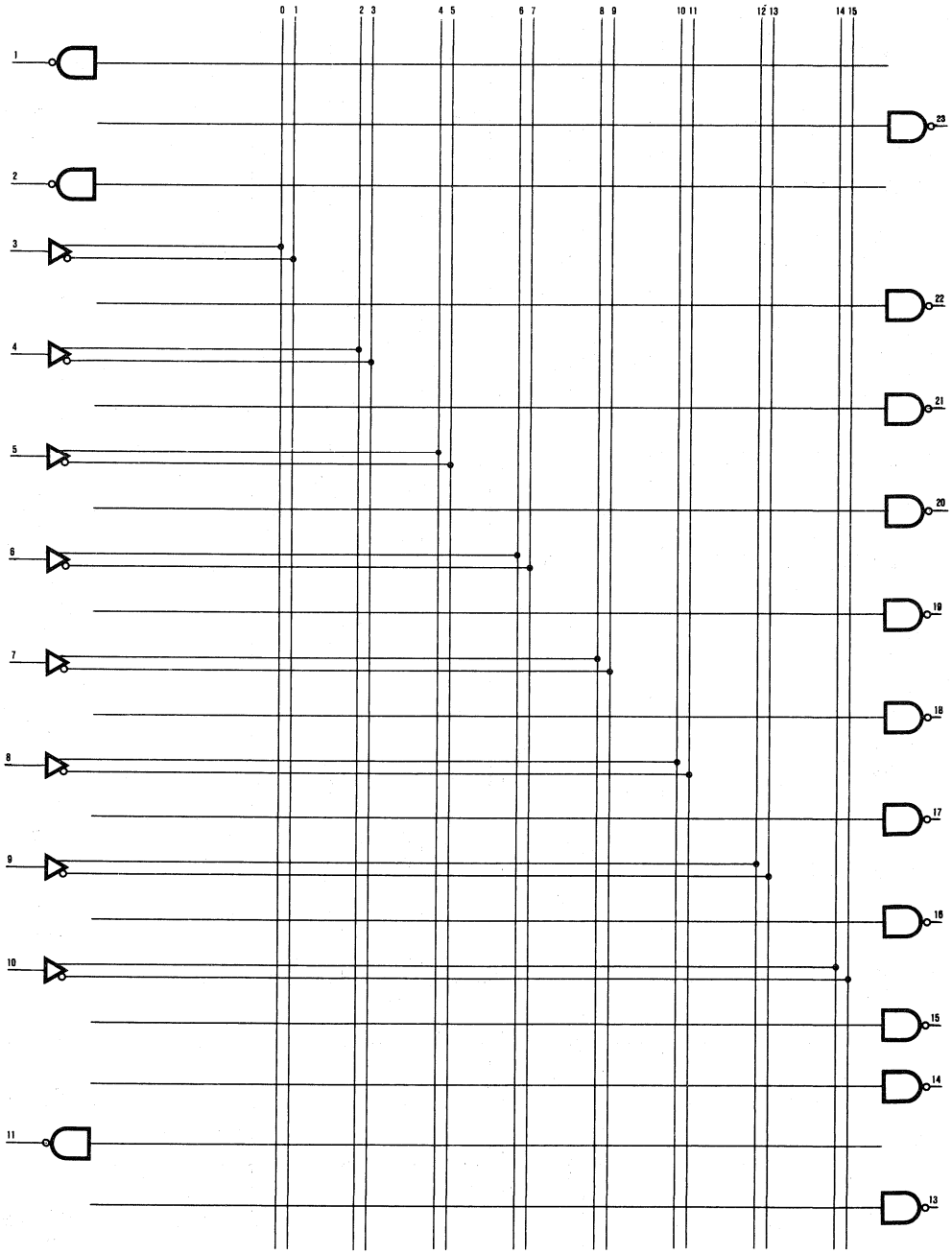
Logic Diagram

6L16A

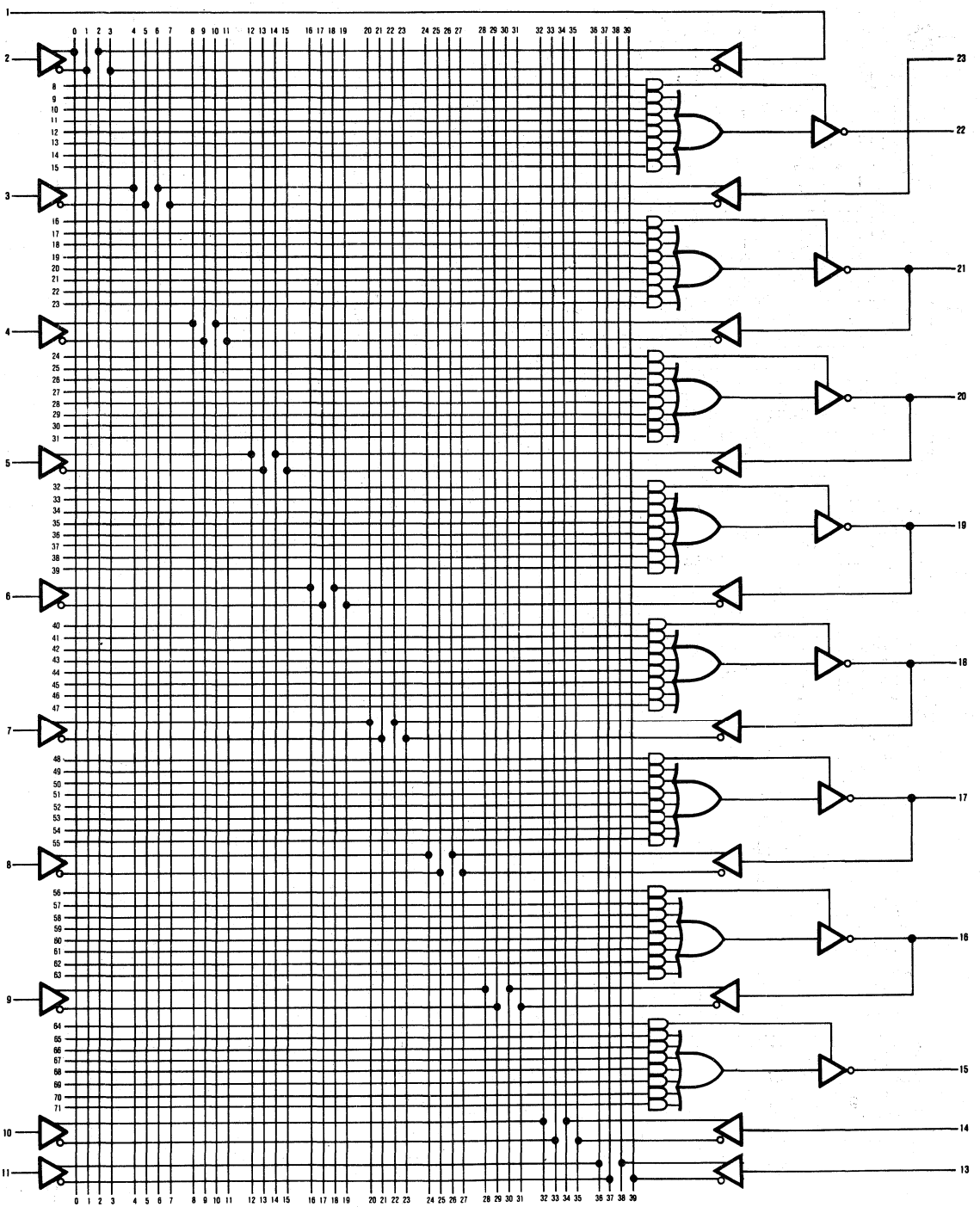


Logic Diagram

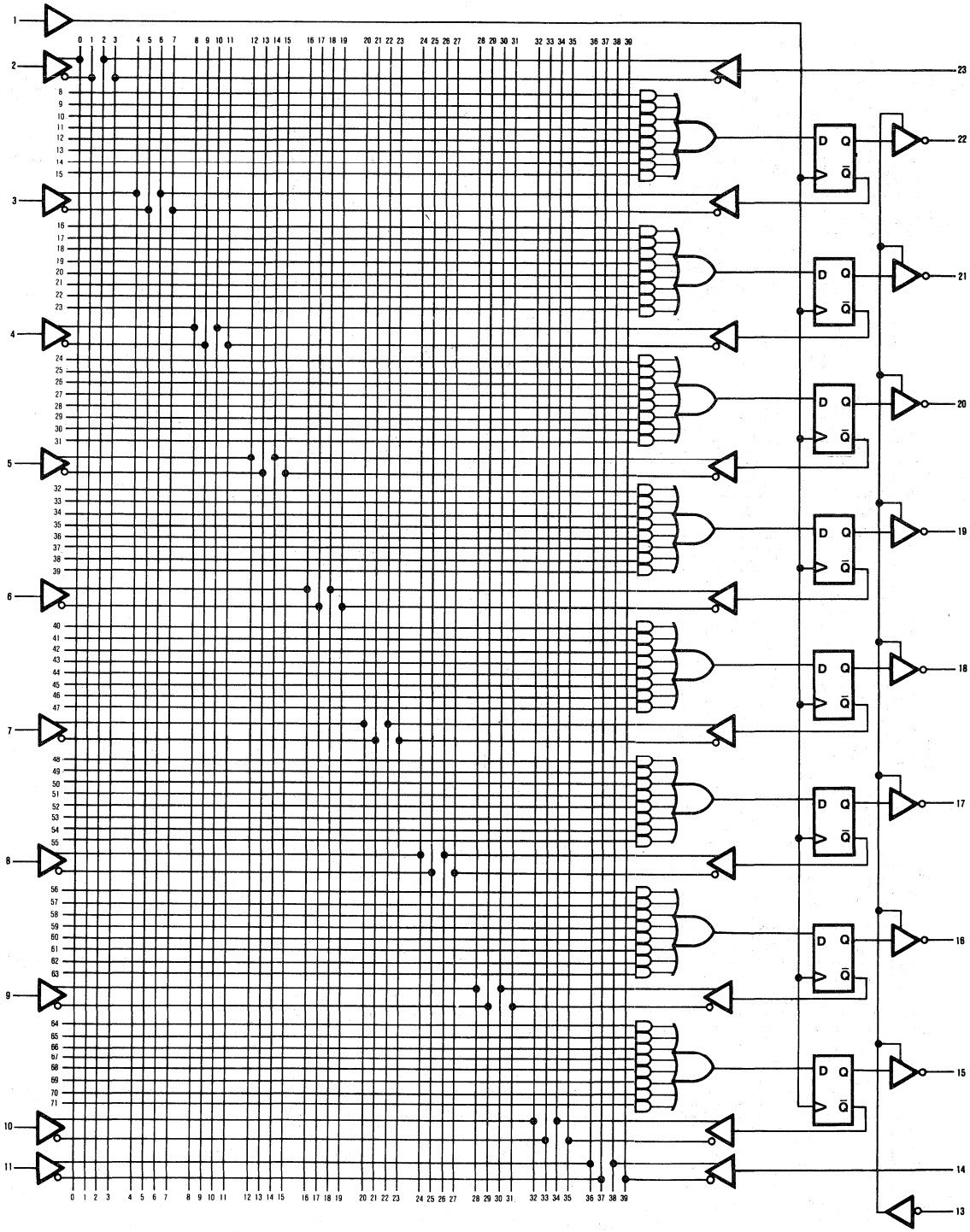
8L14A



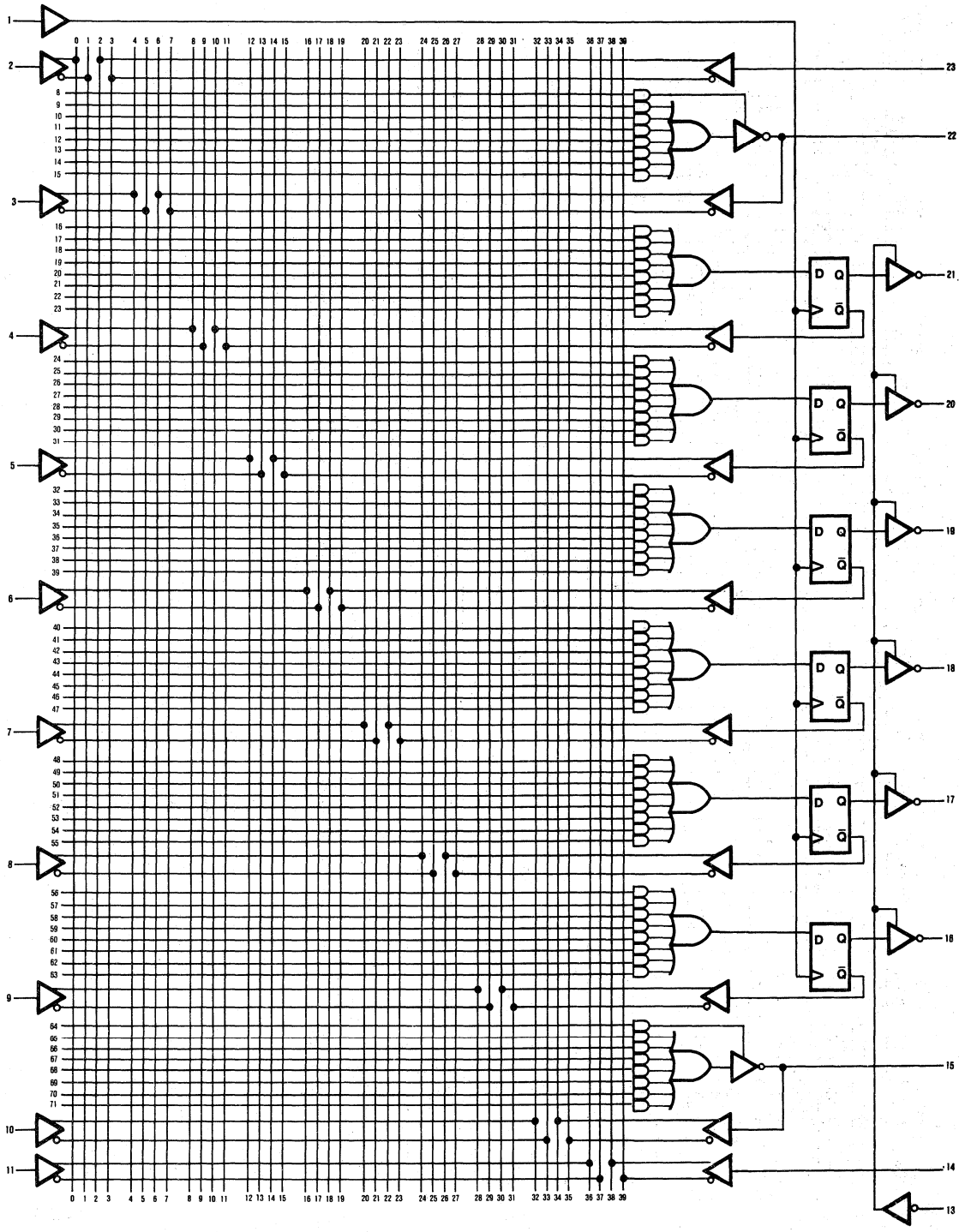
20L8



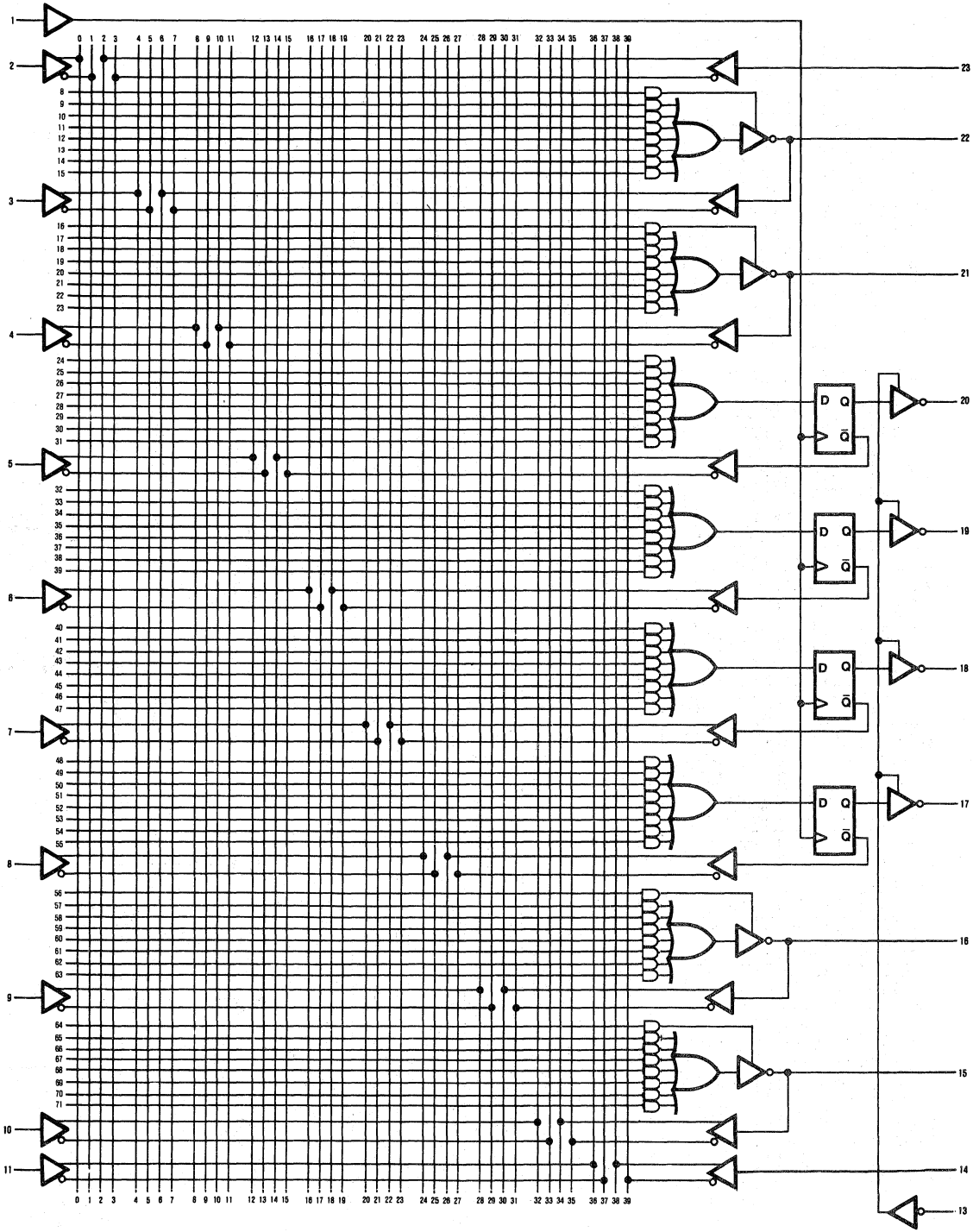
20R8



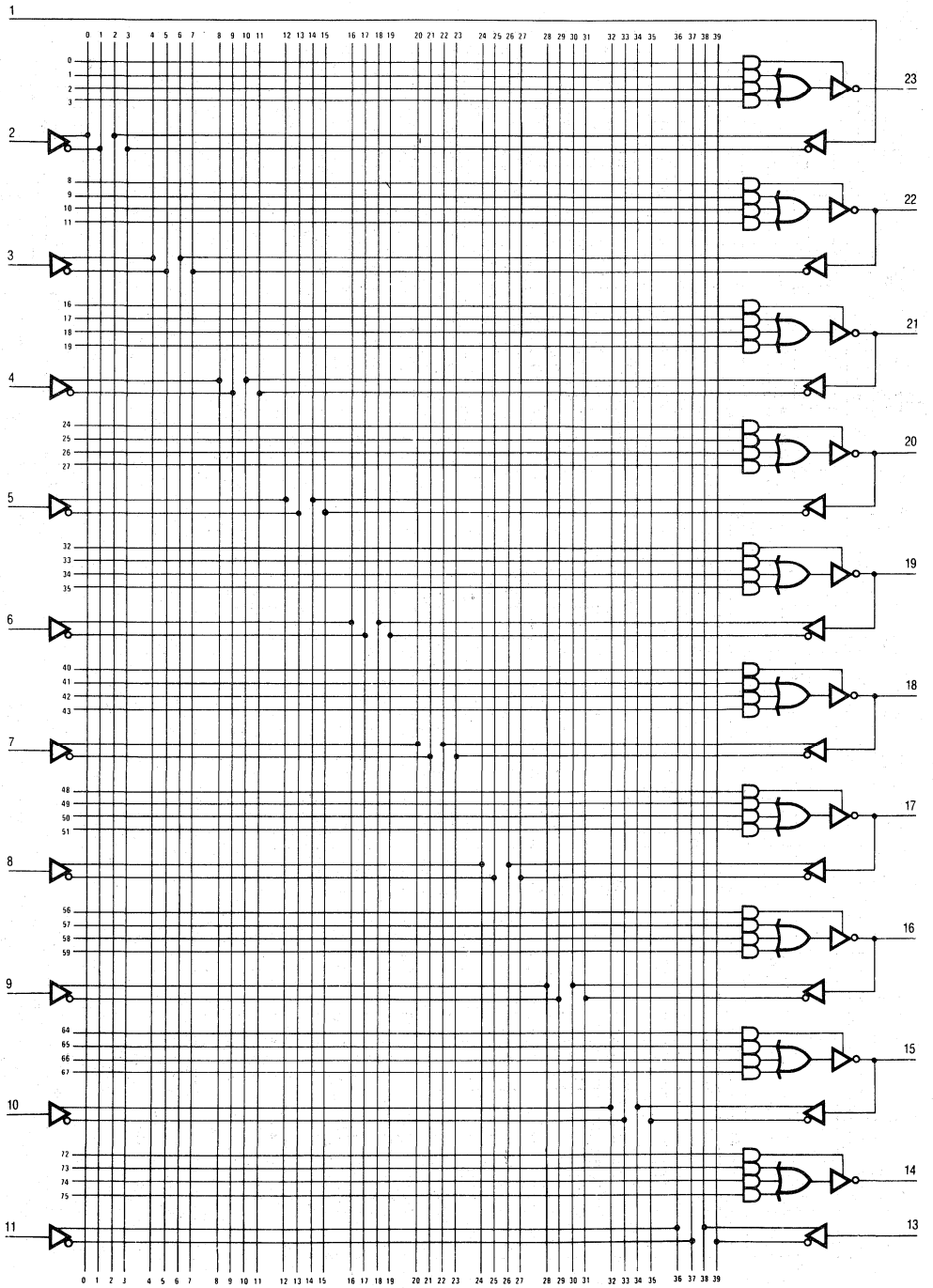
20R6



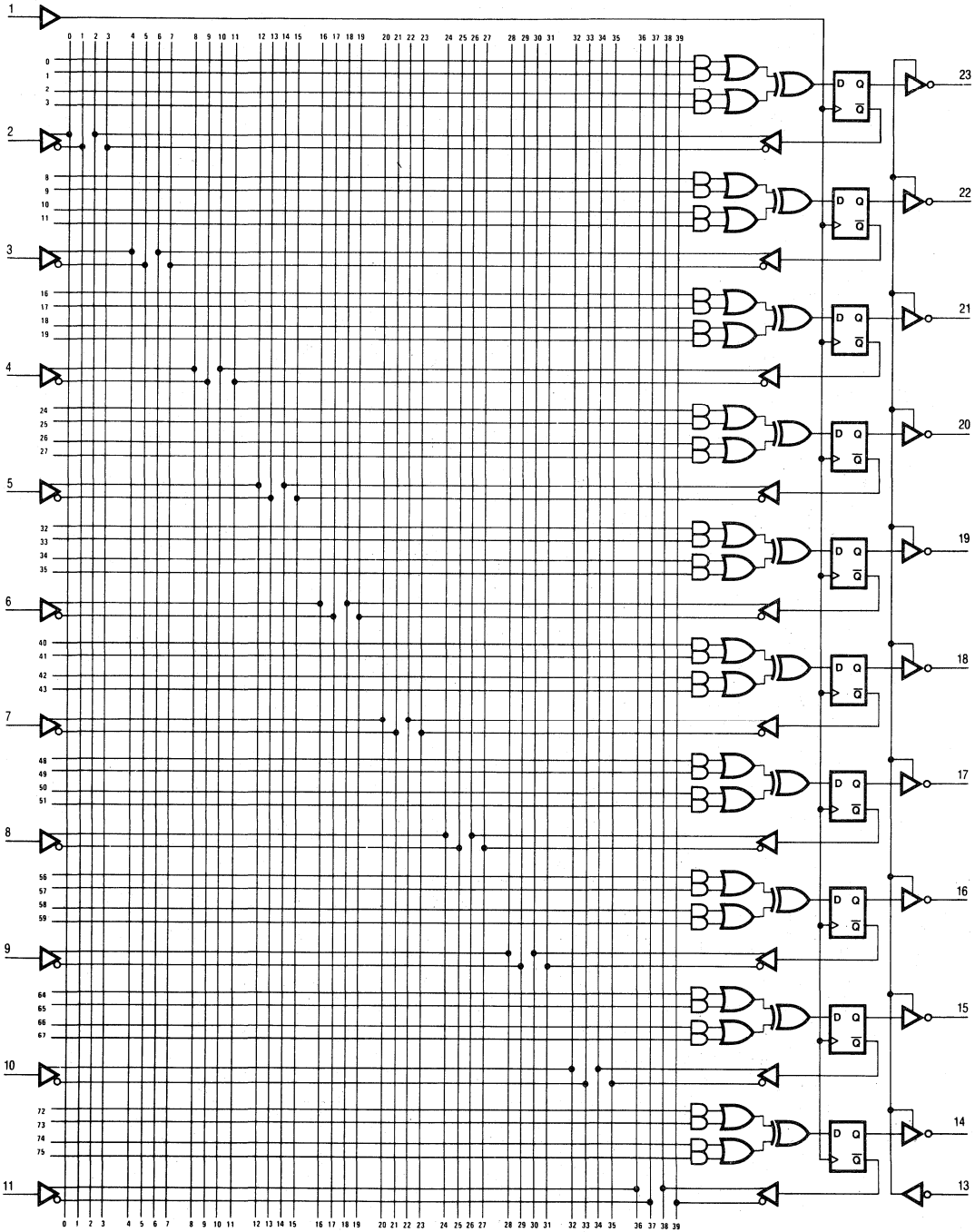
20R4



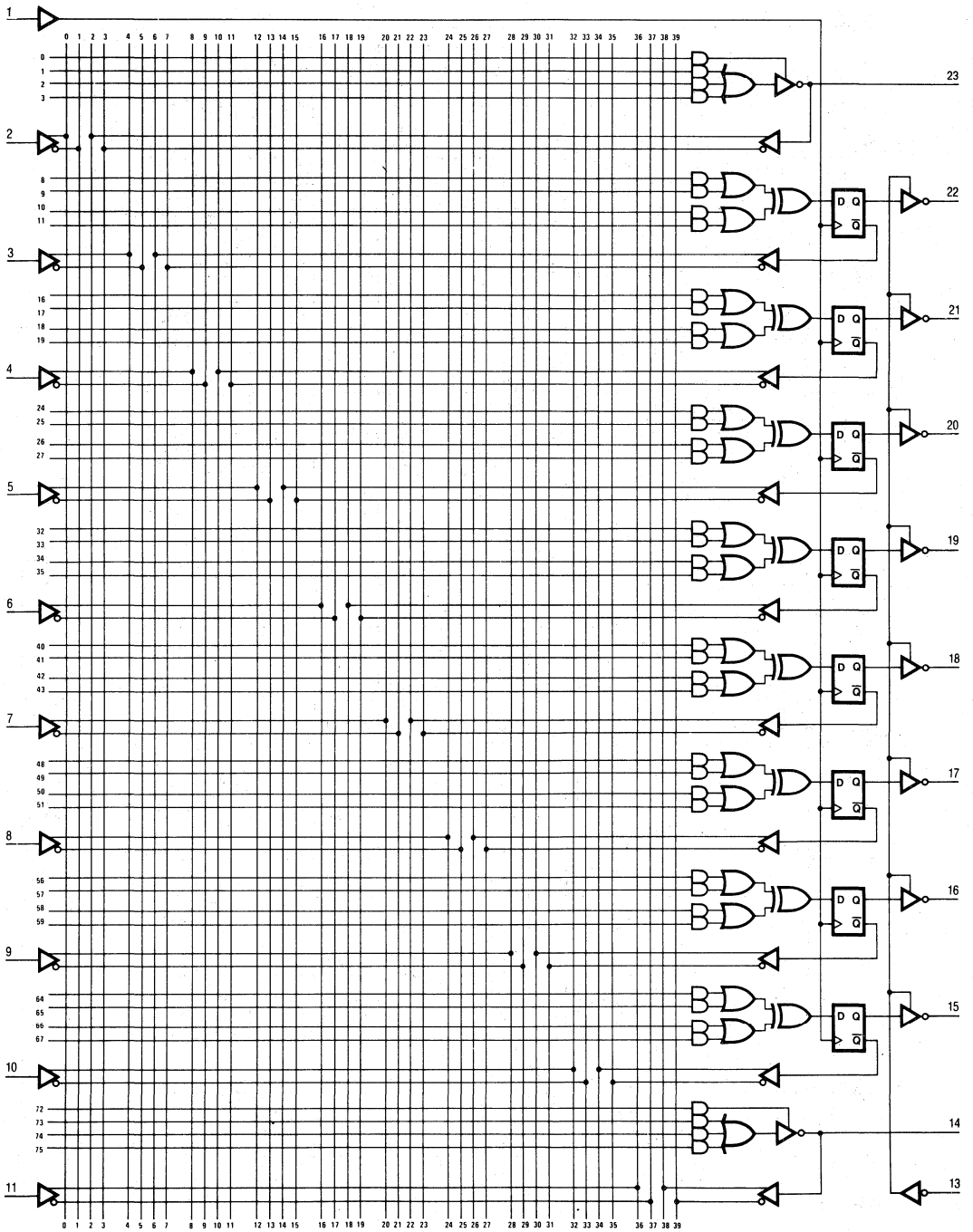
20L10


1
2
3
4
5
6
7
8
9
10
11
23
22
21
20
19
18
17
16
15
14
13
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39

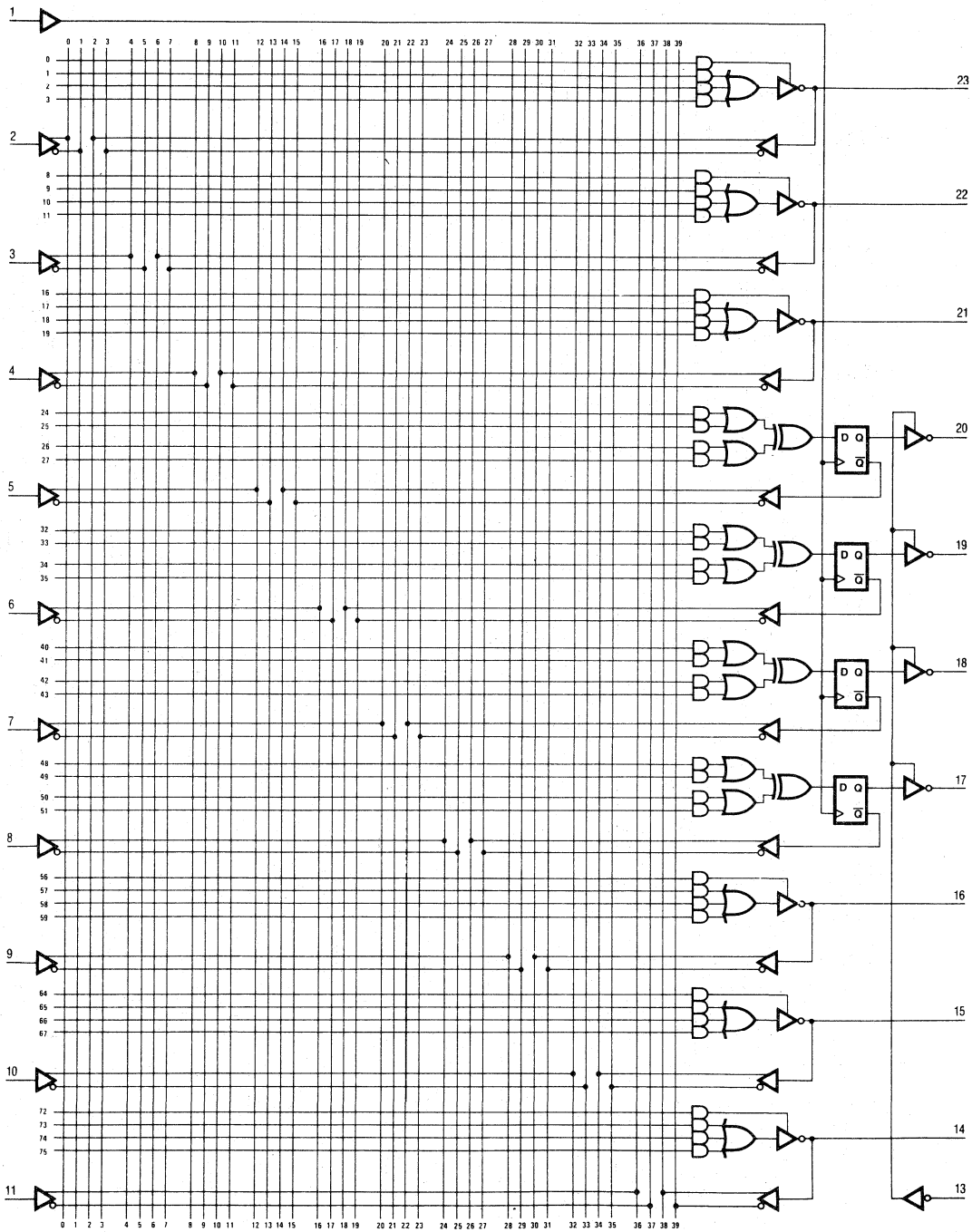
20X10



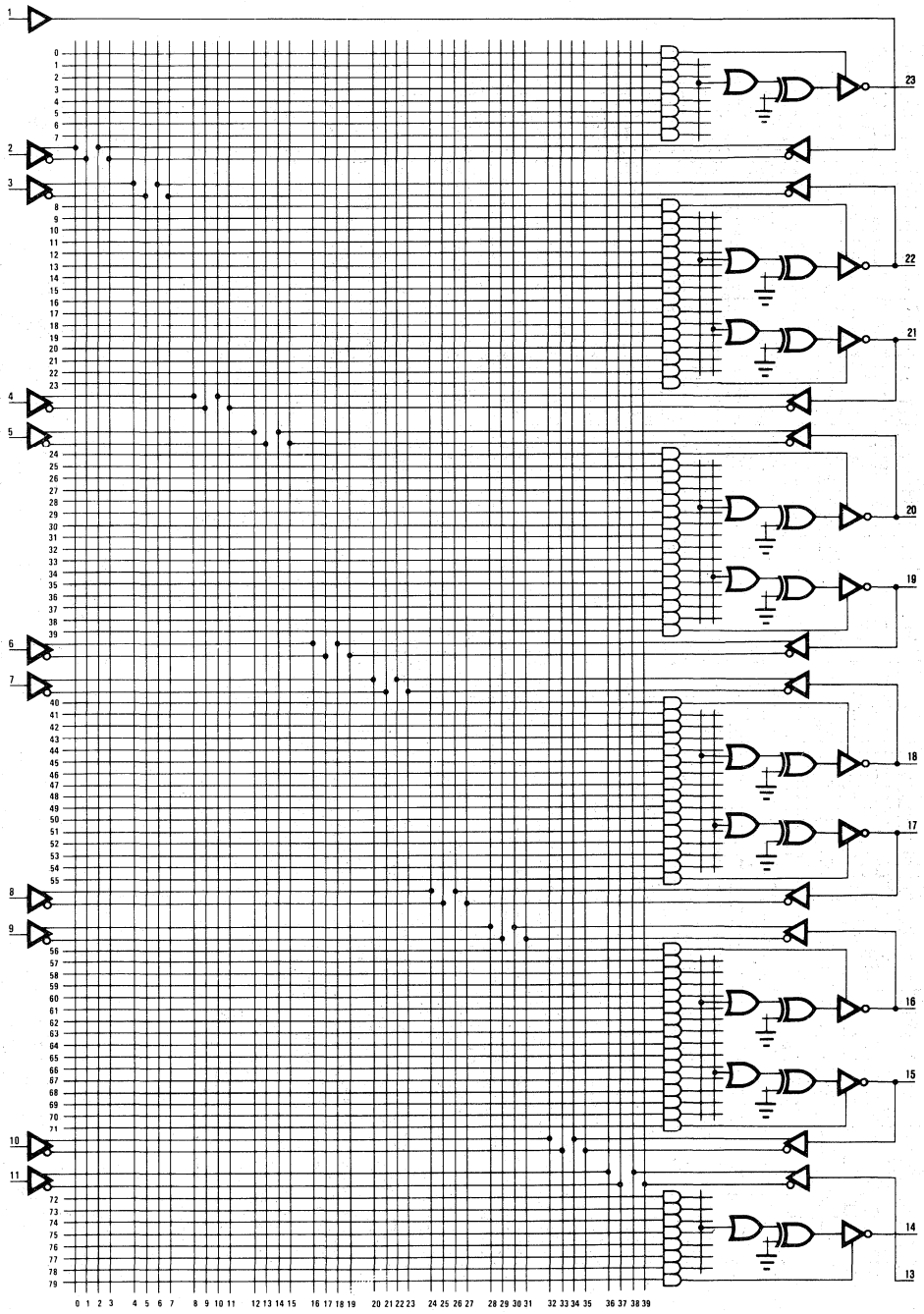
20X8



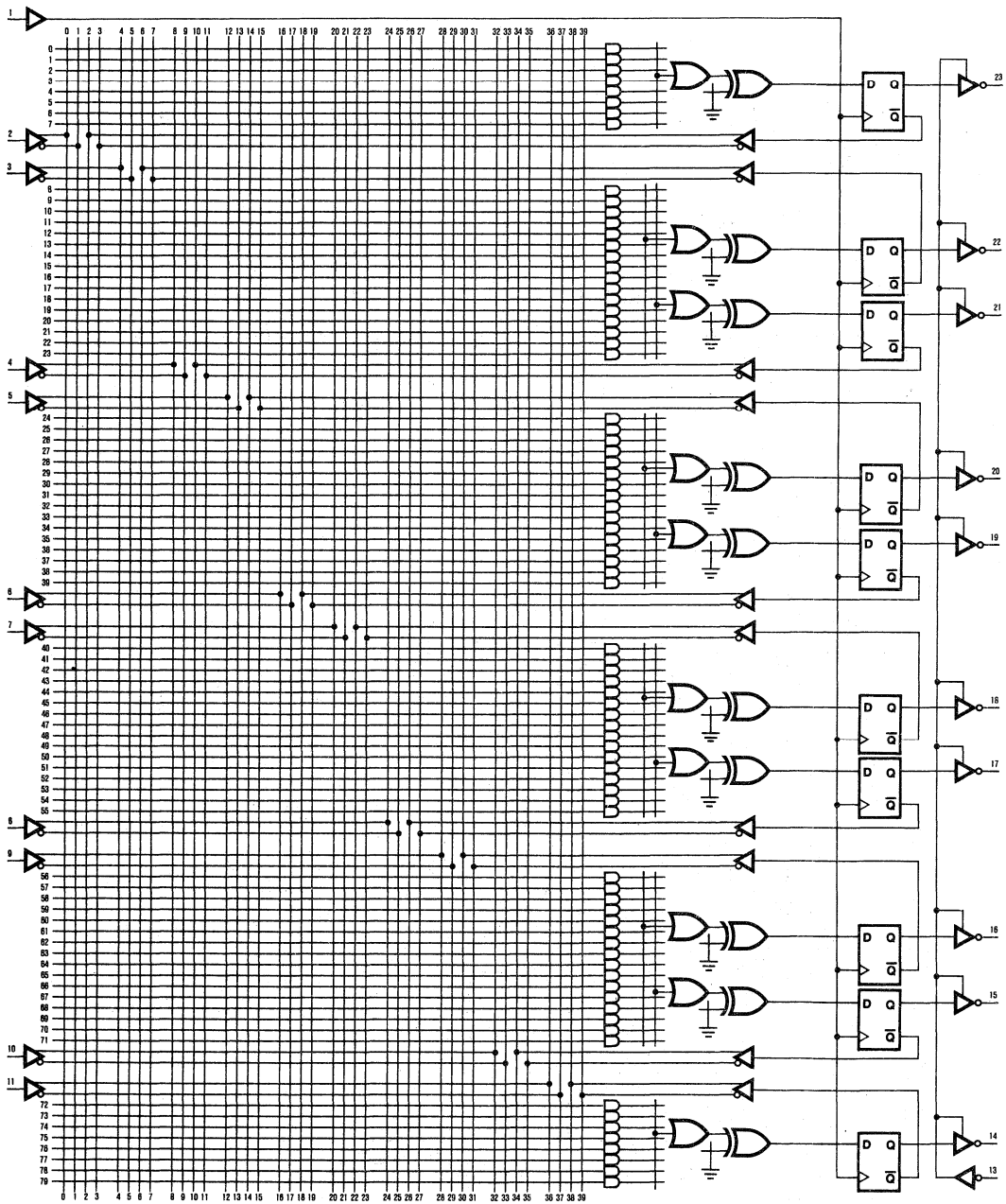
20X4



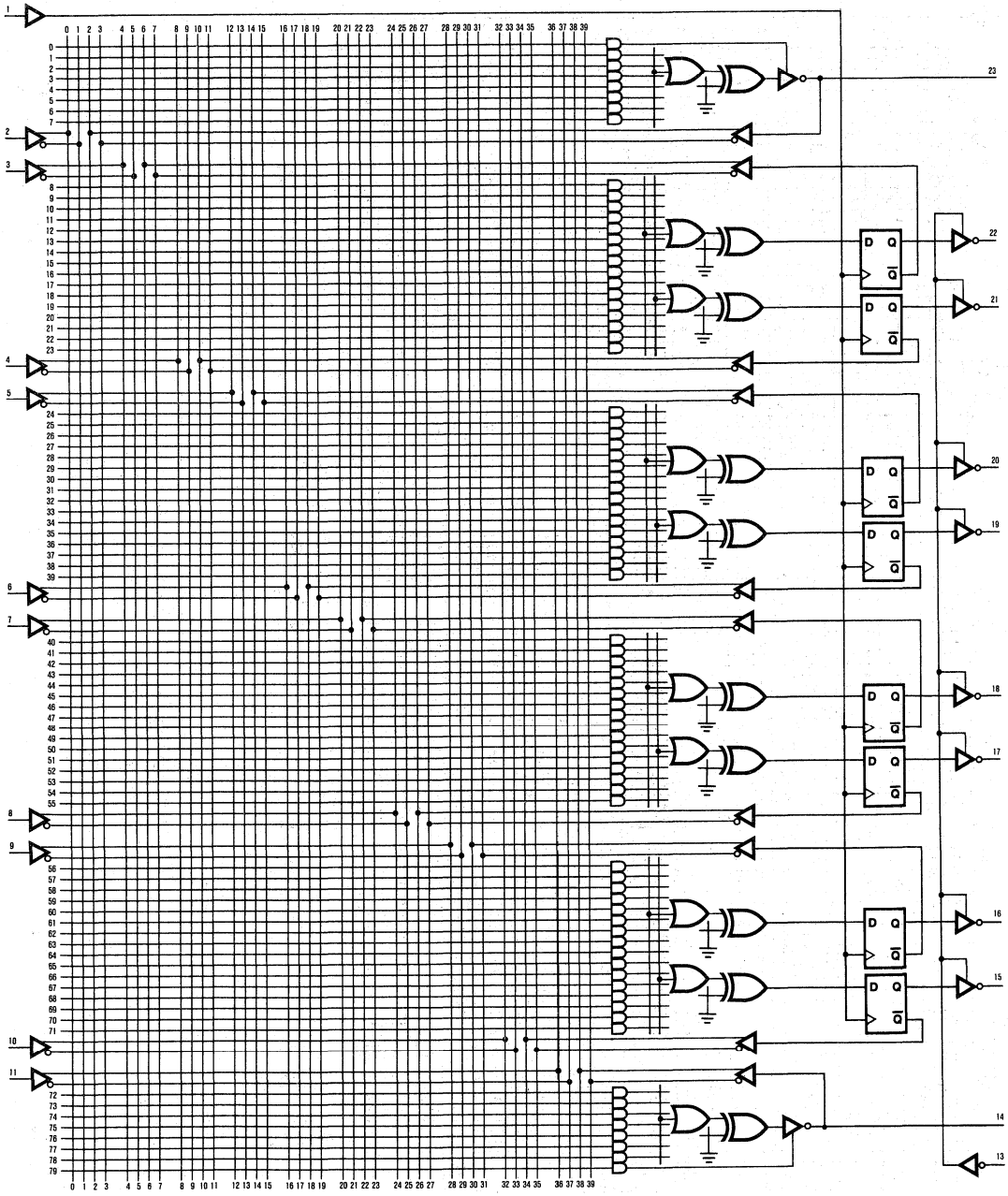
20S10


1
2
3
4
5
6
7
8
9
10
11
23
22
21
20
19
18
17
16
15
14
13
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39

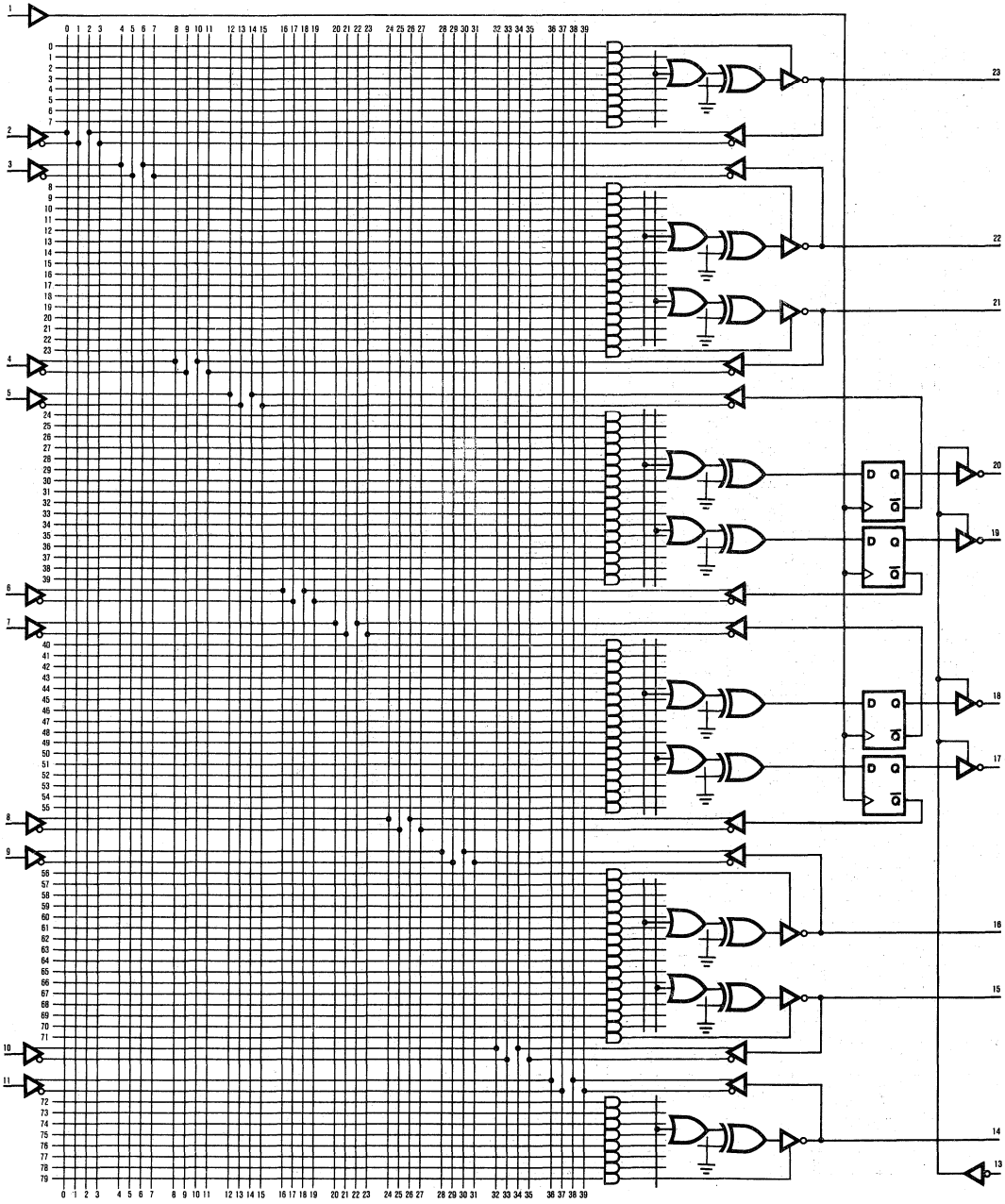
20RS10



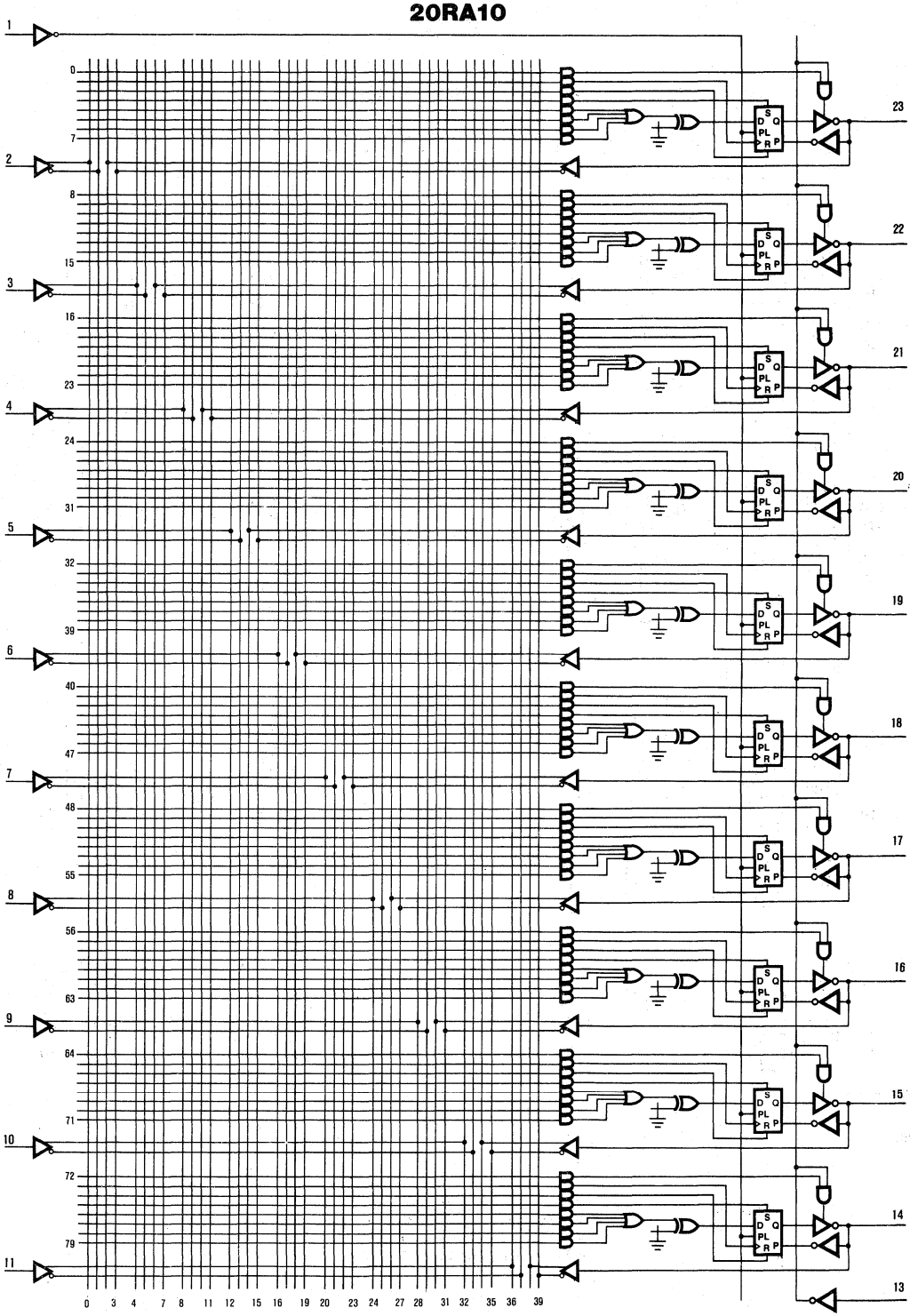
20RS8



20RS4

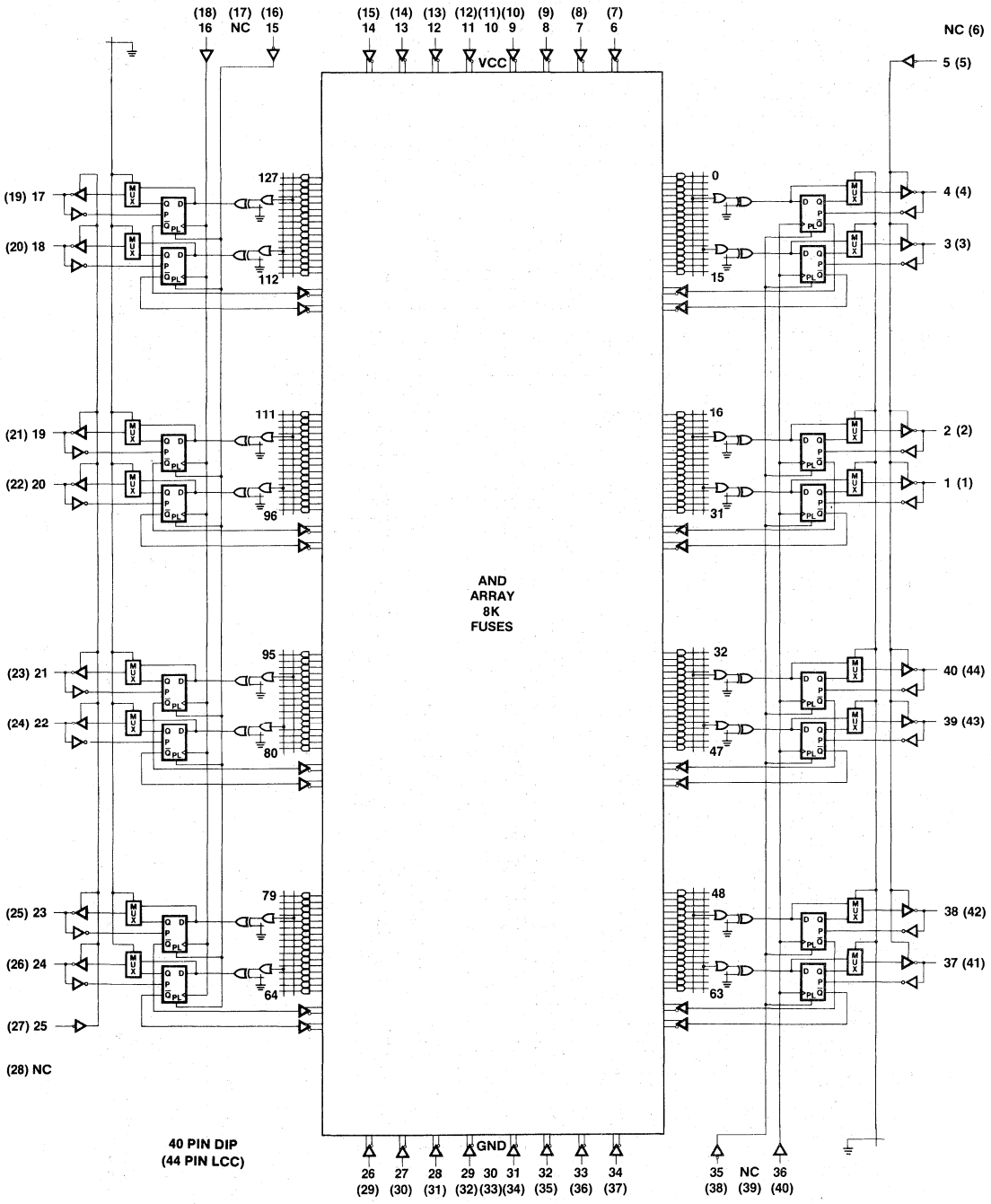


20RA10


1
2
3
4
5
6
7
8
9
10
11
0
7
8
15
16
23
24
31
32
39
40
47
48
55
56
63
64
71
72
79
0 3 4 7 8 11 12 15 16 19 20 23 24 27 28 31 32 35 36 39
S
D
PL
R
Q
P
23
22
21
20
19
18
17
16
15
14
13

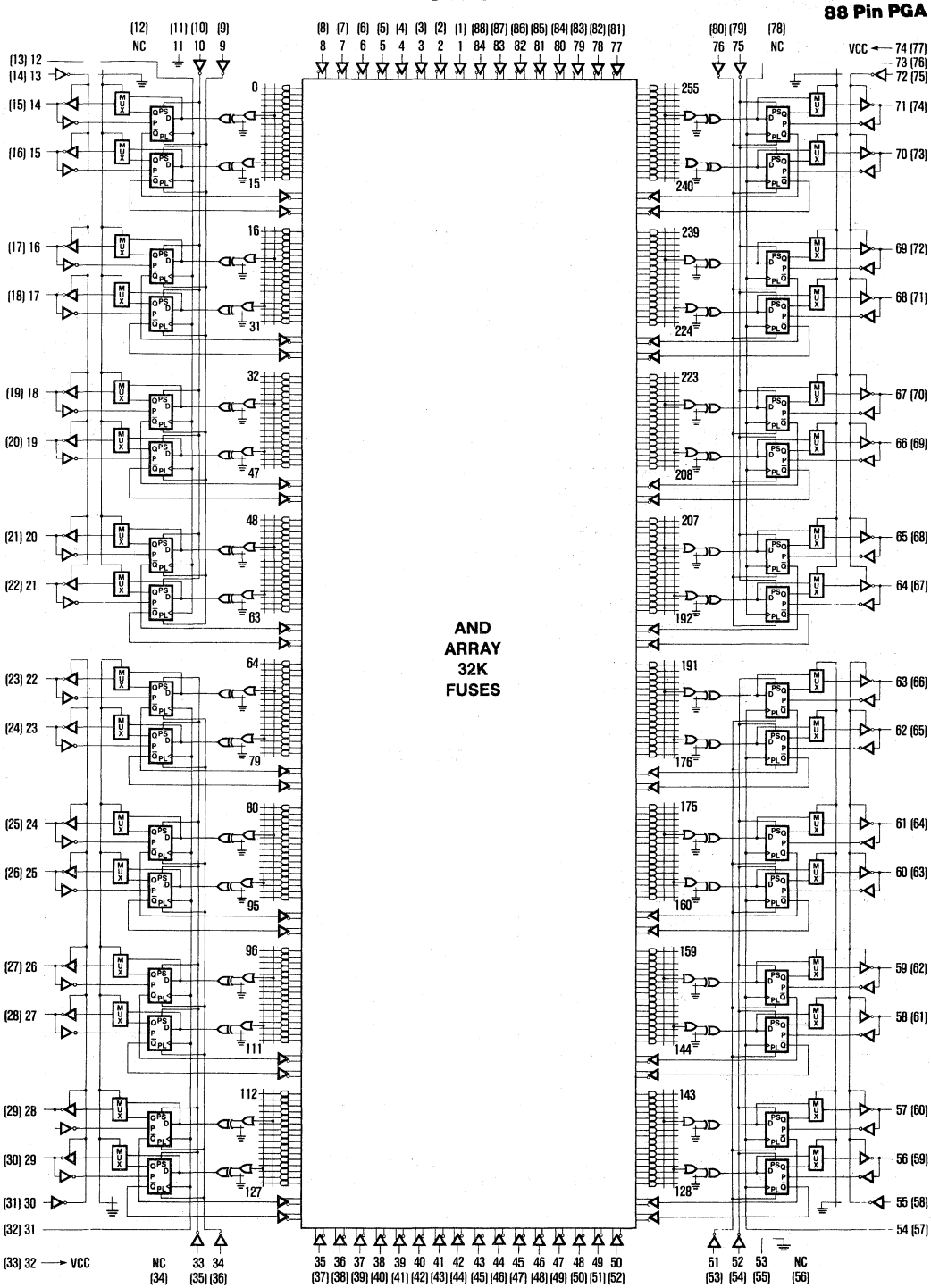
5

32R16


(18) 16
(17) NC
(16) 15
(15) 14
(14) 13
(13) 12
(12) 11
(11) 10
(10) 9
(9) 8
(8) 7
(7) 6
VCC
NC (6)
5 (5)
(19) 17
(20) 18
(21) 19
(22) 20
(23) 21
(24) 22
(25) 23
(26) 24
(27) 25
(28) NC
127
112
111
96
95
80
79
64
0
15
16
31
32
47
48
63
4 (4)
3 (3)
2 (2)
1 (1)
40 (44)
39 (43)
38 (42)
37 (41)
AND ARRAY 8K FUSES
40 PIN DIP
(44 PIN LCC)
GND
26 (29)
27 (30)
28 (31)
29 (32)
30 (33)
31 (34)
32 (35)
33 (36)
34 (37)
35 (38)
NC (39)
36 (40)

64R32

84 Pin LCC
88 Pin PGA



20-Pin Device Family

Data I/O Corporation

10525 Willows Road N.E.
PO Box 97046
Redmond, WA 98073-9746
(800) 247-5700

Models 19, 29A, 29B
Model 60

Series	Part Number	System	LogicPak	Adapter	Family Code	Pinout Code
Small 20/-2 Combinatorial	PAL10H8/-2	Model 60 Rev. V05 Models: 19 29A 29B	303A	303A-002-V08 303A-011A/B-VO1	22	18
	PAL10L8/-2					13
	PAL12H6/-2					19
	PAL12L6/-2					14
	PAL14H4/-2					20
	PAL14L4/-2					15
	PAL16H2/-2					22
	PAL16L2/-2					16
	PAL16C1/-2					21
Medium 20/ 20A/20A-2/4/ 20B-2/-4 Standard	PAL16L8/A/-2/-4/B-2/-4					17
	PAL16R8/A/-2/-4/B-2/-4					24
	PAL16R6/A/-2/-4/B-2/-4					
	PAL16R4/A/-2/-4/B-2/-4					
Medium 20B/D	PAL16L8B/D				30	17
	PAL16R8B/D					24
	PAL16R6B/D					
	PAL16R4B/D					
Medium 20BP Standard	PAL16L8BP		303A-V04		22	17
	PAL16R8BP					67
	PAL16R6BP					
	PAL16R4BP					
Medium 20PA Programmable Polarity	PAL16P8A					30
	PAL16RP8A					31
	PAL16RP6A					
	PAL16RP4A					
Large 20 Arithmetic	PAL16X4		303A			24
	PAL16A4					
Large 20RA Asynchronous	PAL16RA8					30

Note: The software and hardware revisions listed are the earliest revisions that support these products. Later software and hardware revisions can also be assumed to support these products.

24-Pin and MegaPAL™ Device Families

Data I/O

Series	Part Number	System	LogicPak™	Adapter	Family Code	Pinout Code
Small 24 Combinatorial	PAL12L10	Model 60	303A	303A-002-V08	22	01
	PAL14L8	Rev. V05		303A-011A/B-V01		02
	PAL16L6					03
	PAL18L4	Models:19				04
	PAL20L2	29A				05
	PAL20C1	29B				12
Small 24A Decoder	PAL6L16A					48
	PAL8L14A					49
Medium 24A/ 24A-2/B Standard	PAL20L8A/-2/B					26
	PAL20R8A/-2/B					27
	PAL20R6A/-2/B					
	PAL20R4A/-2/B					
Medium 24X Exclusive-OR	PAL20L10					06
	PAL20X10					23
	PAL20X8					
	PAL20X4					
Medium 24XA Exclusive-OR	PAL20L10A		303A-V04			06
	PAL20X10A					36
	PAL20X8A					
	PAL20X4A					
Large 24RS Shared Product Terms	PAL20S10					43
	PAL20RS10					44
	PAL20RS8					
	PAL20RS4					46
Large 24A Registered XOR	PAL22RX8A			303A-011A/B-V01		78
Large 24/A Varied XOR	PAL32VX10/A					77
Large 24RA Asynchronous	PAL20RA10		303A	303A-002-V08 303A-011A/B-V01		45
ECL Combinatorial	PAL10H20P8 [1]		303A-V04	303A-001ME		42
MegaPAL™ Devices	PAL32R16	Model 29B	303A	303A-008-A/B		47
	PAL64R32		350A/-23/A/B			84

Note: The software and hardware revisions listed are the earliest revisions that support these products. Later software and hardware revisions can also be assumed to support these products.

[1] Not supported on Model 19

20-Pin Device Family

Digelec

1602 Lawrence Ave.
Suite 113
Ocean, NJ 07712
(201) 493-2420

System UP803

Series	Part Number	FAM 52 Rev.	Adapter	Adapter Rev.
Small 20/-2 Combinatorial	PAL10H8/-2	5.4	DA53	A-3
	PAL10L8/-2			
	PAL12H6/-2			
	PAL12L6/-2			
	PAL14H4/-2			
	PAL14L4/-2			
	PAL16H2/-2			
	PAL16L2/-2			
	PAL16C1/-2			
Medium 20/ 20A/20A-2/4/ 20B-2/-4 Standard	PAL16L8/A/-2/-4/B-2/-4			
	PAL16R8/A/-2/-4/B-2/-4			
	PAL16R6/A/-2/-4/B-2/-4			
	PAL16R4/A/-2/-4/B-2/-4			
Medium 20B/D	PAL16L8B/D			
	PAL16R8B/D			
	PAL16R6B/D			
	PAL16R4B/D			
Medium 20BP Standard	PAL16L8BP	Under Development		
	PAL16R8BP			
	PAL16R6BP			
	PAL16R4BP			
Medium 20PA Programmable Polarity	PAL16P8A	5.4	DA53	A-3
	PAL16RP8A			
	PAL16RP6A			
	PAL16RP4A			
Large 20 Arithmetic	PAL16X4			
	PAL16A4			
Large 20RA Asynchronous	PAL16RA8	Under Development		

Note: The software and hardware revisions listed are the earliest revisions that support these products. Later software and hardware revisions can also be assumed to support these products.

24-Pin and MegaPAL™ Device Families

Digelec

Series	Part Numbers	FAM 52	Adapter	Adapter Rev.
Small 24 Combinatorial	PAL12L10	5.4 ↓	DA55 ↓	C-1 ↓
	PAL14L8			
	PAL16L6			
	PAL18L4			
	PAL20L2			
	PAL20C1			
Small 24A Decoder	PAL6L16A	Under Development		
	PAL8L14A			
Medium 24A/ 24A-2/B Standard	PAL20L8A/-2/B	5.4 ↓	DA55 ↓	C-1 ↓
	PAL20R8A/-2/B			
	PAL20R6A/-2/B			
	PAL20R4A/-2/B			
Medium 24X Exclusive-OR	PAL20L10			
	PAL20X10			
	PAL20X8			
	PAL20X4			
Medium 24XA Exclusive-OR	PAL20L10A			
	PAL20X10A			
	PAL20X8A			
	PAL20X4A			
Large 24RS Shared Product Terms	PAL20S10			
	PAL20RS10			
	PAL20RS8			
	PAL20RS4			
Large 24A Registered XOR	PAL22RX8A			
Large 24/A Varied XOR	PAL32VX10/A			
Large 24RA Asynchronous	PAL20RA10			
ECL Combinatorial	PAL10H20P8			
MegaPAL™ Devices	PAL32R16	Under Development		
	PAL64R32			

Note: The software and hardware revisions listed are the earliest revisions that support these products. Later software and hardware revisions can also be assumed to support these products.

20-Pin Device Family

Kontron

1230 Charleston Road
Mountain View, CA 94039-7230
(415) 965-7020

System MPP-80S
System EPP-80

Series	Part Number	UPM-B Rev.
Small 20/-2 Combinatorial	PAL10H8/-2	1.44 ↓
	PAL10L8/-2	
	PAL12H6/-2	
	PAL12L6/-2	
	PAL14H4/-2	
	PAL14L4/-2	
	PAL16H2/-2	
	PAL16L2/-2	
	PAL16C1/-2	
Medium 20/ 20A/20A-2/4/ 20B-2/-4 Standard	PAL16L8/A/-2/-4/B-2/-4	
	PAL16R8/A/-2/-4/B-2/-4	
	PAL16R6/A/-2/-4/B-2/-4	
	PAL16R4/A/-2/-4/B-2/-4	
Medium 20B/D	PAL16L8B/D	
	PAL16R8B/D	
	PAL16R6B/D	
	PAL16R4B/D	
Medium 20BP Standard	PAL16L8BP	Under Development
	PAL16R8BP	
	PAL16R6BP	
	PAL16R4BP	
Medium 20PA Programmable Polarity	PAL16P8A	1.44 ↓
	PAL16RP8A	
	PAL16RP6A	
	PAL16RP4A	
Large 20 Arithmetic	PAL16X4	
	PAL16A4	
Large 20RA Asynchronous	PAL16RA8	1.47

Note: The software and hardware revisions listed are the earliest revisions that support these products. Later software and hardware revisions can also be assumed to support these products.

24-Pin and MegaPAL™ Device Families

Kontron

Series	Part Number	UPM-B Rev.
Small 24 Combinatorial	PAL12L10	1.44 ↓
	PAL14L8	
	PAL16L6	
	PAL18L4	
	PAL20L2	
	PAL20C1	
Small 24A Decoder	PAL6L16A	1.48
	PAL8L14A	
Medium 24A/ 24A-2/B Standard	PAL20L8A/-2/B	1.44 ↓
	PAL20R8A/-2/B	
	PAL20R6A/-2/B	
	PAL20R4A/-2/B	
Medium 24X Exclusive-OR	PAL20L10	
	PAL20X10	
	PAL20X8	
	PAL20X4	
Medium 24XA Exclusive-OR	PAL20L10A	
	PAL20X10A	
	PAL20X8A	
	PAL20X4A	
Large 24RS Shared Product Terms	PAL20S10	
	PAL20RS10	
	PAL20RS8	
	PAL20RS4	
Large 24A Registered XOR	PAL22RX8A	
Large 24/A Varied XOR	PAL32VX10/A	1.48
Large 24RA Asynchronous	PAL20RA10	1.44
ECL Combinatorial	PAL10H20P8	1.47
MegaPAL™ Devices	PAL32R16	Under Development
	PAL64R32	

Note: The software and hardware revisions listed are the earliest revisions that support these products. Later software and hardware revisions can also be assumed to support these products.

20-Pin Device Family

Microprоss

Parc d'activite des Pres
5, rue Denis-Papin
59650 Villeneuve-d'Ascq
Tel 20479040

ROM 5000
Programmer

Series	Part Number	Rev.
Small 20/-2 Combinatorial	PAL10H8/-2	3.5 ↓
	PAL10L8/-2	
	PAL12H6/-2	
	PAL12L6/-2	
	PAL14H4/-2	
	PAL14L4/-2	
	PAL16H2/-2	
	PAL16L2/-2	
	PAL16C1/-2	
Medium 20/ 20A/20A-2/4/ 20B-2/-4 Standard	PAL16L8/A/-2/-4/B-2/-4	
	PAL16R8/A/-2/-4/B-2/-4	
	PAL16R6/A/-2/-4/B-2/-4	
	PAL16R4/A/-2/-4/B-2/-4	
Medium 20B/D	PAL16L8B/D	
	PAL16R8B/D	
	PAL16R6B/D	
	PAL16R4B/D	
Medium 20BP Standard	PAL16L8BP	Under Development
	PAL16R8BP	
	PAL16R6BP	
	PAL16R4BP	
Medium 20PA Programmable Polarity	PAL16P8A	3.5 ↓
	PAL16RP8A	
	PAL16RP6A	
	PAL16RP4A	
Large 20 Arithmetic	PAL16X4	
	PAL16A4	
Large 20RA Asynchronous	PAL16RA8	Under Development

Note: The software and hardware revisions listed are the earliest revisions that support these products. Later software and hardware revisions can also be assumed to support these products.

24-Pin and MegaPAL™ Device Families

Microprocess

Series	Part Number	Rev.
Small 24 Combinatorial	PAL12L10	3.5 ↓
	PAL14L8	
	PAL16L6	
	PAL18L4	
	PAL20L2	
	PAL20C1	
Small 24A Decoder	PAL6L16A	Under Development
	PAL8L14A	
Medium 24A/ 24A-2/B Standard	PAL20L8A/-2/B	3.5 ↓
	PAL20R8A/-2/B	
	PAL20R6A/-2/B	
	PAL20R4A/-2/B	
Medium 24X Exclusive-OR	PAL20L10	
	PAL20X10	
	PAL20X8	
	PAL20X4	
Medium 24XA Exclusive-OR	PAL20L10A	
	PAL20X10A	
	PAL20X8A	
	PAL20X4A	
Large 24RS Shared Product Terms	PAL20S10	
	PAL20RS10	
	PAL20RS8	
	PAL20RS4	
Large 24A Registered XOR	PAL22RX8A	
Large 24/A Varied XOR	PAL32VX10/A	
Large 24RA Asynchronous	PAL20RA10	
ECL Combinatorial	PAL10H20P8	
MegaPAL™ Devices	PAL32R16	Under Development
	PAL64R32	

Note: The software and hardware revisions listed are the earliest revisions that support these products. Later software and hardware revisions can also be assumed to support these products.

20-Pin Device Family

Promac

Adams MacDonald Enterprises, Inc.
2999 Monterey/Salinas Highway
Monterey, CA 93940
(408) 373-3607

Promac P3 Programmer

Series	Part Number	Software Rev.	S1/S2
Small 20/-2 Combinatorial	PAL10H8/-2	3.0	0/1
	PAL10L8/-2		0/6
	PAL12H6/-2		0/2
	PAL12L6/-2		0/7
	PAL14H4/-2		0/3
	PAL14L4/-2		0/8
	PAL16H2/-2		0/4
	PAL16L2/-2		0/9
	PAL16C1/-2		0/5
Medium 20/ 20A/20A-2/4/ 20B-2/-4 Standard	PAL16L8/A/-2/-4/B-2/-4		0/10
	PAL16R8/A/-2/-4/B-2/-4		0/11
	PAL16R6/A/-2/-4/B-2/-4		0/12
	PAL16R4/A/-2/-4/B-2/-4		0/13
Medium 20B/D	PAL16L8B/D		5/0
	PAL16R8B/D		5/1
	PAL16R6B/D		5/2
	PAL16R4B/D		5/3
Medium 20BP Standard	PAL16L8BP	Under Development	
	PAL16R8BP		
	PAL16R6BP		
	PAL16R4BP		
Medium 20PA Programmable Polarity	PAL16P8A	3.0	1/0
	PAL16RP8A		1/3
	PAL16RP6A		1/2
	PAL16RP4A		1/1
Large 20 Arithmetic	PAL16X4		0/14
	PAL16A4		0/15
Large 20RA Asynchronous	PAL16RA8		1/12

Note: The software and hardware revisions listed are the earliest revisions that support these products. Later software and hardware revisions can also be assumed to support these products.

24-Pin and MegaPAL™ Device Families

Promac

Series	Part Number	Software Rev.	S1/S2
Small 24 Combinatorial	PAL12L10	3.0	2/2
	PAL14L8		2/3
	PAL16L6		2/4
	PAL18L4		2/5
	PAL20L2		2/6
	PAL20C1		2/1
Small 24A Decoder	PAL6L16A		3/11
	PAL8L14A		3/10
Medium 24A/ 24A-2/B Standard	PAL20L8A/-2/B		2/8
	PAL20R8A/-2/B		2/9
	PAL20R6A/-2/B		2/10
	PAL20R4A/-2/B		2/11
Medium 24X Exclusive-OR	PAL20L10		2/7
	PAL20X10		2/12
	PAL20X8		2/13
	PAL20X4		2/14
Medium 24XA Exclusive-OR	PAL20L10A		2/7
	PAL20X10A		2/15
	PAL20X8A		3/0
	PAL20X4A		3/1
Large 24RS Shared Product Terms	PAL20S10		3/5
	PAL20RS10		3/6
	PAL20RS8		3/7
	PAL20RS4		3/8
Large 24A Registered XOR	PAL22RX8A		
Large 24/A Varied XOR	PAL32VX10/A		
Large 24RA Asynchronous	PAL20RA10		3.4
ECL Combinatorial	PAL10H20P8		
MegaPAL™ Devices	PAL32R16	Under Development	
	PAL64R32		

Note: The software and hardware revisions listed are the earliest revisions that support these products. Later software and hardware revisions can also be assumed to support these products.

20-Pin Device Family

Stag Microsystems

528-5 Weddell Drive
Sunnyvale, CA 94089
(408) 745-1991

ZL30
PPZ

Series	Part Number	Code	ZL30 Rev.	Zm2200
Small 20/-2 Combinatorial	PAL10H8/-2	20-20	30-35 ↓	14 ↓
	PAL10L8/-2	20-25		
	PAL12H6/-2	20-21		
	PAL12L6/-2	20-26		
	PAL14H4/-2	20-22		
	PAL14L4/-2	20-27		
	PAL16H2/-2	20-23		
	PAL16L2/-2	20-28		
	PAL16C1/-2	20-24		
Medium 20/ 20A/20A-2/4/ 20B-2/-4 Standard	PAL16L8/A/-2/-4/B-2/-4	20-29		
	PAL16R8/A/-2/-4/B-2/-4	20-30		
	PAL16R6/A/-2/-4/B-2/-4	20-31		
	PAL16R4/A/-2/-4/B-2/-4	20-32		
Medium 20B/D	PAL16L8B/D	22-29	30-39 ↓	12 ↓
	PAL16R8B/D	22-30		
	PAL16R6B/D	22-31		
	PAL16R4B/D	22-32		
Medium 20BP Standard	PAL16L8BP	Under Development		
	PAL16R8BP			
	PAL16R6BP			
	PAL16R4BP			
Medium 20PA Programmable Polarity	PAL16P8A	20-38	30-35 ↓	12 ↓
	PAL16RP8A	20-11		
	PAL16RP6A	20-12		
	PAL16RP4A	20-13		
Large 20 Arithmetic	PAL16X4	20-33		14
	PAL16A4	20-34		
Large 20RA Asynchronous	PAL16RA8	20-19	30-37	12

Note: The software and hardware revisions listed are the earliest revisions that support these products. Later software and hardware revisions can also be assumed to support these products.

24-Pin and MegaPAL™ Device Families

Stag Microsystems

Series	Part Number	Code	ZL30 Rev.	ZM2200
Small 24 Combinatorial	PAL12L10	21-50	30-35 ↓	14
	PAL14L8	21-51		
	PAL16L6	21-52		12 ↓
	PAL18L4	21-53		
	PAL20L2	21-54		
	PAL20C1	21-55		
Small 24A Decoder	PAL6L16A	Under Development		
	PAL8L14A			
Medium 24A/ 24A-2/B Standard	PAL20L8A/-2/B	21-56	30-35 ↓	12 ↓
	PAL20R8A/-2/B	21-57		
	PAL20R6A/-2/B	21-58		
	PAL20R4A/-2/B	21-59		
Medium 24X Exclusive-OR	PAL20L10	21-60		
	PAL20X10	21-61		
	PAL20X8	21-62		
	PAL20X4	21-63		
Medium 24XA Exclusive-OR	PAL20L10A	21-60		
	PAL20X10A	21-61		
	PAL20X8A	21-62		
	PAL20X4A	21-63		
Large 24RS Shared Product Terms	PAL20S10	21-81	30-39 ↓	
	PAL20RS10	21-80		
	PAL20RS8	21-79		
	PAL20RS4	21-78		
Large 24A Registered XOR	PAL22RX8A			
Large 24/A Varied XOR	PAL32VX10/A			
Large 24RA Asynchronous	PAL20RA10	21-77	30-37	
ECL Combinatorial	PAL10H20P8			
MegaPAL™ Devices	PAL32R16	Under Development		
	PAL64R32			

Note: The software and hardware revisions listed are the earliest revisions that support these products. Later software and hardware revisions can also be assumed to support these products.

20-Pin Device Family

Storey Systems

3201 North Hwy. 67
Suite H
Mesquite, TX 75150
(214) 270-4135

P240
Programmer

Series	Part Number	Rev.
Small 20/-2 Combinatorial	PAL10H8/-2	2.0 ↓
	PAL10L8/-2	
	PAL12H6/-2	
	PAL12L6/-2	
	PAL14H4/-2	
	PAL14L4/-2	
	PAL16H2/-2	
	PAL16L2/-2	
	PAL16C1/-2	
Medium 20/ 20A/20A-2/4/ 20B-2/-4 Standard	PAL16L8/A/-2/-4/B-2/-4	
	PAL16R8/A/-2/-4/B-2/-4	
	PAL16R6/A/-2/-4/B-2/-4	
	PAL16R4/A/-2/-4/B-2/-4	
Medium 20B/D	PAL16L8B/D	4.0 ↓
	PAL16R8B/D	
	PAL16R6B/D	
	PAL16R4B/D	
Medium 20BP Standard	PAL16L8BP	Under Development
	PAL16R8BP	
	PAL16R6BP	
	PAL16R4BP	
Medium 20PA Programmable Polarity	PAL16P8A	4.0 ↓
	PAL16RP8A	
	PAL16RP6A	
	PAL16RP4A	
Large 20 Arithmetic	PAL16X4	2.0
	PAL16A4	
Large 20RA Asynchronous	PAL16RA8	4.04

Note: The software and hardware revisions listed are the earliest revisions that support these products. Later software and hardware revisions can also be assumed to support these products.

24-Pin and MegaPAL™ Device Families

Storey Systems

Series	Part Number	Rev.
Small 24 Combinatorial	PAL12L10	2.0 ↓
	PAL14L8	
	PAL16L6	
	PAL18L4	
	PAL20L2	
	PAL20C1	
Small 24A Decoder	PAL6L16A	Under Development
	PAL8L14A	
Medium 24A/ 24A-2/B Standard	PAL20L8A/-2/B	2.0 ↓
	PAL20R8A/-2/B	
	PAL20R6A/-2/B	
	PAL20R4A/-2/B	
Medium 24X Exclusive-OR	PAL20L10	
	PAL20X10	
	PAL20X8	
	PAL20X4	
Medium 24XA Exclusive-OR	PAL20L10A	
	PAL20X10A	Under Development ↓
	PAL20X8A	
	PAL20X4A	
Large 24RS Shared Product Terms	PAL20S10	
	PAL20RS10	
	PAL20RS8	
	PAL20RS4	
Large 24A Registered XOR	PAL22RX8A	
Large 24/A Varied XOR	PAL32VX10/A	
Large 24RA Asynchronous	PAL20RA10	4.04
ECL Combinatorial	PAL10H20P8	
MegaPAL™ Devices	PAL32R16	Under Development
	PAL64R32	

Note: The software and hardware revisions listed are the earliest revisions that support these products. Later software and hardware revisions can also be assumed to support these products.

20-Pin Device Family

Structured Design

1700 Wyatt Drive
Suite 7
Santa Clara, CA 95054
(408) 988-0725

SD 20/24 System
SD 1000 System

Series	Part Number	SD 20/24	SD 1000
Small 20/-2 Combinatorial	PAL10H8/-2	1.6	1.05
	PAL10L8/-2		
	PAL12H6/-2		
	PAL12L6/-2		
	PAL14H4/-2		
	PAL14L4/-2		
	PAL16H2/-2		
	PAL16L2/-2		
	PAL16C1/-2		
Medium 20/ 20A/20A-2/4/ 20B-2/-4 Standard	PAL16L8/A/-2/-4/B-2/-4		
	PAL16R8/A/-2/-4/B-2/-4		
	PAL16R6/A/-2/-4/B-2/-4		
	PAL16R4/A/-2/-4/B-2/-4		
Medium 20B/D	PAL16L8B/D	Under Development	
	PAL16R8B/D		
	PAL16R6B/D		
	PAL16R4B/D		
Medium 20BP Standard	PAL16L8BP	Under Development	
	PAL16R8BP		
	PAL16R6BP		
	PAL16R4BP		
Medium 20PA Programmable Polarity	PAL16P8A		
	PAL16RP8A		
	PAL16RP6A		
	PAL16RP4A		
Large 20 Arithmetic	PAL16X4	1.6	1.05
	PAL16A4		
Large 20RA Asynchronous	PAL16RA8	Under Development	

Note: The software and hardware revisions listed are the earliest revisions that support these products. Later software and hardware revisions can also be assumed to support these products.

24-Pin and MegaPAL™ Device Families

Structured Design

Series	Part Number	SD 20/24	SD 1000
Small 24 Combinatorial	PAL12L10	1.6 ↓	1.05 ↓
	PAL14L8		
	PAL16L6		
	PAL18L4		
	PAL20L2		
	PAL20C1		
Small 24A Decoder	PAL6L16A	Under Development	
	PAL8L14A		
Medium 24A/ 24A-2/B Standard	PAL20L8A/-2/B	1.6 ↓	1.05 ↓
	PAL20R8A/-2/B		
	PAL20R6A/-2/B		
	PAL20R4A/-2/B		
Medium 24X Exclusive-OR	PAL20L10		
	PAL20X10		
	PAL20X8		
	PAL20X4		
Medium 24XA Exclusive-OR	PAL20L10A		
	PAL20X10A		
	PAL20X8A		
	PAL20X4A		
Large 24RS Shared Product Terms	PAL20S10	Under Development ↓	
	PAL20RS10		
	PAL20RS8		
	PAL20RS4		
Large 24A Registered XOR	PAL22RX8A		
Large 24/A Varied XOR	PAL32VX10/A		
Large 24RA Asynchronous	PAL20RA10		
ECL Combinatorial	PAL10H20P8		
MegaPAL™ Devices	PAL32R16		
	PAL64R32		

Note: The software and hardware revisions listed are the earliest revisions that support these products. Later software and hardware revisions can also be assumed to support these products.

20-Pin Device Family

Valley Data Sciences

Charleston Business Park
2426 Charleston Road
Mountain View, CA 94043
(415) 968-2900

160 Series
Programmer

Series	Part Number	Rev.
Small 20/-2 Combinatorial	PAL10H8/-2	1.03 ↓
	PAL10L8/-2	
	PAL12H6/-2	
	PAL12L6/-2	
	PAL14H4/-2	
	PAL14L4/-2	
	PAL16H2/-2	
	PAL16L2/-2	
	PAL16C1/-2	
Medium 20/ 20A/20A-2/4/ 20B-2/-4 Standard	PAL16L8/A/-2/-4/B-2/-4	
	PAL16R8/A/-2/-4/B-2/-4	
	PAL16R6/A/-2/-4/B-2/-4	
	PAL16R4/A/-2/-4/B-2/-4	
Medium 20B/D	PAL16L8B/D	
	PAL16R8B/D	
	PAL16R6B/D	
	PAL16R4B/D	
Medium 20BP Standard	PAL16L8BP	Under Development
	PAL16R8BP	
	PAL16R6BP	
	PAL16R4BP	
Medium 20PA Programmable Polarity	PAL16P8A	1.03 ↓
	PAL16RP8A	
	PAL16RP6A	
	PAL16RP4A	
Large 20 Arithmetic	PAL16X4	
	PAL16A4	
Large 20RA Asynchronous	PAL16RA8	Under Development

Note: The software and hardware revisions listed are the earliest revisions that support these products. Later software and hardware revisions can also be assumed to support these products.

24-Pin and MegaPAL™ Device Families

Valley Data Sciences

Series	Part Number	Rev.
Small 24 Combinatorial	PAL12L10	1.03 ↓
	PAL14L8	
	PAL16L6	
	PAL18L4	
	PAL20L2	
	PAL20C1	
Small 24A Decoder	PAL6L16A	Under Development
	PAL8L14A	
Medium 24A/ 24A-2/B Standard	PAL20L8A/-2/B	1.03 ↓
	PAL20R8A/-2/B	
	PAL20R6A/-2/B	
	PAL20R4A/-2/B	
Medium 24X Exclusive-OR	PAL20L10	
	PAL20X10	
	PAL20X8	
	PAL20X4	
Medium 24XA Exclusive-OR	PAL20L10A	
	PAL20X10A	
	PAL20X8A	
	PAL20X4A	
Large 24RS Shared Product Terms	PAL20S10	
	PAL20RS10	
	PAL20RS8	
	PAL20RS4	
Large 24A Registered XOR	PAL22RX8A	
Large 24/A Varied XOR	PAL32VX10/A	
Large 24RA Asynchronous	PAL20RA10	
ECL Combinatorial	PAL10H20P8	
MegaPAL™ Devices	PAL32R16	1.04 + 1.1 Adapter
	PAL64R32	Under Development

Note: The software and hardware revisions listed are the earliest revisions that support these products. Later software and hardware revisions can also be assumed to support these products.

20-Pin Device Family

Varix

1210 E. Campbell Road
Richardson, TX 75081
(214) 437-0777

OMNI Programmer

Series	Part Number	Rev.
Small 20/-2 Combinatorial	PAL10H8/-2	3.18 ↓
	PAL10L8/-2	
	PAL12H6/-2	
	PAL12L6/-2	
	PAL14H4/-2	
	PAL14L4/-2	
	PAL16H2/-2	
	PAL16L2/-2	
	PAL16C1/-2	
Medium 20/ 20A/20A-2/4/ 20B-2/-4 Standard	PAL16L8/A/-2/-4/B-2/-4	
	PAL16R8/A/-2/-4/B-2/-4	
	PAL16R6/A/-2/-4/B-2/-4	
	PAL16R4/A/-2/-4/B-2/-4	
Medium 20B/D	PAL16L8B/D	
	PAL16R8B/D	
	PAL16R6B/D	
	PAL16R4B/D	
Medium 20BP Standard	PAL16L8BP	Under Development
	PAL16R8BP	
	PAL16R6BP	
	PAL16R4BP	
Medium 20PA Programmable Polarity	PAL16P8A	3.18 ↓
	PAL16RP8A	
	PAL16RP6A	
	PAL16RP4A	
Large 20 Arithmetic	PAL16X4	
	PAL16A4	
Large 20RA Asynchronous	PAL16RA8	Under Development

Note: The software and hardware revisions listed are the earliest revisions that support these products. Later software and hardware revisions can also be assumed to support these products.

24-Pin and MegaPAL™ Device Families

Varix

Series	Part Number	Rev.
Small 24 Combinatorial	PAL12L10	3.18
	PAL14L8	
	PAL16L6	
	PAL18L4	
	PAL20L2	
	PAL20C1	
Small 24A Decoder	PAL6L16A	
	PAL8L14A	
Medium 24A/ 24A-2/B Standard	PAL20L8A/-2/B	
	PAL20R8A/-2/B	
	PAL20R6A/-2/B	
	PAL20R4A/-2/B	
Medium 24X Exclusive-OR	PAL20L10	
	PAL20X10	
	PAL20X8	
	PAL20X4	
Medium 24XA Exclusive-OR	PAL20L10A	
	PAL20X10A	
	PAL20X8A	
	PAL20X4A	
Large 24RS Shared Product Terms	PAL20S10	Under Development
	PAL20RS10	
	PAL20RS8	
	PAL20RS4	
Large 24A Registered XOR	PAL22RX8A	
Large 24/A Varied XOR	PAL32VX10/A	
Large 24RA Asynchronous	PAL20RA10	3.18
ECL Combinatorial	PAL10H20P8	
MegaPAL™ Devices	PAL32R16	Under Development
	PAL64R32	

Note: The software and hardware revisions listed are the earliest revisions that support these products. Later software and hardware revisions can also be assumed to support these products.


IMPORTANT
NOTES

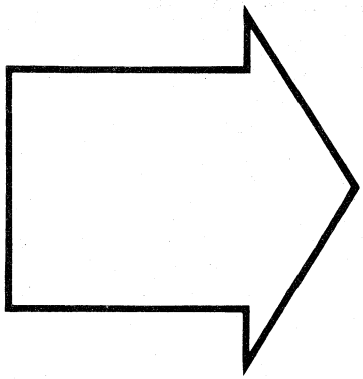


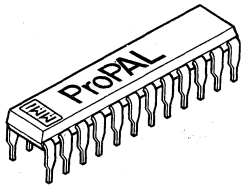
Table of Contents

ProPAL™, HAL®, and ZHAL™ Devices: The Logical Solutions for Volume Programmable Logic

So you have discovered the convenience and flexibility of designing with PAL® devices from Monolithic Memories. You have implemented a design using PAL devices, and taken that design into production. Now may be the time to consider ways of reducing the efforts you put into programming, testing, and marking large volumes of PAL devices. Wouldn't it be more convenient if you could be relieved of the duties and costs of volume programming and testing and still reap the benefits afforded by programmable logic?

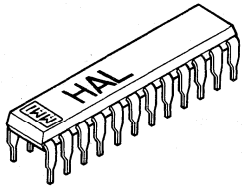
Or perhaps you are considering a semicustom product, but you're a little nervous about going to a gate array. Wouldn't it be preferable if you could find a semicustom product which allows easy, inexpensive prototyping, provides fast prototype turn-around, comes fully tested, can have a custom marking, has low NRE charges, provides design flexibility, and has an assured second source?

Well, Monolithic Memories, the inventor of the PAL device, offers the logical solutions. ProPAL, HAL, and ZHAL devices make the transition from user-programmed devices to customized production-ready devices easy and risk free.



ProPAL Devices

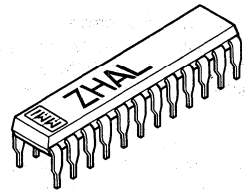
ProPAL (Programmed PAL) devices are simply PAL devices that Monolithic Memories programs and tests for you. You receive a fully functional unit without having to do the programming and testing. But you still have the flexibility to handle design changes easily.



HAL Devices

HAL (Hard Array Logic) devices are to PAL devices as ROMs are to PROMs. Instead of fuses in the logic array, your pattern is implemented using metal links that are masked in during wafer fabrication. So your need to program devices is eliminated. And because the devices have their functionality masked in, Monolithic Memories can provide full functional testing before shipping the product. You can place the devices in your boards with a minimum of handling and the highest level of confidence.

Monolithic Memories offers a HAL device for every PAL device. Any PAL device design you program can be implemented in a HAL version, allowing you to move smoothly into volume production.



ZHAL Devices

Monolithic Memories now provides a third alternative for the programmable logic user: new Zero-Standby-Power CMOS HAL devices.

For the first time there are HAL devices which can implement any pattern from the Series 20 and Series 24 PAL devices with the greatly reduced power consumption only CMOS can offer.

For high complexity designs reaching into the thousands of gates, Zero Power MegaHAL™ devices provide the natural semicustom VLSI alternative to gate arrays. The MegaPAL™ devices provide the flexibility and fast design turn-around you need for prototyping. Once you are ready for production, the CMOS MegaHAL devices provide the same functionality with Zero Power.

All of the ZHAL devices are fully HC/HCT compatible, making them easy to use in TTL and CMOS environments.

Should You Use a PAL, ProPAL, or HAL Device?

PAL devices offer the flexibility and convenience needed for prototyping your innovative designs. They provide a means for designing an efficient system by integrating functions and saving you board space. For flexible production, it makes sense to program and test your own PAL devices. This is especially true if you need low volumes per pattern. You always have the option of making last minute design tweaks as you fine tune your system design.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories MMI

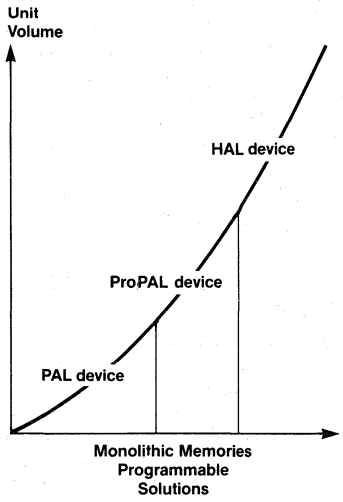
Once your production volumes reach a moderate volume of a few thousand devices per year for each pattern, you may wish to dedicate your production resources to newer designs, instead of programming and testing production volumes. Yet in order to be able to make quick design updates, you might not want to commit to a HAL mask. ProPAL devices provide the ideal solution by eliminating programming and testing needs while retaining enough flexibility to accommodate design changes.

When you feel that your design has stabilized and your volume has ramped up to several thousand devices per year, a HAL device becomes the most cost effective way to purchase our programmable logic. By shifting the burdens to Monolithic Memories, who can handle large volumes easily, you can concentrate your energies on more productive projects.

How Does MMI Do This?

Monolithic Memories takes your proven PAL device design and either arranges to program ProPAL devices in volume, or generates a custom mask for a HAL or ZHAL device. And all without the normal risks inherent in purchasing a semicustom product. Why? Because:

- You can prototype your system and initiate production using standard Monolithic Memories PAL devices. You don't have to worry about making a mistake that could put your design schedule in jeopardy.
- The nominal Non-Recurring Engineering (NRE) charges for ProPAL and HAL devices are far lower than those normally required for a semicustom circuit. And they can even be amortized over your first production quantity.



- You save on the costs of programming devices. This will also shorten your production cycle, since you can plug the devices into the socket with no additional processing.
- All of the devices are tested for full functionality before they leave Monolithic Memories. You save on the costs of testing and generating test programs.
- Monolithic Memories is geared towards providing volumes of high quality devices. No one knows how to test programmable logic as well as Monolithic Memories. Between the thorough, efficient testing and marking capabilities and the option to provide burn-in for extra reliability, you can obtain a higher quality device that if you did the programming and testing yourself.
- MMI can provide custom marking. This saves you the added expense of stripping the mark from standard devices and then remarking them with your own mark.
- HAL devices are secure by design. If you prefer ProPAL devices, they can also be secured for you at the factory.
- ProPAL device lead time is only 1 to 2 weeks longer than that of unprogrammed PAL devices.
- HAL device turn-around time is a mere 6 to 8 weeks or less from acceptance of your design package to receipt of first units.
- If you find yourself with an unexpected demand, you need not turn away business for lack of HAL device stock. You can always use ProPAL devices to make up for any temporary shortfall.

How Can You Take Advantage of This?

The following are some guidelines which you can use to help convert your designs to ProPAL, HAL or ZHAL devices.

1. Send in Your Design

You will need to provide your logic equations from either PALASM® PALASM 2 or ABEL™ on magnetic media*.

When Monolithic Memories generates vectors for use in functionally testing your pattern, "seed" vectors are helpful in providing the foundation upon which the final test vectors will be based.

A master PAL device containing your design is needed for Monolithic Memories to verify that the pattern you submitted has been correctly processed. If you cannot provide a Monolithic Memories master PAL device, Monolithic Memories will accept your design inputs and provide ProPAL samples for your approval.

For your convenience, a checklist is included to help you prepare all of the necessary materials to be submitted to Monolithic Memories. This will also help Monolithic Memories process your design, resulting in smoother and faster turn-around. Copies of this form are available from your Sales Representative, or you can simply copy the attached form.

2. MMI Will Verify the Design

Upon receiving your design package, Monolithic Memories will enter your design into their computer and verify that there are no format or syntax problems. A fuse map will be generated, and sample ProPAL devices programmed.

If any questions are encountered at this stage, they will be resolved with you before any further processing takes place.

3. MMI Will Check the Samples

If you have approved immediate production of your devices, Monolithic Memories will make a fuse for fuse comparison between the samples and the master device you provide. If there are no discrepancies, test generation will be started immediately (or upon receipt of your purchase order).

If you prefer to see programmed sample ProPAL devices prior to initiating production, Monolithic Memories can provide them for your approval before proceeding further. Sample approval is also needed when no master devices are provided or when a discrepancy is found during verification.

4. MMI Will Generate Test Vectors

A functional test sequence is generated using TGEN™, a proprietary software package. Any seed vectors you provide will be used to help initiate test generation. TGEN will check for hazards and race conditions, monitor fault coverage and systematically add vectors until test coverage goals are met.

Monolithic Memories has a test quality standard that sets as a minimum goal 90% coverage of all stuck-at faults. Lower coverage patterns can sometimes be processed as HAL devices, or it is possible to handle them as ProPAL devices only, but your approval will be needed. If acceptable coverage cannot be obtained, ways of increasing the testability of the design may have to be considered before Monolithic Memories can process the pattern.

For more detail on exactly how the test coverage is determined, refer to the article "PAL Design Function and Test Vectors" in the Monolithic Memories Programmable Logic Handbook.

When suitable test coverage is obtained, as is normally the case, there is no need for you to be involved with vector generation. If, however, you wish to approve the test vectors before production units are generated, the vectors will be made available to you.

5. MMI Will Generate Production Units

After an acceptable test sequence has been generated, Monolithic Memories will generate the appropriate HAL or ZHAL mask and build the devices. Or, in the case of a ProPAL device, Monolithic Memories will arrange to program and test blank units.

Having Your Devices Marked

The standard Monolithic Memories mark consists of the device type, the package type, the date code, and the Monolithic Memories logo.

If you wish, you can have the standard marking replaced by a custom marking. The logo and date code are standard, but any other markings can be as you desire. The character and line limitations for the most common packages are in Table 1.

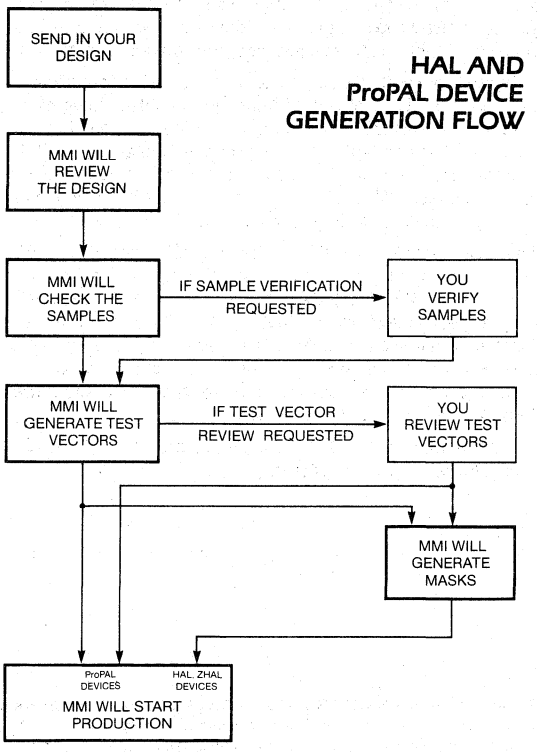
If the package you want is not listed, your local representative can help you determine the guidelines you need.

Whom to Contact

When you are ready to put the power of the Monolithic Memories factory to work for you, just contact your local Monolithic Memories sales representative. And let Monolithic Memories take care of your production programming, testing, and marking needs.

Table 1.

PLASTIC	20 pin (300 mil)	2 lines/13 characters per line
	24 pin (300 mil)	2 lines/17 characters per line
CERDIP	20 pin (300 mil)	2 lines/16 characters per line
	24 pin (300 mil)	2 lines/17 characters per line
PLCC	20 lead	4 lines/11 characters per line
	28 lead	5 lines/12 characters per line



Zero Power CMOS Hard Array Logic ZHAL™ 20A Series

Patent Pending

Features/Benefits

- Zero standby power
- 25-ns maximum propagation delay
- HC and HCT compatible
- Space saving PLCC available
- Low power alternative for Small and Medium 20-pin PAL® devices, including 16L8/16R8/16R6/16R4

Description

The Zero Power Hard Array Logic (ZHAL) devices are ideal in low-power applications that require high-speed operation. These attributes are achieved through the use of Monolithic Memories' advanced high-speed CMOS process. Now system designers have the option of using a ZHAL device that matches fast PAL device speeds, but with the added advantage of zero standby power. These features are ideal for power-critical areas such as portable digital equipment or lap-top computers.

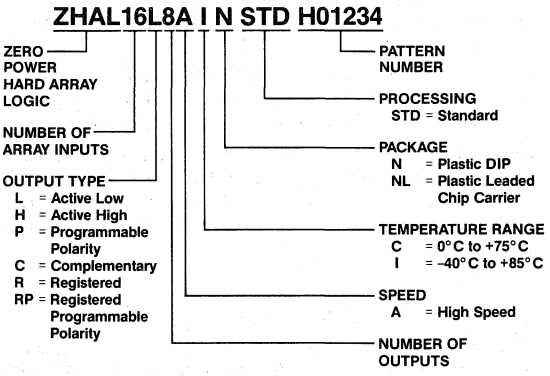
This family of ZHAL devices utilizes a unique architecture that is designed for a high degree of flexibility in implementing most patterns of the listed 20-pin PAL/HAL® devices. Prototyping can be done using standard PAL devices before converting to ZHAL circuits for production. ZHAL devices are fabricated by Monolithic Memories with custom metallization masks defined by a user-supplied HAL Design Specification.

The procedures for designing with Monolithic Memories' ZHAL devices are shown in the flow chart on page 8. The ZHAL20 option in the PALASM®2 CAD package will confirm whether a design specification will fit within the ZHAL20 architecture. For more information on the ZHAL20 software, refer to the PALASM 2 User Manual. For more information on the ZHAL device generation flow, see the Monolithic Memories brochure "ProPAL™, HAL®, and ZHAL Devices."

For evaluation of the ZHAL20A circuit, sample patterns are available. See page 6 for details.

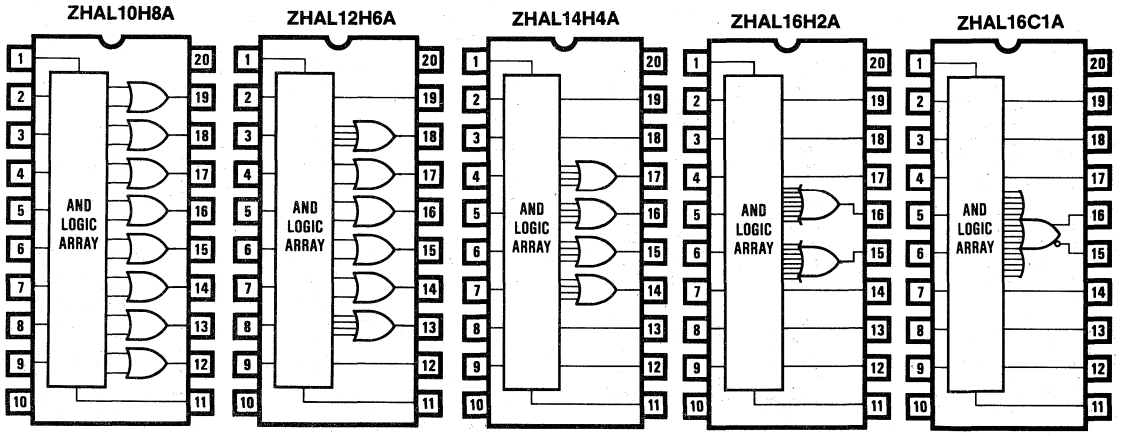
Ordering Information

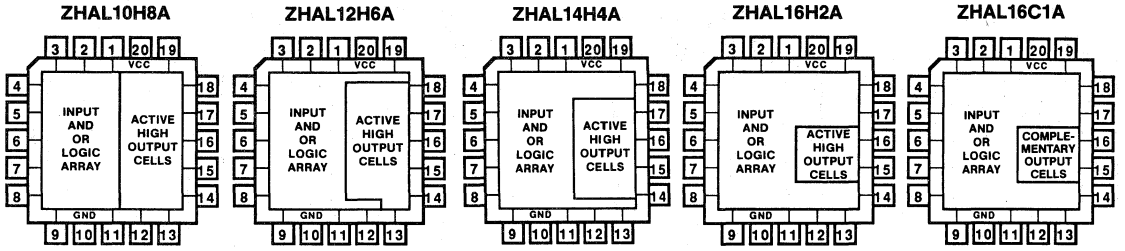
PART NUMBER	PACKAGE	ARRAY	OUTPUTS	
			COMB	REG
ZHAL10H8A	N, NL	10	8	—
ZHAL12H6A		12	6	—
ZHAL14H4A		14	4	—
ZHAL16H2A		16	2	—
ZHAL16C1A		16	2	—
ZHAL10L8A		10	8	—
ZHAL12L6A		12	6	—
ZHAL14L4A		14	4	—
ZHAL16L2A		16	2	—
ZHAL16L8A	N, NL	16	8	—
ZHAL16R8A		16	—	8
ZHAL16R6A		16	2	6
ZHAL16R4A		16	4	4
ZHAL16P8A	N, NL	16	8	—
ZHAL16RP8A		16	—	8
ZHAL16RP6A		16	2	6
ZHAL16RP4A		16	4	4



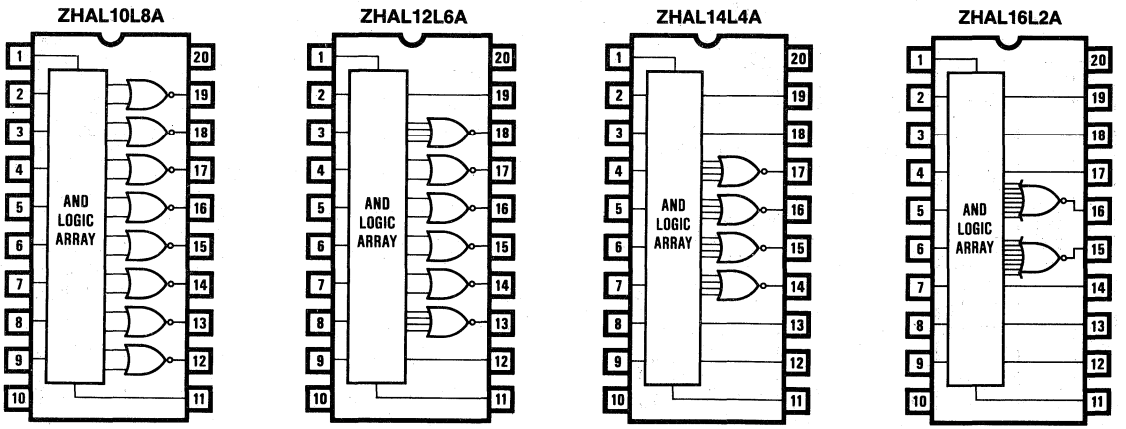
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

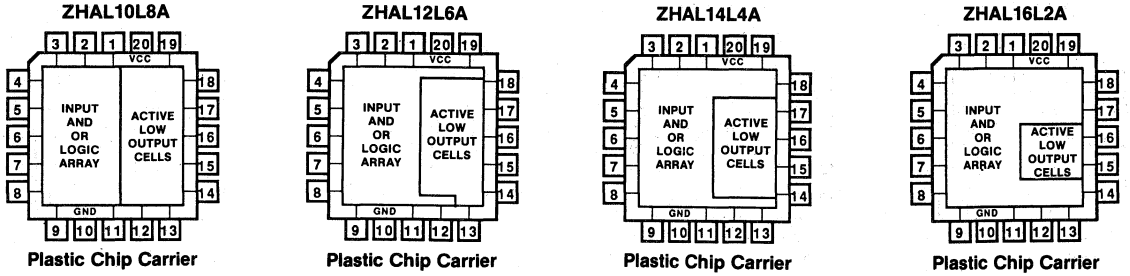
Monolithic Memories





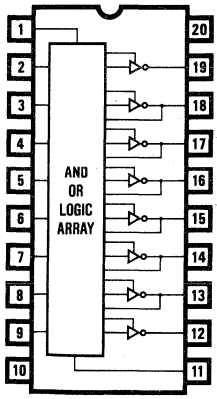
Plastic Chip Carrier | Plastic Chip Carrier | Plastic Chip Carrier | Plastic Chip Carrier | Plastic Chip Carrier



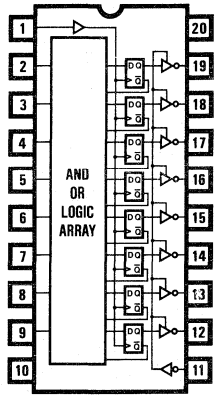


Plastic Chip Carrier | Plastic Chip Carrier | Plastic Chip Carrier | Plastic Chip Carrier

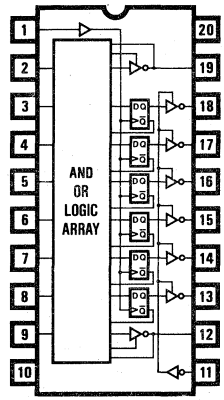
ZHAL16L8A



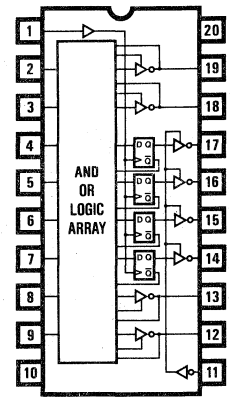
ZHAL16R8A



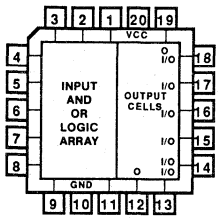
ZHAL16R6A



ZHAL16R4A

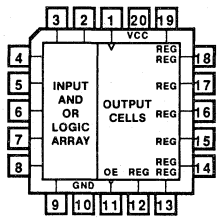


ZHAL16L8A



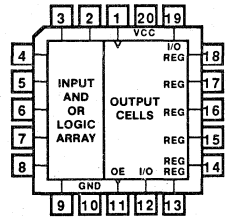
Plastic Chip Carrier

ZHAL16R8A



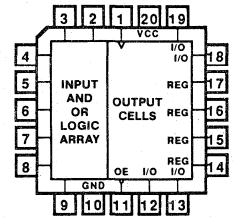
Plastic Chip Carrier

ZHAL16R6A



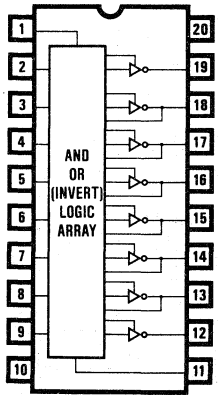
Plastic Chip Carrier

ZHAL16R4A

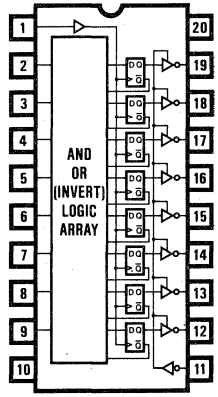


Plastic Chip Carrier

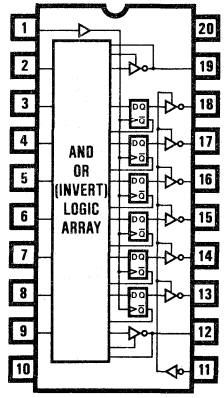
ZHAL16P8A



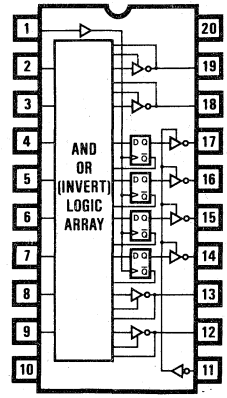
ZHAL16RP8A



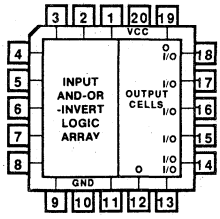
ZHAL16RP6A



ZHAL16RP4A

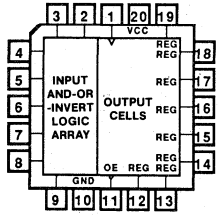


ZHAL16P8A



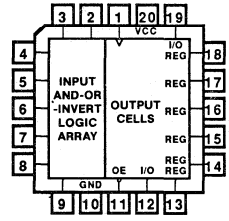
Plastic Chip Carrier

ZHAL16RP8A



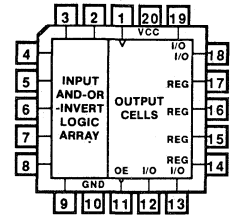
Plastic Chip Carrier

ZHAL16RP6A



Plastic Chip Carrier

ZHAL16RP4A



Plastic Chip Carrier

Operating Conditions

SYMBOL	PARAMETER		INDUSTRIAL MIN	TYP	MAX	COMMERCIAL MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	16R4A, 16R6A, 16R8A, 16RP4A, 16RP6A, 16RP8A	15	10		15	10		ns
t_{su}	Setup time from input or feedback to clock		20	13		20	13		ns
t_h	Hold time		0	−10		0	−10		ns
T_A	Operating free-air temperature		−40	25	85	0	25	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}[1]	Low-level input voltage				0		0.8	V
V_{IH}[1]	High-level input voltage				2		V_{CC}	V
I_{IL}	Low-level input current		V_{CC} = MAX	V_I = GND			−1	μA
I_{IH}	High-level input current	Pin 8[2]	V_{CC} = MAX	V_I = V_{CC}		1	10	μA
		All other pins					1	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN	I_{OL} = 8 mA		0.1	0.4	V
			V_{CC} = 5 V	I_{OL} = 1 μA			0.05	
V_{OH}	High-level output voltage		V_{CC} = MIN	I_{OH} = −6 mA	3.76[3]	4.1		V
			V_{CC} = 5 V	I_{OH} = −1 μA	4.95			
I_{OZL}[3]	Off-state output current		V_{CC} = MAX	V_O = GND		0	−10	μA
I_{OZH}[3]				V_O = V_{CC}		0	10	μA
I_{CC}	Standby supply current[4]		I_O = 0 mA, V_I = GND or V_{CC}			0	100	μA
	Operating supply current		f = 1 MHz, I_O = 0 mA, V_I = GND or V_{CC}			2	5[5]	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS (See Test Load)	INDUSTRIAL MIN	TYP	MAX	COMMERCIAL MIN	TYP	MAX	UNIT
t_{PD}	Input or feedback to output 10H8A, 12H6A, 14H4A, 16H2A, 16C1A, 10L8A, 12L6A, 14L4A 16L2A, 16L8A, 16R6A, 16R4A, 16P8A, 16RP6A, 16RP8A		R_L = 1 KΩ C_L = 50 pF		15	25		15	25	ns
t_{CLK}	Clock to output or feedback 16R4A, 16R6A, 16R8A, 16RP4A, 16RP6A, 16RP8A				10	15		10	15	ns
t_{PZX}	Input to output enable	16L8A, 16R4A, 16R6A, 16P8A, 16RP4A, 16RP6A			12	25		12	25	ns
t_{PXZ}[6]	Input to output disable				14	25		14	25	ns
t_{PXZ}[6] t_{PZX}	Pin 11 to output disable/enable	16R4A, 16R6A, 16R8A, 16RP4A, 16RP6A, 16RP8A			12	15		12	15	ns
f_{MAX}	Maximum frequency			28.5	40		28.5	40		MHz

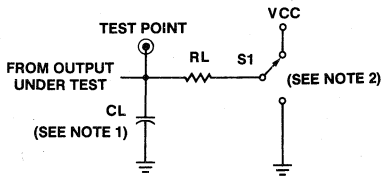
Notes: Apply to electrical and switching characteristics.

1. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. Pin 8 (PRELOAD pin). Applies to all devices whether registered or non-registered.
3. JEDEC standard no. 7 for high-speed CMOS devices.
4. Disable output pins = V_{CC} or GND.
5. Add 3 mA per additional 1.0 MHz of operation over 1 MHz.
6. C_L = 5 pF.

Absolute Maximum Ratings

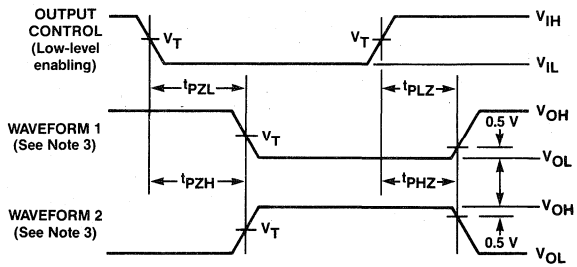
Supply voltage, V_{CC} ..... −0.5 V to 7 V
DC input voltage, V_I ..... −0.5 V to V_{CC} +0.5 V
DC output voltage, V_O ..... −0.5 V to V_{CC} +0.5 V
DC output source/sink current per output pin, I_O ..... ±35 mA
DC V_{CC} or ground current, I_{CC} or I_{GND} ..... ±100 mA
Input diode current, I_{IK}:
V_I<0 ..... −20 mA
V_I>V_{CC} ..... +20 mA
Output diode current, I_{OK}:
V_O<0 ..... −20 mA
V_O>V_{CC} ..... +20 mA
Storage temperature ..... −65°C to 150°C

Switching Test Load

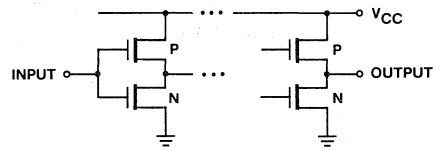


Notes: 1. CL includes probe and jig capacitance.
2. When measuring t_{PLZ} and t_{PZL}, S1 is tied to V_{CC}.
When measuring t_{PHZ} and t_{PZH}, S1 is tied to ground.
t_{PZX} is measured with C_L = 50 pF. t_{PXZ} is measured with C_L = 5 pF.
When measuring propagation delay times of 3-state outputs, S1 is open, i.e., not connected to V_{CC} or ground.
3. Waveform 1 is for an output with internal conditions such that the output is Low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is High except when disabled by the output control.

Enable/Disable Delay



Schematic of Inputs and Outputs

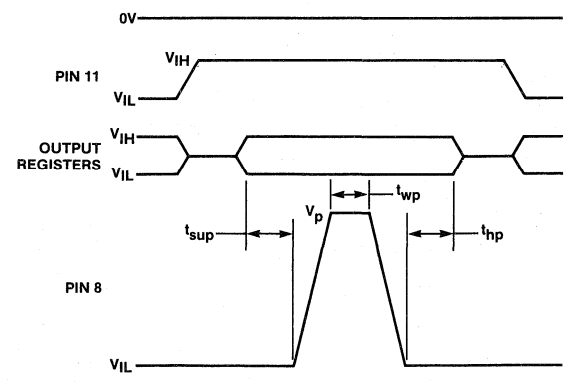


Output Register PRELOAD†

The PRELOAD function allows the register to be loaded from data placed on the output pins. This feature aids functional testing of state sequencer designs by allowing direct setting of output states for improved test coverage. The procedure for PRELOAD is as follows:

1. Raise V_{CC} to 4.5 V.
2. Disable output registers by setting pin 11 to V_{IH}. Set pin 1 to 0 V.
3. Apply V_{IL}/V_{IH} to all registered output pins.
4. Pulse pin 8 to V_p (12 V), then back to 0 V.
5. Remove V_{IL}/V_{IH} from all registered output pins.
6. Lower pin 11 to V_{IL} to enable the output registers.
7. Verify for V_{OL}/V_{OH} at all registered output pins.

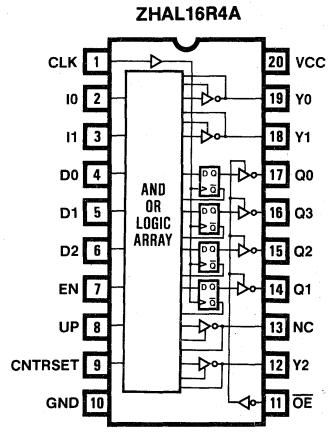
† Note: Only applies to parts with output registers.
Typical t_{sup} = 50 ns
t_{wp} = 100 ns
t_{hp} = 50 ns
I_{IH} = 30 μA (Pin 8)



Features/Benefits

- **Demonstrates all features of ZHAL20A product**
- **4-bit up/down counter with reset**
- **3-bit shifter**
- **25-ns maximum propagation delay**
- **Zero standby power**

Logic Symbol



Description

The ZHAL20A Evaluation Pattern is provided as an example of the features and characteristics of the ZHAL20A Series products.

This design consists of two functionally independent patterns: a 4-bit up/down counter and a 3-bit shifter. The 4-bit counter can count up or count down and has reset capability. These features are controlled by two control signals: UP and CNTRSET (Count Reset). When UP is high, the counter counts up. When UP is low, the counter counts down. CNTRSET overrides the count function and resets the counter to all ones, synchronous with the clock.

The 3-bit shifter shifts data bits by 0, 1 or 2 positions. The three bits of the shifter are enabled when EN (enable) is high, and are disabled (high-Z) when EN is low.

The PALASM®2 software file and simulation results are shown on the next page. Below are the function tables that summarize the functions of the counter and the shifter.

Counter Function Table

$\overline{OE}$	UP	CNTRSET	CLK	Q3-Q0	OPERATION
H	X	X	X	Z	High-Z
L	H	L	↑	Q plus 1	Increment
L	L	L	↑	Q minus 1	Decrement
L	X	H	↑	High	Reset

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance (off) state
↑ = LOW-to-HIGH clock transition

Shifter Function Table

EN	I1	I0	Y2	Y1	Y0	OPERATION
L	X	X	Z	Z	Z	High-Z
H	L	L	$\overline{D2}$	$\overline{D1}$	$\overline{D0}$	No operation
H	L	H	$\overline{D0}$	$\overline{D2}$	$\overline{D1}$	Shift by one
H	H	L	$\overline{D1}$	$\overline{D0}$	$\overline{D2}$	Shift by two

PALASM Design Specification

```
TITLE    PDS CONVERSION FILE
PATTERN  EXAMPLE
REVISION 1.00
AUTHOR   JOHN DOE
COMPANY  MONOLITHIC MEMORIES, INC
DATE     9/23/85

CHIP zzz PAL16RP4 CLK I0 I1 D0 D1 D2 EN UP CNTRSET GND
                  /OE Y2 NC Q1 Q2 Q3 Q0 Y1 Y0 VCC

EQUATIONS

 Y0 = /I1*/I0*/D0
    + /I1* I0*/D1
    +  I1*/I0*/D2
 Y0.TRST = EN

 Y1 = /I1*/I0*/D1
    + /I1* I0*/D2
    +  I1*/I0*/D0
 Y1.TRST = EN

 Y2 = /I1*/I0*/D2
    + /I1* I0*/D0
    +  I1*/I0*/D1
 Y2.TRST = EN


Q0 :=/Q0
    + CNTRSET

Q1 :=/Q1* Q0* UP
    + Q1* Q0*/UP
    + Q1*/Q0* UP
    +/Q1*/Q0*/UP
    + CNTRSET

Q2 := CNTRSET
    +/Q2*/Q1*/Q0*/UP
    + Q2*/Q1*     UP
    + Q2* Q1*/Q0
    +/Q2* Q1* Q0* UP
    + Q2*     Q0*/UP

Q3 := CNTRSET
    + Q3*          Q0*/UP
    +/Q3*/Q2*/Q1*/Q0*/UP
    +/Q3* Q2* Q1* Q0* UP
    + Q3* Q2*/Q1
    + Q3*     /Q1*     UP
    + Q3*/Q2* Q1
    + Q3*     Q1*/Q0
```

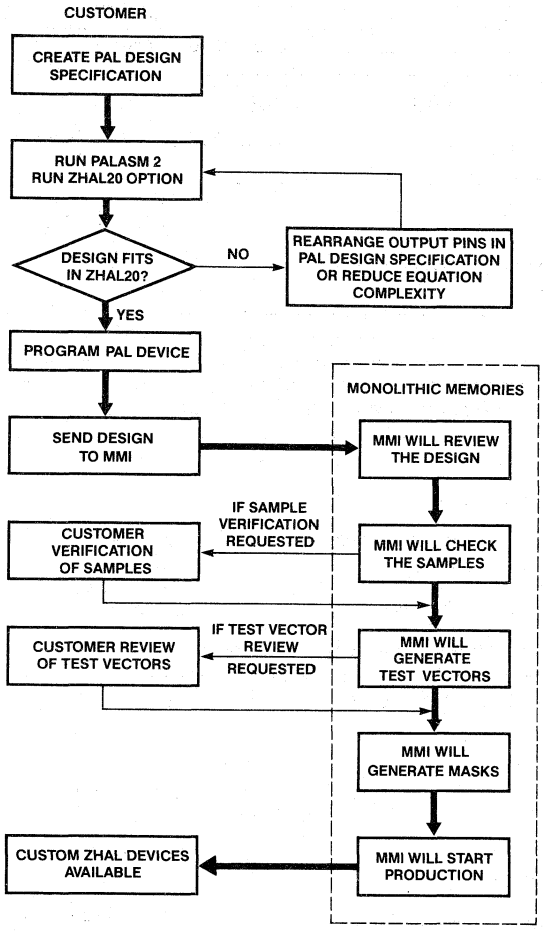
Simulation Results

```
PALASM SIMULATION HISTORY LISTING

ZZZ
Page :  1
          g g  cg cg  cg cgcgcg cgcgcgcgcg cgcgcgcgc
 CLK      LLLLHLLHLL HLLHLHLHLH LHLHLHLHLH LHLHLHLHL
 I0       XXLLLLLLLH HHLLLLLLLL LLLLLLLLLL LLLLLLLLL
 I1       XXLLLLLLLL LLHHHHHHHH HHHHHHHHHH HHHHHHHHH
 D0       XXLLLLLLLH HHLLLLLLLL LLLLLLLLLL LLLLLLLLL
 D1       XXLLLLLLLL LLHHHHHHHH HHHHHHHHHH HHHHHHHHH
 D2       XXLLLLLLLH HHLLLLLLLL LLLLLLLLLL LLLLLLLLL
 EN       LLHHHHHHHH HHHHHHHHHH HHHHHHHHHH HHHHHHHHH
 UP       XXXXXXHHHH HHHHHHHHHH HHHHHHHHHH HHHHHHHHH
 CNTRSET  XXHHHHLLLL LLLLLLLLLL LLLLLLLLLL LLLLLLLLL
 GND      LLLLLLLLLL LLLLLLLLLL LLLLLLLLLL LLLLLLLLL
/OE       HHLLLLLLLL LLLLLLLLLL LLLLLLLLLL LLLLLLLLL
 Y2       XZHHHHHHHL LLLLLLLLLL LLLLLLLLLL LLLLLLLLL
 Q1       ZZXXXHHHLL LLLLHHHHLL LLHHHHLLLL HHHHLLLLH
 Q2       ZZXXXHHHLL LLLLLLLLHH HHHHHHLLLL LLLLHHHHH
 Q3       ZZXXXHHHLL LLLLLLLLLL LLLLLLHHHH HHHHHHHHH
 Q0       ZZXXXHHHLL LHHHLLHHLL HHLLHHLLHH LLHHLLHHL
 Y1       XZHHHHHHHL LLHHHHHHHH HHHHHHHHHH HHHHHHHHH
 Y0       XZHHHHHHHH HHHHHHHHHH HHHHHHHHHH HHHHHHHHH
 VCC      HHHHHHHHHH HHHHHHHHHH HHHHHHHHHH HHHHHHHHH
```

Simulation File

```
SIMULATION

TRACE_ON CLK I0 I1 D0 D1 D2 EN UP CNTRSET /OE Y2 Q1 Q2 Q3 Q0 Y1 Y0

SETF /CLK /OE /EN

SETF OE EN /I1 /I0 /D2 /D1 /D0 Y2 Y1 Y0 CNTRSET
CLOCKF CLK

CHECK Q3 Q2 Q1 Q0

SETF /I1 /I0 /D2 /D1 /D0 Y2 Y1 Y0 /CNTRSET UP
CLOCKF CLK

CHECK /Q3 /Q2 /Q1 /Q0

SETF /I1 I0 D2 /D1 D0 /Y2 /Y1 Y0
CLOCKF CLK

CHECK /Q3 /Q2 /Q1 Q0

SETF I1 /I0 /D2 D1 /D0 /Y2 Y1 Y0
CLOCKF CLK

CHECK /Q3 /Q2 Q1 /Q0

SETF OE /CNTRSET UP
CLOCKF CLK

CHECK /Q3 /Q2 Q1 Q0

SETF OE /CNTRSET UP
CLOCKF CLK

CHECK /Q3 Q2 /Q1 /Q0

SETF OE /CNTRSET UP
CLOCKF CLK

CHECK /Q3 Q2 /Q1 Q0

SETF OE /CNTRSET UP
CLOCKF CLK

CHECK /Q3 Q2 Q1 /Q0

SETF OE /CNTRSET UP
CLOCKF CLK

CHECK /Q3 Q2 Q1 Q0

SETF OE /CNTRSET UP
CLOCKF CLK

CHECK Q3 /Q2 /Q1 /Q0

SETF OE /CNTRSET UP
CLOCKF CLK

CHECK Q3 /Q2 /Q1 Q0

SETF OE /CNTRSET UP
CLOCKF CLK

CHECK Q3 /Q2 Q1 /Q0

SETF OE /CNTRSET UP
CLOCKF CLK

CHECK Q3 /Q2 Q1 Q0

SETF OE /CNTRSET UP
CLOCKF CLK

CHECK Q3 Q2 /Q1 /Q0

SETF OE /CNTRSET UP
CLOCKF CLK

CHECK Q3 Q2 /Q1 Q0

SETF OE /CNTRSET UP
CLOCKF CLK

CHECK Q3 Q2 Q1 /Q0

TRACE_OFF
```

ZHAL 20A Device Generation Flow



Company name: _____
Address: _____
_____
Contact: _____ Phone Number: _____

Do you want: ___ HAL ___ ProPAL ___ ZHAL

Part Type: _____ Customer Part Number: _____

What package type do you want? _____

How do you want the devices marked?
- — Standard
- — Custom mark: please specify the mark below.
  Refer to page 6-5

_____
_____
_____

For ProPAL devices, do you want the security fuse blown? _____

Design Specification Format:

___ PALASM ___ PALASM 2 ___ ABEL

Input medium:
(Choose 1 of 3)

1. 9-track Magnetic_Tape
   ___ card image
   ___ files-11
   ___ VAX VMS backup
2. Floppy_Disk
   ___ RT-11
   ___ RSX-11M
   ___ IBM PC
3. ___ PALASM printout (signed and dated)

The following items are requested but not required. Please check if provided:

___Seed vectors
___Master PAL device

OPTIONS

A. ___ I want to start production immediately (or upon submittal of purchase order) if:
   1. Design is acceptable;
   2. MMI samples match my master device fuse for fuse;
   3. Minimum test coverage goals are met.

   (Master device must be provided.)

B. ___ I want to verify the MMI generated sample devices prior to production implementation.

___ I want to approve the test vectors prior to production implementation.

Please complete this form for each pattern submitted to Monolithic Memories, and include it in your design package.

Submitted by: _____ Date: _____
Title: _____

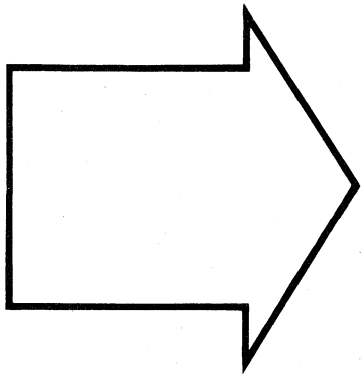


Table of Contents

SYSTEM BUILDING BLOCKS/HMSI™ SELECTION GUIDE

System Building Blocks/HMSI Selection Guide

FUNCTION	PART NUMBER
8-Bit Counter	SN54/74LS461A
8-Bit Up/Down Counter	SN54/74LS469A
10-Bit Counter	SN54/74LS491A
16:1 Mux	SN54/74LS450
Dual 8:1 Mux	SN54/74LS451
Quad 4:1 Mux	SN54/74LS453
Increment and Skip Counter	671492
2-Digit BCD Counter	671493
8-Bit Priority Encoder with Register	5/671494

8-Bit Counter
SN54/74LS461A

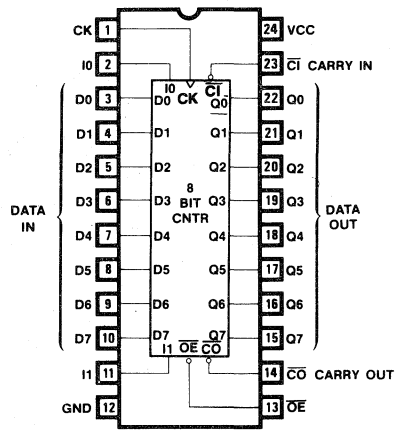
Features/Benefits

- **8-bit counter for microprogram-counter, DMA-controller and general-purpose counting applications**
- **8 bits match byte boundaries**
- **Bus-structured pinout**
- **24-pin SKINNYDIP® saves space**
- **Three-state outputs drive bus lines**
- **Low-current PNP inputs reduce loading**
- **Expandable in 8-bit increments**

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN54LS461A	JS, W, 28L	Mil
SN74LS461A	NS, JS	Com

Logic Symbol



Description

The 'LS461A is an 8-bit synchronous counter with parallel load, clear, and hold capability. Two function select inputs (I0, I1) provide one of four operations which occur synchronously on the rising edge of the clock (CK).

The LOAD operation loads the inputs (D7-D0) into the output register (Q7-Q0). The CLEAR operation resets the output register to all LOWs. The HOLD operation holds the previous value regardless of clock transitions. The INCREMENT operation adds one to the output register when the carry-in input is TRUE ($\overline{CI}$ = LOW), otherwise the operation is a HOLD. The carry-out ($\overline{CO}$) is TRUE ($\overline{CO}$ = LOW) when the output register (Q_7-Q_0) is all HIGHs, otherwise FALSE ($\overline{CO}$ = HIGH).

The data output pins are enabled when $\overline{OE}$ is LOW, and disabled (HI-Z) when $\overline{OE}$ is HIGH. The output drivers will sink the 24 mA required for many bus interface standards.

Two or more 'LS461A 8-bit counters may be cascaded to provide larger counters. The operation codes were chosen such that when I1 is HIGH, I0 may be used to select between LOAD and INCREMENT as in a program counter (JUMP/INCREMENT).

Function Table

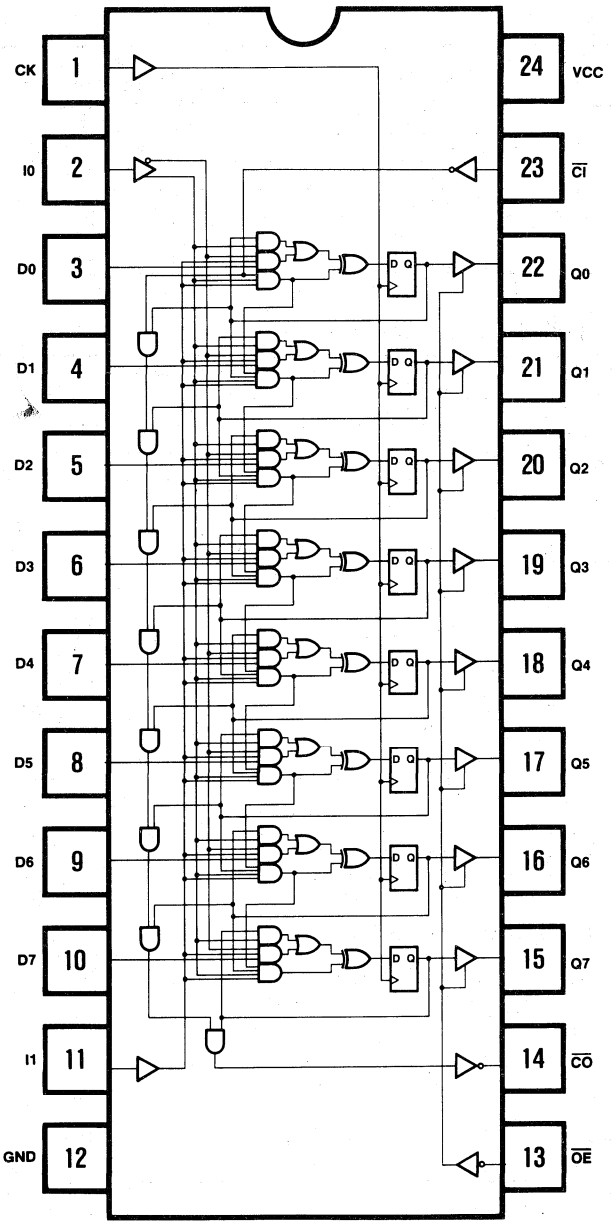
$\overline{OE}$	CK	I1	I0	CI	D7-D0	Q7-Q0	OPERATION
H	*	*	*	*	*	Z	HI-Z*
L	↑	L	L	X	X	L	CLEAR
L	↑	L	H	X	X	Q	HOLD
L	↑	H	L	X	D	D	LOAD
L	↑	H	H	H	X	Q	HOLD
L	↑	H	H	L	X	Q plus 1	INCREMENT

* When $\overline{OE}$ is HIGH, the three-state outputs are disabled to the high-impedance states; however, sequential operation of the counter is not affected.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374
Monolithic Memories

Logic Diagram

8-Bit Counter



Absolute Maximum Ratings

Supply voltage V_{CC} ..... 7 V
Input voltage ..... 5.5 V
Off-state output voltage ..... 5.5 V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP†	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP†	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		−55		125*	0		75	°C
t_w	Width of clock	Low	35	15		25	15		ns
		High	20	7		15	7		
t_{su}	Setup time		40	20		30	20		ns
t_h	Hold time		0	−15		0	−15		

* Case temperature

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IL}**	Low-level input voltage						0.8	V
V_{IH}**	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA			−0.8	−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			−0.02	0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4 V				25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, V_{IH} = 2 V	Mil	I_{OL} = 12 mA		0.3	0.5	V
			Com	I_{OL} = 24 mA				
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, V_{IH} = 2 V	Mil	I_{OH} = −2 mA	2.4	2.8		V
			Com	I_{OH} = −3.2 mA				
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8 V, V_{IH} = 2 V		V_O = 0.4 V			−100	μA
I_{OZH}				V_O = 2.4 V			100	
I_{OS}	Output short-circuit current*	V_{CC} = 5.0 V		V_O = 0 V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX				140	180	mA

* No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

** V_{IL} and V_{IH} parameters are, in effect, input conditions of D.C. and functional output tests are not directly tested. V_{IL} is specified at ≤0.8 V and V_{IH} is specified at ≥2.0 V.

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

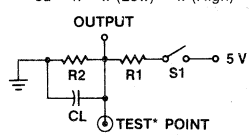
Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	MILITARY MIN	MILITARY TYP†	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP†	COMMERCIAL MAX	UNIT
f_{MAX}	Maximum clock frequency*	Commercial	16.6			25			MHz
t_{PD}	CI to CO delay	R_1 = 200 Ω		15	35		15	25	ns
t_{CLK}	Clock to Q	R_2 = 390 Ω		10	25		10	15	ns
t_{PD}	Clock to CO	Military		25	60		25	40	ns
t_{PZX}	Output enable delay	R_1 = 390 Ω		11	25		11	20	ns
t_{PXZ}	Output disable delay	R_2 = 750 Ω		10	25		10	20	ns

* f_{MAX} is derived from: 1/MAX [(t_{su} + t_h), $t_{w\ (Low)}$ + $t_{w\ (High)}$, t_{CLK}].

Test Load

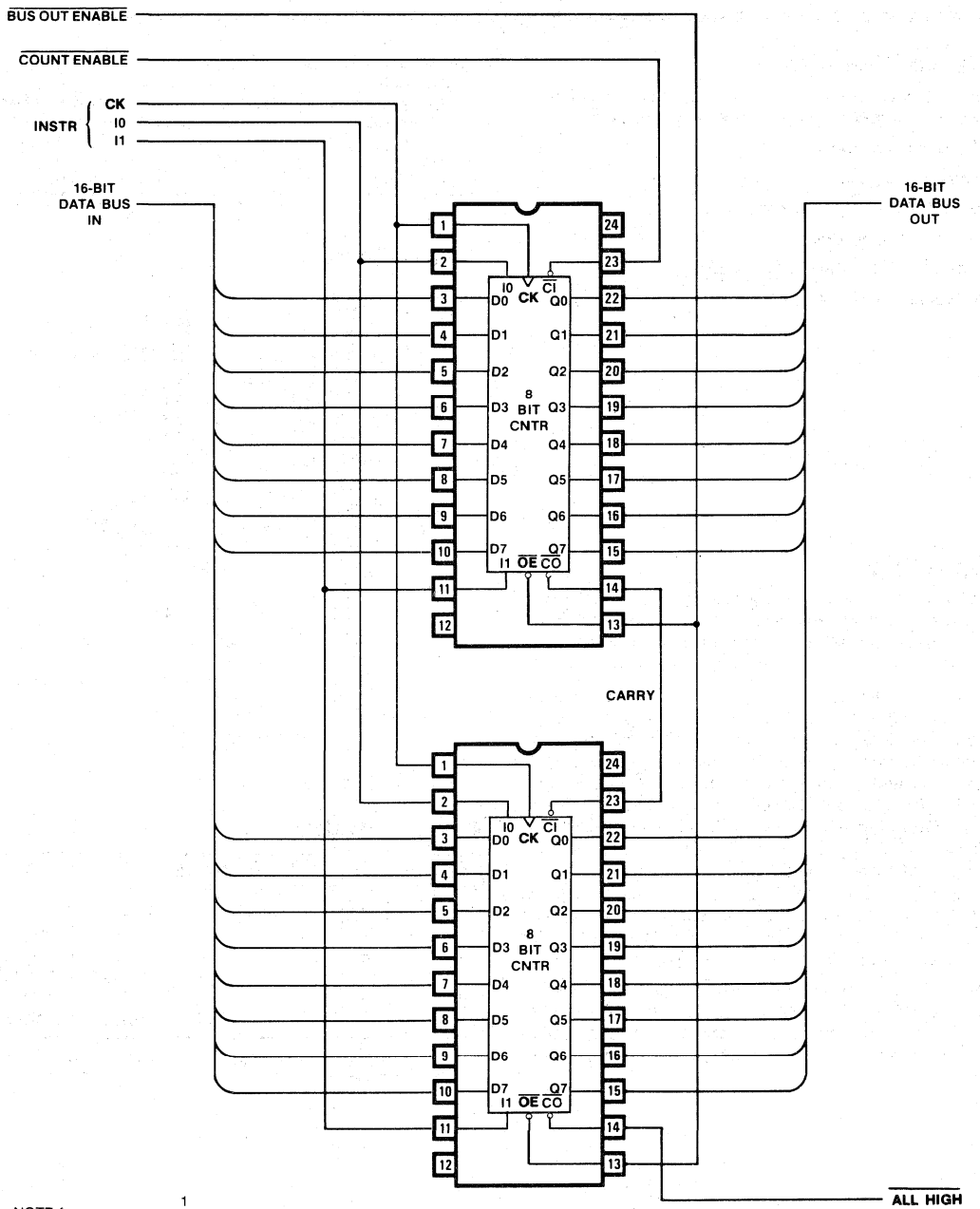
* The "Test Point" is driven by the outputs under test, and observed by instrumentation



Notes:
1. t_{PD} is tested with switch S_1 closed. C_L = 50 pF and measured at 1.5 V output level.
2. t_{PZX} is measured at the 1.5 V output level with C_L = 50 pF. S_1 is open for high impedance to "1" test, and closed for high impedance to "0" test.
3. t_{PXZ} is tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} −0.5 V output level; S_1 is closed for "0" to high impedance test measured at V_{OL} +0.5 V output level.

Application

16-Bit Counter



NOTE: $f_{MAX} = \frac{1}{t_{PD\ CLK\ TO\ CO} + t_{SU}}$

8-Bit Up/Down Counter
SN54/74LS469A

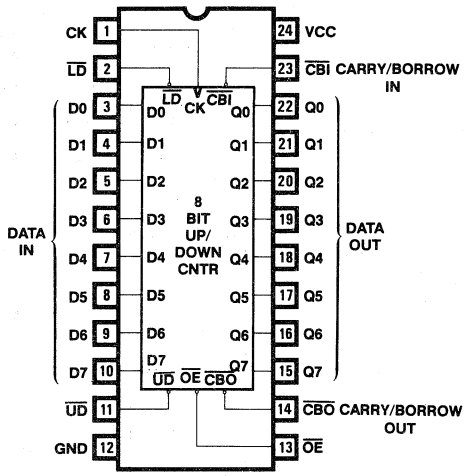
Features/Benefits

- **8-bit up/down counter for microprogram-counter, DMA-controller and general-purpose counting applications**
- **8 bits match byte boundaries**
- **Bus-structured pinout**
- **24-pin SKINNYDIP® saves space**
- **Three-state outputs drive bus lines**
- **Low-current PNP inputs reduce loading**
- **Expandable in 8-bit increments**

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN54LS469A	JS, W, 28L	Mil
SN74LS469A	NS, JS	Com

Logic Symbol



Description

The 'LS469A is an 8-bit synchronous up/down counter with parallel load and hold capability. Three function-select inputs ($\overline{LD}$, $\overline{UD}$, $\overline{CBI}$) provide one of four operations which occur synchronously on the rising edge of the clock (CK).

The LOAD operation loads the inputs (D7-D0) into the output register (Q7-Q0). The HOLD operation holds the previous value regardless of clock transitions. The INCREMENT operation adds one to the output register when the carry-in input is TRUE ($\overline{CBI}$ = LOW), and the up/down control line ($\overline{UD}$) is LOW, otherwise the operation is a HOLD. The carry-out ($\overline{CBO}$) is TRUE ($\overline{CBO}$ = LOW) when the output register (Q7-Q0) is all HIGHs, otherwise FALSE ($\overline{CBO}$ = HIGH). The DECREMENT operation subtracts one from the output register when the borrow-in input is TRUE ($\overline{CBI}$ = LOW), and the up/down control line ($\overline{UD}$) is HIGH, otherwise the operation is a HOLD. The borrow-out ($\overline{CBO}$) is TRUE ($\overline{CBO}$ = LOW) when the output register (Q7-Q0) is all LOWs, otherwise FALSE ($\overline{CBO}$ = HIGH).

The data output pins are enabled when $\overline{OE}$ is LOW, and disabled (HI-Z) when $\overline{OE}$ is HIGH. The output drivers will sink the 24 mA required for many bus-interface standards. Two or more 'LS469A 8-bit up/down counters may be cascaded to provide larger counters.

Function Table

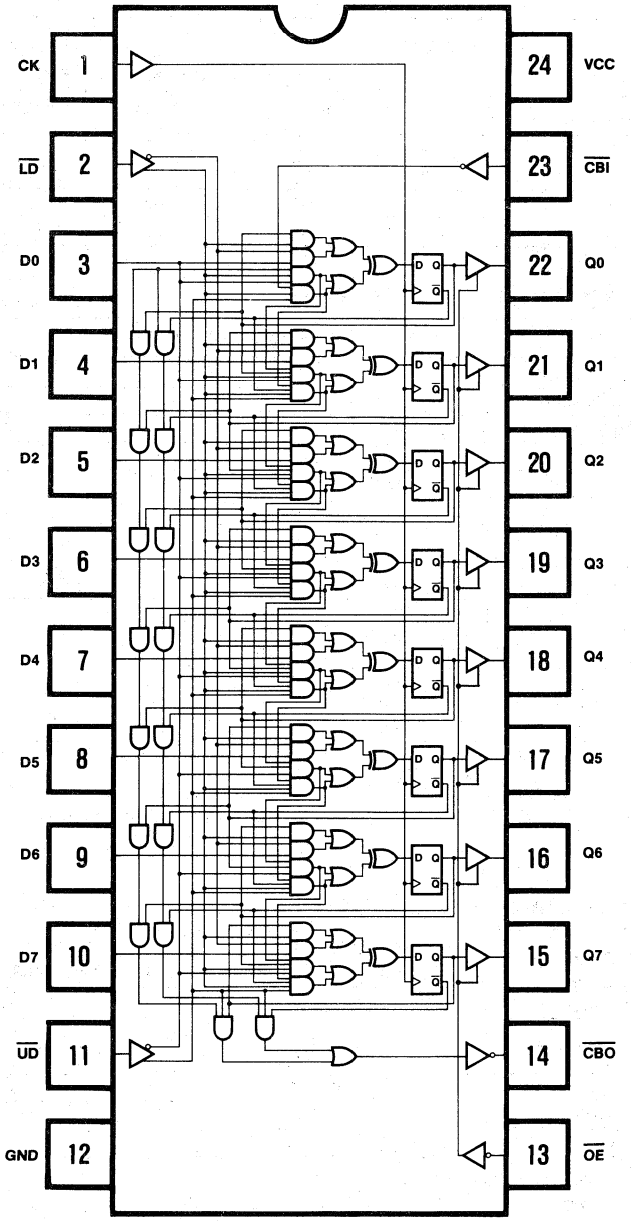
$\overline{OE}$	CK	$\overline{LD}$	$\overline{UD}$	$\overline{CBI}$	D7-D0	Q7-Q0	OPERATION
H	*	*	*	*	*	Z	HI-Z*
L	↑	L	X	X	D	D	LOAD
L	↑	H	L	H	X	Q	HOLD
L	↑	H	L	L	X	Q plus 1	INCREMENT
L	↑	H	H	H	X	Q	HOLD
L	↑	H	H	L	X	Q minus 1	DECREMENT

* When $\overline{OE}$ is HIGH, the three-state outputs are disabled to the high-impedance state; however, sequential operation of the counter is not affected.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories

Logic Diagram

8-Bit Up/Down Counter



Absolute Maximum Ratings

Supply voltage V_{CC} ..... 7.0 V
Input voltage ..... 5.5 V
Off-state output voltage ..... 5.5 V
Storage temperature ..... −65° to +150° C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP†	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP†	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		−55		125*	0		75	°C
t_w	Width of clock	Low	35	15		25	15		ns
		High	20	7		15	7		
t_{su}	Setup time		40	20		30	20		ns
t_h	Hold time		0	−15		0	−15		

* Case temperature

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IL}**	Low-level input voltage						0.8	V
V_{IH}**	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA			−0.8	−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			−0.02	0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4 V				25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, V_{IH} = 2 V	Mil	I_{OL} = 12 mA		0.3	0.5	V
			Com	I_{OL} = 24 mA				
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, V_{IH} = 2 V	Mil	I_{OH} = −2 mA	2.4	2.8		V
			Com	I_{OH} = −3.2 mA				
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8 V, V_{IH} = 2 V		V_O = 0.4 V			−100	μA
I_{OZH}				V_O = 2.4 V			100	
I_{OS}	Output short-circuit current*	V_{CC} = 5.0 V		V_O = 0 V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX				140	180	mA

* No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

** V_{IL} and V_{IH} parameters are, in effect, input conditions of D.C. and functional output tests are not directly tested. V_{IL} is specified at ≤0.8 V and V_{IH} is specified at ≥2.0 V.

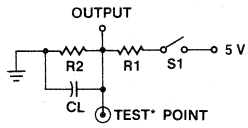
† All typical values are at V_{CC} = 5 V, T_A = 25°C.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	MILITARY MIN	MILITARY TYP†	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP†	COMMERCIAL MAX	UNIT
f_{MAX}	Maximum clock frequency*	Commercial	16.6			25			MHz
t_{PD}	CI to CO delay	R_1 = 200 Ω		15	35		15	25	ns
t_{CLK}	Clock to Q	R_2 = 390 Ω		10	25		10	15	ns
t_{PD}	Clock to CO	Military		25	60		25	40	ns
t_{PZX}	Output enable delay	R_1 = 390 Ω		11	25		11	20	ns
t_{PXZ}	Output disable delay	R_2 = 750 Ω		10	25		10	20	ns

* f_{MAX} is derived from: 1/MAX [(t_{su} + t_h), $t_{w\ (Low)}$ + $t_{w\ (High)}$, t_{CLK}].

Test Load

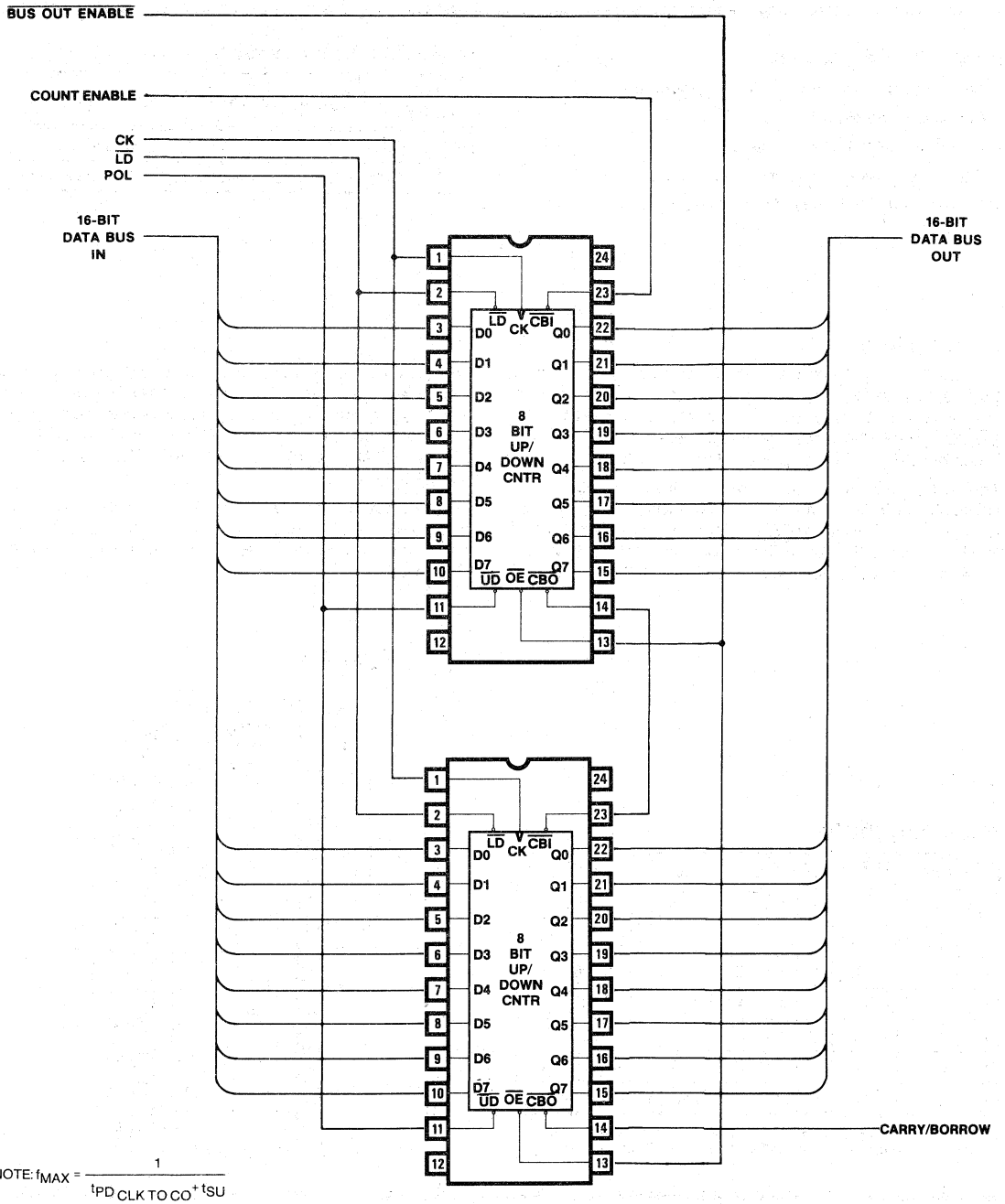


* The "Test Point" is driven by the outputs under test, and observed by instrumentation

Notes:
1. t_{PD} is tested with switch S_1 closed. C_L = 50 pF and measured at 1.5 V output level.
2. t_{PZX} is measured at the 1.5 V output level with C_L = 50 pF. S_1 is open for high impedance to "1" test, and closed for high impedance to "0" test.
3. t_{PXZ} is tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} −0.5 V output level; S_1 is closed for "0" to high impedance test measured at V_{OL} +0.5 V output level.

Application

16-Bit Up/Down Counter



NOTE: $f_{MAX} = \frac{1}{t_{PD\ CLK\ TO\ CO} + t_{SU}}$

10-Bit Counter
SN54/74LS491A

Features/Benefits

- **CRT vertical and horizontal timing generation**
- **Bus-structured pinout**
- **24-pin SKINNYDIP® saves space**
- **Three-state outputs drive bus lines**
- **Low-current PNP inputs reduce loading**

Ordering Information

PART NUMBER	TEMP	PACKAGE	DESCRIPTION
SN54LS491A	Mil	JS,W,L(28)	10.5 MHz Counter
SN74LS491A	Com	NS,JS,NL(28)	25 MHz Counter

Description

The 'LS491/A is a 10-bit up/down counter with set, load and hold capabilities for two LSB, two MSB and six middle bits that are HIGH or LOW as a group. Five control inputs (SET, $\overline{LD}$, $\overline{CNT}$, $\overline{CIN}$ and $\overline{UP}$) provide one of five operations which occur synchronously on the rising edge of the clock (CK).

The SET operation sets the output register (Q9-Q0) to all HIGHs. The LOAD operation loads the inputs (D9-D0) into the register. When COUNT or CARRY IN are not asserted ($\overline{CNT}$ = HIGH or $\overline{CIN}$ = HIGH), the HOLD operation holds the previous value regardless of clock transitions. The COUNT UP operation adds one to the output of the register when the count up input is asserted ($\overline{UP}$ = LOW). The COUNT DOWN operation subtracts one from the output register when the count up input is not asserted ($\overline{UP}$ = HIGH). SET overrides both LOAD and COUNT, LOAD overrides COUNT, and COUNT is conditional on CARRY IN.

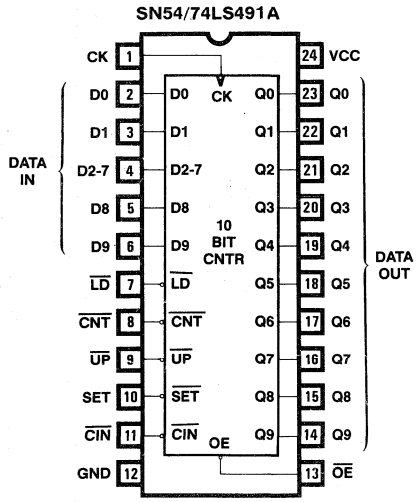
The data output pins are enabled when $\overline{OE}$ is LOW, and disabled (HI-Z) when $\overline{OE}$ is HIGH. The 24-mA I_{OL} outputs are suitable for driving RAM/PROM address lines in video graphics systems.

Function Table

$\overline{OE}$	CK	SET	$\overline{LD}$	$\overline{CNT}$	$\overline{CIN}$	$\overline{UP}$	D9-D0	Q9-Q0	OPERATION
H	*	*	*	*	*	*	*	Z	HI-Z*
L	↑	H	X	X	X	X	X	H	SET all HIGH
L	↑	L	L	X	X	X	D	D	LOAD D
L	↑	L	H	H	X	X	X	Q	HOLD
L	↑	L	H	L	H	X	X	Q	HOLD
L	↑	L	H	L	L	L	X	Q plus 1	COUNT UP
L	↑	L	H	L	L	H	X	Q minus 1	COUNT DN

* When $\overline{OE}$ is HIGH, the three-state outputs are disabled to the high-inpedance states; however, sequential operation of the counter is not affected.

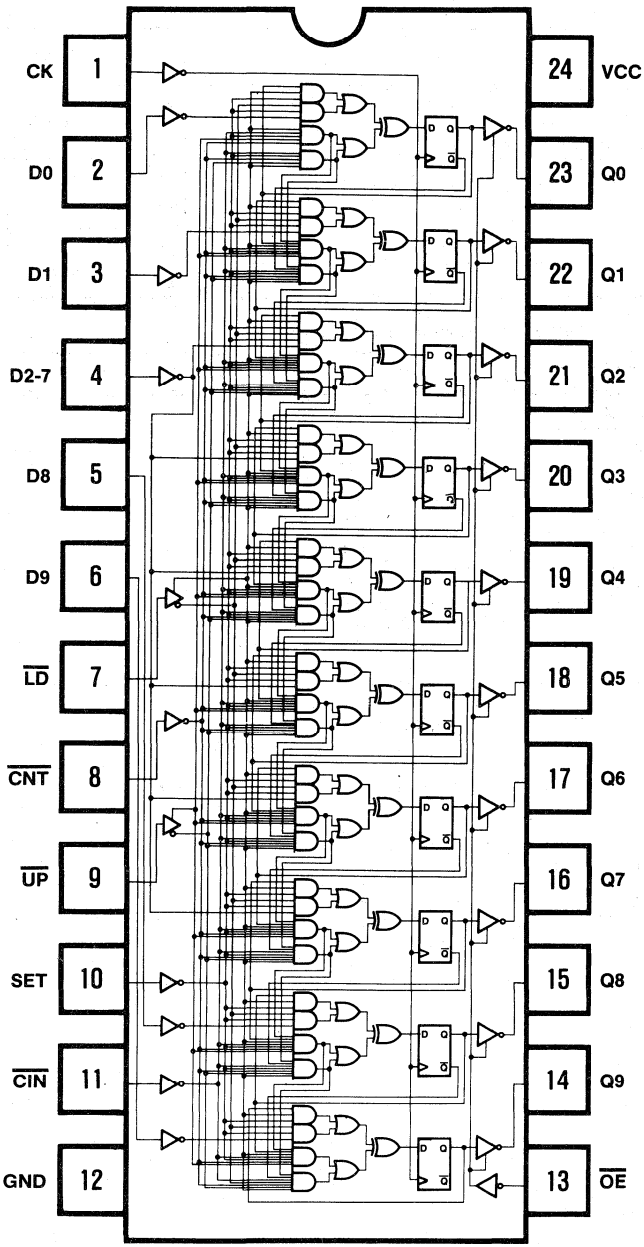
Logic Symbol



TWX: 910-338-2376
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
Monolithic Memories MMI

Logic Diagram

10-Bit Up/Down Counter



Absolute Maximum Ratings

Supply voltage V_{CC} ..... 7 V
Input voltage ..... 5.5 V
Off-state output voltage ..... 5.5 V
Storage temperature ..... −65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	COMMERCIAL TYP†	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		75	°C
t_w	Width of clock	High	15	7		ns
		Low	25	15		
t_{su}	Setup time		30	20		ns
t_h	Hold time		0	−15		ns

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}*	Low-level input voltage					0.8	V
V_{IH}*	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA			−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4 V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, V_{IH} = 2 V	I_{OL} = 24 mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, V_{IH} = 2 V	I_{OH} = −3.2 mA	2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8 V, V_{IH} = 2 V	V_O = 0.4 V			−100	μA
I_{OZH}			V_O = 2.4 V			100	μA
I_{OS}**	Output short-circuit current	V_{CC} = 5 V	V_O = 0 V	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX			120	180	mA

* V_{IL} ad V_{IH} parameters are, in effect, input conditions of D.C. and Functional output tests and are not directly tested. V_{IL} is specified at 0.8 V, and V_{IH} is specified at 2.0 V.

** Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

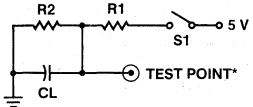
† All typical values are set at V_{CC} = 5 V, T_A = 25°C.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load)	MILITARY MIN	MILITARY TYP†	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP†	COMMERCIAL MAX	UNIT
f_{MAX}	Maximum counting frequency**	Commercial $R_1 = 200\ \Omega$ $R_2 = 390\ \Omega$ Mil $R_1 = 390\ \Omega$ $R_2 = 750\ \Omega$	15.3			25			MHz
t_{CLK}	Clock to Q			10	25		10	15	ns
t_{PZX}	Output enable delay			11	25		11	20	ns
t_{PXZ}	Output disable delay			10	25		10	20	ns

** f_{MAX} is derived from: 1/MAX [(t_{su} + t_h), t_w (High) + t_w (Low), t_{CLK}].

Test Load

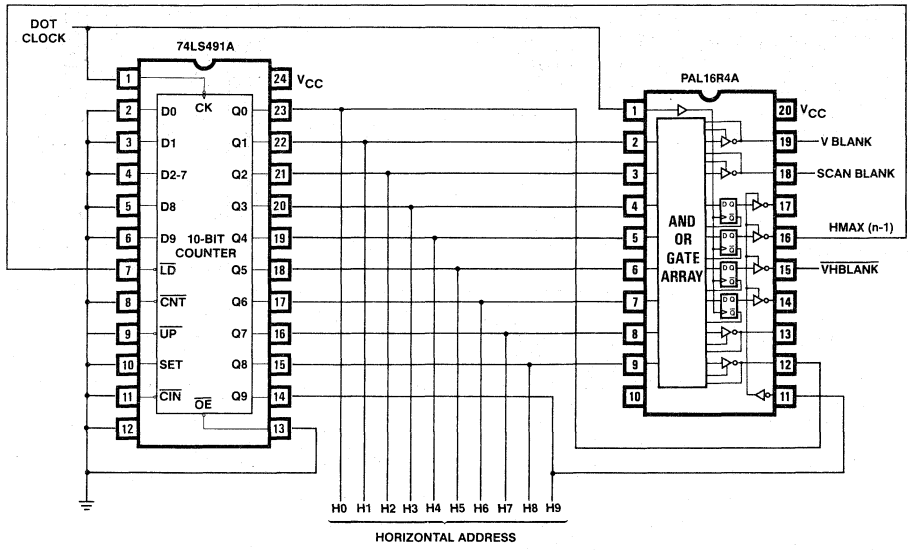


* The "Test Point" is driven by the outputs under test, and observed by instrumentation.

Notes: 1. t_{PD} is tested with switch S_1 closed. C_L = 50 pF and measured at 1.5 V output level.
2. t_{PZX} is measured at the 1.5 V output level with C_L = 50 pF. S_1 is open for high impedance to "1" test, and closed for high impedance to "0" test.
3. t_{PXZ} is tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} -0.5 V output level; S_1 is closed for "0" to high impedance test measured at V_{OL} +0.5 V output level.

Application

Video Horizontal Timing and Blanking



Timing Analysis:

Path 1 — Outputs of 74LS491A setting up at PAL16R4A inputs

$$t_{PD_{CK\text{-}Q/74LS491A}} + t_{SU_{PAL16R4A}} = 15\text{ ns} + 25\text{ ns} = 40\text{ ns}$$

Path 2 — Outputs of PAL16R4A setting up at 74LS491A inputs

$$t_{PD_{CK\text{-}Q/PAL16A}} + t_{SU_{74LS491A}} = 25\text{ ns} + 30\text{ ns} = 55\text{ ns}$$

Accordingly, the worst-case timing of the two paths is 55-ns, which results in a maximum video dot clock frequency of 18.18 MHz. Strict interpretation of the 60 Hz field rate NTSC Standard suggests that up to 52.1 μsec of time is available for active-raster-line duration. In practice however, most CRT monitors overscan the screen to correct horizontal sweep nonlinearities. As a consequence, the horizontal blanking time is increased, and the active video time decreased, typically to about 40 μsec. For the application circuit shown above, over 512 dots (pixels) for one line can be displayed:

$$\frac{40\ \mu\text{sec per line}}{55\text{ ns per pixel per line}} = 727\text{ pixels}$$

Normally, at least a 10-bit counter is required to provide a video timing chain for such resolutions. The 74LS491A combined with a high-speed PAL® (PAL16R4A) is capable of generating a complete set of video timing signals. Note that in the application circuit, the maximum horizontal count [H MAX (n-1)] is decoded one clock early, due to the 1-level pipelining used to obtain circuit speed.

16:1 Mux
SN54/74LS450

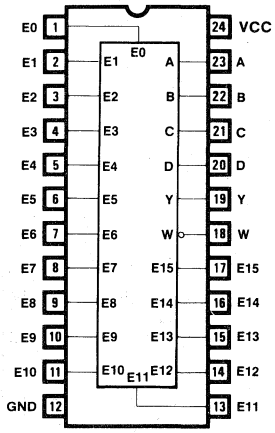
Features/Benefits

- 24-pin SKINNYDIP® saves space
- Similar to SN5/74150
- Low-current PNP inputs reduce loading

Ordering Information

PART NUMBER	PACKAGE		TEMPERATURE
SN54LS450	JS, W	28L	Mil
SN74LS450	NS, JS		Com

Logic Symbol



Description

The 16:1 Mux selects one of sixteen inputs, E0 through E15, specified by four binary select inputs, A, B, C and D. The true data is output on Y and the inverted data on W. Propagation delays are the same for both inputs and addresses and are specified for 50 pF loading. Outputs conform to the standard 8 mA LS totem-pole drive standard.

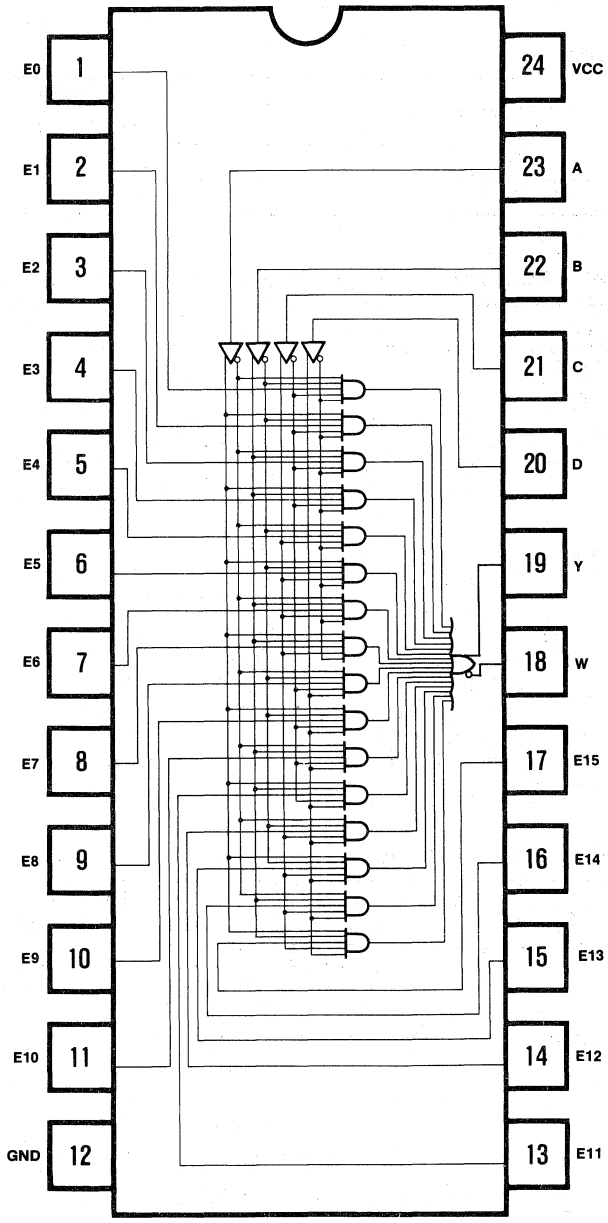
Function Table

INPUT SELECT				OUTPUT	
D	C	B	A	W	Y
L	L	L	L	$\overline{E0}$	E0
L	L	L	H	$\overline{E1}$	E1
L	L	H	L	$\overline{E2}$	E2
L	L	H	H	$\overline{E3}$	E3
L	H	L	L	$\overline{E4}$	E4
L	H	L	H	$\overline{E5}$	E5
L	H	H	L	$\overline{E6}$	E6
L	H	H	H	$\overline{E7}$	E7
H	L	L	L	$\overline{E8}$	E8
H	L	L	H	$\overline{E9}$	E9
H	L	H	L	$\overline{E10}$	E10
H	L	H	H	$\overline{E11}$	E11
H	H	L	L	$\overline{E12}$	E12
H	H	L	H	$\overline{E13}$	E13
H	H	H	L	$\overline{E14}$	E14
H	H	H	H	$\overline{E15}$	E15

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories

Logic Diagram

16:1 Mux



Absolute Maximum Ratings

Supply voltage V_{CC} ..... 7.0 V
Input voltage ..... 5.5 V
Off-state output voltage ..... 5.5 V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125*	0		75	°C

* Case temperature.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = −18mA			−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX		V_I = 0.4V			0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V		I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	Mil	I_{OH} = −2mA	2.4			V
			Com	I_{OH} = −3.2mA				
I_{OS}	Output short-circuit current*	V_{CC} = 5.0V		V_O = 0V	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX				60	100	mA

* No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

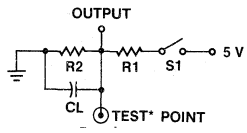
† All typicals values are at V_{CC} = 5 V, T_A = 25°C.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load)	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Any input to Y or W	C_L = 50 pF R_1 = 560Ω R_2 = 1.1kΩ		25	45		25	40	ns

Test Load

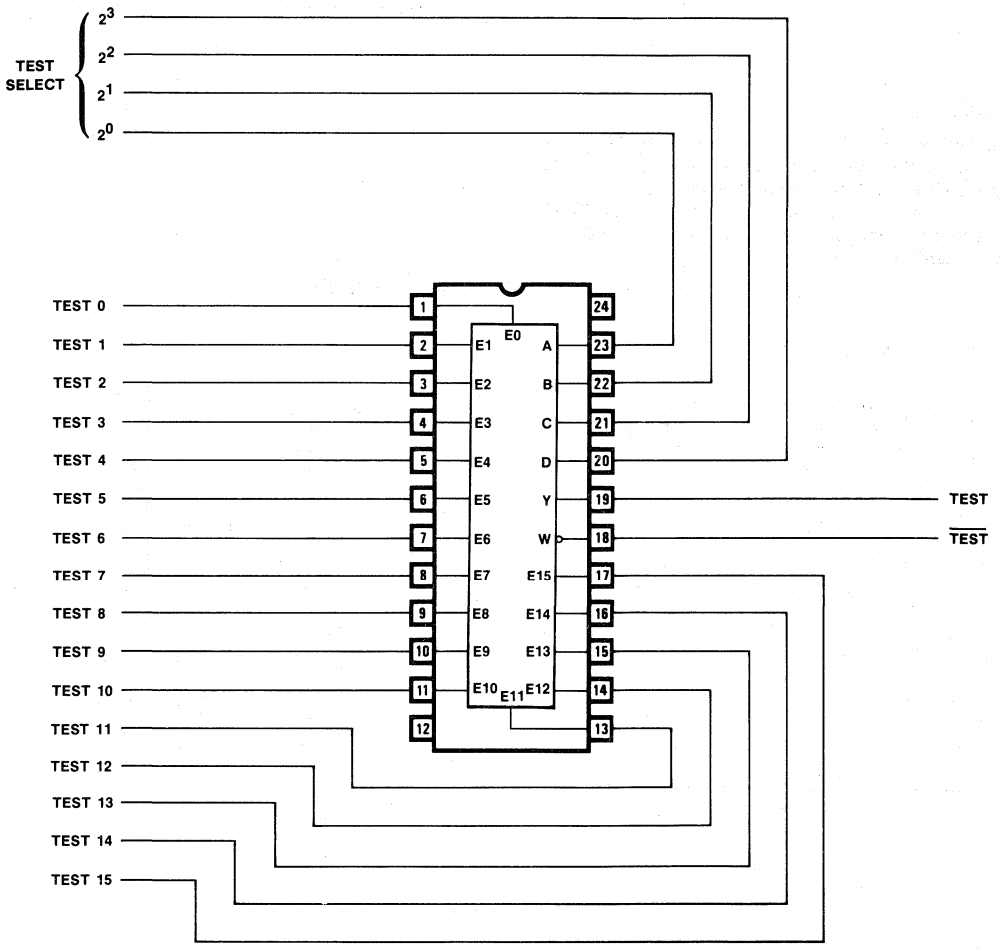
* The "Test Point" is driven by the outputs under test, and observed by instrumentation



Notes: 1. t_{PD} is tested with switch S_1 closed. C_L = 50 pF and measured at 1.5 V output level.
2. t_{PZX} is measured at the 1.5 V output level with C_L = 50 pF. S_1 is open for high impedance to "1" test, and closed for high impedance to "0" test.
3. t_{PXZ} is tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} −0.5 V output level; S_1 is closed for "0" to high impedance test measured at V_{OL} +0.5 V output level.

Application

Test Condition Mux



Dual 8:1 Mux
SN54/74LS451

Features/Benefits

- 24-pin SKINNYDIP® saves space
- Twice the density of SN5/741S151
- Low-current PNP inputs reduce loading

Ordering Information

PART NUMBER	PACKAGE		TEMPERATURE
SN54LS451	JS, W	28L	Mil
SN74LS451	NS, JS		Com

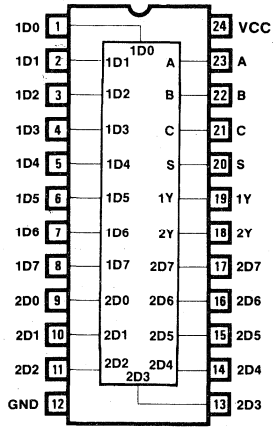
Description

The Dual 8:1 Mux selects one of eight inputs, D0 through D7, specified by three binary select inputs, A, B and C. The true data is output on Y when strobed by S. Propagation delays are the same for inputs, addresses and strobes and are specified for 50 pF loading. Outputs conform to the standard 8 mA LS totem-pole drive standard.

Function Table

INPUTS				OUTPUTS
SELECT			STROBE	Y
C	B	A	S	
X	X	X	H	H
L	L	L	L	D0
L	L	H	L	D1
L	H	L	L	D2
L	H	H	L	D3
H	L	L	L	D4
H	L	H	L	D5
H	H	L	L	D6
H	H	H	L	D7

Logic Symbol



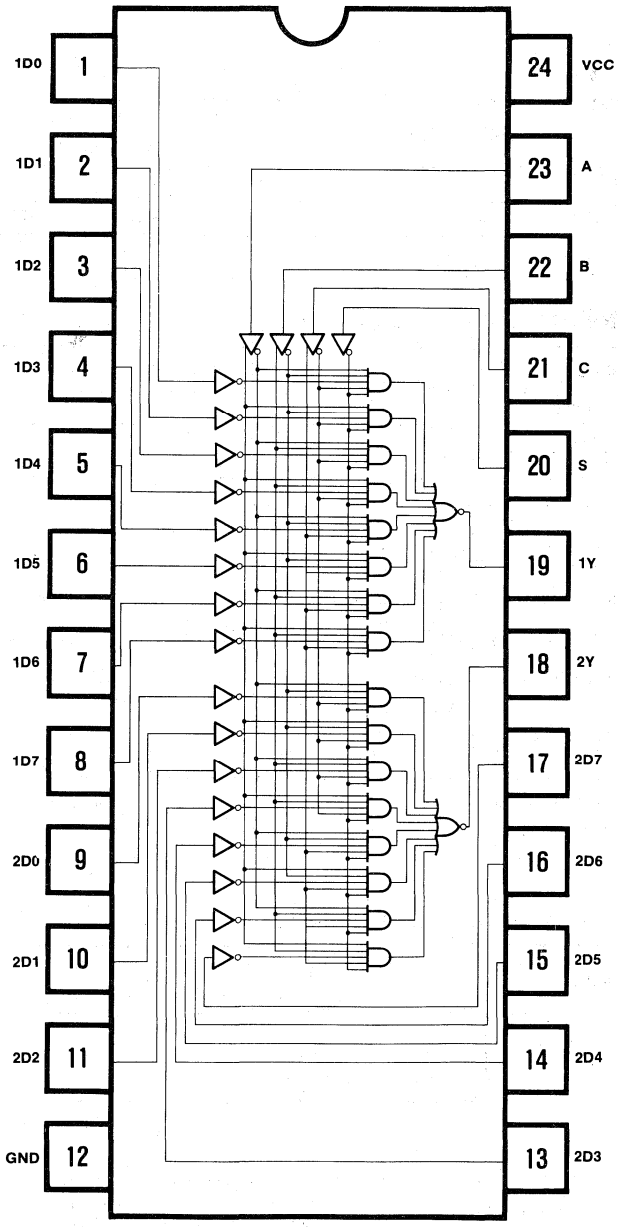
SKINNYDIP® is a registered trademark of Monolithic Memories.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Monolithic Memories MMI

Logic Diagram

Dual 8:1 Mux



Absolute Maximum Ratings

Supply voltage V_{CC} ..... 7.0 V
Input voltage ..... 5.5 V
Off-state output voltage ..... 5.5 V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125*	0		75	°C

* Case temperature.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = −18mA			−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX		V_I = 0.4V			0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V		I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	Mil	I_{OH} = −2mA	2.4			V
			Com	I_{OH} = −3.2mA				
I_{OS}	Output short-circuit current*	V_{CC} = 5.0V		V_O = 0V	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX				60	100	mA

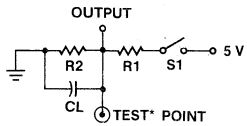
* No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† All typicals values are at V_{CC} = 5 V, T_A = 25°C.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load)	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Any input to Y	C_L = 50 pF R_1 = 560Ω R_2 = 1.1kΩ		25	45		25	40	ns

Test Load

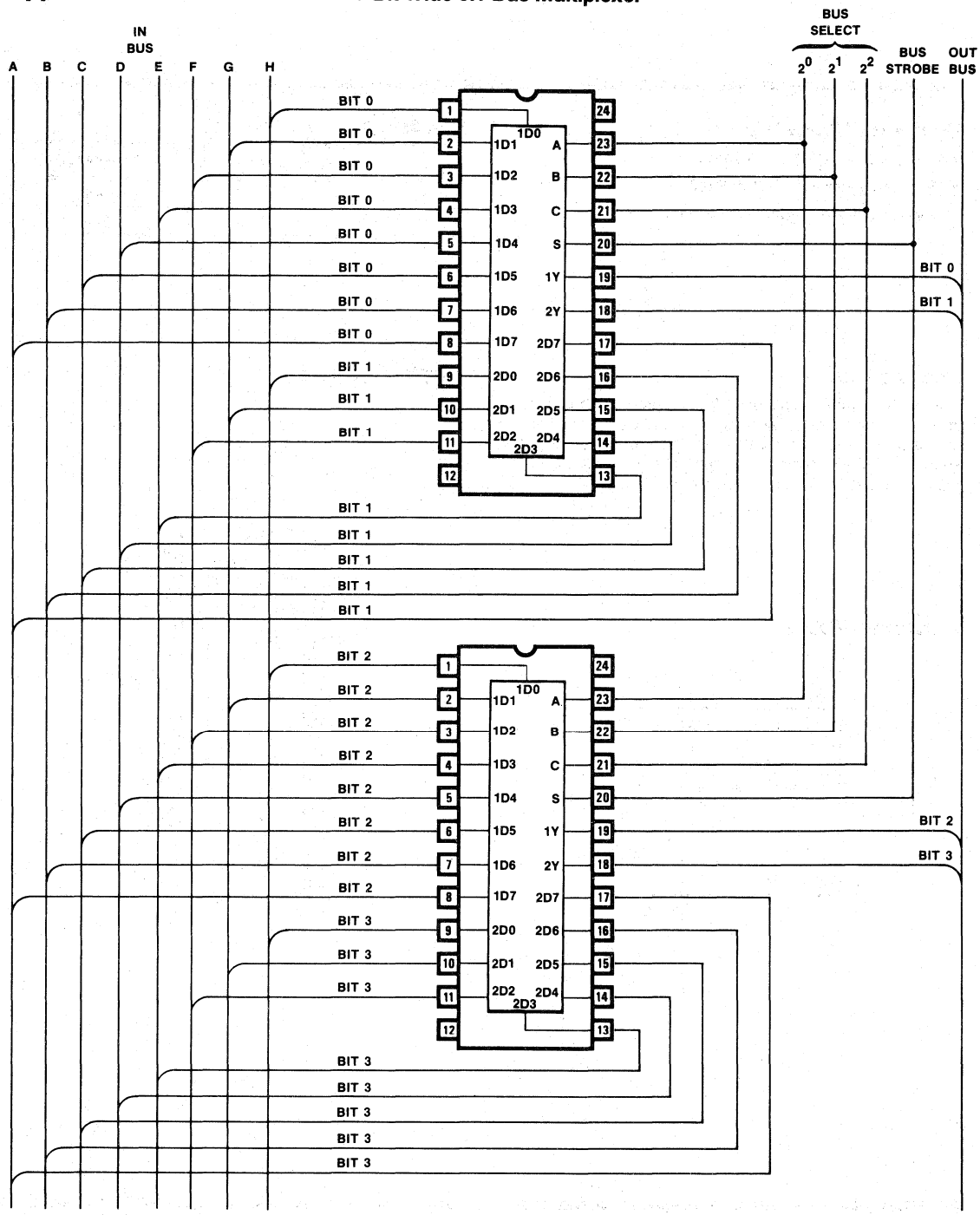


* The "Test Point" is driven by the outputs under test, and observed by instrumentation

Notes: 1. t_{PD} is tested with switch S_1 closed. C_L = 50 pF and measured at 1.5 V output level.
2. t_{PZX} is measured at the 1.5 V output level with C_L = 50 pF. S_1 is open for high impedance to "1" test, and closed for high impedance to "0" test.
3. t_{PXZ} is tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} −0.5 V output level; S_1 is closed for "0" to high impedance test measured at V_{OL} +0.5 V output level.

Application

4-Bit Wide 8:1 Bus Multiplexer



Quad 4:1 Mux
SN54/74LS453

Features/Benefits

- 24-pin SKINNYDIP® saves space
- Twice the density of SN5/74LS153
- Low-current PNP inputs reduce loading

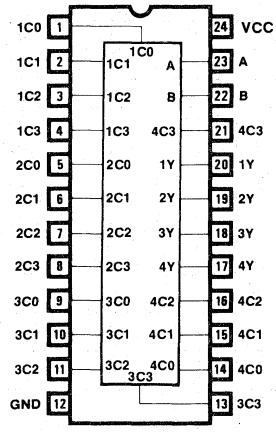
Ordering Information

PART NUMBER	PACKAGE		TEMPERATURE
SN54LS453	JS, W	28L	Mil
SN74LS453	NS, JS		Com

Description

The Quad 4:1 Mux selects one of four inputs, C0 through C3, specified by two binary select inputs, A and B. The true data is output on Y. Propagation delays are the same for inputs and addresses and are specified for 50 pF loading. Outputs conform to the standard 8 mA LS totem-pole drive standard.

Logic Symbol



Function Table

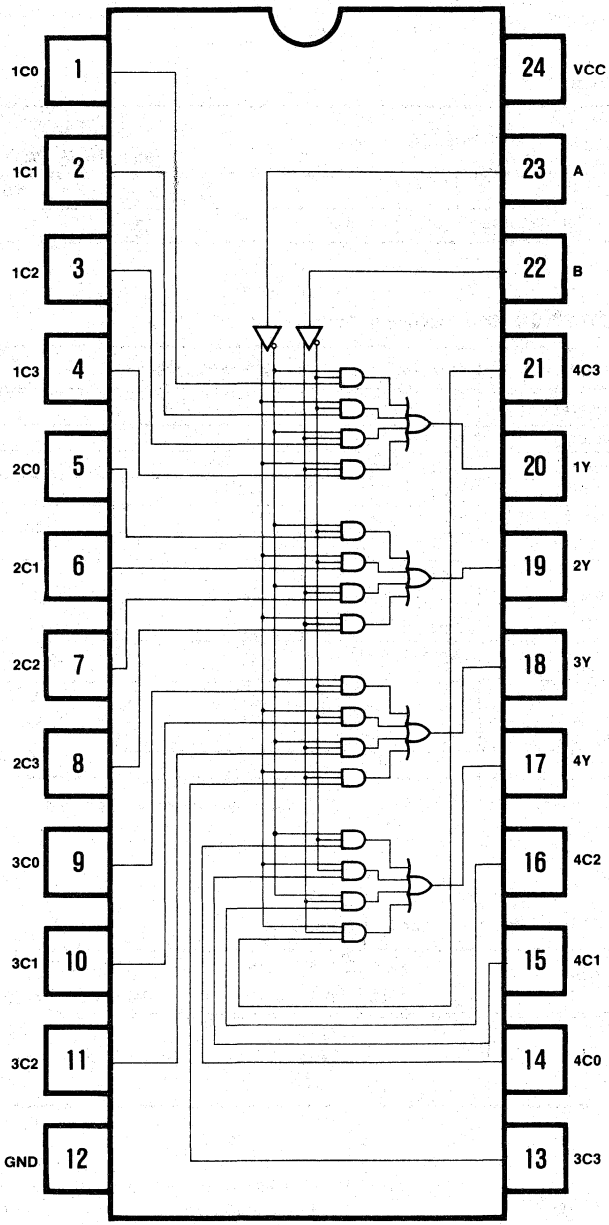
INPUT SELECT		OUTPUTS Y
B	A	
L	L	C0
L	H	C1
H	L	C2
H	H	C3

SKINNYDIP® is a registered trademark of Monolithic Memories.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories

Logic Diagram

Quad 4:1 Mux



Absolute Maximum Ratings

Supply voltage V_{CC} ..... 7.0 V
Input voltage ..... 5.5 V
Off-state output voltage ..... 5.5 V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125*	0		75	°C

* Case temperature.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA				−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V				0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4V				25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V		I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	Mil	I_{OH} = −2mA	2.4			V
			Com	I_{OH} = −3.2mA				
I_{OS}	Output short-circuit current*	V_{CC} = 5.0V		V_O = 0V	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX				60	100	mA

* No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

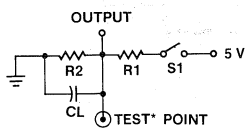
† All typicals values are at V_{CC} = 5 V, T_A = 25°C.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load)	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Any input to Y	C_L = 50 pF R_1 = 560Ω R_2 = 1.1kΩ		25	45		25	40	ns

Test Load

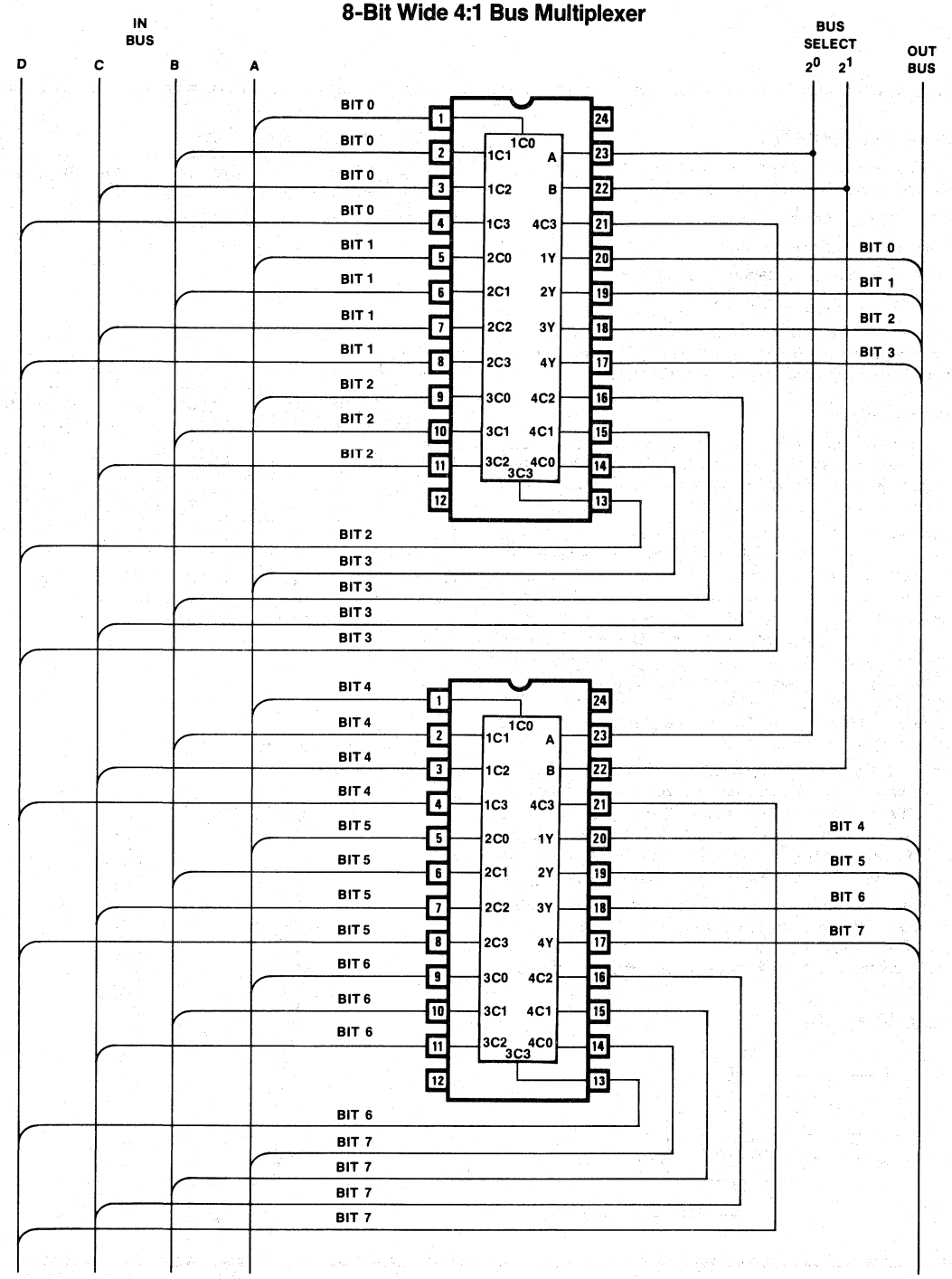
* The "Test Point" is driven by the outputs under test, and observed by instrumentation



Notes: 1. t_{PD} is tested with switch S_1 closed. C_L = 50 pF and measured at 1.5 V output level.
2. t_{PZX} is measured at the 1.5 V output level with C_L = 50 pF. S_1 is open for high impedance to "1" test, and closed for high impedance to "0" test.
3. t_{PXZ} is tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} −0.5 V output level: S_1 is closed for "0" to high impedance test measured at V_{OL} +0.5 V output level.

Application

8-Bit Wide 4:1 Bus Multiplexer



Increment and Skip Counter
671492

Features/Benefits

- **Octal counter for microprogram counters, DMA controllers, and general purpose counting applications**
- **Bus-structured pinout**
- **24-pin SKINNYDIP® saves space**
- **Low current PNP inputs reduce loading**
- **Expandable in multiples of 8-bits**
- **Increment by two function can be used as a microprogrammed SKIP or Short BRANCH, resulting in simplified microprogrammed control structures**

Description

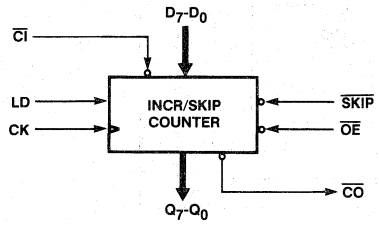
The Increment and Skip Counter (ISC) is an 8-bit cascadable synchronous counter with the ability to be incremented by one or two on the rising edge of the clock line CK. All of the control inputs are synchronous with respect to CK.

The LD input initializes the counter with data setup at the D7-D0 inputs. When the LD pin is HIGH prior to the rising edge of CK, data present at the inputs will be stored. If LD is LOW prior to clocking, a HOLD operation will take place. The LD pin, though synchronous with CK, operates independently of the count increment control $\overline{SKIP}$. When $\overline{SKIP}$ is HIGH, the counter is instructed to count by one upon clocking. Alternately, when $\overline{SKIP}$ is LOW the counter will increment by two. To enable counting, the Count Input line $\overline{CI}$ is required to be LOW. In many applications of the ISC, the $\overline{CI}$ input can be used as a count enable/disable control node.

During the increment by one operation, the Count Output signal $\overline{CO}$ is LOW when the count becomes hexadecimal FF. Similarly, $\overline{CO}$ is LOW for a count of hexadecimal FE during the increment by two operation. At all other times, $\overline{CO}$ is HIGH. Accordingly, the $\overline{CO}$ output can be connected to the $\overline{CI}$ input of a succeeding counter to expand in multiples of 8-bits. $\overline{CO}$ is not affected by $\overline{OE}$.

The outputs Q7-Q0 are enabled when the output enable control $\overline{OE}$ is LOW. Otherwise, when $\overline{OE}$ is HIGH, the outputs are three-stated. Q7-Q0 are fully buffered, and have 24 mA sink current capability, which is required of many bus interface standards.

Block Diagram



Ordering Information

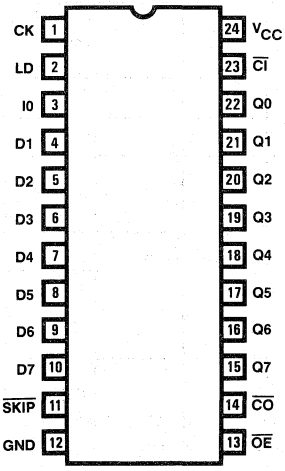
PART NUMBER	PACKAGE	TEMPERATURE
671492	NS, JS	Commercial

Function Table

$\overline{OE}$	CK	LD	$\overline{SKIP}$	$\overline{CI}$	D7-D0	Q7-Q0	OPERATION
H	*	*	*	*	*	*	HI-Z*
L		H	X	X	D	D	Load
L		L	X	H	X	Q0	Hold
L		L	H	L	X	Q0+1	Incr +1
L		L	L	L	X	Q0+2	Incr +2

* When $\overline{OE}$ is HIGH, Q7-Q0 are disabled to the high-impedance state; however, sequential operation of the counter is not affected.

Pin Configuration



SKINNYDIP® is a registered trademark of Monolithic Memories.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories MMI

Absolute Maximum Ratings

Supply voltage V_{CC} ..... 7 V
Input voltage ..... 5.5 V
Off-state output voltage ..... 5.5 V
Storage temperature ..... −65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free air temperature		0		75	°C
t_w	Clock width	Low	35			ns
		High	25			
t_{su}	Setup time		50			ns
t_h	Hold time		0	−15		ns

7

Electrical Characteristics Over Operating Conditions

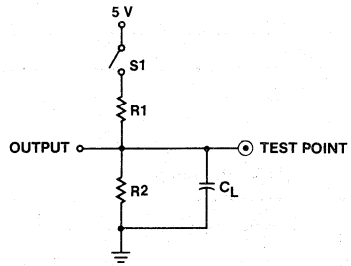
SYMBOL	PARAMETER	TEST CONDITIONS		COMMERCIAL MIN	COMMERCIAL TYP†	COMMERCIAL MAX	UNIT
V_{IL}*	Low-level input voltage					0.8	V
V_{IH}*	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA			−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4 V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, V_{IH} = 2 V	I_{OL} = 24 mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, V_{IH} = 2 V	I_{OH} = −3.2 mA	2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8 V, V_{IH} = 2 V	V_O = 0.4 V			−100	μA
I_{OZH}			V_O = 2.4 V			100	
I_{OS}**	Output short-circuit current**	V_{CC} = 5.0 V	V_O = 0 V	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX			120	180	mA

* V_{IL} and V_{IH} are input conditions of output tests and are not, themselves, directly tested. As conditions of tests, $V_{IL} \leq 0.8$ V and $V_{IH} \geq 2.0$ V.
** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
† Typicals at V_{CC} = 5 V, T_A = 25°C.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See test load)	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{MAX}	Maximum clock frequency	Commercial C_L = 50 pF R_1 = 200 Ω R_2 = 390 Ω	12.5			MHz
t_{PD3}	CI to CO delay			35	50	ns
t_{PD1}	Clock to Q			20	30	ns
t_{PD2}	Clock to CO			55	80	ns
t_{PZX}	Output enable delay			35	45	ns
t_{PXZ}	Output disable delay			35	45	ns

Standard Test Load

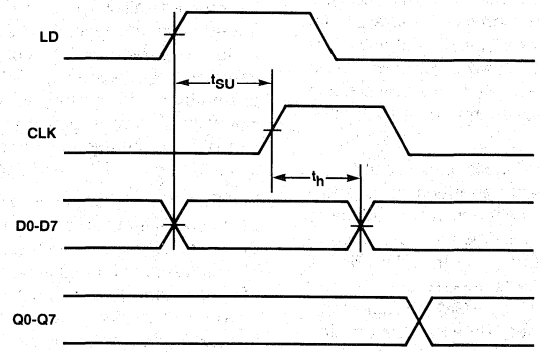


Notes: 1. t_{PD} is tested with switch S_1 closed. C_L = 50 pF and measured at 1.5 V output level.

2. t_{PZX} is measured at the 1.5 V output level with C_L = 50 pF. S_1 is open for high impedance to "1" test, and closed for high impedance to "0" test.

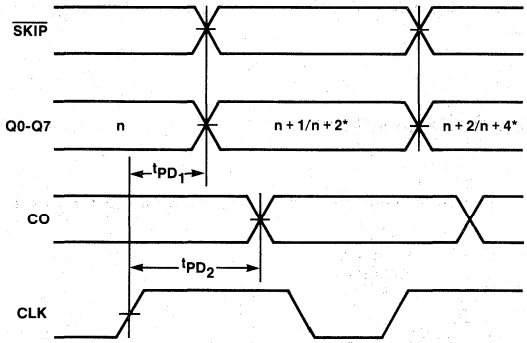
3. t_{PXZ} is tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} -0.5 V output level; S_1 is closed for "0" to high impedance test measured at V_{OL} +0.5 V output level.

Load Timing



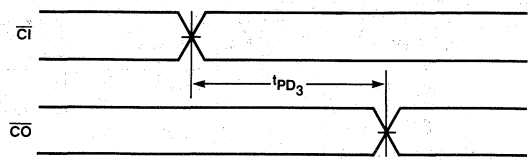
7

Timing During Operation



* IF $\overline{SKIP}$ IS HIGH, Q0-Q7 = n + 1
IF $\overline{SKIP}$ IS LOW, Q0-Q7 = n + 2

Carry In To Carry Out Timing



Application

The Increment and Skip Counter (ISC) is useful as a microprogram counter for a Micro-Programmed Control Unit (MCU). A block diagram of a general-purpose MCU is shown in Figure 1. The ISC, being the central element, provides addresses for microprogram memory. This memory is typically built with bipolar PROMs (such as the 63RS88 shown). However, MOS EPROMs and EEPROMs can be used for greater density and lower cost, if speed is not particularly an important application requirement.

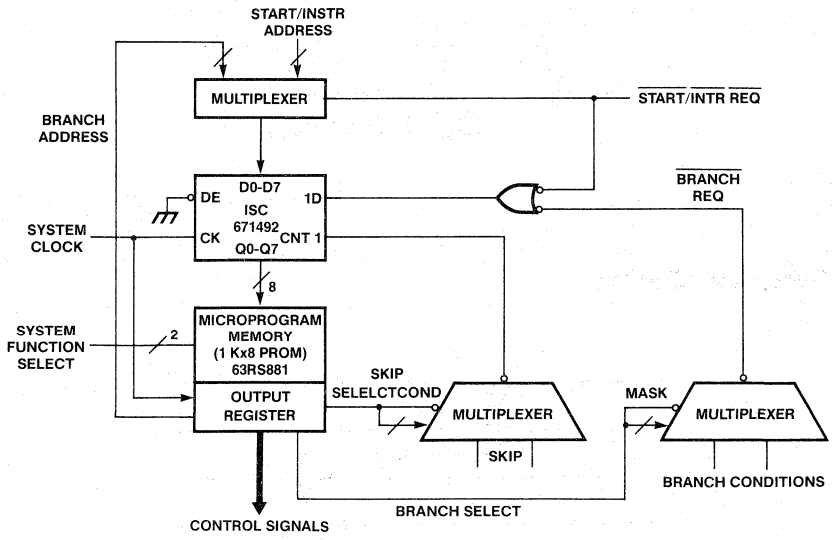
As shown in Figure 1, the Interrupt Request Lines position the microprogram Start Address through a priority encoder and a small (32x8) PROM. The priority encoder serves to reduce as many as eight Interrupt Request Lines down to a 3-bit binary-weighted field used as the address for the mapping PROM. Since only three of the five PROM addresses are used, an optional 2-bit field can be applied to the PROM for diagnostics, or for task context switching. The Start Address, in conjunction with the Branch Address field, are connected to the Next Address multiplexer. Hence the Next Address multiplexer can select either of the two sources for branch address. The Start Address, essentially a forced branch operation, is used when an interrupt operation is requested externally to the MCU; whereas the 8-bit Branch Address Field, which can have up to 256 words of microinstruction memory, is utilized for specific conditional branches.

The Control Field bits represent the control lines to the hardware that the MCU controls. These bit fields can either be encoded or unencoded. In most microprogrammed systems, the bit fields are usually unencoded and connected directly to the specific device under control. However, a performance compromise can be achieved if all or a portion of the Control Field is encoded. The advantage of this technique is that more functions can be controlled. The trade-off is in conserving the number of microinstruction bits allocated to the Control Field, versus the number of possible controlled functions. The two techniques are termed Horizontal and Vertical microprogramming. Horizontal refers to fully parallel operation of the bit fields; whereas, Vertical implies some form of bit field encoding.

The Conditional Control Field selects from among various condition codes that can cause microprogram branch operations. Two kinds of branch operations can be performed in this MCU. The conventional branching described previously uses the ISC LD line to allow the Branch Address to be loaded. Loading new data in the ISC effectively causes the microprogram to branch to the next instruction set by the Branch Address. The Skip facility can be used to quickly test several conditions, then finally take a conventional branch upon exiting all of the tests. If a test is not passed, then a single increment occurs. The microinstruction sequence can then branch to another part of the program, rather than complete the remaining tests. This conditional control structure makes complex test operations more manageable because the test operations can be unified by +2 offset caused by a skip. This contrasts to the longer branch operation, which required precomputing all of the target address in the microprogram for every exit a loop has.

671492 Increment and Skip Counter

Application: General Purpose Microprogram Control Unit



2-Digit BCD Counter
671493

Features/Benefits

- **Drive numeric displays**
- **Expansion in 2-digit increments**
- **24-pin SKINNYDIP® saves space**
- **Bus structured pinout**
- **Low current PNP inputs reduce loading**
- **Three-state output drive bus lines**

Description

The 2-digit BCD (Binary Coded Decimal) Counter is a synchronous counter with complementary count enables ($\overline{CE1}$, CE2), parallel load ($\overline{LD}$), and carry out ($\overline{CO}$). Three control inputs ($\overline{LD}$, $\overline{CE1}$, CE2) provide one of three operations which occur synchronously on the rising edge of the clock (CK).

The load operation loads the inputs (D1 and D2) into the output register (Q1 and Q2) when load is LOW. Note that the load line overrides the increment.

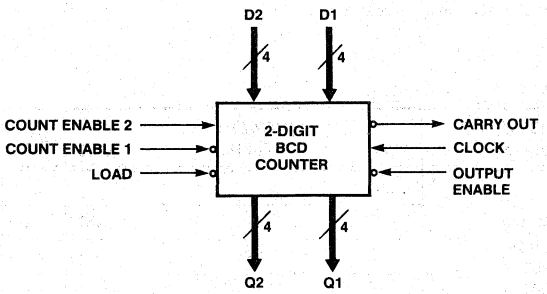
When $\overline{LD}$ is not active, the counter will increment in a Binary-Coded-Decimal sequence if both count enables are asserted ($\overline{CE1}$ = L and CE2 = H), otherwise it holds.

Two or more BCD Counters can be cascaded to implement larger BCD counters by connecting carry out ($\overline{CO}$) of the first stage to count enable ($\overline{CE1}$) of the second stage. This signal is not affected by $\overline{OE}$.

Parallel loading allows programmability of the BCD Counter and numeric indicator.

This BCD Counter is ideal in an industrial control application where an event counter is needed to drive numeric displays. The device can receive one count enable in the form of strobes from a motor or other device. The second count enable can receive the period signal. With connections in this manner, the counter counts events during a period. The device will provide two active high BCD outputs (Q1 and Q2) to drive two numeric indicators, which feature an on-board decoder/driver.

Block Diagram



Ordering Information

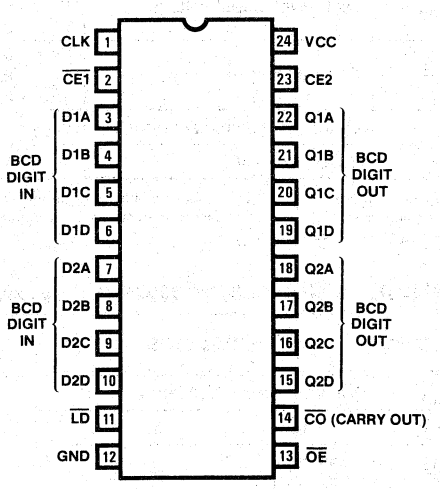
PART NUMBER	PACKAGE	TEMPERATURE
671493	NS, JS	Com

Function Table

$\overline{OE}$	CK	$\overline{LD}$	$\overline{CE1}$	CE2	D1A-D1D/ D2A-D2D	Q1A-Q1D/ Q2A-Q2D	OPERATION
H	*	*	*	*	*	Z	HI-Z*
L	↑	L	X	X	D	D	Load
L	↑	H	H	X	X	Q	Hold (CE1=H)
L	↑	H	X	L	X	Q	Hold (CE2=L)
L	↑	H	L	H	X	Q plus 1	Increment

* When $\overline{OE}$ is HIGH, Q1 and Q2 are disabled to the high-impedance state; however, sequential operation of the counter is not affected.

Pin Configuration



SKINNYDIP® is a registered trademark of Monolithic Memories.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Monolithic Memories MMI

Absolute Maximum Ratings

Supply voltage V_{CC} ..... 7 V
Input voltage ..... 5.5 V
Off-state output voltage ..... 5.5 V
Storage temperature ..... −65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free air temperature		0		75	°C
t_w	Clock width	Low	35			ns
		High	25			
t_{su}	Setup time		50			ns
t_h	Hold time		0	−15		ns

Electrical Characteristics Over Operating Conditions

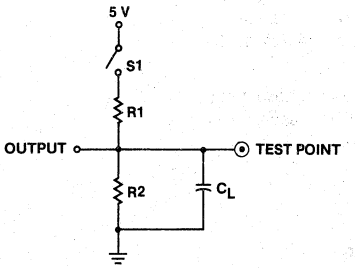
SYMBOL	PARAMETER	TEST CONDITIONS		COMMERCIAL MIN	COMMERCIAL TYP†	COMMERCIAL MAX	UNIT
V_{IL}*	Low-level input voltage					0.8	V
V_{IH}*	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA			−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4 V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, V_{IH} = 2 V	I_{OL} = 24 mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, V_{IH} = 2 V	I_{OH} = −3.2 mA	2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8 V, V_{IH} = 2 V	V_O = 0.4 V			−100	μA
I_{OZH}			V_O = 2.4 V			100	
I_{OS}**	Output short-circuit current**	V_{CC} = 5.0 V	V_O = 0 V	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX			120	180	mA

* V_{IL} and V_{IH} are, in effect, input conditions of output tests and are not, themselves, directly tested. As conditions of tests, $V_{IL} \leq 0.8$ V and $V_{IH} \geq 2.0$ V.
** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
† Typicals at V_{CC} = 5 V, T_A = 25°C.

Switching Characteristics Over Operating Conditions

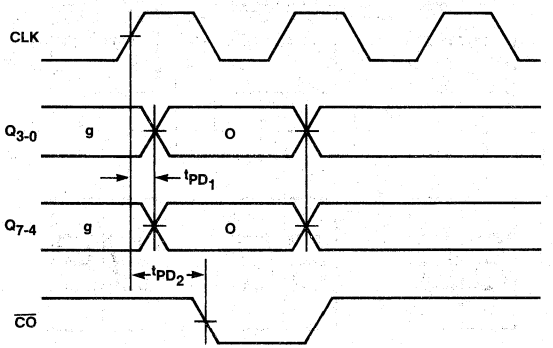
SYMBOL	PARAMETER	TEST CONDITIONS (See test load)	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{MAX}	Maximum clock frequency	Commercial, C_L = 50 pF, R_1 = 200 Ω, R_2 = 390 Ω	12.5			MHz
t_{PD1}	Clock to Q			20	30	ns
t_{PD2}	Clock to CO			55	80	ns
t_{PZX}	Output enable delay			35	45	ns
t_{PXZ}	Output disable delay			35	45	ns

Standard Test Load

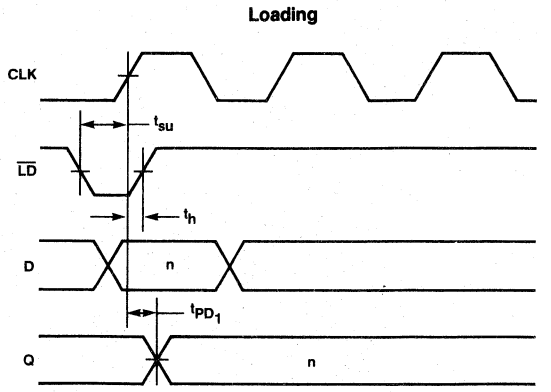


Notes: 1. t_{PD} is tested with switch S_1 closed. C_L = 50 pF and measured at 1.5 V output level.
2. t_{PZX} is measured at the 1.5 V output level with C_L = 50 pF. S_1 is open for high impedance to "1" test, and closed for high impedance to "0" test.
3. t_{PXZ} is tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} −0.5 V output level; S_1 is closed for "0" to high impedance test measured at V_{OL} +0.5 V output level.

Output Timing



Input Timing



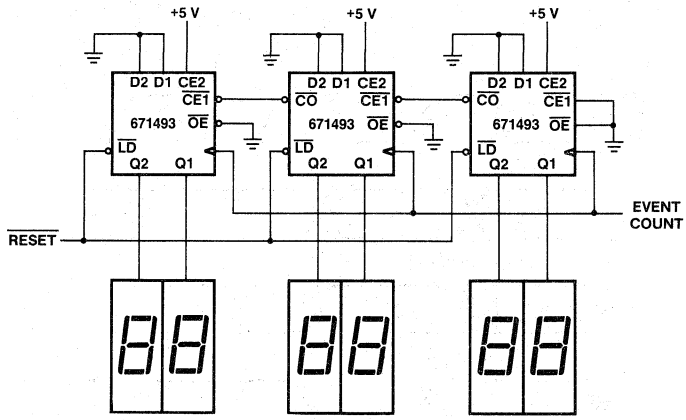
Application: LED Displays

The Event Counter can be implemented using the 2-Digit BCD Counters. The 2-Digit BCD Counters control the display for three pairs of LED displays. The 2-Digit BCD Counters count the events.

The displays are controlled by the output enable. These counters display the count in 10s, 100s and 1000s respectively. These simply count the occurrence of an external event.

671493 2-Digit BCD Counter

Application: Event Counter



8-Bit Priority Encoder with Register

671494

Features/Benefits

- **Encodes eight data lines in priority**
- **Output enable capability**
- **Three-state outputs drive bus lines**

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
671494	N, J	Com

Description

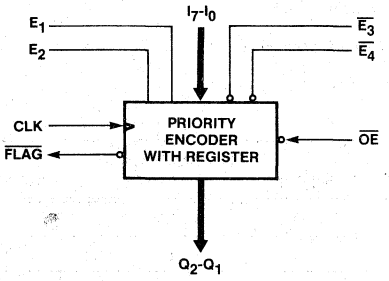
The 8-Bit Registered Priority Encoder accepts data from eight inputs (I7-I0) and provides a binary representation on the three outputs (Q2-Q0). A priority is assigned to each input (with I0 having the highest priority line, and I7 the lowest), so that when two or more inputs are simultaneously active, the input with the highest priority is loaded into the output registers. Pin 14 serves as the interrupt flag ($\overline{FLAG}$) and goes LOW when there is an interrupt present and remains HIGH when there is not interrupt present. The Priority Encoder registers are updated on the rising edge of the clock. The device also features four priority interrupt enable lines: E1, E2, $\overline{E3}$, $\overline{E4}$, which enable or disable the $\overline{FLAG}$ output. These enable lines have no effect on the priority outputs Q2-Q0. All outputs are HIGH-Z when the output control line ($\overline{OE}$) is HIGH, and $\overline{OE}$ operates independently of all other inputs.

Function Table

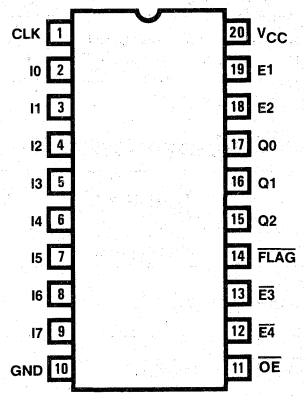
I7	I6	I5	I4	I3	I2	I1	I0	CLK	$\overline{OE}$	$\overline{FLAG}$*	Q2	Q1	Q0
L	X	X	X	X	X	X	H	↑	L	L	H	H	H
L	X	X	X	X	X	H	L	↑	L	L	H	H	L
L	X	X	X	X	H	L	L	↑	L	L	H	L	H
L	X	X	X	H	L	L	L	↑	L	L	H	L	L
L	X	X	H	L	L	L	L	↑	L	L	L	H	H
L	X	H	L	L	L	L	L	↑	L	L	L	H	L
L	H	L	L	L	L	L	L	↑	L	L	L	L	H
H	L	L	L	L	L	L	L	↑	L	L	L	L	L
L	L	L	L	L	L	L	L	↑	L	H	H	H	H
X	X	X	X	X	X	X	X	X	H	Z	Z	Z	Z

* Presumes E1, E2 = HIGH and $\overline{E3}$, $\overline{E4}$ = LOW. If the states of these four lines are different, the $\overline{FLAG}$ output will be disabled (HIGH), regardless of I0-I7.

Block Diagram



Pin Configuration



Absolute Maximum Ratings

Supply voltage V_{CC} ..... 7 V
Input voltage ..... 7 V
Off-state output voltage ..... 5.5 V
Storage temperature ..... −65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature				75	°C
T_C	Operating case temperature					°C
t_w	Clock width	Low	25	10		ns
		High	25	10		
t_{su}	Setup time		35	15		ns
t_h	Hold time		0			ns

Electrical Characteristics Over Operating Conditions

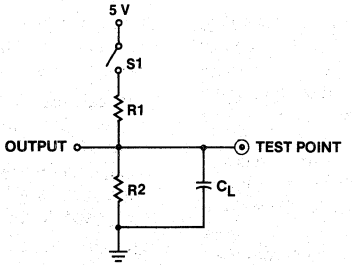
SYMBOL	PARAMETER	TEST CONDITIONS		COMMERCIAL MIN	COMMERCIAL TYP†	COMMERCIAL MAX	UNIT
V_{IL}*	Low-level input voltage					0.8	V
V_{IH}*	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA		−0.73	−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V		−0.02	−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4 V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, V_{IH} = 2 V	I_{OL} = 24 mA		0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, V_{IH} = 2 V	I_{OH} = −3.2 mA	2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8 V, V_{IH} = 2 V	V_O = 0.4 V			−100	μA
I_{OZH}			V_O = 2.4 V			100	
I_{OS}	Output short-circuit current**	V_{CC} = MAX	V_O = 0 V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open			120	180	mA

* V_{IL} and V_{IH} are, in effect, input conditions of DC and functional output tests and are not directly tested. V_{IL} is specified at ≤ 0.8 V and V_{IH} is specified ≥ 2.0 V.
** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
† Typicals at V_{CC} = 5 V, T_A = 25°C.

Switching Characteristics Over Operating Conditions

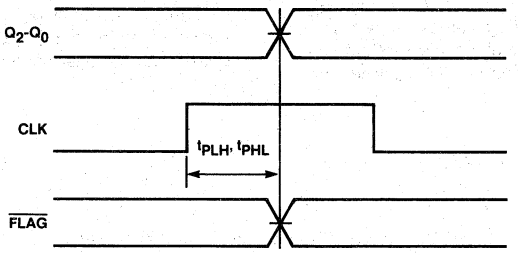
SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{MAX}	Maximum clock frequency	Commercial, C_L = 50 pF, R_1 = 200 Ω, R_2 = 390 Ω	16	25		MHz
t_{PLH}	Clock to output delay			15	25	ns
t_{PHL}				15	25	
t_{PZL}	Output enable delay			15	25	ns
t_{PZH}				15	25	
t_{PLZ}	Output disable delay			15	25	ns
t_{PHZ}				15	25	

Standard Test Load

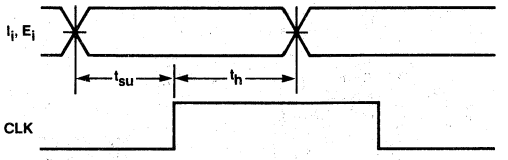


Notes: 1. t_{PD} is tested with switch S_1 closed. C_L = 50 pF and measured at 1.5 V output level.
2. t_{PZX} is measured at the 1.5 V output level with C_L = 50 pF. S_1 is open for high impedance to "1" test, and closed for high impedance to "0" test.
3. t_{PXZ} is tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} -0.5 V output level; S_1 is closed for "0" to high impedance test measured at V_{OL} +0.5 V output level.

Output Timing



Input Timing



Application: DMA and Interrupt Arbitration

The Priority Encoder with Register has several applications in systems requiring arbitration among several competing request lines. In order to obtain a sufficiently quick response in a real time system, access to resources must be ordered, or weighted by priority of importance. For example, a computer and its peripherals may use a number of interrupt request lines for service requests. In some applications, a normal interrupt request is processed too slowly, and a faster means of receiving or sending data is required. In this situation, direct access to system memory could be required, and a DMA Controller used to perform the operations in cooperation with the host computer. Disk Drives commonly use this technique; if more than one drive is in a system, a flexible means of arbitrating DMA requests would be required.

Figure 1 details how a Priority Encoder can be used to construct a Priority Interrupt Controller. Note that in this application, the inputs can either be DMA or Interrupt requests to the Host Computer. In fact, two circuits can be combined in one system to accommodate both types of requests. The expansion possibilities of Figure 1 will be covered after the basic operation of the circuit is explained.

The Interrupt Controller consists of the Priority Encoder, an Interrupt Latch, an Interrupt Level Register, a Comparator, Flip-Flop and a single gate. For many applications the Comparator, Flip-Flop and gate could be realized in a PAL device, but are shown as separate elements for clarity. The Interrupt Latch can be a common 74LS373, or if additional speed is required, a 74S373 can be used.

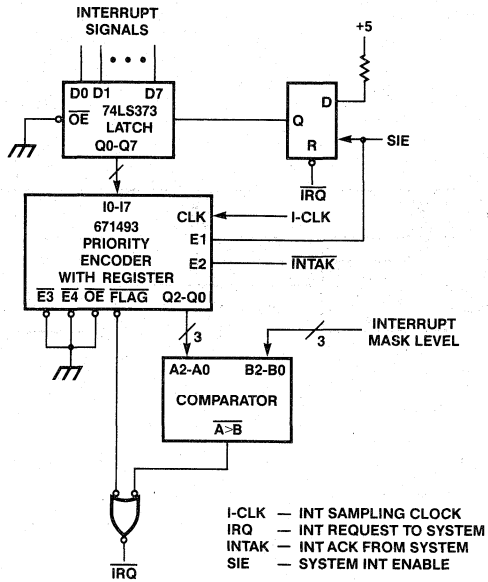
The registers of a Priority Encoder are clocked at a constant rate by the I-CLK signal, which means that any of the interrupt request lines 17-10 passed on by the interrupt latch are continously sampled by I-CLK. The purpose of the interrupt latch is to freeze, or lock out, all interrupt requests once a validated interrupt is sent to the system.

An interrupt is validated by the 3-bit comparator shown in Figure 1, and by the Priority Encoder flag signal. A prestored Mask Value from the Interrupt Level Register is compared with the current value of Q2-Q0, and if the priority code is greater, and if FLAG is LOW, the system is informed that an interrupt is needed. FLAG normally goes low when any of the 17-10 lines are asserted High, if simultaneously all of the Priority Encoder enables (E1, E2, E3 and E4) are asserted.

Because of the fact that in a typical system interrupts can occur at irregular intervals, the Interrupt Controller must be capable of synchronizing to the cycle timing of the host machine. The on-chip registers of the Priority Encoder make possible this synchronization activity. The FLAG signal in combination with the host system timing, and the Interrupt Latch allows the host positive control over the Interrupt Controller.

5/671494 Priority Encoder with Register

Application: Priority Interrupt Controller Application



SiBER (Single Burst Error Recovery IC)

673480

Features/Benefits

- 15 MHz data rate
- Selectable CRC or ECC polynomials
- Standard 16-bit CRC-CCITT polynomial detects errors
- Computer-generated 32-bit ECC polynomial exceeds the performance of Fire code polynomials
- Double-burst error detection and single-burst error correction with ECC polynomial
- Programmable correction span of 5, 8 or 11 bits
- Hardware or software correction modes
- Separate receiver and transmitter ports
- HOLD pin for idle operation
- Maximum of 1024 bytes of data
- Inverted checkbits and selective initialization to a HIGH state improve reliability

Description

The SiBER (Single Burst Error Recovery) is a LSI error detection and correction circuit used to insure data integrity between two serial ports. An industry standard 16-bit CRC polynomial and a 32-bit computer-generated ECC polynomial are both implemented on this chip. Both polynomials have error detection capabilities, but only the ECC polynomial is used for error correction. The ECC polynomial has a maximum correction span of 11 bits in series and a maximum record length of 1024 bytes of data. The 16-bit CRC polynomial is the industry standard CCITT polynomial:

$$x^{16} + x^{12} + x^5 + 1$$

The 32-bit computer-generated ECC polynomial is selected for its error detection span, and the high probability of detecting short double-burst errors:

$$x^{32} + x^{28} + x^{26} + x^{19} + x^{17} + x^{10} + x^6 + x^2 + 1$$

The SiBER implements the transmit, receive, search, and correct algorithms, which are basically serial division operations. By simply asserting the appropriate control signals, spelled out in the "modes of operation" section of this data sheet, the user can:

1) Append checkbits to the data under transmission.
2) Generate the syndrome from received data.
3) Correct erroneous data bits with the information embedded in the syndrome.

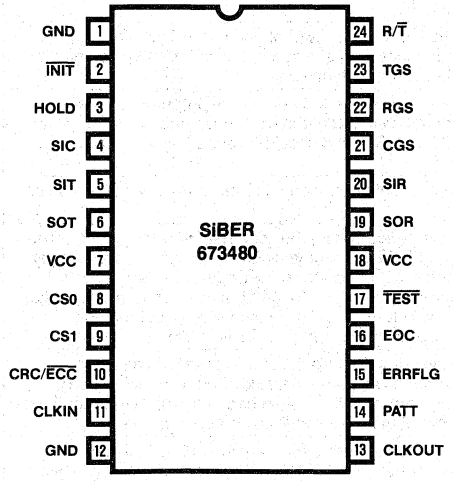
Selective inversion of checkbits and selective initialization of the internal registers to an all-one-state insure randomness in the encoded checkbits and, consequently, improve reliability.

Typical applications of the SiBER include mass storage environments and data communication channels.

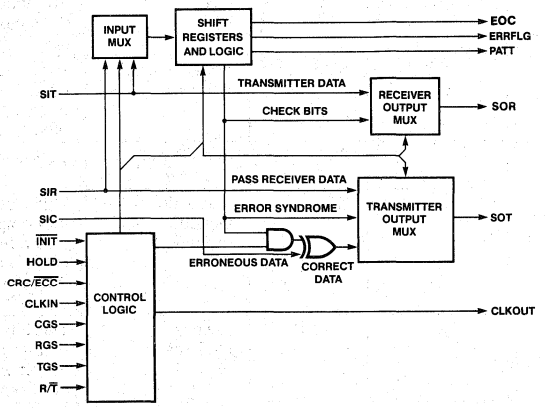
Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
673480	J	Com

Pin Configuration



Block Diagram



2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories

SiBER Pin Description

PIN NUMBER	SYMBOL	PIN NAME	FUNCTION
1, 12	GND	Ground	Electrical Ground
2	$\overline{INIT}$	Initialize	An active LOW asynchronous input pulse is used to reset all internal registers and output flags before transmitting or receiving any data.
3	HOLD	Hold	Raising this input HIGH puts the device in idle operation by holding its present state. The data present on SIT is sent to SOT. A LOW presented on this pin resumes normal operation.
4	SIC	Serial Input Correction	During hardware correction, the buffered data is presented to this input one bit at a time in reverse order. If the data bit is erroneous it is corrected and placed on SOT. See block diagram for data flow.
5	SIT	Serial Input Transmitter	During the transmit mode, data to be transmitted is presented to this input in a serial fashion.
6	SOT	Serial Output Transmitter	Four different types of data are shifted out on this output (see block diagram). Data on SIR appears on this pin during receive mode; corrected data appears during hardware correction, error syndrome appears during software correction; and error pattern appears during hardware/software correction.
7, 18	V_{CC}	V_{CC}	+5 volt supply.
8, 9	CS_0, CS_1	Correction Span Select	Correction spans that can be selected by specifying CS_0 and CS_1 are: a 5-bit correction span (CS_0 = LOW, CS_1 = LOW), an 8-bit correction span (CS_0 = LOW, CS_1 = HIGH), and an 11-bit correction span (CS_0 = HIGH, CS_1 = HIGH). The fourth state (CS_0 = HIGH, CS_1 = LOW) is restricted and must never be entered. It is used by the factory during manufacturing to test the device for enhanced quality assurance and guaranteed functionality.
10	CRC/$\overline{ECC}$	CRC/$\overline{ECC}$ Select	This input control line is used to select the desired polynomial. The 32-bit computer-generated ECC polynomial is selected when CRC/$\overline{ECC}$ is LOW and the 16-bit standard CRC-CCITT polynomial when CRC/$\overline{ECC}$ is HIGH.
11	CLKIN	Clock Input	This is the clock input, and the rising edge is used to strobe the data during the transmit, receive, and correction modes of operation.
13	CLKOUT	Clock Output	The Clock output is a delayed clock input. It is generally used for synchronization of all output signals from the SiBER.
14	PATT	Pattern Flag	This output is set HIGH (and remains set until initialized) when the error pattern is found by the SiBER.
15	ERRFLG	Error Flag	This output is set HIGH (and remains set until initialized) when the syndrome is nonzero. A nonzero syndrome at the end of the receive cycle means that the data read is in error.
16	EOC	End of Correction	This output is set HIGH (and remains set until initialized) eleven clock cycles after the pattern flag is set.
17	$\overline{TEST}$	$\overline{Test}$	This input must be tied to V_{CC} for normal operation. This pin is used by the factory during manufacturing to test the device for enhanced quality assurance and guaranteed functionality.
19	SOR	Serial Output Receiver	Two different types of data are shifted out on this output (see block diagram). During the transmit mode, the data presented on SIT appears on this pin when TGS is HIGH, and checkbits appear when TGS is pulled LOW.
20	SIR	Serial Input Receiver	During the receive mode, data is presented to this input in a serial fashion.
21	CGS	Correction Generate or Shift	This input controls the device during the search and correct modes. The four options are: (1) Shift the syndrome when CGS is LOW immediately after a receive operation, (2) generate the error pattern when CGS is HIGH and the output PATT is LOW, (3) shift the error pattern when CGS is LOWered and the output PATT is HIGH, and (4) correct the burst of erroneous data when CGS is HIGH and PATT is HIGH.
22	RGS	Receive Generate or Shift	This input controls the device during the receive mode. When RGS=HIGH the syndrome is being generated. On the HIGH-to LOW transition of RGS, the error condition is latched; the error flag is set if the syndrome is nonzero and the SiBER enters correction mode.
23	TGS	Transmit Generate or Shift	This input controls the device during the transmit mode. The two options are to generate checkbits (TGS = HIGH) and to shift checkbits (TGS = LOW).
24	R/$\overline{T}$	Receive/ $\overline{Transmit}$	This input pin controls the mode of operation. A LOW enables the transmit mode, and a HIGH enables the receive mode.

Modes of Operation

Prior to performing any operation, the appropriate correction span and polynomial type must be selected. The settings of the control signals for each of the four options are summarized below:

SIGNALS			DESCRIPTION
CRC/$\overline{ECC}$	CS0	CS1	
0	0	0	5-bit correction span, ECC polynomial
0	0	1	8-bit correction span, ECC polynomial
0	1	1	11-bit correction span, ECC polynomial
1	X	X	No correction, CRC polynomial generation
X	1	0	Illegal state. It is only used by the factory for testing the devices.

"X" Designates "Don't Care".

The four different modes of operation are tabulated below. Note that the CRC polynomial cannot go into the search/correct mode, but the other modes and functions are common to both the CRC and ECC polynomials.

MODE	CONTROL SIGNALS				DATA PATH		DESCRIPTION
	R/$\overline{T}$	TGS	RGS	CGS	IN	OUT	
TRANSMIT	0	1	X	X	SIT	SOR	Generate checkbits from the data placed on SIT. This data appears on SOR.
	0	0	X	X	X	SOR	Shift the checkbits serially on SOR.
RECEIVE	1	X	1	X	SIR	SOT	The data on SIR appears on SOT. Simultaneously, the syndrome is generated in the 32-bit feedback shift register.
	1	X	↓	X	X	X	Set the error flag if the syndrome is nonzero.
SEARCH (ERRFLG = H, PATT = L)	1	X	0	1	X	X	Search for the error pattern.
	1	X	0	0	X	SOT	Shift the syndrome serially on SOT. (software correction)
CORRECT (ERRFLG = H, PATT = H)	1	X	0	1	SIC	SOT	Data placed on SIC is corrected and placed on SOT. (hardware correction)[1]
	1	X	0	0	X	SOT	Shift the error pattern. (software/hardware correction)

NOTE: 1. In this mode, data placed on SIC is transmitted to SOT. This feature allows the user to implement a read-modify-write operation on buffered data without paying attention to the pattern flag PATT.

Transmit Mode

In this mode, the SiBER generates the unique checkbits for the data being transmitted. These checkbits are appended to the end of the data stream. To initialize the device $\overline{INIT}$ is asserted while R/$\overline{T}$ is LOW. The internal registers and the output flags are reset and the device is in the transmit mode. If TGS is LOW the SiBER will remain initialized until TGS is pulled HIGH. This feature is implemented to allow relaxed initialization timing. Once TGS is HIGH the device starts to generate checkbits for the data present on SIT. The data on SIT also appears on the SOR output. When the last data bit is transmitted, LOWer TGS and the 32 checkbits for the ECC polynomial or the 16 checkbits for the CRC polynomial are serially shifted out on SOR. Figure 1 shows the data flow during the transmit mode. TGS must remain low for at least 32 clock cycles for the ECC polynomial or 16 clock cycles for the CRC polynomial to allow all the checkbits to be shifted out.

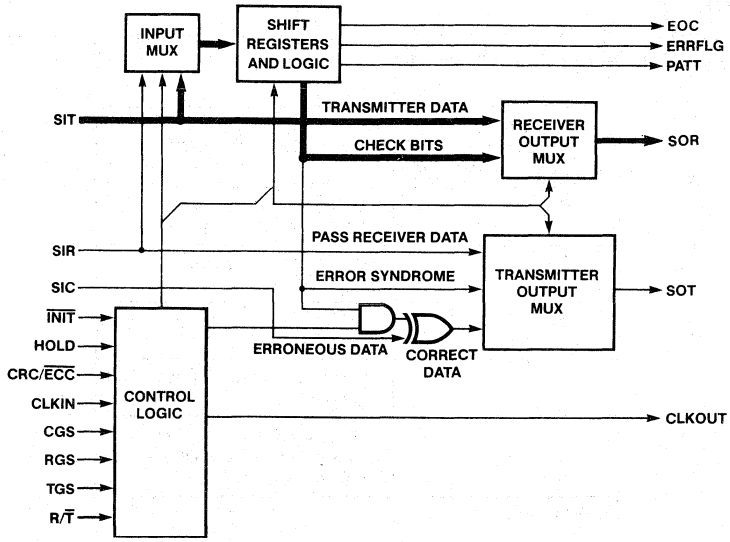


Figure 1. Data Flow During the Transmit Mode

Receive Mode

In this mode, data and checkbits are read from the SIR pin and the SiBER generates a syndrome. To initialize the device $\overline{INIT}$ is asserted while R/$\overline{T}$ is HIGH. The internal registers and the output flags are reset and the device is in the receive mode. If RGS is LOW the SiBER will remain initialized until RGS is pulled HIGH. The feature is implemented to allow relaxed initialization timing. Once RGS is HIGH, the device starts to generate the syndrome for the data present on SIR. The data on SIR also appears on the SOT output. When the last data bit, which is really the last checkbit that was appended to the block of data, is presented on SIR, the error flag ERRFLG is latched on the HIGH-to-LOW transition of RGS; the error flag is set for the case of a non-zero syndrome. When the syndrome is non-zero (ERRFLG = HIGH) and the ECC polynomial is asserted, then the search mode is invoked. The state of the control pin CGS determines the operation performed. The correction cycle is not invoked when the CRC polynomial is asserted. Figure 2 shows the data flow during the receive mode.

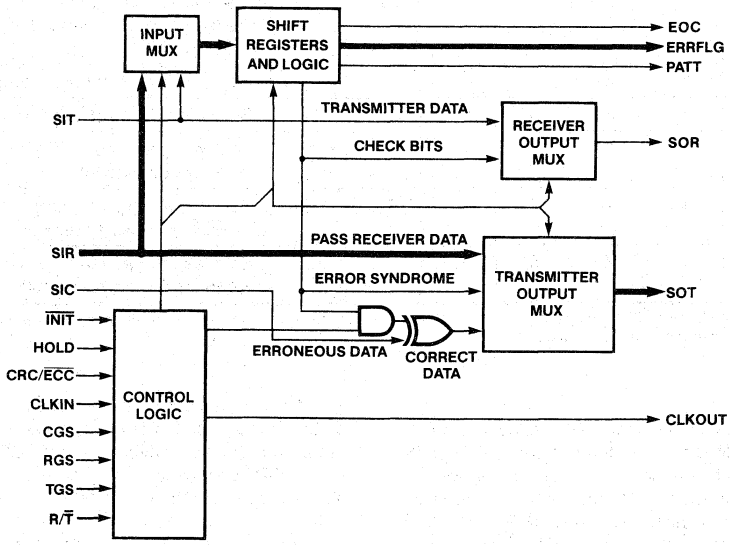


Figure 2. Data Flow During the Receive Mode

Search/Correct Mode

The search/correct mode is used to find the error pattern required to correct the erroneous data record that has just been received. The error pattern can be found by shifting the 32-bit syndrome (left by the receive operation) backwards until a correctable pattern is found, or the search is exhausted by clocking beyond the length of the data record (which indicates the error is uncorrectable). Note that the search/correct mode pertains only to ECC operations and not to CRC operations.

When an error occurs, and correction of the error is desired, there are three methods of finding the error and correcting it, as follows:

1) Pass the syndrome on to the host processor for software correction.
2) Perform a correction pattern search inside the SiBER and pass the error pattern on to the host processor for correction (hardware/software correction).
3) Pass the data record to be corrected through the SiBER (in reverse order) while the SiBER performs the pattern search AND corrects the data record 'on the fly' as it passes through the SiBER chip.

Typically, after the last bit of the ECC field of the data record being read is clocked into the SiBER, RGS is deactivated and HOLD is activated. One clock later, the ERRFLG signal will reflect the final state of the ECC/CRC shift register. It is at this time the system must decide whether to perform a correction or not. Typically, in magnetic media implementations, the system may perform one or more retries on the data record before attempting the correction (some systems will retry until subsequent received ECC fields or syndromes generated by receive operations, are found to be identical).

The Syndrome can be clocked out of the SiBER by simply deactivating the HOLD signal, allowing the syndrome to be shifted out of the SiBER on the SOT line. If the SiBER is to be used to perform all or part of the correction function (as in method 2 or 3), the CGS signal is activated and the HOLD signal is deactivated and the search operation begins.

The first clock cycle of the search operation is used to prepare the syndrome for reverse polynomial shifting. From then on, the SiBER looks for error burst patterns to appear in the ECC shift register. The exact type of pattern searched for is dependent on the correction span selection input signals, CS0 and CS1 (5-, 8-, or 11-bit maximum burst lengths). When an error pattern that fits the qualifications of the correction span inputs is found in the proper position of the ECC shift register, the PATT signal is activated by the SiBER. If method 2 is being used, then the error pattern is shifted out of the SiBER (by lowering the CSG input) when the PATT signal has become active (the HOLD signal can be used to aid in controlling the transition between searching and error pattern shifting, for system timing constraints). *Note: the error pattern being shifted out of the SiBER will be generated in the reverse order with respect to the original data received.* It may also be noted that the error pattern extracted will be CS bits long (where CS represents the selected correction span) regardless of the actual error burst length. When an error burst whose length is less than the correction span selected is found, the first N bits of the error pattern from the SiBER will be zeros (where N = correction span - actual error burst length). For example, if a single-bit error burst occurs and correction is performed with an 8-bit correction span selected, then when the error pattern is found, the first seven bits of the error pattern out of the SiBER will be zeros, and the eighth bit will be a one.

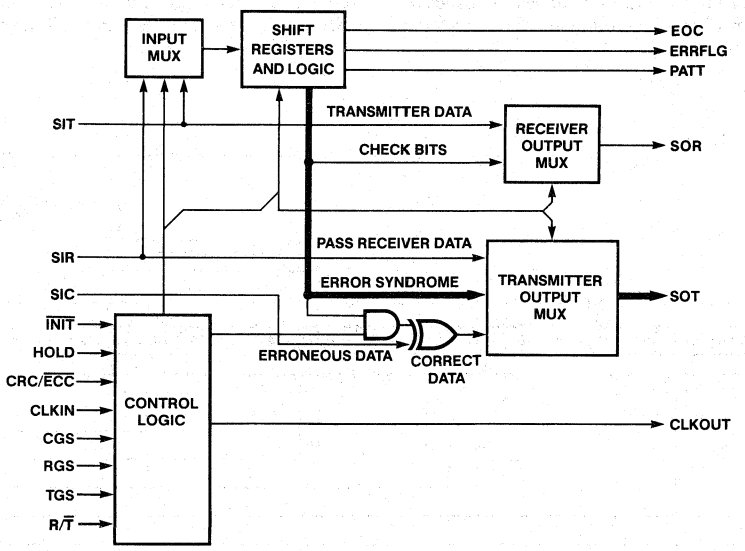


Figure 3. Data Flow During the Search/Correct Mode for Method 1 and Method 2. The Error Syndrome or Pattern is Shifted Out on SOT

Once the pattern is found, the number of clock cycles required to find it, NCC, is used to calculate the position of the error. The calculation is made with respect to the end of the data record *including* the 32-bit ECC field. The calculation is as follows: ED = NCC - 1 (where ED is the Error Displacement in bits, NCC is the Number of Clock Cycles required to find the pattern, and 1 for the search preparation). Therefore, if the pattern is found in one clock, the error displacement, ED, will be zero, indicating the error pattern was found at the end of the ECC field of the data record.

Since the ECC field is used only for error detection and correction, many systems do not store this field if dedicated hardware is used for correction. Therefore the Error Displacement equation can be modified to calculate the distance with respect to the end of the data field, instead of the ECC field. The calculation would then be: ED = NCC - 33. Note that the Error Displacement can, in this case, be a negative number. This simply indicates that the error burst is partially, if not entirely, contained in the ECC field. Careful consideration for boundary conditions are required in these cases.

The maximum number of clock cycles, MNC, to find a correctable error pattern with the SiBER is calculated as: MNC = DL + 33 - CS (where DL is the number of bits in the data field, and CS the selected correction span), which corresponds to an error burst at the beginning of the data field. The search operation should be terminated if the PATT signal has not been activated within the number of clock cycles calculated in the above equation for MNC. If the error pattern cannot be found within MNC clock cycles, then the error is considered uncorrectable and no further action can be taken.

Method 3 is implemented with the SiBER by retransmitting the data record through the SiBER during the pattern search. *Note: The data record is transmitted in reverse order with respect to the receive operation, during the search/correct operation.*

When the SiBER finds the error pattern, the data being presented at the SIC input is XORed with the error pattern and retransmitted, via the SOT output, as corrected data. During other periods of the search/correct operation, the data presented at the SIC input is retransmitted to the SOT output, unchanged.

After a receive operation with an error condition present, the SiBER starts the search/correct operation, just as described for method 2, by asserting the CGS input line. For proper positioning of the retransmitted data with respect to the error pattern to be found, the SiBER must be clocked once (if the data record retransmission includes the 32-bit ECC field) or thirty-three times (if the data record retransmission does not include the 32-bit ECC field) before data bits are presented at the SIC input and captured at the SOT output.

If the PATT output does not become active within MNC clock cycles, as calculated above, then the error is uncorrectable.

Example:

Data Field = 512 bytes = 4096 bits
Correction Span = 11 bits

MNC = (4096 + 33 - 11) = 4118 clock cycles

Therefore, with this format, all correctable error patterns must be found within 4118 clock cycles from when the search/correct operation began, otherwise the error is uncorrectable.

If a search operation finds the error pattern in 1787 clock cycles, then the 11-bit error burst starts (in reverse order) 1786 bits from the end of the ECC field or 1754 bits from the end of the data field. This can be recalculated for forward displacement as (4096-1754-11) bits = 2331 bits from the beginning of, or starting with bit 4 of the 292nd byte, of the data field. Figure 4 shows the position of the error pattern in the data field.

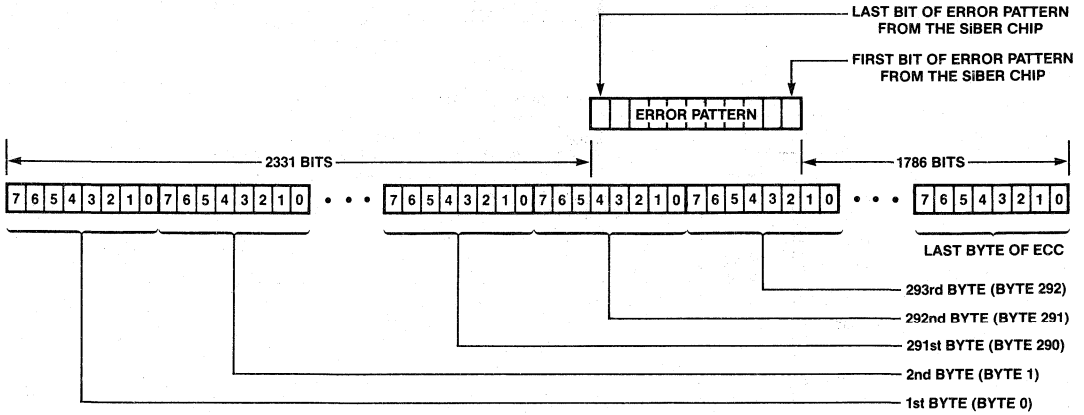


Figure 4. Example

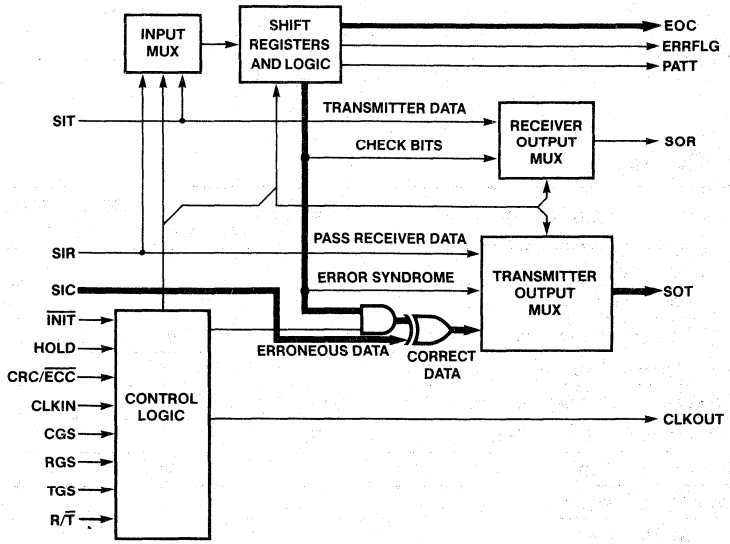


Figure 5. Data Flow During Search/Correct Mode for Method 3. Data on SIC is Corrected and Placed on SOT

Multiple Burst Errors

When there is an error, the error flag ERRFLG goes HIGH. If this error is within the correcting capability of the code, then PATT goes HIGH when the error pattern is found. If there is a multiple error of two or more bursts and the capability of the code is exceeded, then the pattern flag PATT remains LOW during the search mode. The SiBER is recommended for detecting and correcting bursts of errors in 1K bytes of data or a total of 8K bits in a serial stream. It can be used for even larger streams, but the probability of miscorrection is increased.

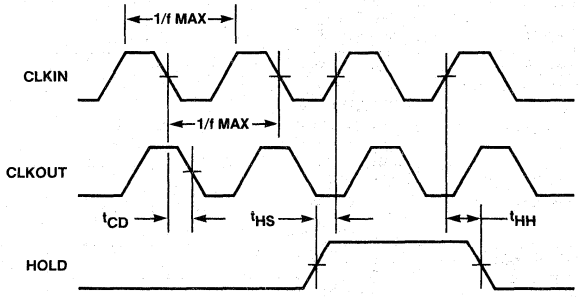


Figure 6. Clock and Hold Timing

Absolute Maximum Ratings

Supply Voltage V_{CC} ..... 7 V
Input Voltage ..... 7 V
Off-state output Voltage ..... 5.5 V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
t_{IPW}	Initialization Pulse Width	7, 8	20			ns
t_{CRCS}	CRC Initialize Set-Up Time	7, 8	20	12		ns
t_{RTS}	R/T Initialize Set-Up Time	7, 8	15	8		ns
t_{GSS}	Generate and Shift Set-Up Time	7, 8, 10, 11	50	27		ns
t_{GSH}	Generate and Shift Hold Time	7, 8, 10	0			ns
t_{SIS}	Serial Input Set-Up Time	7, 8, 11	50	32		ns
t_{SIH}	Serial Input Hold Time	7, 8	0			ns
t_{HS}	Hold Set-Up Time	6	45	24		ns
t_{HH}	Hold Time for Hold Input	6	0			ns
T_A	Operating free-air temperature		0		75	°C

Electrical Characteristics Over Operating Conditions

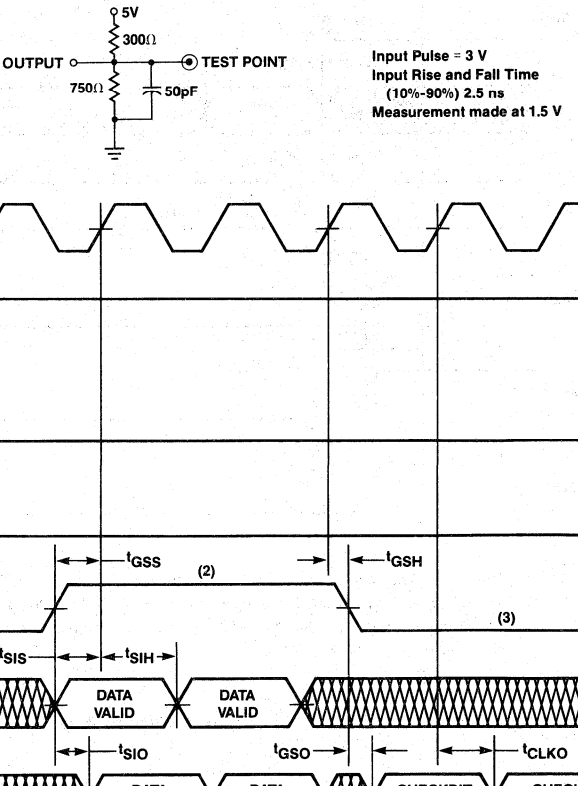
SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage				0.8	V
V_{IH}	High-level input voltage		2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA			−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			25	μA
I_I	Maximum input current	V_{CC} = MAX, V_I = 5.5 V			1	mA
V_{OL}	Low level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, V_{IH} = 2 V, I_{OL} = 16 mA			0.5 V	V
V_{OH}	High level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, V_{IH} = 2V, I_{OH} = −3.2 mA	2.4			V
I_{OS}	Output short-circuit current*	V_{CC} = 5 V, V_O = 0 V	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX		280	360	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics Over Operating Conditions

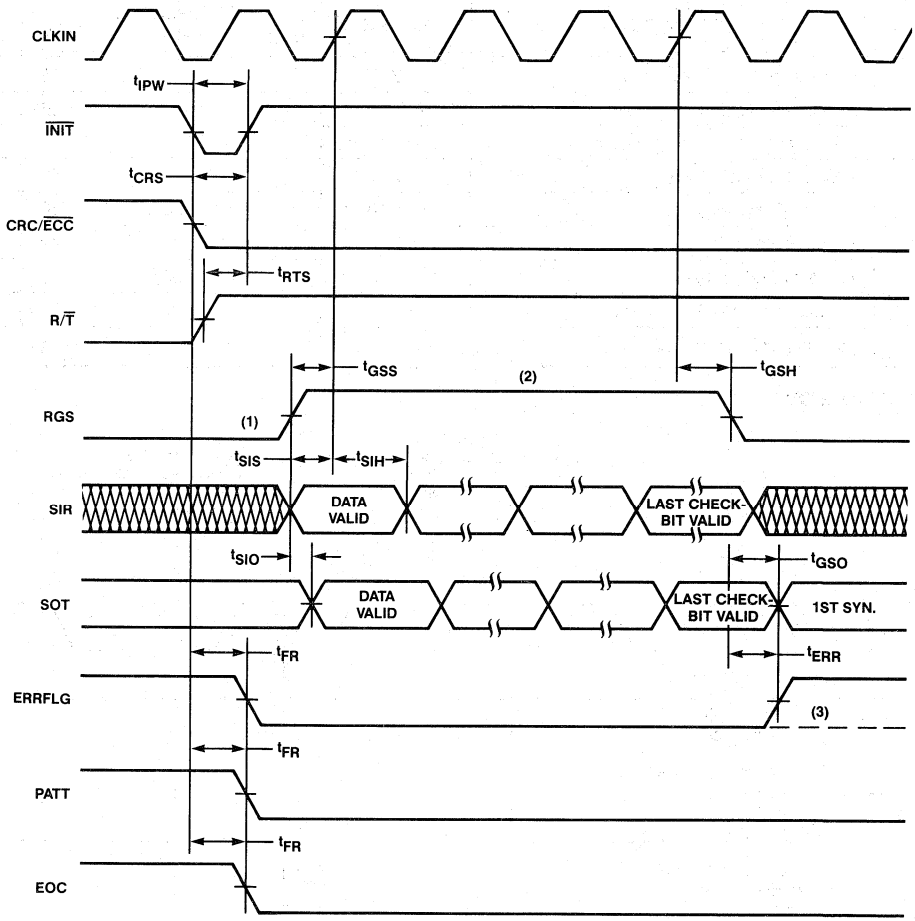
SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	TYP	MAX	UNIT
f_{MAX}	Maximum Clock Frequency	6			15	MHz
t_{SIO}	Serial Input to Output Delay	7, 8, 11		25	35	ns
t_{GSO}	Generate to Serial Output Delay	7-11		25	35	ns
t_{CLKO}	Clock to Output Delay	7, 9, 10		49	60	ns
t_{ERR}	RGS to ERR Delay	8, 9, 10		20	30	ns
t_{PAT}	Clock to PATT Delay	10, 11		33	42	ns
t_{EOC}	Clock to EOC delay	10, 11		33	40	ns
t_{FR}	Initialize to Flags Reset Delay	8		27	35	ns
t_{CD}	CLKIN to CLKOUT Delay	6		12	18	ns

Standard Test Load



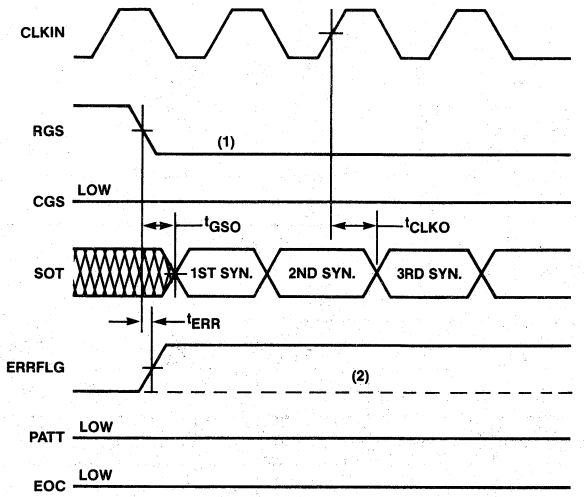
NOTES: 1. After Initialization the chip is in a hold mode (idle) for as long as TGS is LOW.
2. When TGS is HIGH, the data to be encoded is shifted into SIT. The maximum data length is 1K bytes.
3. When TGS is lowered in the transmit mode the checkbits are shifted out on SOR. There are 32 checkbits for the ECC polynomial and 16 for the CRC polynomial.

Figure 7. Transmit Mode



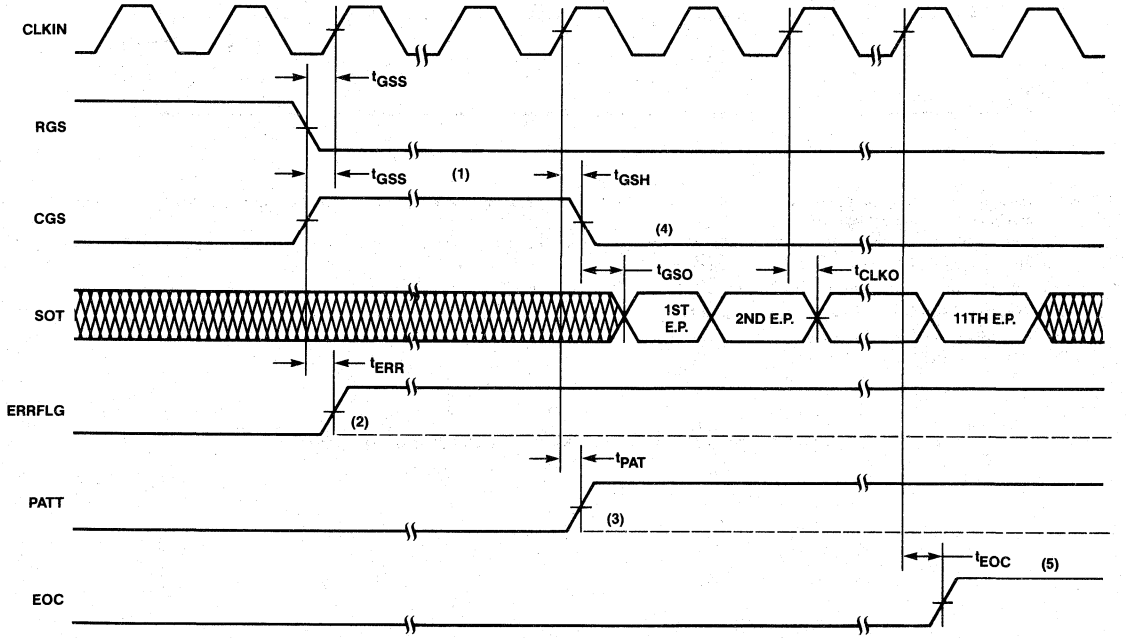
NOTES: 1. After Initialization the chip is in a hold mode (idle) for as long as RGS is LOW.
2. When RGS is HIGH, the data followed by the checkbits is shifted into SIR. The syndrome is generated from this data.
3. The error flage ERRFLG is pulled HIGH if the syndrome is non-zero or kept LOW if there is no error.
SYN. = Syndrome Bit Valid

Figure 8. Receive Mode



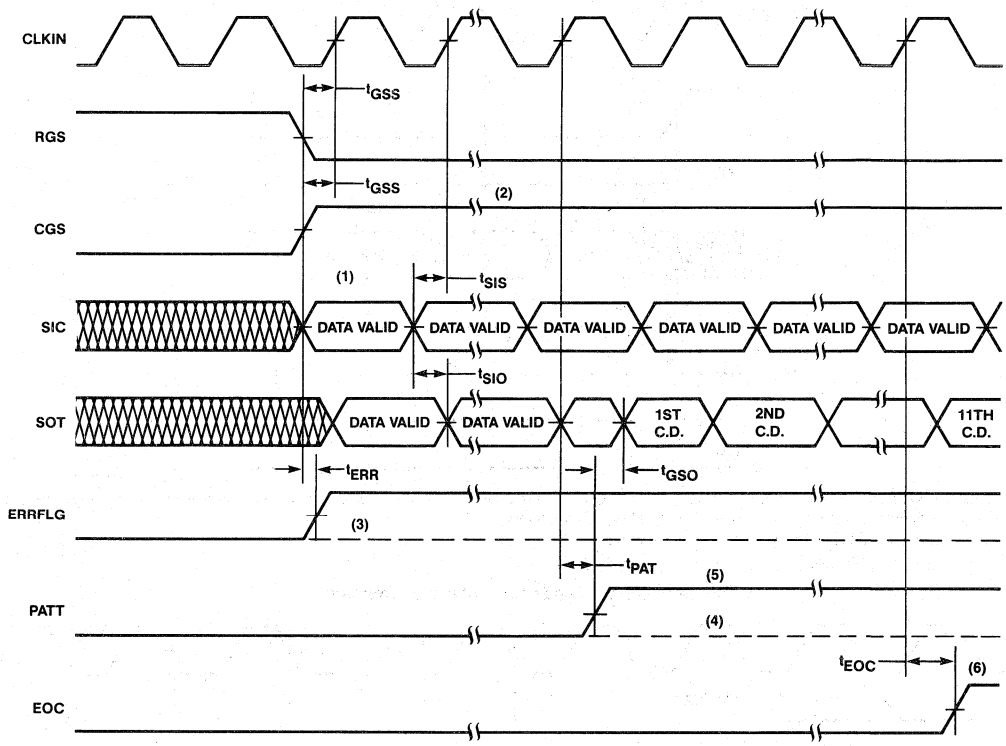
NOTES: 1. When RGS is pulled LOW in the receive mode and CGS and PATT are LOW, the 16-bit syndrome for the CRC polynomial or the 32-bit syndrome for the ECC polynomial is shifted out on SOT. This is called the search mode.
2. The error flag ERRFLG remains LOW when there is no error.
SYN. = Syndrome Bit Valid

Figure 9. Search Mode for Software Correction



NOTES: 1. When CGS is HIGH, the SiBER is clocked until PATT is flagged. This is the search mode in which the location of the error pattern is determined.
2. The error flag ERRFLG remains LOW if there is no error.
3. A multiple error is indicated when ERRFLG is HIGH and PATT remains LOW.
4. When CGS is LOWered after PATT goes HIGH, the error pattern is shifted out on SOT. This is called the correction mode.
5. 11 clock cycles after PATT is flagged, EOC goes HIGH.
E.P. = Error Pattern Bit Valid

Figure 10. Search and Correct Modes for Software/Hardware Correction



NOTES: 1. Data placed on SIC is transmitted to SOT. This feature allows the user to implement a ready-modify-write operation on buffered data without paying attention to the pattern flag PATT.
2. When CGS is HIGH the SiBER is clocked until PATT is flagged. This is the search mode in which the location of the error pattern is determined.
3. The error flag ERRFLG remains LOW if there is no error.
4. A multiple error is indicated when ERRFLG is HIGH and PATT remains LOW.
5. When PATT is HIGH, the data across SIC is inverted, if erroneous, and shifted out on SOT.
6. 11 clock cycles after PATT is flagged, EOC goes HIGH.
C.D. = Corrected Data Bit Valid

Figure 11. Search and Correct Modes for Hardware Correction

Application

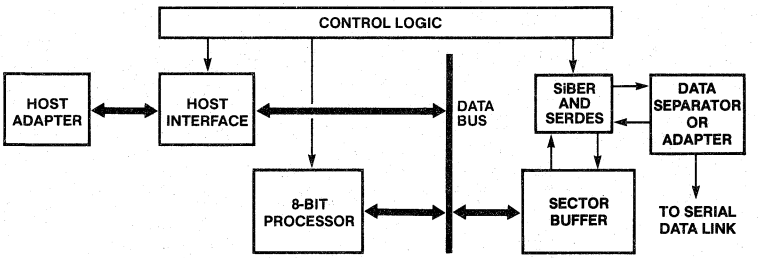


Figure 12. System Block Diagram

The SiBER and the Serializer/Deserializer (SERDES) block, shown in more detail in Figure 13, reside in the front end of a typical system. This block will append the checkbits to the data under transmission and it will generate the syndrome from the received data. Correction can be performed in case of an error. Four operations take place under external control provided by the control logic block.

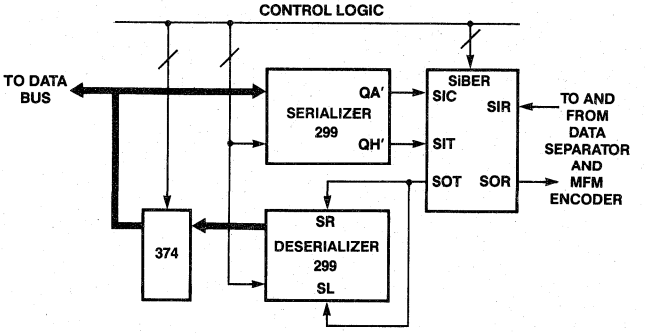
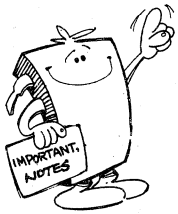


Figure 13. Detailed SiBER and Serializer/Deserializer (SERDES) Block


IMPORTANT
NOTES

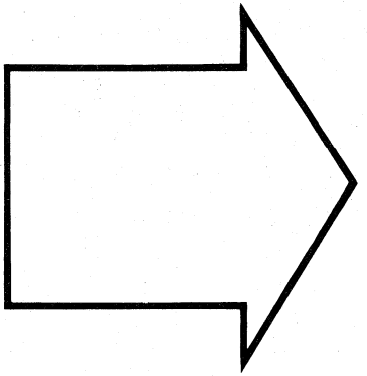


Table of Contents

FIFOs

8

FIRST-IN FIRST-OUT BUFFER MEMORIES

Product Selection and Application Reference Guide

Low-Power FIFOs

CASCADABLE/ STANDALONE	MAXIMUM DATA RATE	ORG.	MAXIMUM I_{CC}	FEATURES	PACKAGES	PINS
67L401*	5 MHz	64x4	100 mA		N,J,NL (20)	16
67L402*	5 MHz	64x5	130 mA		N,J,NL (20)	18
C67L401D*	15 MHz	64x4	100 mA	I_{OL} = 24 mA	N,J,NL (20)	16
C67L402D	15 MHz	64x5	100 mA	I_{OL} = 24 mA	N,J,NL (20)	18
C67L4033D	15 MHz	64x5	115 mA	I_{OL} = 24 mA, Three-State, Status Flags	N,J,NL (20)	20
C67L4013D	15 MHz	64x4	100 mA	I_{OL} = 24 mA, Three-State	N,J,NL (20)	16

* Standalone only.

High-Performance FIFOs

STANDALONE	MAXIMUM DATA RATE	ORGANIZATION	FEATURES	PACKAGES	PINS
67411A	35 MHz	64x4	I_{OL} = 24 mA	J	16
67412A	35 MHz	64x5	I_{OL} = 24 mA	J	18
67413A	35 MHz	64x5	I_{OL} = 24 mA, Three-State, Status Flags	J	20
67411	25 MHz	64x4	I_{OL} = 24 mA	J	16
67412	25 MHz	64x5	I_{OL} = 24 mA	J	18
67413	25 MHz	64x5	I_{OL} = 24 mA, Three-State, Status Flags	J	20

Standard FIFOs

CASCADABLE	STANDALONE	MAXIMUM DATA RATE	ORGANIZATION	PACKAGES	PINS
C67401	67401	10 MHz	64x4	N, J, NL (20)	16
C67402	67402	10 MHz	64x5	N, J, NL (20)	18
C67401A	67401A	15 MHz	64x4	N, J, NL (20)	16
C67402A	67402A	15 MHz	64x5	N, J, NL (20)	18
C67401B	67401B	16.7 MHz	64x4	N, J	16
C67402B	67402B	16.7 MHz	64x5	N, J	18

System FIFOs

DEVICE	DESCRIPTION	ORGANIZATION	PACKAGES	PINS	MAXIMUM FREQUENCY
67417	Serializing FIFO Memory Serial data buffering with optional Serial-to-Parallel or Parallel-to-Serial data conversion	64x8/9	J	24	28 MHz Serial 10 MHz Parallel
674219	FIFO RAM Controller Provides control for SRAM to act as a FIFO buffer	Up to 64K words	J	40	24 MHz Clock

FIFO Applications

APPLICATION	KEY REQUIREMENTS	FIFO PRODUCTS
Microprocessor/CPU Buffering	Data rate of processor System architecture (word width)	74S225/A C/67401/2A/B 67411/2/3A
Peripherals	High data rate or low power Status flag	C/67401/2A/B 67L401/2 C67L401/2/3D
Data/Telecom	High data rate or low power Status flags Word depth (high storage capacity) Data format (serial or parallel)	C67L401/2/3D C67401/2/3D 674219 67417
Data Acquisition	High data rate	67411/2/3A 74S225A

FIFO Application Notes From Monolithic Memories "System Design Handbook"

NUMBER	TITLE	PAGE
AN-112	FIFOs: Rubber-Band Memories to Hold Your System Together	5-3
AN-149	FIFOs: Operations and Applications	5-11
AN-150	Second Generation FIFOs Simplify System Design and Open New Application Areas	5-23
CP-123	Multiprocessing Architectures: A New Frontier for VLSI Applications	5-31
AN-100	PROMs, PALs, FIFO, and Multipliers Team Up to Implement Single-Board High-Performance Audio Spectrum Analyzer	12-3
CP-116	System Solutions for a High-Speed Processor Using Innovative ICs	7-3

Monolithic Memories FIFO Technical Support Hotline
1-800-247-6527 ex. 6197 or 6239

FIFOs: Rubber-Band Memories to Hold Your System Together

Chuck Hastings

Introduction

Data-rate matching problems are a very basic part of the life of a builder of digital systems. Some important electromechanical devices such as disk drives produce or absorb data at totally inflexible rates governed by media recording densities and by the speeds at which small electric motors are naturally willing to rotate. Other devices such as letter-quality printers have maximum data rates beyond which they cannot be hurried up, and which are relatively slow compared to the rates of other devices in the system.

Microprocessors and their associated main memories are generally faster and more flexible than other system components, but often operate with severly degraded efficiency if they must be diverted from their main tasks every few milliseconds to handle data-ready interrupts for individual dribs and drabs of data. While "one day at a time" may be a sound principle by which to live your life, "one bit at a time" or even "one byte at a time" is not a philosophy by which to make your microprocessor live if you want the best possible service from it.

Today there are components called "FIFOs" which let you keep your hardware design simple, and let each portion of your system see the data rate which it wants to see, and yet let you avoid hobbling the performance of your software by constantly interrupting your microprocessor, or even by intermittently halting it in order to let DMA (Direct Memory Access) circuits take over control of the main memory for a short time. FIFOs may be thought of as "elastic storage" devices — "logical rubber bands" between the different parts of your system, which stretch and go slack so that data rates between different subsystems do not need to match up on a short-term microsecond-by-microsecond basis, but only need to average out to be the same over a much longer period of time.

This tutorial paper both describes what FIFOs are in general, and introduces the 64x4 and 64x5 Monolithic Memories FIFOs in particular.

What is a FIFO?

FIFO is one of those made-up words, or *acronyms,* formed from the initials of a phrase — in this case, "*F*irst-*I*n, *F*irst-*O*ut." Originally, the phrase "First-In, First-Out" came from the field of operations research, where it describes a *queue discipline* which may be applied to the processing of the elements of any *queue* or waiting line. There is also a LIFO, or "Last-In, First-Out" queue discipline. The terms FIFO and LIFO have also been used for many years by accountants to describe formal procedures for allocating the costs of items withdrawn from an inventory, where these items have been bought over a period of time at varying prices.

You can probably think of some simple, everyday objects which in some manner behave according to the FIFO queue discipline. For instance, little two-seater cable-drawn boats are drawn through an amusement park tunnel of love one by one, and must emerge from the other end in the same order in which they entered the tunnel — "First-In, First-Out." The old-time coin dispensers used by the attendants at such amusement park features, or by city bus drivers, are "buffer storage" devices for coins which handle the coins in this same manner. (See Figure 1.)

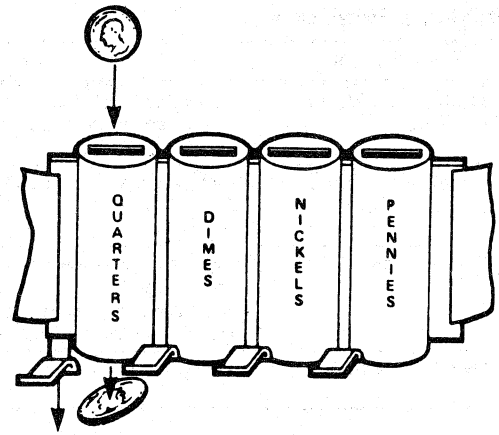


Figure 1. Primitive Mechanical FIFO Device

Notice also that the input of a coin into one of the tubes of such a coin dispenser through the slot at the top, and the output of a coin at the bottom of that tube when the lever for that tube is pushed, are completely independent events which do not have to be synchronized in any way, as long as the tube is neither totally empty nor totally full. However, if the tube fills up completely, a coin inserted into the slot will not go into the tube. Likewise, if the tube empties out completely, no coin is released from the tube at the bottom when the lever is pressed. The coin tube thus behaves as an *asynchronous* FIFO. Keep this homely example in mind.

In computer technology, both the FIFO queue discipline and the LIFO queue discipline are frequently used to control the insertion and withdrawal of information from a buffer memory, or from a dedicated buffer region of some larger memory. In input/output programming practice, a FIFO memory region is sometimes referred to as a *circular buffer,* and in programming for computer-controlled telephone systems it is called a *hopper.* A LIFO memory region is usually referred to as a *stack.*

Both FIFO and LIFO memories have frequently been implemented as special-purpose digital systems or subsystems, but as of the present time only FIFO memories are commonly implemented as individual, self-contained semiconductor devices.

Representative FIFOs

To give you the flavor of what these semiconductor devices are like, I'll describe the type 67401 64x4 FIFO and type 67402 64x5 FIFO which have been available for several years from Monolithic Memories. ("64x4" here means containing 64 words of 4 bits each.) These parts have a basic, easy-to-understand architecture and control philosophy. They also happen to be the fastest FIFOs available through normal commercial channels as of this writing, and they are in widespread use for applications ranging from microcomputers up to IBM-lookalike mainframes and large special-purpose military radar processors. A 67401 is internally organized as follows:

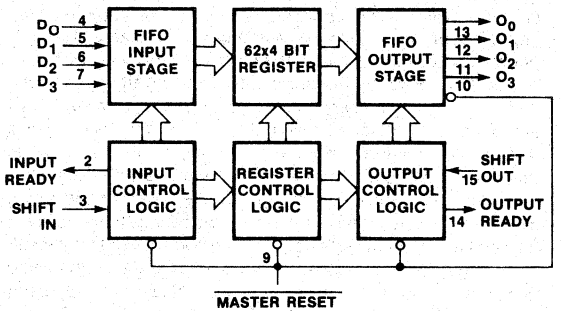


Figure 2. Architecture of the 67401 FIFO

The list of signals/pins for the 67401 is:

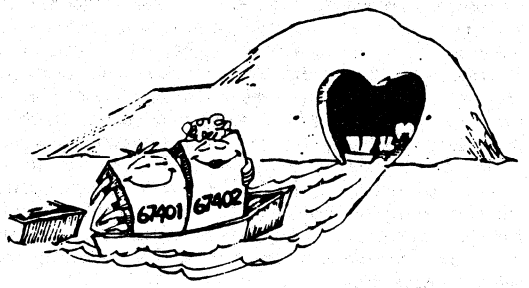
TYPE	HOW MANY	(CUM.)	I/O/V
Data In	4	4	I
Output	4	8	O
Control:			
Shift In	1	9	I
Shift Out	1	10	I
Master Reset	1	11	I
Status:			
Input Ready	1	12	O
Output Ready	1	13	O
Not Connected	1	14	—
Voltage:			
V_{CC} (+5V)	1	15	V
Ground	1	16	V

The corresponding list for the 67402 differs only in that there are five Data in lines rather than four, and five Output lines rather than four. The reason that there is an unused pin is that the 67401 was originally designed as a faster bipolar upgrade of a MOS part, the Fairchild 3341, which needs a second power-supply voltage (-12 V) as well as V_{CC}. Much of the description to be given here of the 67401 also applies to the 3341, except for data rate — the 67401 can operate at 5-35 MHz depending on the exact version, compared with approximately 1 MHz for the 3341. Pinouts are indicated in the data sheet.

The reason for having a 5-bit model as well as a 4-bit model of basically the same part is that if two 4-bit FIFOs are placed side-by-side they make only an 8-bit FIFO, and many people have FIFO applications which entail using a parity bit with each byte, and/or a frame-marker bit with the last byte of a frame or block, which means that they want 9-bit or 10-bit FIFOs. A 67402 next to a 67401 makes a 9-bit FIFO, and two 67402s make a 10-bit FIFO. But I'm getting ahead of myself.

A logic HIGH signal on the Input Ready line indicates that there is at least one vacant memory location within the FIFO into which a new data word may be inserted.Likewise, a logic HIGH on the Output Ready line indicates that there is at least one data word currently stored within the FIFO and available for reading at the outputs. The operation of the FIFO is such that, once a data word has been inserted at the Data In lines (the *top* of the FIFO, as it were), this word automatically *sinks all the way to the bottom* (assuming that the FIFO was previously empty) and forthwith appears at the Output lines. (Remember the synonym *hopper*?) in keeping with the FIFO queue discipline, the first word which was inserted is the first one available at the outputs, and additional words may be withdrawn *only* in the order in which they were originally inserted.

There is no provision for *random access* in these FIFOs, since their internal implementation uses one particular variation of shift-register technology. Each FIFO word consists of 4 (for the 67401) or 5 (for the 67402) data bits, plus a control or "presence" bit which indicates whether or not the word contains significant information. There are thus 4 or 5 data "tracks" and one presence "track" if you look at a FIFO *from a magnetic-tape* perspective. What the Master Reset input does is to clear all of the bits in the presence track, and in addition to clear the very last data word (at the "bottom") which controls the Output lines. The other 63 data words are not cleared, but it doesn't really matter; their status is like unto that of operating-system files whose Directory entries have been deleted, in that they can no longer be read out and will get written over as soon as new information comes in.



"'FIRST-IN, FIRST-OUT' ... DESCRIBES A QUEUE DISCIPLINE WHICH MAY BE APPLIED TO THE PROCESSING OF THE ELEMENTS OF ANY QUEUE ..."

We now return to what happens when a new data word gets inserted at the "top" of the FIFO. A mark (call it a "one") is made in the presence bit for word 00, the first word. Assume now that word 01 is vacant, so that there is a "zero" in its presence bit. The internal logic of the FIFO then operates so that the data from word 00 is automatically written into word 01, the presence bit for word 01 is automatically set to "one," and the presence bit for word 00 is automatically reset to "zero." If word 02 is likewise vacant, the process gets repeated, and so forth until the same piece of data has settled into the lowest vacant word in the FIFO — the next lower word, and all the rest, have "ones" in their presence bits, blocking further changes.

Conversely, now assume that at the moment no data word is being input, but that one has just been output. Then the bottom word in the FIFO — word 63 — has a "zero" in its presence bit, but there are a number of other words above it which have "ones" in their presence bits. The data in word 62 then moves into word 63 in the same manner described above, and the data in word 61 moves into word 62, and so forth, until there is no longer any word in the FIFO having a "one" in its presence bit which is above a word having a "zero" in its presence bit. The effect is that of empty locations bubbling up to the top of the FIFO. Or, in case you are one of those elite individuals who has been exposed to the concepts and jargon of modern semiconductor theory, you may prefer to think of the FIFO operation as one in which data ("electrons") flow from the top of the FIFO to the bottom, and vacancies ("holes") flow from the bottom of the FIFO to the top. In the general case, of course, new data words are being input at the top and old ones are being output at the bottom at random times, and there is a dynamic and continually changing situation within the FIFO as the new data words drop towards the bottom and the vacancies bubble up towards the top, and they intermix along the way.

An obvious consequences of this manner of operation in shift-register-technology FIFOs is that it takes quite a bit longer for a data word to pass all the way through the FIFO than the minimum time between successive input or output operations. There are various versions of the 67401 and 67402, rated at 5, 7, 10, 15, 16.7 or 35 MHz over commercial (0°C to +75°C) or military (-55°C to +125°C) temperature ranges. Thus, for instance, a 16.7-MHz FIFO can input data words at the top and/or output data words at the bottom at a sustained rate of a word every 60 nanoseconds. However, the "fall-through" time, t_{PT} for these same FIFOs is stated in the data sheet as 1.3 microseconds, which is a long enough time for 24 words to be input or 24 words to be output! There is in principle also a "bubble-through" time for a single vacancy to travel from word 63 all the way back to word 00, which should be identical to t_{PT}, and probably is although as *measured* on a semiconductor tester it may differ by as much as 50 nanoseconds, which is probably due to artifacts of measurement. By the way, the stated operating frequencies and the t_{PT} value are "worst-case" (guaranteed) numbers; the "typical" values observed in actual parts are necessarily somewhat better, since semiconductor manufacturers are obliged to take any parts back which customers can prove do not meet the worst-case numbers, and some margin of safety is always nice.

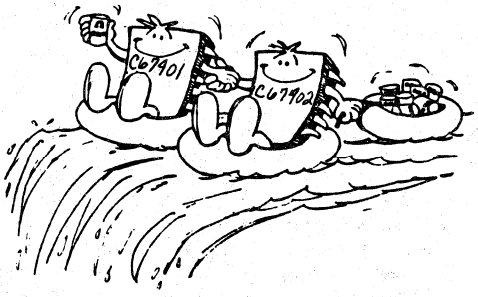
Besides Monolithic Memories, other manufacturers of high-speed FIFOs include Fairchild Semiconductor, Mostek, National Semiconductor, RCA, Texas Instruments, and TRW LSI Products. MOS (slow) FIFOs are available from Advanced Micro Devices, Fairchild Semiconductor, Texas Instruments, Western Digital, Zilog, and probably other firms. FIFOs in development or available at just about all of these vendors also offer new bells and whistles which I haven't discussed, such as three-state outputs, serial (one-bit-at-a-time) as well as parallel data ports, and additional status flags. For instance, Monolithic Memories now has the 67413 FIFO which has a "half-full" flag which tells when half of the FIFO's words contain data, and also a second flag which indicates that the FIFO is either "almost full" (within 8 words of full) or "almost empty" (within 8 words of empty), reminiscent of the "yellow warning interrupt" in Digital Equipment Corporation PDP-11 computers. This "almost-full/empty flag" can be used as an interrupt to a microprocessor to indicate that *some* action must be taken, and the microprocessor can then examine the "half-full flag" to see what it actually has to do.

There are also other design approaches to the insides of a FIFO besides the one based on shift-register technology which has been described here. For instance, a FIFO may be organized as a random-access memory ("RAM") with two counters capable of addressing the RAM right within the chip, an "in-pointer" and an "out-pointer." The counting sequences, of course, "wrap around" from the highest RAM address back to zero. The out-pointer chases the in-pointer, the region just traversed by the in-pointer but not yet by the out-pointer contains significant data, and the complementary region is logically "empty." This approach involves good news and bad news: the good news is that the long fall-through time goes away, but the bad news is that now reading and writing typically interfere with each other — unless the RAM is "two-port," they cannot be done simultaneously at all. Also, since this approach is more costly in "silicon area" than the shift-register approach, it would not result in as large FIFO capacities for the same size die or the same power consumption. In practice, this approach has only been used for MOS FIFOs which have turned out to be quite slow.

Another design approach is somewhat intermediate between the pure RAM approach as just described and the shift-register approach. It uses "ring counters" on the chip instead of full-blown binary counters. What this means in practice is that there are now *two* extra "tracks" along with the data tracks within the FIFO, plus also an input data bus and an output data bus. Single "one" bits move along the in-pointer track and the out-pointer track, and the out-pointer chases the in-pointer as before. The RAM is effectively two-port, and the two parallel buses both go to each and every word. Texas Instruments has announced some small (16x4) bipolar FIFOs based on this technical approach. Like the pure RAM approach, it gets rid of the fall-through time but needs proportionally more silicon area to store a given number of bits.

Designing with FIFOs

Returning now to the Monolithic Memories 67401 and 67402, if what you *really* need is a "deeper" FIFO, say 128x4 instead of just 64x4, these parts are designed to *cascade* using a simple "handshaking" procedure, without any external logic at all! If FIFO B follows FIFO A in the cascading sequence, the Shift In control input of FIFO B is connected to the Output Ready status output of FIFO A, and likewise the Shift Out control input of FIFO A is connected to the Input Ready status output of FIFO B, and the Master Reset control inputs are all tied together. (See Figure 3.) That's all there is to it. Any number of FIFOs may be cascaded in this manner.



"...THE MONOLITHIC MEMORIES C67401 AND C67402...ARE DESIGNED TO CASCADE USING A SIMPLE 'HANDSHAKING' PROCEDURE..."

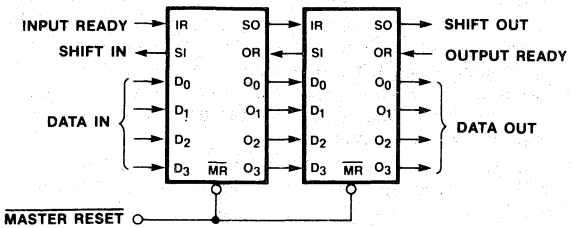


Figure 3. Cascading FIFOs to Form 128x4 FIFO

If what you *really* need is a "wider" FIFO, then you simply arrange 64x4 or 64x5 FIFOs side-by-side up to the required width. Then, you use an external AND gate such as a 74S08 or 74S11 to AND the Input Ready signals of the first rank of FIFOs if there is more than one rank, or of the only rank of FIFOs if there isn't. (See Figure 12 in the FIFO data sheet.) Likewise, a similar AND gate is also needed to AND the Output Ready signals of the last rank of FIFOs. If you didn't provide these AND gates and just took the Input Ready signal of one FIFO as representative of when the whole array was ready, you would be taking the rather large gamble that you had correctly chosen the slowest row in this array — and if you chose wrongly, 4-bit or 5-bit chunks of your input word might not get read correctly into the FIFO where they were supposed to go. Ditto on the output side. So like use the AND gates.

Although a humungus number of 67401s and 67402s are in use world-wide giving hassle-free service, it should be kept in mind that these devices are *asynchronous sequential circuits.* (One definition of "asynchronous sequential circuit" is "a fortuitous collection of race conditions," but that definition is unduly sardonic for very carefully designed parts such as these.) If your board is subject to noise, or if certain data sheet setup-time and hold-time conditions are occasionally not met, errors may occur. It is prudent system-design practice to every so often allow an array of FIFOs to empty out completely, and then issue a $\overline{\text{Master Reset}}$. (I'm assuming, of course, to start with that you're not the kind of turkey who has to be *told* to issue a $\overline{\text{Master Reset}}$ as part of your power-up sequence.) In the event that you still get what appear to be occasional errors, very small (say from 22 to 68 picofarads) capacitors from both the Shift In control input and the Shift Out input of a FIFO to ground will often eliminate these. But by all means start with a *good* circuit board — these are high-speed-Schottky-technology circuits, and like to see a lot of ground-plane metal on the board, along with other reputable interconnection practices such as 0.1-microfarad disk capacitors between V_{CC} and ground for each chip to bypass switching noise.

The sequence of events which occurs during the operation of shifting a new data word into the "top" of a FIFO is shown in Figure 3 in the FIFO data sheet, and the corresponding sequence of events for shifting out the bottom word is shown in Figure 7 in the FIFO data sheet. In both of these figures, it has been assumed that the external logic — whether it be the rest of your system, or just another FIFO — refrains from raising the respective Shift line to HIGH until the respective Ready line has gone HIGH. If the Shift line is raised any earlier, it simply gets ignored.

When two FIFOs are cascaded as shown in Figure 3, the sequences of events shown in data-sheet Figures 3 and 7 are subject to the additional ground rule that the Output Ready line of the FIFO on the left in Figure 3 (call it "FIFO A") is identically the Shift In line of the FIFO on the right (call it "FIFO B"). And likewise, the Input Ready line of FIFO B is identically the Shift Out line of FIFO A. In the terminology we have been using. FIFO A is the "upper" FIFO and FIFO B is the "lower" FIFO. Although you do not normally need to be concerned about what happens when two FIFOs are hooked together for cascaded operation in this manner, since the "handshake" occurs quite automatically without the rest of your logic having to do anything to make it happen, it is an illuminating exercise to consider data-sheet Figures 3 and 7 together in this light and see why the cascading works.

In the general case, both FIFO A and FIFO B are neither completely full nor completely empty. Thus, from the description already given of FIFO internal operation, after some period of time there will be a significant piece of data in word 63 or FIFO A and a "one" in the presence bit for that word. Since the word-63 presence bit is what controls the Output Ready signal, the latter will at some point in time go HIGH and at that same point in time the data word in FIFO A word 63 is present at the output lines. Likewise, after some period of time there will be a vacancy in word 00 of FIFO B, and a "zero" in the presence bit for that word which in turn results in the Input Ready signal going HIGH. Remembering now that each of these Ready signals is in fact the respectively-opposite Shift signal for the other FIFO, it may be seen from data-sheet Figure 3 that the conditions for inputting a word into FIFO B have now been met, and from data-sheet Figure 7 that the conditions for outputting a word from FIFO A and allowing the next available piece of data from somewhere further "up" in FIFO A to enter FIFO A word 63 have also been met. The time delays shown in both data-sheet Figure 3 and data-sheet Figure 7 from the event at 2 to the event at 3, and from the event at 4 to the event at 5A, are asynchronous internal-logic-determined times of the order of four or five gate delays, where the gates in question are high-speed-Schottky LSI *internal* gates and have significantly less propagation delay than the SSI gates you can read about in data sheets.

Returning now to applying the timing analysis shown in data-sheet Figures 3 and 7 to the case of FIFO A and FIFO B operating in cascaded mode, notice that each movement (rising or falling) of the Ready signal for one FIFO is activated by the movement in

the opposite sense (falling or rising, that is) for the Ready signal from the other part. The two signals, ORA/SIB (meaning "Output Ready A" which is the same signal as "Shift In B") and IRB/SOA, cannot both remain HIGH at the same time for more than a few nanoseconds, since if they are both HIGH a data word will pass between the two FIFOs as already described. So, at the point when *both* the sequence of events shown in data-sheet Figure 3 and the sequence of events shown in data-sheet Figure 7 have been completed, and consequently ORA/SIB and IRB/-SOA have both gone HIGH again, another similar sequence of events occurs for both FIFOs and another word is passed, and so forth. This process continues apace until either ORA/SIB sticks LOW, which can happen if FIFO A gets completely emptied out of data words and has "zeroes" everywhere in its presence track; or until IRB/SOA sticks LOW, which can likewise happen if FIFO B gets completely filled and has "ones" everywhere in its presence track. When such a deadlock situation occurs, it lasts until a new data word has been input into FIFO A and has had time to "fall all the way through" and settle into FIFO A word 63, or until the data word in word 63 of FIFO B has been read out and the resulting vacancy has had time to "bubble all the way back up" into FIFO B word 00, as the case may be.

Various Uses for FIFOs

The classical FIFO application, as already mentioned at the beginning of this paper, is that of matching the instantaneous data rates of two digital systems in a simple, economical way. One of the two systems may, for reasons of design economics or even of utter necessity, want to emit or absorb data words in ultra-high-speed bursts, whereas the other one may prefer to operate at a slow-but-steady data rate or even at an erratic rate which varies between ultra-slow and slow or even between slow and fast. No matter — it's all the same to an asynchronous FIFO such as the 67401 or 67402, as long as the input rate and the output rate do match up over a long period of time so that it neither fills up nor empties out.

There are, however, some additional uses for FIFOs which arise from other, rather different circumstances. For instance, your digital system may simply need some extra buffer storage scattered around locally at different points on your block diagram, and you and your system may really just not care whether this storage is accessed on a random or on a queue basis. Under these circumstances, it is ordinarily less hassle to use a FIFO than to use a small RAM and come up with some extra logic to generate addresses and timing signals for it. Often the FIFO modus operandi is in fact the natural one for the application; as for instance when your system must accumulate a block of 64 characters and then run them by all at once in order to examine them for the presence of some control character, using some scanning logic — or perhaps even a microprocessor — which is otherwise occupied most of the time.

A less obvious but interesting application of FIFOs is as automatic "bus-watchers" for jump-history recording for hardware or even software diagnostic purposes. A FIFO whose inputs are connected to a minicomputer's program counter or microprogram counter, or to a microcomputer's main address bus, may be operated so as to record every new jump address generated by the program. This way, if at some point the hardware freaks out or the operating system crashes, a record exists of the last 64 jumps which were taken before the system was halted, assuming of course that you have provided some way for the system to sense that all is not well and halt itself. Such a record of jumps can be very valuable in tracing out what happened just before everything went haywire. FIFOs may be used in this way either as part of built-in self-monitoring features in digital systems, or as part of various kinds of external test equipment.

FIFOs may also be used as controllable delay elements for digital information which cannot be used immediately upon receipt — perhaps it must be matched against other information which is not yet available, or perhaps it must be synchronized with other streams of information which are out of phase by a varying amount. An example of the latter situation is deskewing several bit-streams off a parallel-format magnetic tape, which commonly has to be done when high recording densities are used. One FIFO *per bit-stream* is required — but the net resulting logic may still be the most reliable and economical way to get the job done, when compared with other possible digital designs. Another example is that of using FIFOs as data memories in digital correlators; the lag in an autocorrelation operation can be set simply by controlling how many words are in the FIFO at one time, and so forth. There are even some applications in which it is advantageous to operate a FIFO with all of its input and output cycles synchronized, so that absolutely all it does is to delay the data by some certain number of clock intervals.

References (1), (2), and (3) are formal applications notes available from Monolithic Memories, which discuss FIFOs from different viewpoints than this paper has taken. Each of them presents a more detailed explanation of one or more applications than there has been room for here. Reference (1) is mainly an overall applications survey, reference (2) emphasizes digital communications, and reference (3) emphasizes digital spectrum analyzers and also includes an overview of digital signal processing in general.

"A LESS OBVIOUS BUT INTERESTING APPLICATION OF FIFOS IS AS AUTOMATIC 'BUS-WATCHERS' . . ."

References

(1) "First In First Out Memories...Operations and Applications," applications note published March 1978 by Monolithic Memories Inc. and being reissued.

(2) "Understanding FIFO's," applications note published by Monolithic Memories Inc. The author, Alan Weissberger, has also gotten a modified version of this note published as a magazine article, "FIFOs Eliminate the Delay when Data Rates Differ," in *Electronic Design*, November 27, 1981, Despite the general title, the emphasis is on digital communications applications.

(3) "PROMs, PALs, FIFOs and Multipliers Team Up to Implement Single-Board High-Performance Audio Spectrum Analyzer," applications note published by Monolithic Memories Inc. The author, Richard Wm. Blasco, also got this note published in *Electronic Design* in two installments, in the issues of August 20 and September 3, 1981 under the titles "PAL Shrinks Audio Spectrum Analyzer" and "PAL Improves Spectrum Analyzer Performance" respectively.

Asynchronous First-In First-Out Memory (FIFO) 16x5 74S225/A

Features/Benefits

- DC to 20-MHz shift-in/shift-out rates
- Fully expandable by word width and depth
- Three-state outputs
- TTL-compatible inputs and outputs
- Functionally compatible with T.I. SN74S225
- Designed for extended testability

Description

The 74S225/A is a Schottky-clamped transistor-transistor logic (STTL) 16x5 First-In-First-Out memory (FIFO) which operates from DC to 10/20 MHz. The data is loaded and emptied on a first-in-first-out basis through asynchronous input and output ports. These devices are used in digital systems performing data transfers when source and receiver are not operating at the same data rate. FIFOs are also used as data buffers where the source and receiver are not operating at the same time. Both word length and FIFO depth are expandable. Unload clock output (Pin 3) is designed for testability of V_{OL}.

Ordering Information

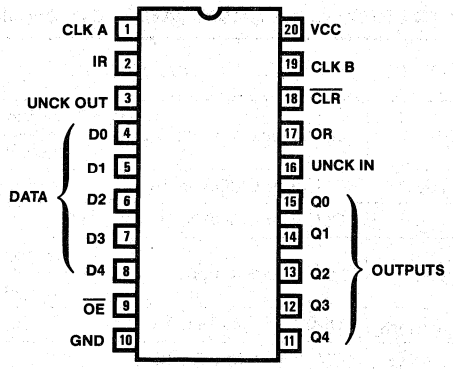
PART NUMBER	PACKAGE	TEMPERATURE
74S225	J, N	10 MHz Com
74S225A	J, N	20 MHz Com

Pin Names

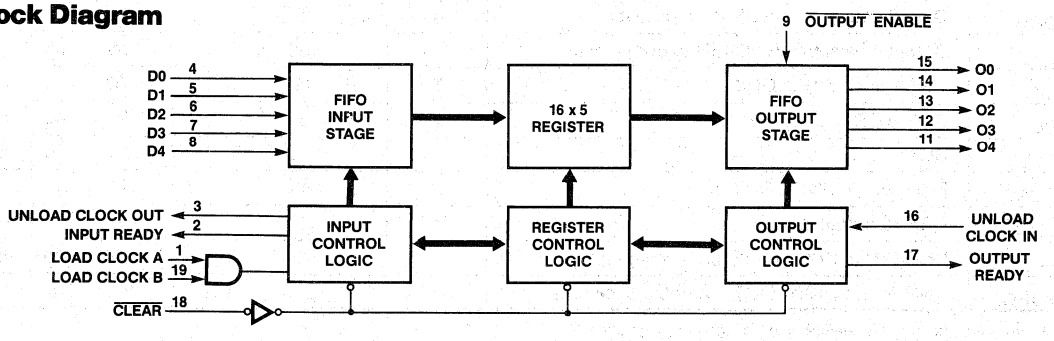
PIN #	PIN NAME	DESCRIPTION
1	CLK A	Load clock A
2	IR	Input ready
3	UNCK OUT	Unload clock output
4-8	D0-D4	Data inputs
9	$\overline{OE}$	Output enable
10	GND	Ground pin
11-15	Q4-Q0	Data outputs
16	UNCLK IN	Unload clock input
17	OR	Output ready
18	$\overline{CLR}$	Clear
19	CLK B	Load clock B
20	V_{CC}	Supply voltage

Pin Configuration

74S225/A . . J or N Package
(Top View)



Block Diagram



2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374
Monolithic Memories

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65 to +150°C

Operating Conditions

SYMBOL	PARAMETER	FIGURE	74S225 MIN	74S225 TYP	74S225 MAX	74S225A MIN	74S225A TYP	74S225A MAX	UNIT
V_{CC}	Supply voltage		4.75		5.25	4.75		5.25	V
t_A	Operating free-air temperature		0		75	0		75	°C
t_{LCKH}	LOAD CLOCK pulse width, A or B, t_w (HIGH)	2	25			22		36	ns
t_{IDS}	Setup time, data to load clock	2	-20↑ *			-20↑ *			ns
t_{IDH}	Hold time, data from load clock	2	70↑			50↑			ns
t_{UCKL}	UNLOAD CLOCK INPUT pulse width, t_w (LOW)	4	7			7		36	ns
t_{CLW}	CLEAR pulse width, t_w (low)	2	40			20			ns
t_{CLCK}	Setup time, clear release to load clock, t_{su}	2	25↑			10			ns

* Data must be setup within 20 ns after valid Load Clock (A or B) pulse (positive transition).

↑ = Arrow indicates that it is referenced to the o-high transition.

Switching Characteristics Over Operating Conditions

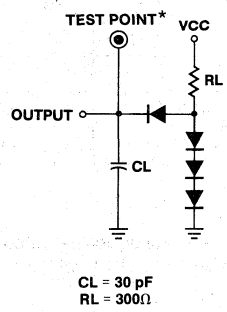
SYMBOL	PARAMETER		FIGURE	74S225 MIN	74S225 TYP	74S225 MAX	74S225A MIN	74S225A TYP	74S225A MAX	UNIT
f_{IN}	Load clock A or clock B	Cascade Mode**	2	10	20		20	22		MHz
		Standalone Mode								
t_{LCIRL}	CLK A or CLK B to IR↓ **		2		55	75		43	55	ns
t_{LCCOL}	CLK A or CLK B to UNCK OUT↓		2		25	50		31	40	ns
f_{OUT}	Unload clock input	Cascade Mode***	4	10	20		20	22		MHz
		Standalone Mode								
t_{UCKORL}	UNCK IN↓ to OR LOW		4		30	45		26	35	ns
t_{UCKORH}	UNCK IN↑ to OR HIGH		4		40	60		32	45	ns
t_{ODH}	Output data hold, UNCK IN to output data		4	20	50		20	30		ns
t_{ODS}	Output data setup, UNCK IN to output data		4		50	75		41	55	ns
t_{RIP}	CLK A or CLK B to OR↑		7		190	300		167	220	ns
t_{CLOL}	CLR to OR↓		6		35	60		31	40	ns
t_{CLIH}	CLR to IR↑		6		16	35		15	20	ns
t_{UCKOW}	Pulse width, UNCK OUT, t_w		2	7	14		7	11		ns
t_{ORD}	OR↑ to output data		4		10	20		9	15	ns
t_{BUBI}	UNCK IN to IR↑ (bubble-back time)		8		255	400		214	290	ns
t_{BUBC}	UNCK IN to UNCK OUT↓ (bubble-back time)		8		270	400		226	290	ns

↓ Arrow indicates that it is referenced to the high-to-low transition.
** 16th word only
*** Devices connected to provide FIFO of greater than 16 word depth.

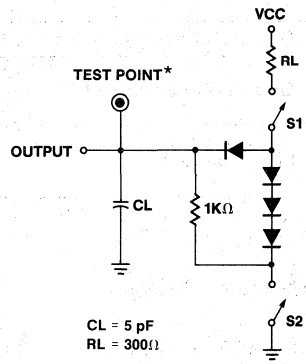
Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	74S225 MIN	74S225 TYP	74S225 MAX	74S225A MIN	74S225A TYP	74S225A MAX	UNIT
t_{PHZ}	Output disable delay, $\overline{OE}$ to Q_i, C_L = 5 pF	1		10	25		8	25	ns
t_{PLZ}							18	25	
t_{PZL}	Output enable delay, $\overline{OE}$ to Q_i, C_L = 5 pF	1		25	40		19	40	ns
t_{PZH}							23	40	

Test Load for Bi-State Output



Test Load for Three-State Output



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Input Pulse Amplitude = 3.0 V
Input Rise and Fall Time (15%–90%) = 2.5 ns
Measurements made at 1.5 V

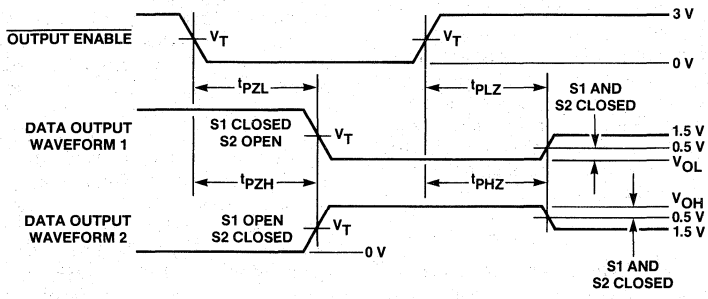


Figure 1. Enable and Disable

Waveform 1 is for an output with internal conditions such that the output is low except when disabled.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage							0.8	V
V_{IH}	High-level input voltage					2.0			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18 mA				−1.5	V
I_{IL1}	Low-level input current	D_0–D_4	V_{CC} = MAX	V_I = 0.5 V				−1	mA
I_{IL2}		All others						−.25	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7 V	Data inputs			40	μA
					Others			25	
I_I	Maximum input current		V_{CC} = MAX	V_I = 5.5 V				1	mA
V_{OL}	Low-level output voltage*		V_{CC} = MIN	I_{OL} = 16 mA (Data outputs)				0.5	V
				I_{OL} = 8 mA (All others)					
V_{OH}	High-level output voltage		V_{CC} = MIN	I_{OH} = −6.5 mA (Data outputs)		2.4			V
				I_{OH} = −3.2 mA (All others)					
I_{OS}	Output short-circuit current**		V_{CC} = MAX	V_O = 0 V		−30		−100	mA
I_{HZ}	Off-state output current		V_{CC} = MAX	V_O = 2.4 V				50	μA
I_{LZ}			V_{CC} = MAX	V_O = 0.5 V				−50	μA
I_{CC}	Supply current		V_{CC} = MAX	Inputs low, All outputs open	74S225		80	120	mA
					74S225A		80	125	

* To measure V_{OL} on Pin 3, force 10 V on Pin 9 (Extended Testability).

** Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Functional Description

Data Input

After power up the CLEAR is pulsed low (Figure 5) to prepare the FIFO to accept data in the first location. Clear must be applied prior to use to ensure proper operation. When Input Ready (IR) is HIGH, the first location is ready to accept data from the D_X inputs. Data then present at the data inputs is entered into the first location when both Load Clocks (CLK A and CLK B) are brought HIGH. The CLK A HIGH and CLK B HIGH signal causes the IR and UNCK OUT to pulse LOW. Once data is entered into the first cell, the transfer of data from any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{RIP} defines the time required for the first data to travel from input to the output of a previously empty device. When the sixteenth word is clocked into the device, the memory is full (sixteen words) and IR remains low. The Unload Clock Output is provided chiefly for use in cascading devices to extend FIFO depth (Figure 9). When Input Ready is Low, do not attempt to shift-in new data.

Data Output

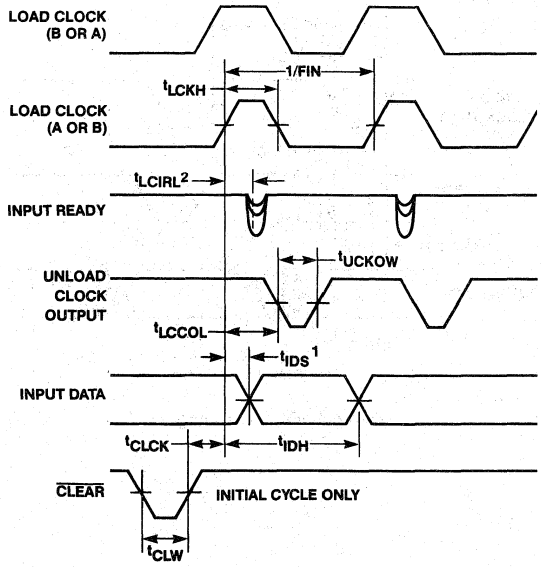
Data is read from the Q_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Unload Clock Input (UNCK IN) LOW. A LOW signal at UNCK IN causes the OR to go LOW. Valid data is maintained while the UNCK IN is LOW. When UNCK IN is brought HIGH the upstream data, provided that stage has valid data, is shifted to the output stage.

When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW and Data remains valid for the last word.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{BUBI}) or completely empty (Output Ready stays LOW for at least t_{RIP}).

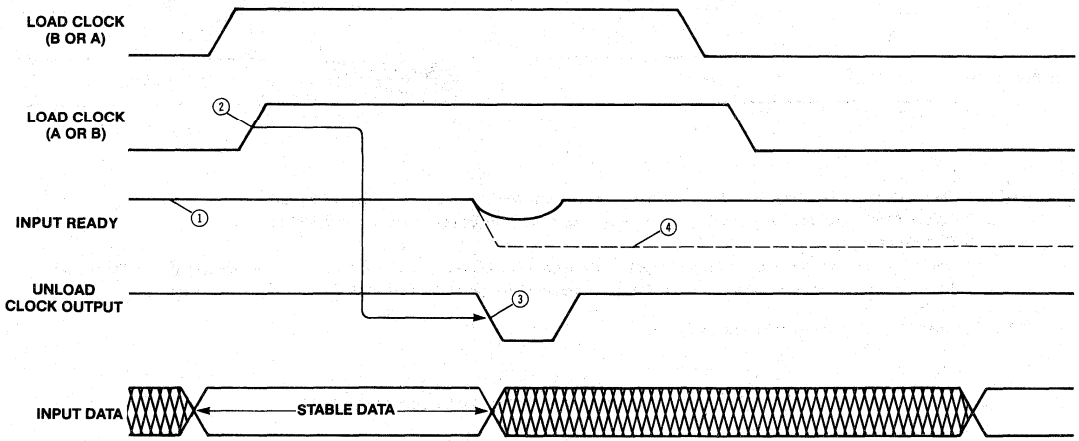
AC Test and High-Speed App. Notes

Since the FIFO is a high-speed device, care must be exercised in the design of the hardware and the timing utilized within the PC board design. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1 μF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Load Clocks (A, B) — Unload Clock Output-Input Ready combination, as well as the Unload Clock Input-Output Ready combination, timing measurements may be misleading, i.e., rising edge of the Load Clock pulse is not recognized until Input Ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or affected by ($\overline{CLR}$), the LOAD-CK activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time (t_{IDH}) and the next activity of Input Ready (t_{LCIRL}) to be extended relative to Load Clock (A or B) going HIGH.



NOTES: 1. Permissible negative setup time for input data
2. Measure t_{LCIRL} for 16th input word only

Figure 2. Input Timing



NOTES: 1. Input Ready HIGH indicates space is available and a Load Clock (A and B) pulse may be applied.
2. Input Data is loaded into the first word.
3. Unload Clock Output pulses indicating the first word is full and the Data from the first word is released for "fall-through" to second word.
4. If the second word is already full, then the data remains at the first word. Since the FIFO is now full, Input Ready remains LOW.

Figure 3. The Mechanism of Clocking Data into the FIFO

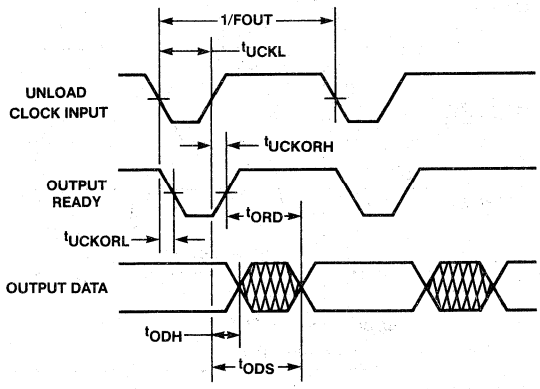
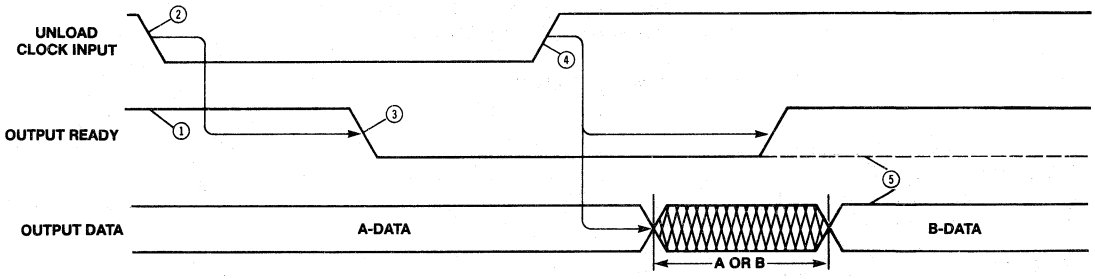


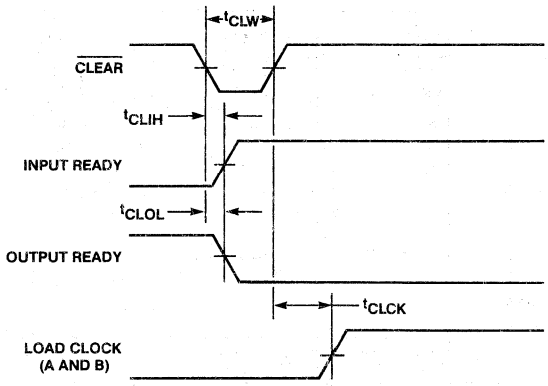
Figure 4. Output Timing



NOTES: 1. Output Ready HIGH indicates that data is available and an Unload Clock Input pulse may be applied.
2. Unload Clock Input goes LOW creating an empty position at word 16 for word 15 to "fall-through" to.
3. Output Ready goes LOW.
4. Unload Clock Input goes HIGH, causing Output Ready to go HIGH, indicating that new data (B) is now available at the FIFO outputs.
5. If the FIFO has only one word loaded (A-DATA), then Output Ready stays LOW and the A-DATA remains on the outputs.

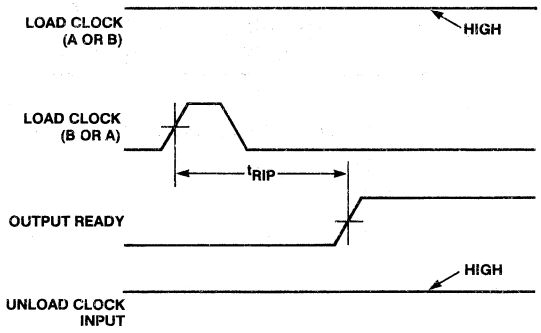
NOTE: Assume FIFO initially contains at least two words.

Figure 5. The Mechanism of Shifting Data Out of the FIFO



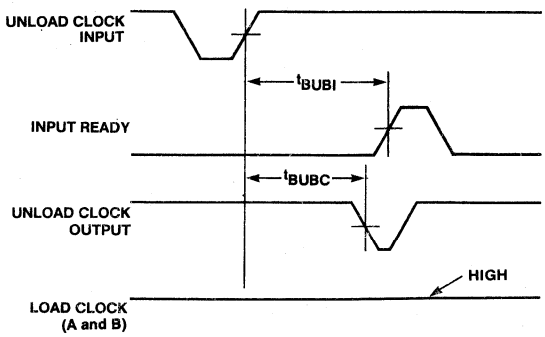
NOTE: Assume FIFO is full before CLEAR goes active.

Figure 6. Clear Timing



NOTES: 1. FIFO is initially empty.
2. Unload Clock Input and one Load Clock held HIGH throughout.

Figure 7. t_{RIP} Specifications



NOTES: 1. FIFO is initially full.
2. Load Clock (A and B) held HIGH throughout.

Figure 8. t_{BUBI}, t_{BUBC} Specifications

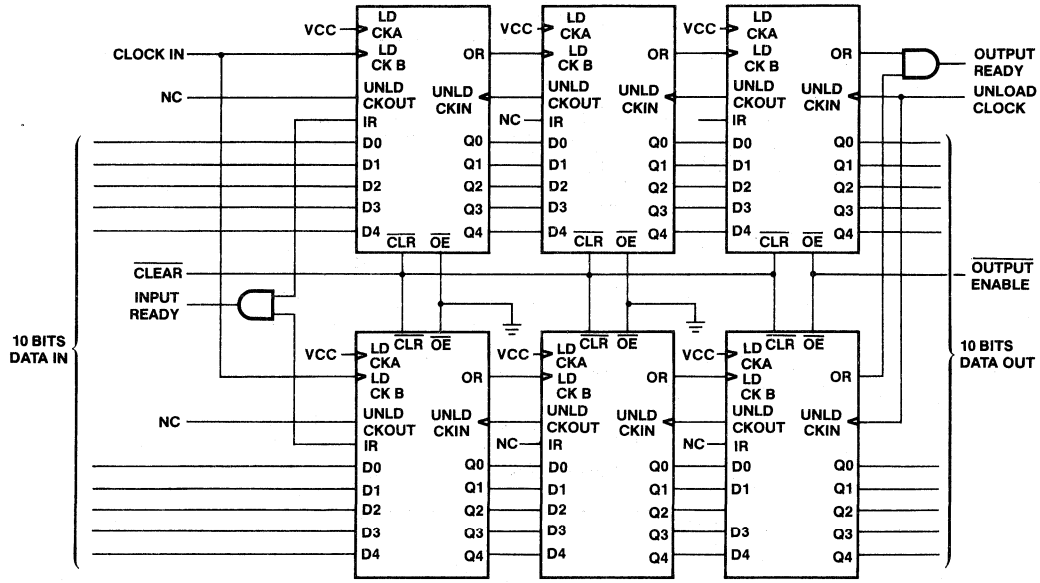


Figure 9. 48x10 FIFO with 74S225/A

First-In First-Out (FIFO) 64x4 64x5 Cascadable Memory

C5/67401 C5/67401A C67401B
C5/67402 C5/67402A C67402B

Features/Benefits

- Choice of 16.7, 15 and 10 MHz shift-out/shift-in rates
- Choice of 4-bit or 5-bit data width
- TTL inputs and outputs
- Readily expandable in the word and bit dimensions
- Structured pinouts. Output pins directly opposite corresponding input pins
- Asynchronous operation
- Pin-compatible with Fairchild's F3341 MOS FIFO and many times faster

Ordering Information

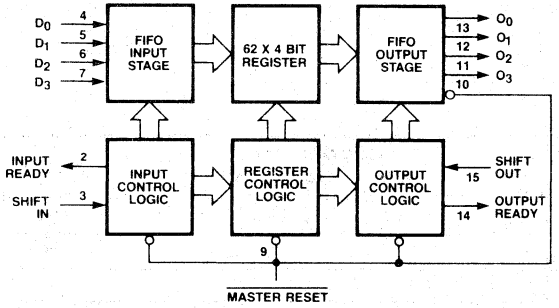
PART NUMBER	PKG	TEMP	DESCRIPTION
C57401	J(20)(L)	Mil	7 MHz 64x4 FIFO
C67401	J,N,NL(20)	Com	10 MHz 64x4 FIFO
C57402	J(20)(L)	Mil	7MHz 64x5 FIFO
C67402	J,N,NL(20)	Com	10 MHz 64x5 FIFO
C57401A	J,(20)(L)	Mil	10 MHz 64x4 FIFO
C67401A	J,N,NL(20)	Com	15 MHz 64x4 FIFO
C57402A	J,(20)(L)	Mil	10 MHz 64x5 FIFO
C67402A	J,N,NL(20)	Com	15 MHz 64x5 FIFO
C67401B	J	Com	16.7 MHz 64x4 FIFO
C67402B	J	Com	16.7 MHz 64x5 FIFO

Description

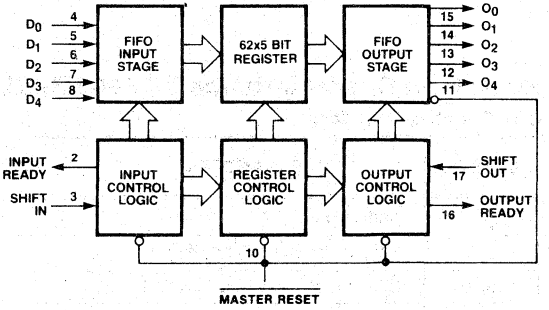
The C5/C67401B/2B/1A/2A/1/2 are "fall-through" high speed First-In First-Out (FIFO) memory organized 64 words by 4 bits and 64 words by 5 bits respectively. A 16.7 MHz data rate allows usage in digital video systems; a 15 MHz data rate allows usage in high speed tape or disc controllers and communications buffer applications. Both word length and FIFO depth are expandable.

Block Diagrams

C57401/A 64x4
C67401A/B 64x4

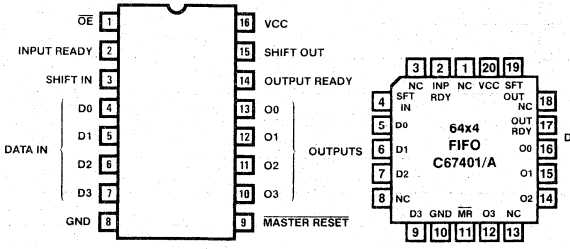


C57402/A 64x5
C67402A/B 64x5

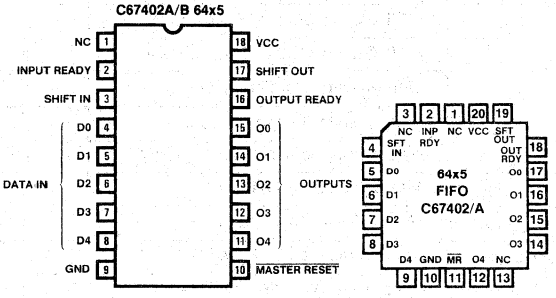


Pin Configurations

C57401/A 64x4
C67401A/B 64x4



C57402/A 64x5
C67402A/B 64x5



Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65° to +150° C

Operating Conditions C67401B/2B

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		75	°C
t_{SIH}†	Shift in HIGH time	1	18			ns
t_{SIL}	Shift in LOW time	1	18			ns
t_{IDS}	Input data setup	1	0			ns
t_{IDH}	Input data hold time	1	40			ns
t_{SOH}†	Shift Out HIGH time	5	18			ns
t_{SOL}	Shift Out LOW time	5	18			ns
t_{MRW}	Master Reset pulse	10	35			ns
t_{MRS}	Master Reset to SI	10	35			ns

Switching Characteristics C67401B/2B

Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	TYP	MAX	UNIT
f_{IN}	Shift in rate	1	16.7			MHz
t_{IRL}	Shift In to Input Ready LOW	1			35	ns
t_{IRH}†	Shift In to Input Ready HIGH	1			37	ns
f_{OUT}	Shift Out rate	5	16.7			MHz
t_{ORL}†	Shift Out to Output Ready LOW	5			38	ns
t_{ORH}†	Shift Out to Output Ready HIGH	5			48	ns
t_{ODH}	Output Data Hold (previous word)	5	5			ns
t_{ODS}	Output Data Shift (next word)	5			44	ns
t_{PT}	Data throughput or "fall through"	4, 8			1.45	μs
t_{MRORL}	Master Reset to OR LOW	10			55	ns
t_{MRIRH}	Master Reset to IR HIGH	10			55	ns
t_{IPH}*	Input Ready pulse HIGH	4	20			ns
t_{OPH}*	Output Ready pulse HIGH	8	20			ns

†See AC test and High Speed application note.
*This parameter applies to FIFOs communicating with each other in a cascaded mode.

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65° to +150° C

Operating Conditions C5/C67401A/2A

SYMBOL	PARAMETER	FIGURE	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		–55		*125	0		75	°C
t_{SIH}†	Shift in HIGH time	1	35			23			ns
t_{SIL}	Shift in LOW time	1	35			25			ns
t_{IDS}	Input data setup	1	0			0			ns
t_{IDH}	Input data hold time	1	45			40			ns
t_{SOH}†	Shift Out HIGH time	5	35			23			ns
t_{SOL}	Shift Out LOW time	5	35			25			ns
t_{MRW}	Master Reset pulse	10	40			35			ns
t_{MRS}	Master Reset to SI	10	45			35			ns

*Case temperature.

Switching Characteristics C5/C67401A/2A Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{IN}	Shift in rate	1	10			15			MHz
t_{IRL}†	Shift In to Input Ready LOW	1			50			40	ns
t_{IRH}†	Shift In to Input Ready HIGH	1			50			40	ns
f_{OUT}	Shift Out rate	5	10			15			MHz
t_{ORL}†	Shift Out to Output Ready LOW	5			65			45	ns
t_{ORH}†	Shift Out to Output Ready HIGH	5			65			50	ns
t_{ODH}	Output Data Hold (previous word)	5	10			10			ns
t_{ODS}	Output Data Shift (next word)	5			60			45	ns
t_{PT}	Data throughput or "fall through"	4, 8			2.2			1.6	μs
t_{MRORL}	Master Reset to OR LOW	10			65			60	ns
t_{MRIRH}	Master Reset to IR HIGH	10			65			60	ns
t_{IPH}*	Input Ready pulse HIGH	4	30			23			ns
t_{OPH}*	Output Ready pulse HIGH	8	30			23			ns

† See AC test and High Speed application note.
* This parameter applies to FIFOs communicating with each other in a cascaded mode.

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65° to +150°C

Operating Conditions C5/C67401/2

SYMBOL	PARAMETER	FIGURE	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		−55		*125	0		75	°C
t_{SIH}†	Shift in HIGH time	1	45			23			ns
t_{SIL}	Shift in LOW time	1	45			35			ns
t_{IDS}	Input data setup	1	0			0			ns
t_{IDH}	Input data hold time	1	55			45			ns
t_{SOH}†	Shift Out HIGH time	5	45			23			ns
t_{SOL}	Shift Out LOW time	5	45			35			ns
t_{MRW}	Master Reset pulse	10	30			35			ns
t_{MRS}	Master Reset to SI	10	45			35			ns

*Case temperature.

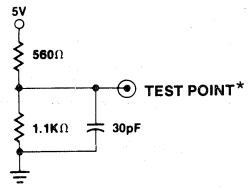
Switching Characteristics C5/C67401/2 Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{IN}	Shift in rate	1	7			10			MHz
t_{IRL}†	Shift In to Input Ready LOW	1			60			45	ns
t_{IRH}†	Shift In to Input Ready HIGH	1			60			45	ns
f_{OUT}	Shift Out rate	5	7			10			MHz
t_{ORL}†	Shift Out to Output Ready LOW	5			65			55	ns
t_{ORH}†	Shift Out to Output Ready HIGH	5			70			60	ns
t_{ODH}	Output Data Hold (previous word)	5	10			10			ns
t_{ODS}	Output Data Shift (next word)	5			65			55	ns
t_{PT}	Data throughput or "fall through"	4, 8			4			3	μs
t_{MRORL}	Master Reset to OR LOW	10			65			60	ns
t_{MRIRH}	Master Reset to IR HIGH	10			65			60	ns
t_{IPH}*	Input Ready pulse HIGH	4	30			23			ns
t_{OPH}*	Output Ready pulse HIGH	8	30			23			ns

† See AC test and High Speed application note.
*This parameter applies to FIFOs communicating with each other in a cascaded mode.

Test Load

* The "TEST POINT" is driven by the output under test, and observed by instrumentation.



Input Pulse 0 to 3 V
Input Rise and Fall Time (10% - 90%)
5 ns minimum
Measurements made at 1.5 V

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage						0.8†	V
V_{IH}	High-level input voltage				2†			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18mA			−1.5	V
I_{IL1}	Low-level input current	D_0-D_n, $\overline{MR}$	V_{CC} = MAX	V_I = 0.45V			−0.8	mA
I_{IL2}		SI, SO					−1.6	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.4V			50	μA
I_I	Maximum input current		VCC = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN	I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN	I_{OH} = −0.9mA	2.4			V
I_{OS}	Output short-circuit current *		V_{CC} = MAX	V_0 = 0V	−20		−90	mA
I_{CC}	Supply current		V_{CC} = MAX Inputs low, outputs open	C5/67401			160	mA
				C5/67402			180	
				C67401A			170	
				C6702A			190	
				C67401B, C57401A			180	
				C67402B, C57402A			200	

*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
†There are absolute voltage with respect to device GND (Pin 8 or 9) and includes all overshoots due to test equipment

8

Functional Description

Data Input

After power up the Master Reset is pulsed low (Fig. 10) to prepare the FIFO to accept data in the first location. When Input Ready (IR) is HIGH the location is ready to accept data from the D_X inputs. Data then present at the data inputs is entered into the first location when the Shift In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. The first word is present at the outputs before a shift out is applied. If the memory is full, IR will remain LOW.

Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device.

Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW, and O_X remains as before, (i.e. data does not change if FIFO is empty). Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

AC Test and High Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 20 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitance and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1 μF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift In-Input Ready combination, as well as the Shift Out-Output Ready combination, timing measurements may be misleading, i.e. rising edge of the Shift-In pulse is not recognized until Input-Ready is High. If Input-Ready is not high due to too high a frequency or FIFO being full or affected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Time (t_{IDH}) and the next activity of Input Ready (t_{IRL}) to be extended relative to Shift-In going High. This same type of problem is also related to t_{IRH}, t_{ORL} and t_{ORH} as related to Shift-Out.

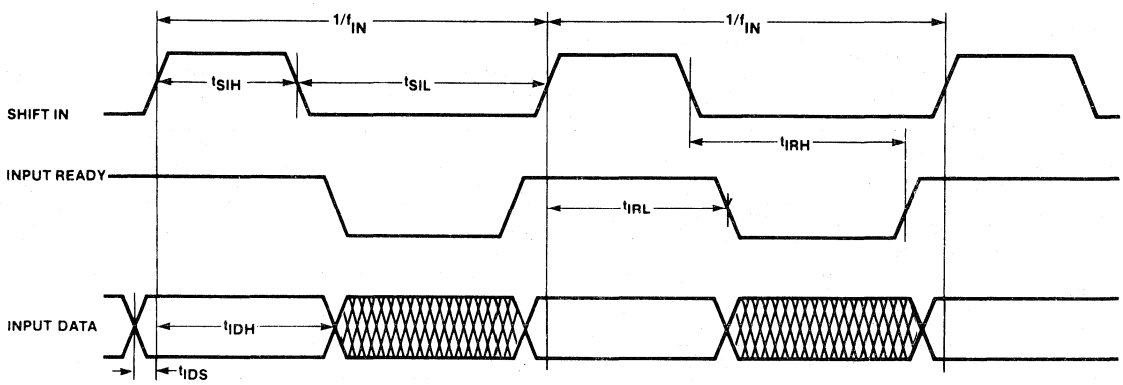


Figure 1. Input Timing

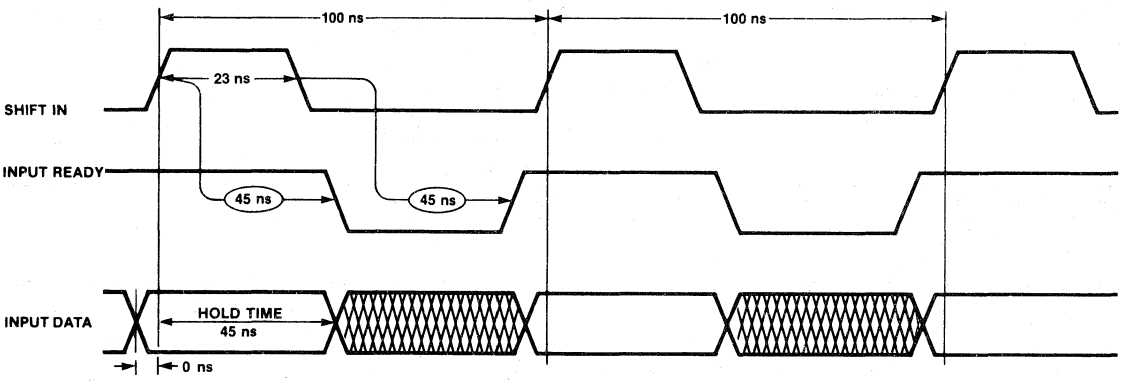


Figure 2. Typical Waveforms for 10 MHz Shift In Data Rate

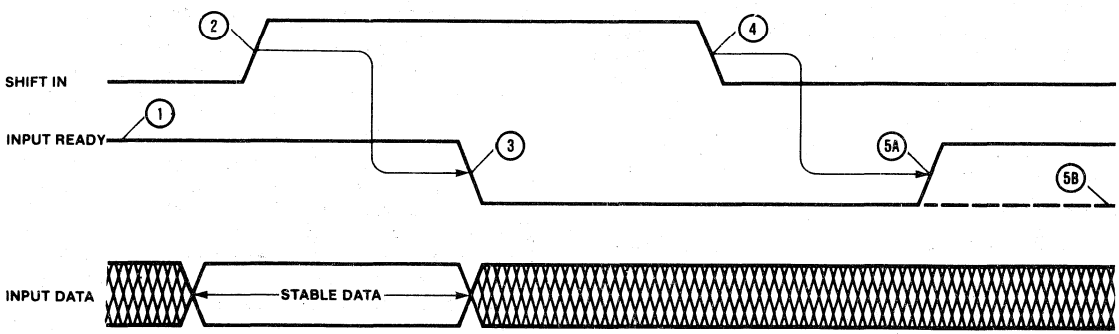


Figure 3. The Mechanism of Shifting Data into the FIFO

(1) Input Ready HIGH indicates space is available and a Shift In pulse may be applied.

(2) Input Data is loaded into the first word.

(3) Input Ready goes LOW indicating the first word is full.

(4) The Data from the first word is released for "fall-through" to second word.

(5A) The Data from the first word is transferred to second word. The first word is now empty as indicated by Input Ready HIGH.

(5B) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

NOTE: Shift In pulses applied while Input Ready is LOW will be ignored (See Figure 4).

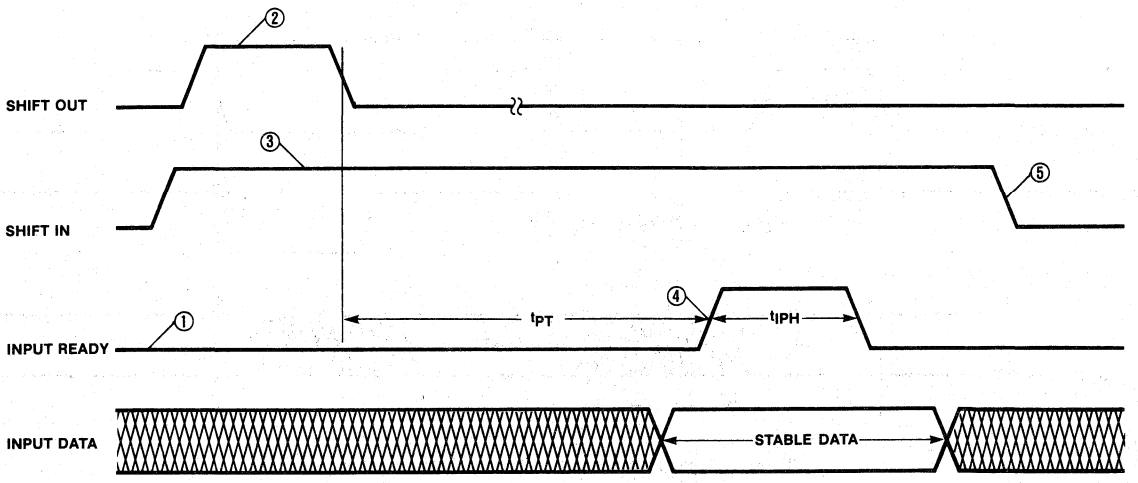
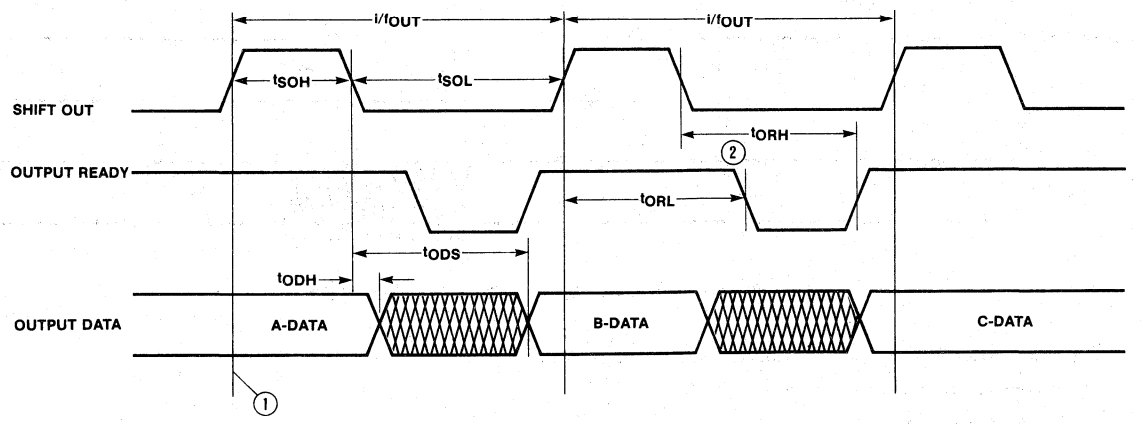


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

(1) FIFO is initially full.
(2) Shift Out pulse is applied. An empty location starts "bubbling" to the front.
(3) Shift In is held HIGH.
(4) As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.
(5) The Data from the first word is released for "fall through" to second word.



(1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively.

(2) Data is shifted out when Shift Out makes a HIGH to LOW transition.

Figure 5. Output Timing

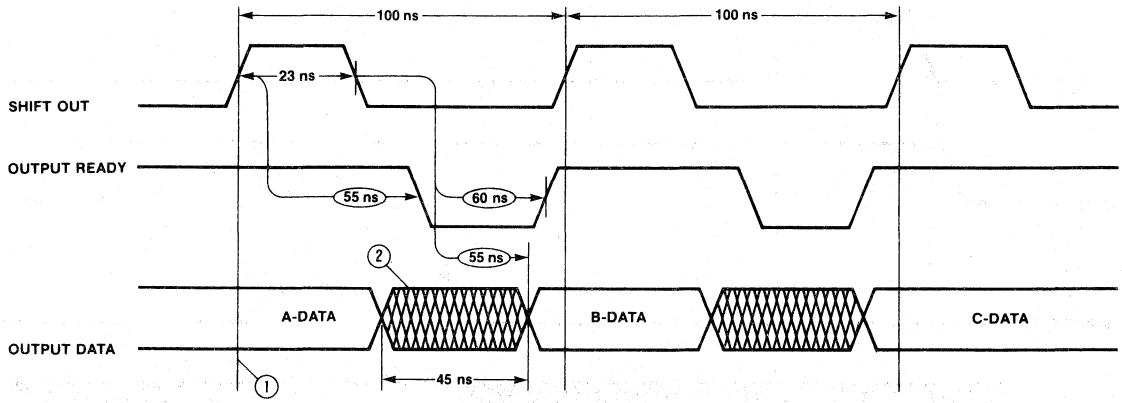


Figure 6. Typical Waveforms for 10 MHz Shift Out Data Rate

(1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively.

(2) Data in the crosshatched region may be A or B Data.

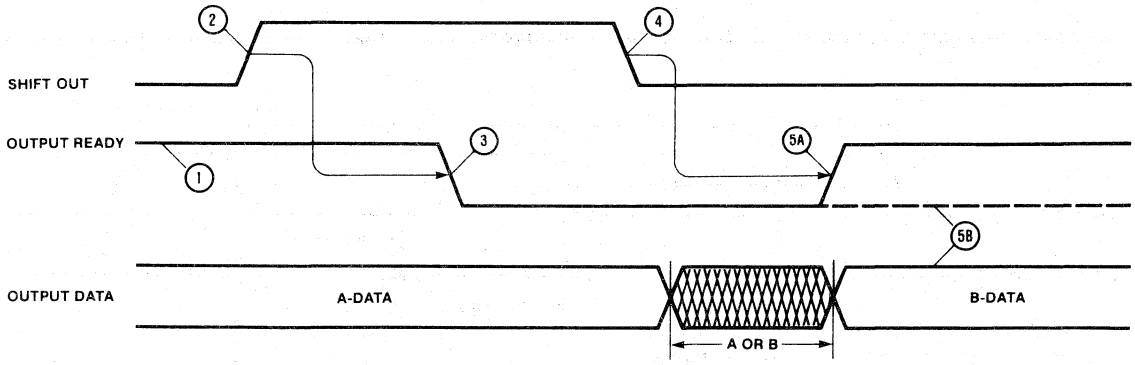


Figure 7. The Mechanism of Shifting Data Out of the FIFO.

(1) Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.

(2) Shift Out goes HIGH causing the next step.

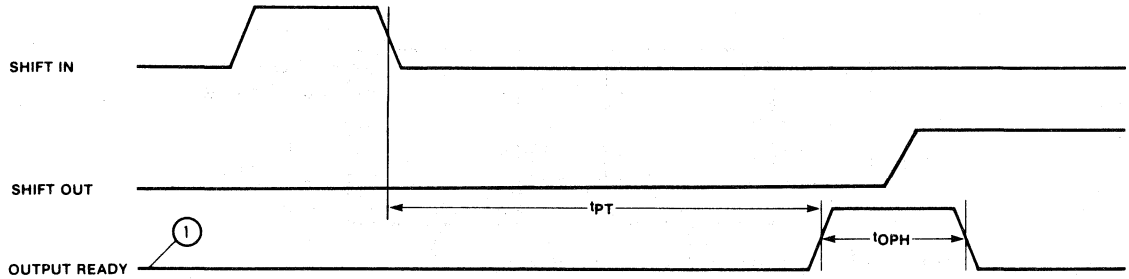
(3) Output Ready goes LOW.

(4) Contents of word 62 (B-DATA) is released for "fall through" to word 63.

(5A) Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.

(5B) If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs.

NOTE: Shift Out pulses applied when Output Ready is LOW will be ignored.



1 FIFO initially empty.

Figure 8. t_{PT} and t_{OPH} Specification

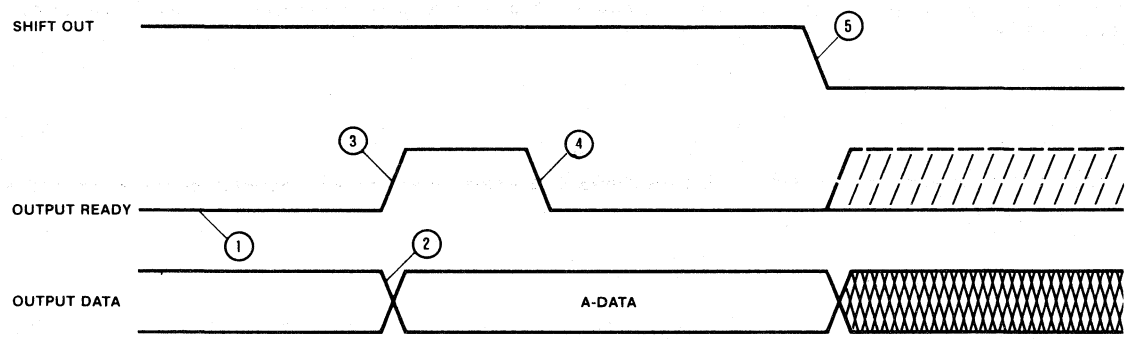
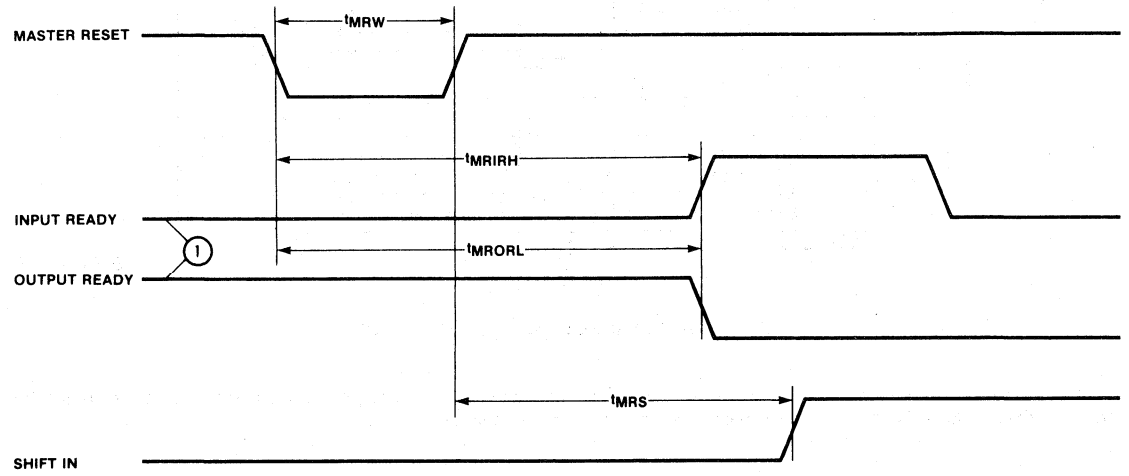


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH.

1. Word 63 is empty.
2. New data (A) arrives at the outputs (word 63).
3. Output Ready goes HIGH indicating the arrival of the new data.
4. Since Shift Out is held HIGH, Output Ready goes immediately LOW.
5. As soon as Shift Out goes LOW the Output Data is subject to change as shown by the dashed line on Output Ready.



1 FIFO initially full.

Figure 10. Master Reset Timing

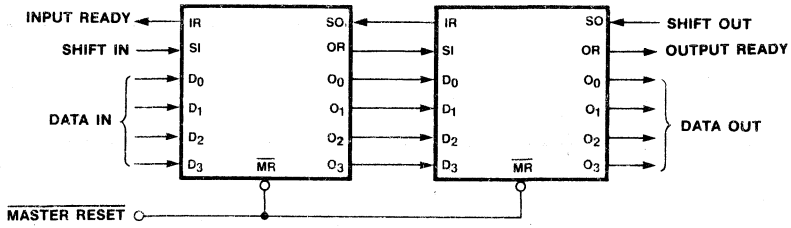


Figure 11. Cascading FIFOs to Form 128x4 FIFO with C5/C67401A/1

FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the FIFOs themselves.

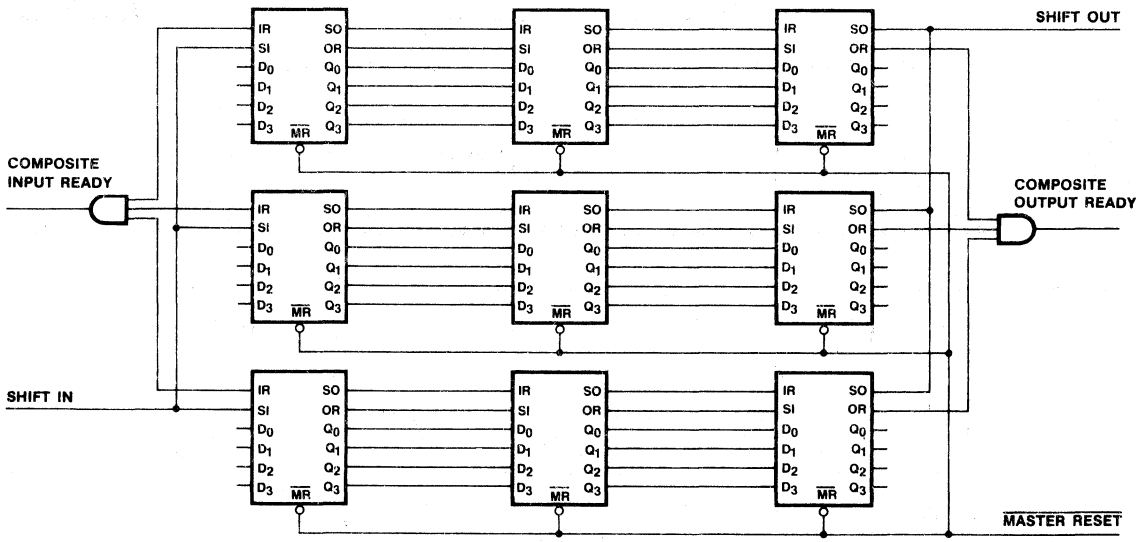
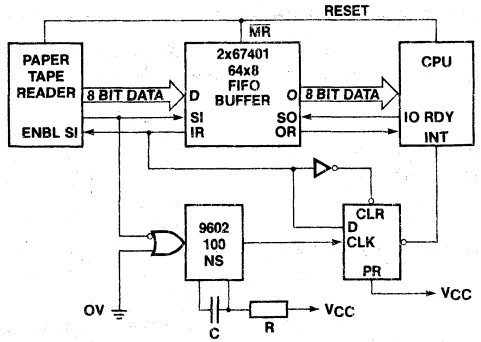


Figure 12. 192x12 FIFO with C5/C67401/1A/1B

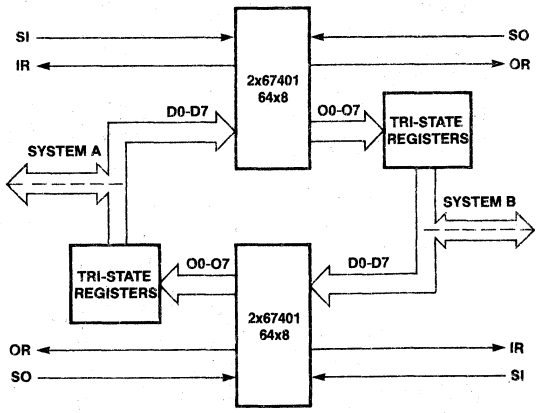
FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This need is due to the different fall-through times of the FIFOs.

Applications



NOTE: The output of monostable holds off the "Buffer full" interrupt for 100ns. If 100ns after shift in, there has not been an input Ready to reset the "D Flip-flop" an interrupt is issued, as the FIFO is full. The CPU then empties the FIFO before the next character is output from the tape drive.

Figure 13. Slow Steady Rate to Fast "Blocked" Rate



NOTE: Both depth and width expansion can be used in this mode. The IR and OR signals are the anded versions of the individual IR and OR signals.

Figure 14. Bidirectional FIFO Application

First-In First-Out (FIFO) 64x4 64x5
Standalone Memory

5/67401 5/67401A 67401B
5/67402 5/67402A 67402B

Features/Benefits

- Choice of 16.7, 15 and 10 MHz shift-out/shift-in rates
- Choice of 4-bit or 5-bit data width
- TTL inputs and outputs
- Readily expandable in the word dimension only
- Structured pin outs. Output pins directly opposite corresponding input pins
- Asynchronous operation
- Pin-compatible with Fairchild's F3341 MOS FIFO and many times as fast

Description

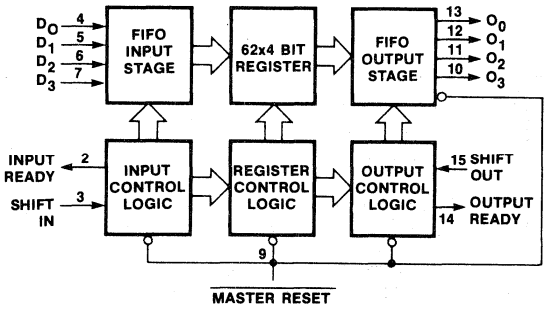
The 5/67401B/2B/1A/2A/1/2 are "fall-through" high speed First-In First-Out (FIFO) memory organized 64 words by 4-bits and 64 words by 5-bits respectively. A 16.7 MHz data rate allows usage in digital video systems; a 15 MHz data rate allows usage in high speed tape or disc controllers and communication buffer applications. Word length is expandable; FIFO depth is not expandable.

Ordering Information

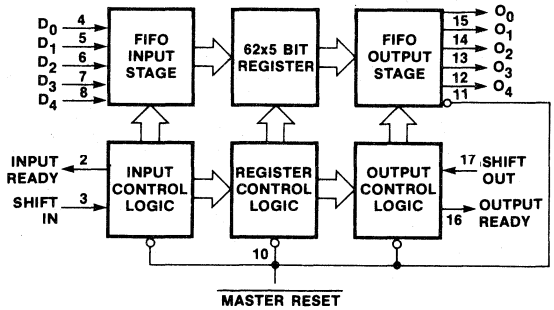
PART NUMBER	PKG	TEMP	DESCRIPTION
57401	J(20)(L)	Mil	7 MHz 64x4 FIFO
67401	J,N,NL(20)	Com	10 MHz 64x4 FIFO
57402	J(20)(L)	Mil	7MHz 64x5 FIFO
67402	J,N,NL(20)	Com	10 MHz 64x5 FIFO
57401A	J,(20)(L)	Mil	10 MHz 64x4 FIFO
67401A	J,N,NL(20)	Com	15 MHz 64x4 FIFO
57402A	J,(20)(L)	Mil	10 MHz 64x5 FIFO
67402A	J,N,NL(20)	Com	15 MHz 64x5 FIFO
67401B	J	Com	16.7 MHz 64x4 FIFO
67402B	J	Com	16.7 MHz 64x5 FIFO

Block Diagrams

67401/A/B 64x4
57401/A 64x4

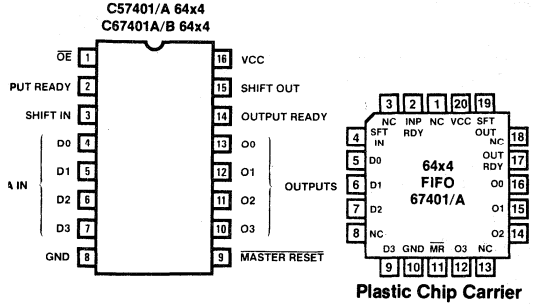


5/67402/A/B 64x5
57402/A 64x5

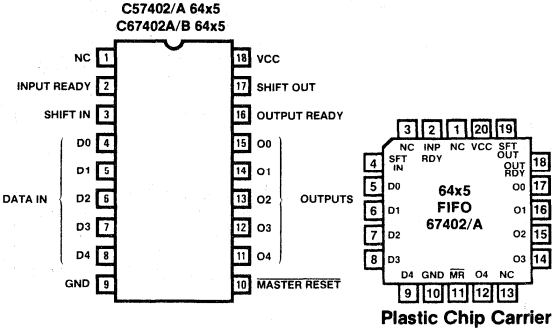


Pin Configurations

C57401/A 64x4
C67401A/B 64x4



C57402/A 64x5
C67402A/B 64x5



TWX: 910-338-2376
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374

Monolithic Memories

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -1.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65° to +150°C

Operating Conditions 67401B/2B

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		75	°C
t_{SIH}†	Shift in HIGH time	1	18			ns
t_{SIL}	Shift in LOW time	1	18			ns
t_{IDS}	Input data setup	1	5			ns
t_{IDH}	Input data hold time	1	40			ns
t_{SOH}†	Shift Out HIGH time	5	18			ns
t_{SOL}	Shift Out LOW time	5	18			ns
t_{MRW}	Master Reset pulse	10	35			ns
t_{MRS}	Master Reset to SI	10	35			ns

8

Switching Characteristics 67401B/2B

Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	TYP	MAX	UNIT
f_{IN}	Shift in rate	1	16.7			MHz
t_{IRL}	Shift In to input ready LOW	1			35	ns
t_{IRH}	Shift In to input ready HIGH	1			37	ns
f_{OUT}	Shift Out rate	5	16.7			MHz
t_{ORL}†	Shift Out to Output Ready LOW	5			38	ns
t_{ORH}†	Shift Out to Output Ready HIGH	5			48	ns
t_{ODH}	Output Data Hold (previous word)	5	5			ns
t_{ODS}	Output Data Shift (next word)	5			44	ns
t_{PT}	Data throughput or "fall through"	4,8			1.45	µs
t_{MRORL}	Master Reset to OR LOW	10			55	ns
t_{MRIRH}	Master Reset to IR HIGH	10			55	ns
t_{IPH}	Input Ready pulse HIGH	4	15			ns
t_{OPH}	Output Ready pulse HIGH	8	15			ns

†See A/C Test and High Speed Application Note.

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65° to +150°C

Operating Conditions 5/67401A/2A

SYMBOL	PARAMETER	FIGURE	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		-55		*125	0		75	°C
t_{SIH}†	Shift in HIGH time	1	35			23		28†	ns
t_{SIL}	Shift in LOW time	1	35			25			ns
t_{IDS}	Input data setup	1	5			5			ns
t_{IDH}	Input data hold time	1	45			40			ns
t_{SOH}†	Shift Out HIGH time	5	35			23			ns
t_{SOL}	Shift Out LOW time	5	35			25			ns
t_{MRW}	Master Reset pulse	10	40			35			ns
t_{MRS}	Master Reset to SI	10	45			35			ns

*Case temperature.

Switching Characteristics 5/67401A/2A

Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{IN}	Shift in rate	1	10			15			MHz
t_{IRL}†	Shift In to Input Ready LOW	1			50			40	ns
t_{IRH}†	Shift In to Input Ready HIGH	1			50			40	ns
f_{OUT}	Shift Out rate	5	10			15			MHz
t_{ORL}†	Shift Out to Output Ready LOW	5			65			45	ns
t_{ORH}†	Shift Out to Output Ready HIGH	5			65			50	ns
t_{ODH}	Output Data Hold (previous word)	5	10			10			ns
t_{ODS}	Output Data Shift (next word)	5			60			45	ns
t_{PT}	Data throughput or "fall through"	4, 8			2.2			1.6	μs
t_{MRORL}	Master Reset to OR LOW	10			65			60	ns
t_{MRIRH}	Master Reset to IR HIGH	10			65			60	ns
t_{IPH}	Input Ready pulse HIGH	4	20			20			ns
t_{OPH}	Output Ready pulse HIGH	8	20			20			ns

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65° to +150°C

Operating Conditions 5/67401/2

SYMBOL	PARAMETER	FIGURE	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		−55		*125	0		75	°C
t_{SIH}†	Shift in HIGH time	1	45			35			ns
t_{SIL}	Shift in LOW time	1	45			35			ns
t_{IDS}	Input data setup	1	10			5			ns
t_{IDH}	Input data hold time	1	55			45			ns
t_{SOH}†	Shift Out HIGH time	5	45			35			ns
t_{SOL}	Shift Out LOW time	5	45			35			ns
t_{MRW}	Master Reset pulse†	10	30			35			ns
t_{MRS}	Master Reset to SI	10	45			35			ns

*Case temperature.

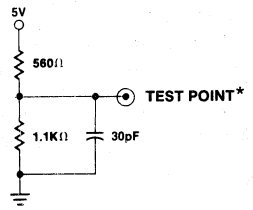
Switching Characteristics 5/67401/2

Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{IN}	Shift in rate	1	7			10			MHz
t_{IRL}†	Shift In to input ready LOW	1			60			45	ns
t_{IRH}†	Shift In to input ready HIGH	1			60			45	ns
f_{OUT}	Shift Out rate	5	7			10			MHz
t_{ORL}†	Shift Out to Output Ready LOW	5			65			55	ns
t_{ORH}†	Shift Out to Output Ready HIGH	5			70			60	ns
t_{ODH}	Output Data Hold (previous word)	5	10			10			ns
t_{ODS}	Output Data Shift (next word)	5			65			55	ns
t_{PT}	Data throughput or "fall through"	4,8			4			3	μs
t_{MRORL}	Master Reset to OR LOW	10			65			60	ns
t_{MRIRH}	Master Reset to IR HIGH	10			65			60	ns
t_{IPH}	Input Ready pulse HIGH	4	20			20			ns
t_{OPH}	Output Ready pulse HIGH	8	20			20			ns

†See AC test and high speed application note.

Test Load



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Input Pulse 0 to 3 V
Input Rise and Fall Time (10% - 90%)
5 ns minimum
Measurements made at 1.5 V

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage						0.8†	V
V_{IH}	High-level input voltage				2†			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18mA			−1.5	V
I_{IL1}	Low-level input current	D_0-D_n, $\overline{MR}$	V_{CC} = MAX	V_I = 0.45V			−0.8	mA
I_{IL2}		SI, SO					−1.6	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.4V			50	μA
I_I	Maximum input current		VCC = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN	I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN	I_{OH} = −0.9mA	2.4			V
I_{OS}	Output short-circuit current *		V_{CC} = MAX	V_O = 0V	−20		−90	mA
I_{CC}	Supply current		V_{CC} = MAX Inputs low, outputs open.	5/67401			160	
				5/67402			180	
				67401A			170	
				67402A			190	
				67401B, 57401A			180	
				67402B, 57402A			200	

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
†There are absolute voltages with respect to degree GND (PIN 8 or 9) and includes all overshoots due to test equipment.

Functional Description

Data Input

After power up the Master Reset is pulsed low (Fig. 10) to prepare the FIFO to accept data in the first location. When Input Ready (IR) is HIGH the location is ready to accept data from the D_X inputs. Data then present at the data inputs is entered into the first location when the Shift In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. The first word is present at the outputs before a shift out is applied. If the memory is full, IR will remain LOW.

Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device.

Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW, and O_X remains as before, (i.e. data does not change if FIFO is empty).

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

AC Test and High Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 20 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitance and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1 μF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift In-Input Ready combination, as well as the Shift Out-Output Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input-Ready is High.If Input-Ready is not high due to too high a frequency or FIFO being full or affected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Time (t_{IDH}) and the next activity of Input Ready (t_{IRL}) to be extended relative to Shift-In going High. This same type of problem is also related to t_{IRH}, t_{ORL} and t_{ORH} as related to Shift-Out.

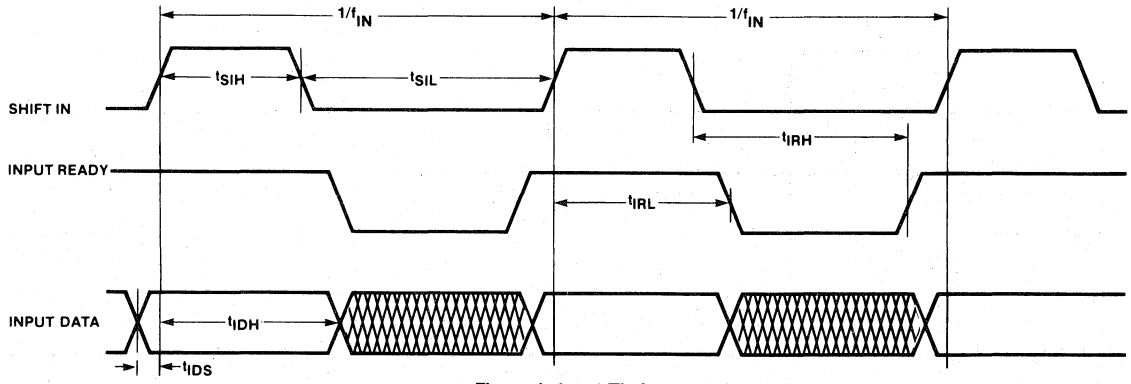


Figure 1. Input Timing

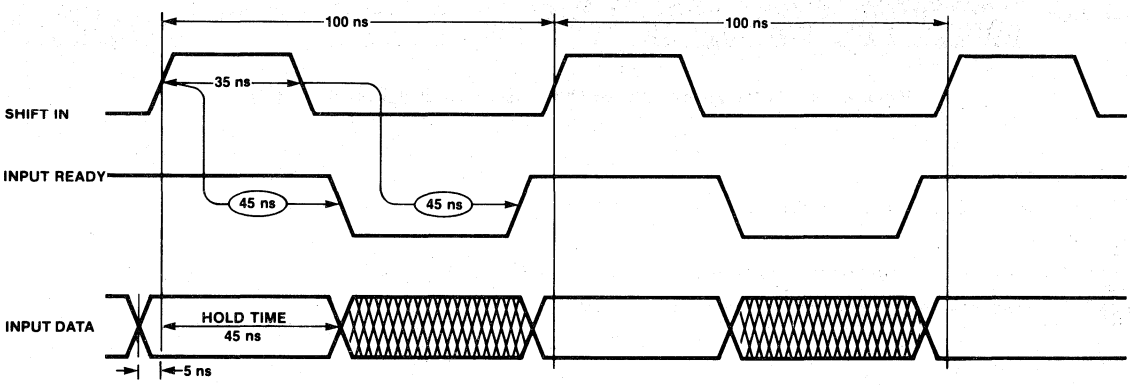


Figure 2. Typical Waveforms for 10 MHz Shift In Data Rate (67401/2)

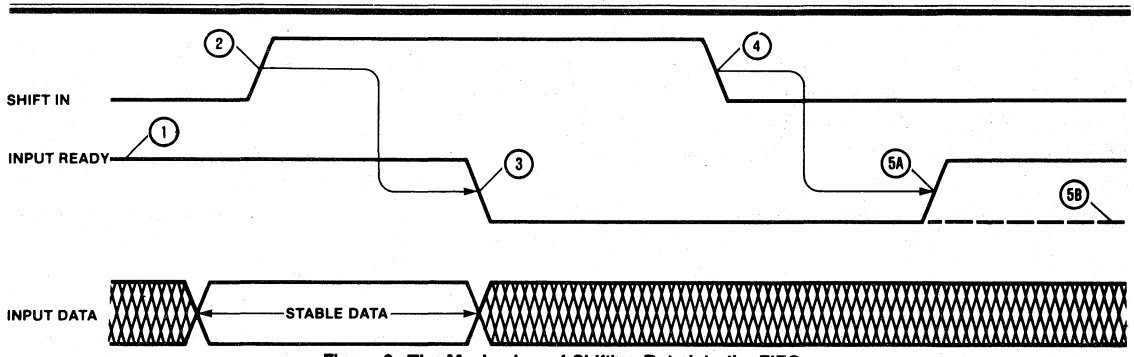


Figure 3. The Mechanism of Shifting Data into the FIFO

(1) Input Ready HIGH indicates space is available and a Shift In pulse may be applied.

(2) Input Data is loaded into the first word.

(3) Input Ready goes LOW indicating the first word is full.

(4) The Data from the first word is released for "fall-through" to second word.

(5A) The Data from the first word is transferred to second word. The first word is now empty as indicated by Input Ready HIGH.

(5B) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

NOTE: Shift In pulses applied while Input Ready is LOW will be ignored. (See Figure 4.)

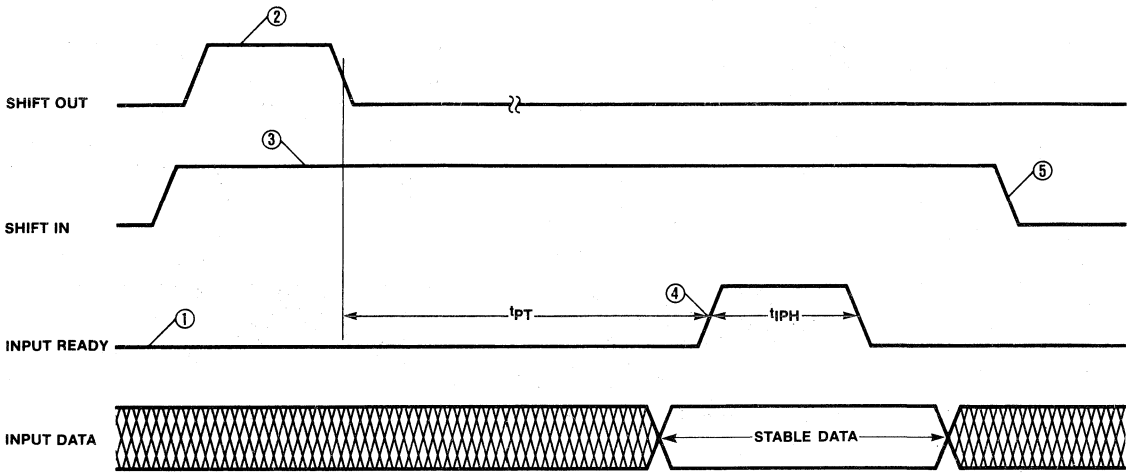


Figure 4. Data is Shifted In Whenever Shift In and Input Ready are Both HIGH

(1) FIFO is initially full.

(2) Shift Out pulse is applied. An empty location starts "bubbling" to the front.

(3) Shift In is held HIGH.

(4) As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.

(5) The Data from the first word is released for "fall through" to second word.

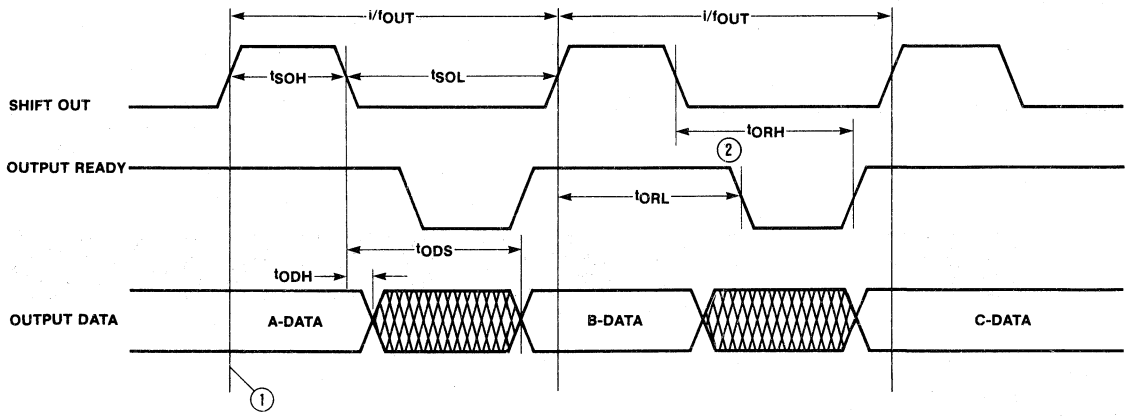


Figure 5. Output Timing

(1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively.

(2) Data is shifted out when Shift Out makes a HIGH to LOW transition.

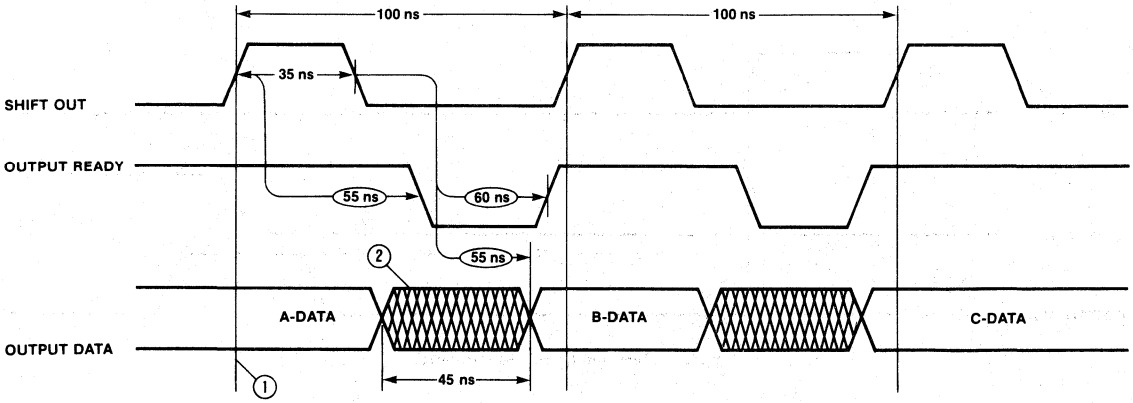


Figure 6. Typical Waveforms for 10 MHz Shift Out Data Rate (67401/2)

(1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively.

(2) Data in the crosshatched region may be A or B Data.

8

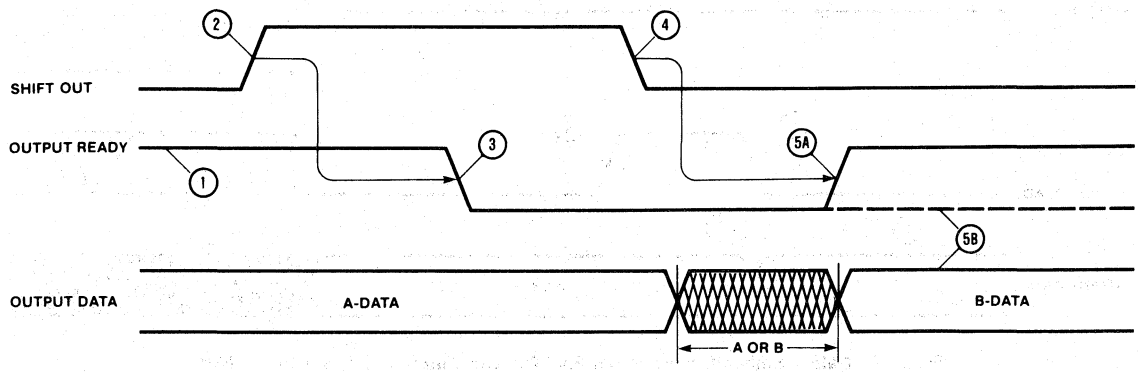


Figure 7. The Mechanism of Shifting Data Out of the FIFO.

(1) Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.

(2) Shift Out goes HIGH causing the next step.

(3) Output Ready goes LOW.

(4) Contents of word 62 (B-DATA) is released for "fall through" to word 63.

(5A) Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.

(5B) If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs.

NOTE: Shift Out pulses applied when Output Ready is LOW will be ignored.

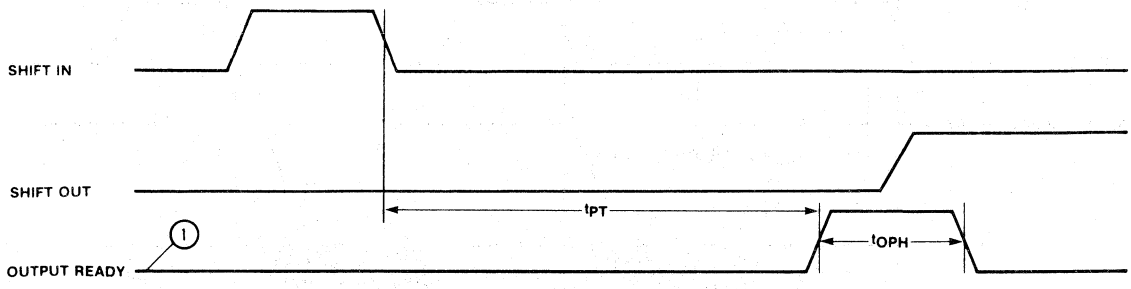


Figure 8. t_{PT} and t_{OPH} Specification

(1) FIFO initially empty.

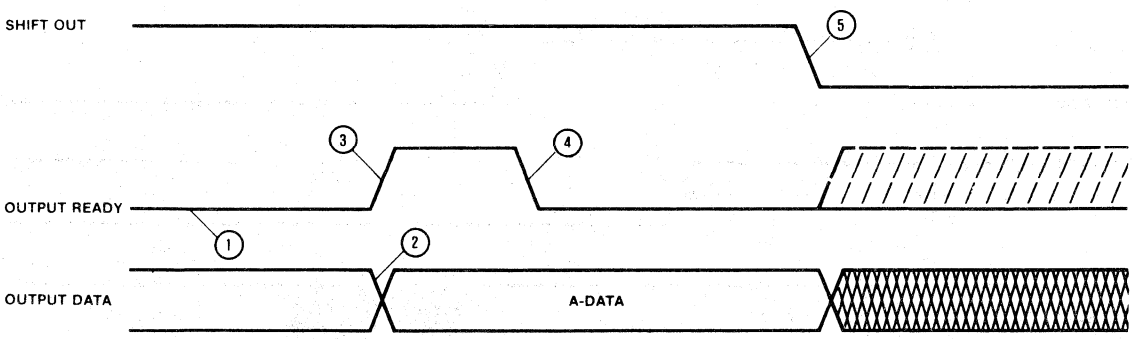


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH.

(1) Word 63 is empty.

(2) New data (A) arrives at the outputs (word 63).

(3) Output Ready goes HIGH indicating the arrival of the new data.

(4) Since Shift Out is held HIGH, Output Ready goes immediately LOW.

(5) As soon as Shift Out goes LOW the Output Data is subject to change as shown by the dashed line on Output Ready.

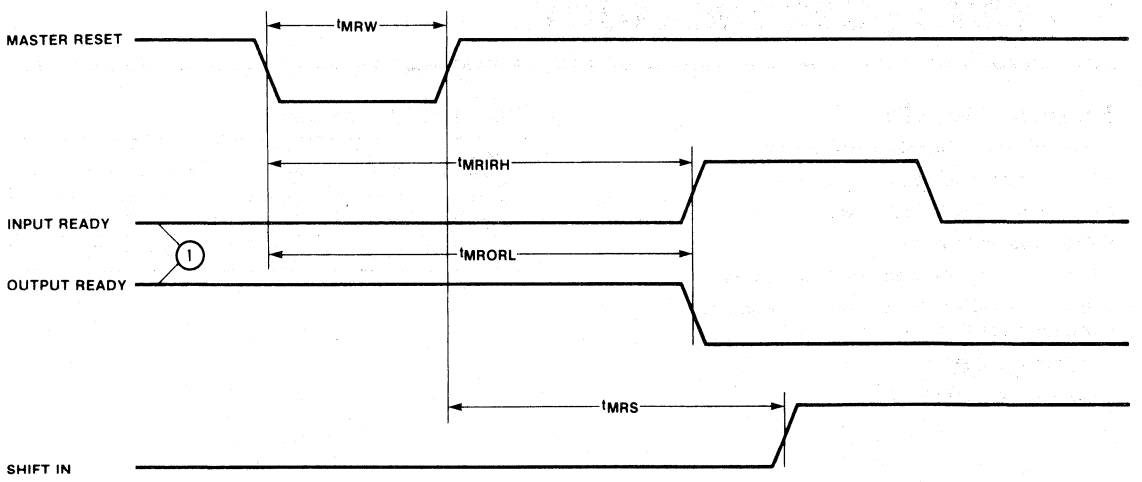


Figure 10. Master Reset Timing

(1) FIFO initially full.

First-In First-Out (FIFO) 64x4 64x5 Memory 15 MHz (Cascadable)

C67L401D C67L402D

Features/Benefits

- High-speed 15-MHz shift-in/shift-out rates
- Low power consumption
- Choice of 4-bit or 5-bit data width
- TTL inputs and outputs
- Readily expandable in word width and depth
- Structured pinouts. Output pins directly opposite corresponding input pins
- High-drive capability
- Asynchronous operation

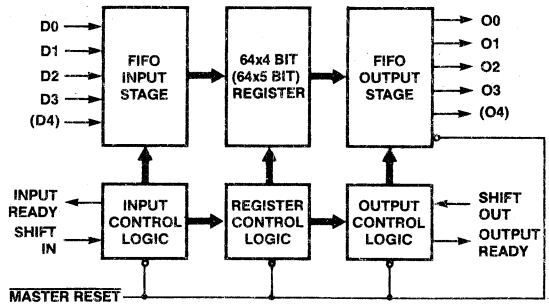
Ordering Information

PART NUMBER	PKG	TEMP	DESCRIPTION
C67L401D	N, J	Com	15 MHz 64x4 FIFO
C67L402D	N, J	Com	15 MHz 64x5 FIFO

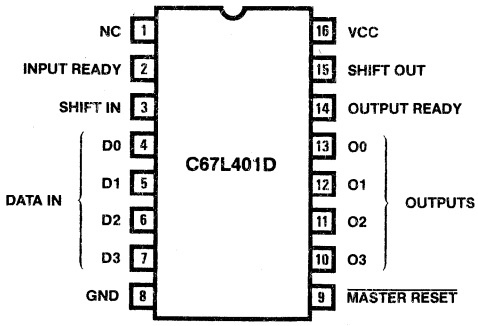
Description

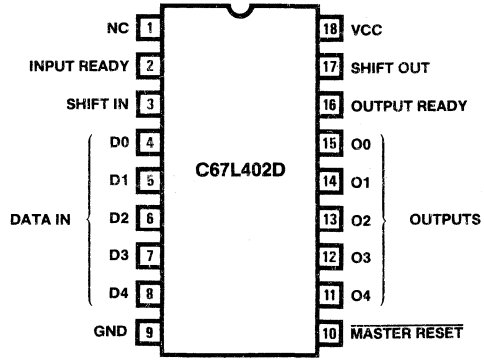
The C67L401D/2D are "fall-through" high-speed First-In First-Out (FIFO) memories organized 64 words by 4 bits and 64 words by 5 bits respectively. The FIFO is expandable in word width and depth. The FIFO is attractive for many applications such as disk controllers, communication buffers, rate buffers, etc. They feature high-drive (I_{OL} = 24 mA) outputs.

C67L401D
(C67L402D)



Pin Configurations





2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65°C to +150°C

Operating Conditions Over Temperature Range

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		70	°C
f_{IN}	Shift in rate	1			15	MHz
t_{SIH}	Shift in High time	1	24			ns
t_{SIL}	Shift in Low time		15			
t_{IDS}	Input data setup to SI (Shift In)	1	0			ns
t_{IDH}	Input data hold from SI (Shift In)	1	26			ns
t_{RIDS}	Input data setup to IR (Input Ready)	4	0			ns
t_{RIDH}	Input data hold from IR (Input Ready)	4	26			ns
f_{OUT}	Shift out rate	5			15	MHz
t_{SOH}	Shift out High time	5	17			ns
t_{SOL}	Shift out Low time		15			
t_{MRW}	Master Reset pulse**	10	35			ns
t_{MRS}	Master Reset to SI*	10	35			ns

* If the FIFO is not full (IR High), $\overline{MR}$ low forces IR low, followed by IR returning high when $\overline{MR}$ goes high.
** See AC test and high-speed application note.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITION		COMMERCIAL MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage						0.8**	V
V_{IH}	High-level input voltage				2**			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = -18 mA			-1.5	V
I_{IL}	Low-level input current		V_{CC} = MAX	V_I = 0.45 V			-250	μA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.4 V			50	μA
I_I	Maximum input current		V_{CC} = MAX	V_I = 5.5 V			1	mA
V_{OL}	Low-level Output voltage	Output, O	V_{CC} = MIN	I_{OL} = 24 mA			0.5	V
		IR, OR	V_{CC} = MIN	I_{OL} = 8 mA				
V_{OH}	High-level Output voltage	Output, O	V_{CC} = MIN	I_{OH} = -3.0 mA	2.4			V
		IR, OR	V_{CC} = MIN	I_{OH} = -0.9 mA				
I_{OS}	Output short-circuit current*		V_{CC} = MAX	V_O = 0V	-20		-90	mA
I_{CC}	Supply current		V_{CC} = MAX All inputs low. All outputs open.	L401D/2D			100	mA

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
** These are absolute voltages with respect to GND (Pin 8 or 9) and include all overshoots due to test equipment

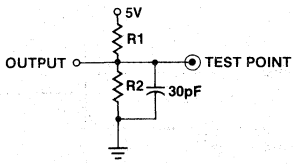
Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	TYP	MAX	UNIT
t_{IRL}†	Shift In ↑ to Input Ready LOW	1			40	ns
t_{IRH}†	Shift In ↓ to Input Ready HIGH				26	ns
t_{ORL}†	Shift Out ↑ to Output Ready LOW	5			45	ns
t_{ORH}†	Shift Out ↓ to Output Ready HIGH				50	ns
t_{ODH}†	Output Data Hold (previous word)		12			ns
t_{ODS}	Output Data Shift (next word)				40	ns
t_{PT}	Data throughput	4,8			1600	ns
t_{MRORL}	Master Reset ↓ to Output Ready LOW	10			60	ns
t_{MRIRH}*	Master Reset ↑ to Input Ready HIGH				30	ns
t_{MRIRL}*	Master Reset ↓ to Input Ready LOW				50	ns
t_{MRO}	Master Reset ↓ to Outputs LOW				60	ns
t_{IPH}	Input ready pulse HIGH	4	17			ns
t_{OPH}	Output ready pulse HIGH	8	24			ns
t_{ORD}	Output ready ↑ to Data Valid	5			-3	ns

* If the FIFO is not full (IR High), $\overline{MR}$ low forces IR low, followed by IR returning high when $\overline{MR}$ goes high.

† See AC test and high-speed application note.

Standard Test Load



I_{OL}	R1	R2
24 mA	200 Ω	300 Ω
8 mA	600 Ω	1200 Ω

Input Pulse Amplitude = 3 V
Input Rise and Fall Time (10%–90%) = 2.5 ns
Measurements made at 1.5 V

8

Functional Description

Data Input

After power up the Master Reset is pulsed low (Figure 10) to prepare the FIFO to accept data in the first location. Master reset must be applied prior to use to ensure proper operation. When Input Ready (IR) is HIGH the first location is ready to accept data from the D_X inputs. Data then present at the data inputs is entered into the first location when the Shift-In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Once data is entered into the first cell, the transfer of data from any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating more room is available. If the memory is full, IR will remain LOW. The FIFO should always be cleared by using master reset.

Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided the upstream stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW and Data output will not be valid.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

AC Test and High-Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 20 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. Monolithic Memories recommends a monolithic ceramic capacitor of 0.1 μF directly between VCC and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input-Ready combination, as well as the Shift-Out-Output-Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input Ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or effected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input

Data Hold time (T_{IDH}) and the next activity of Input Ready (T_{IRL}) to be extended relative to shift-in going HIGH. This same type of situation occurs with T_{ORL} and T_{ORH} as related to Shift-Out. For high-speed applications, proper grounding technique is essential.

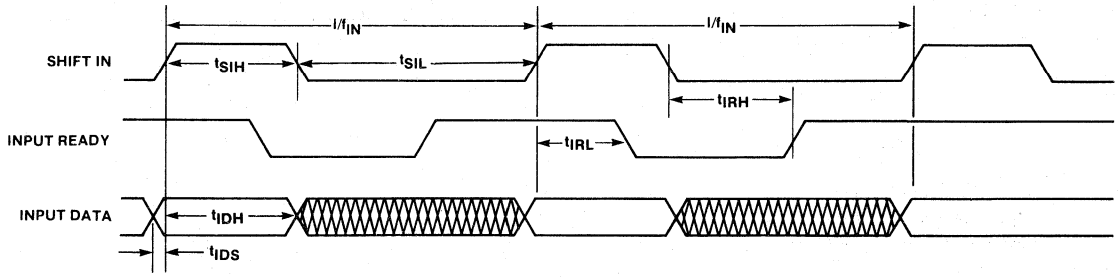


Figure 1. Input Timing

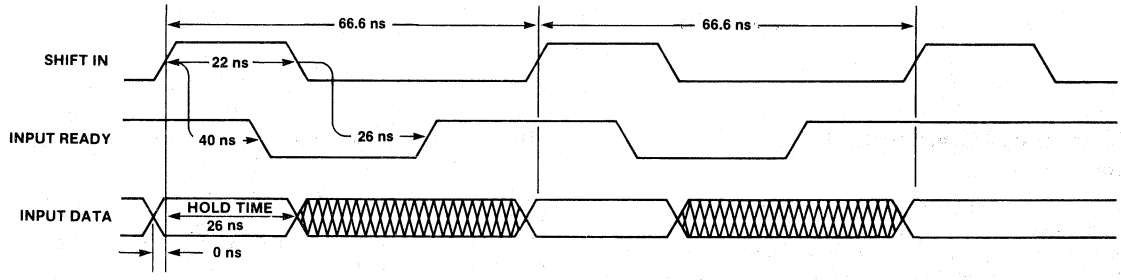


Figure 2. Typical Waveforms for 15-MHz Shift-In Rate

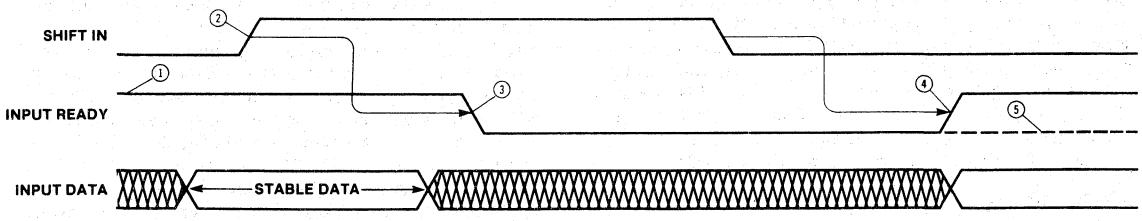


Figure 3. The Mechanism of Shifting Data into the FIFO

(1) Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.
(2) Input Data is loaded into the first word. The Data from the first word is released for "fall-through" to second word.
(3) Input Ready goes LOW indicating the first word is full.
(4) Shift-In going LOW allows Input Ready to sense the status of first word. The first word is now empty as indicated by Input Ready HIGH.
(5) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.
NOTE: Shift-In pulses applied while Input Ready is LOW will be ignored

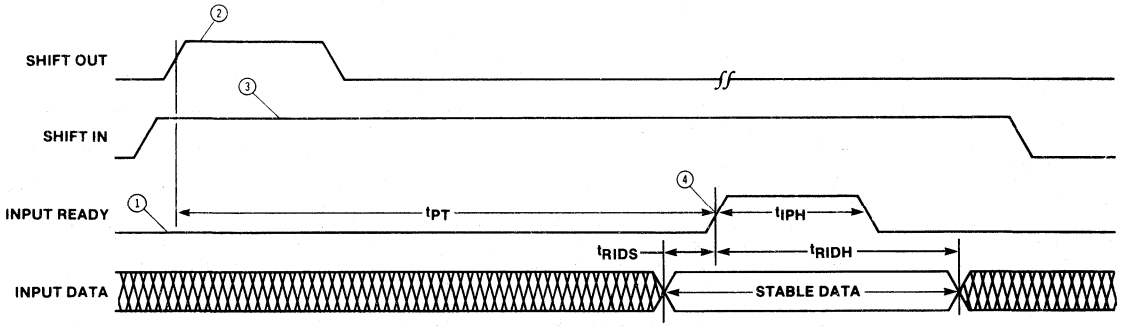


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

① FIFO is initially full.

② Shift Out pulse is applied. An empty location starts "bubbling" to the front.

③ Shift In is held HIGH

④ As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.

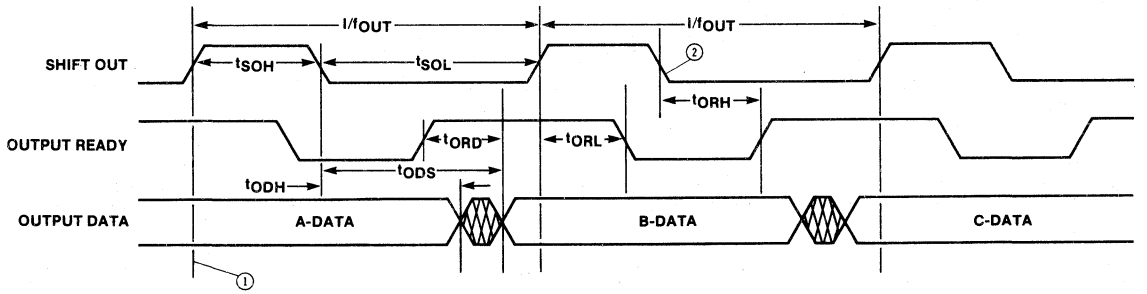


Figure 5. Output Timing

① The diagram assumes that at this time, words 63, 62 and 61 are loaded with A, B and C Data, respectively.

② Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e. OR and SO are both high together.

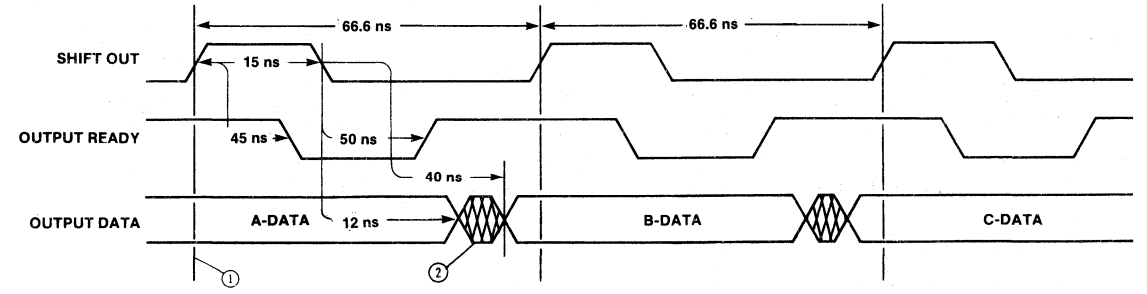


Figure 6. Typical Waveforms for 15-MHz Shift-Out Data Rate

① The diagram assumes that at this time words 63, 62 and 61 are loaded with A, B and C Data, respectively.

② Data in the first crosshatched region may be A or B Data.

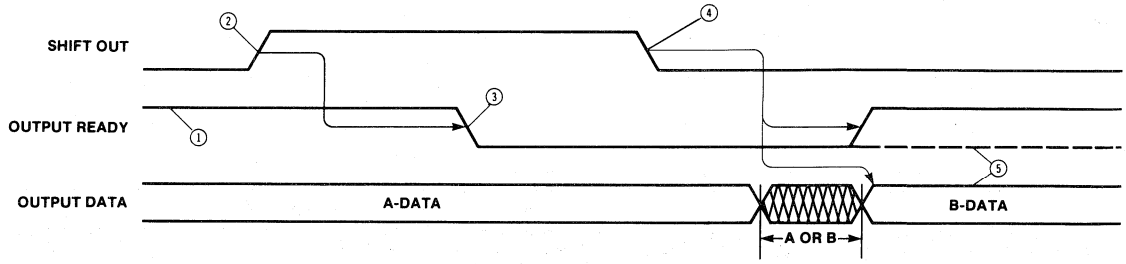


Figure 7. The Mechanism of Shifting Data Out of the FIFO

(1) Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.

(2) Shift-Out goes HIGH causing the contents of word 62 (B-Data) to be released for fall-through to word 63. Output data remains as valid A-Data while Shift-Out is HIGH.

(3) Output Ready goes LOW.

(4) Shift-out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.

(5) If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data becomes invalid.

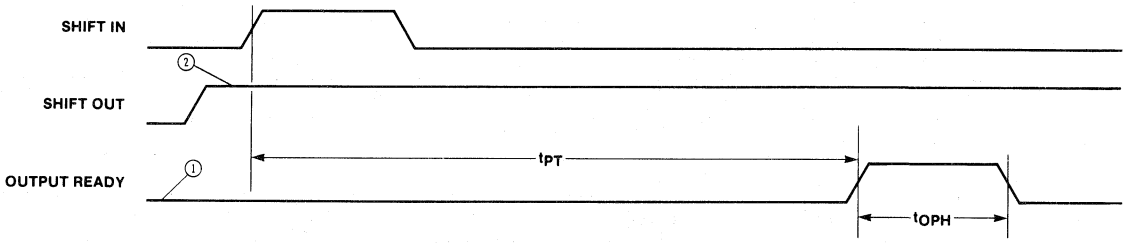


Figure 8. t_{PT} and t_{OPH} Specification

(1) FIFO initially empty.

(2) Shift Out held HIGH

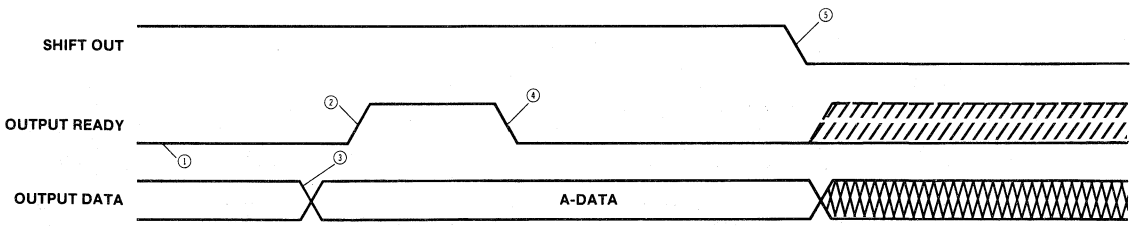


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH.

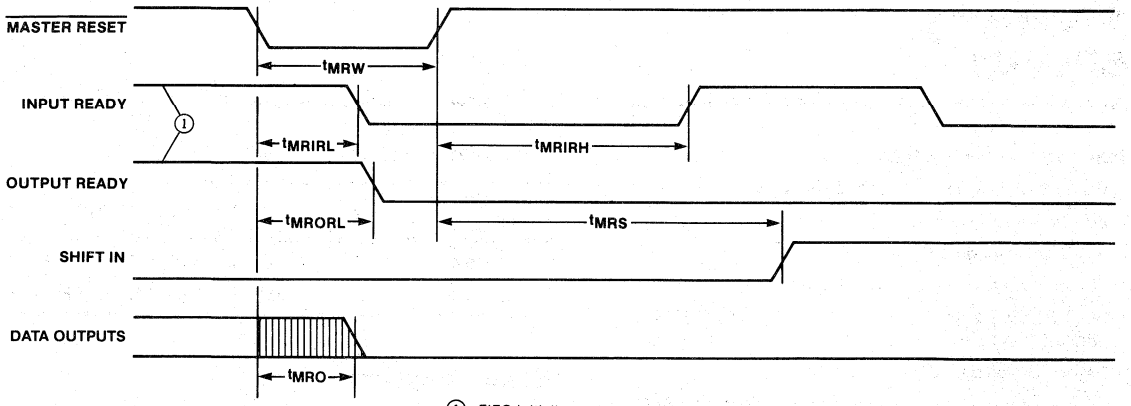
(1) Word 63 is empty.

(2) Output Ready goes HIGH indicating arrival of the new data.

(3) New data (A) arrives at the outputs (word 63).

(4) Since Shift Out is held HIGH, Output Ready goes immediately LOW.

(5) As soon as Shift Out goes LOW the Output Data is subject to change. Output Ready will go HIGH or LOW depending on whether there are any additional upstream words in the FIFO.



1 FIFO initially partially full.

Figure 10. Master Reset Timing

Low Power First-In First-Out (FIFO) 64x4 Memory
67L401

Features/Benefits

- Guaranteed 5 MHz shift-out/shift-in rates
- Low Power Consumption
- TTL inputs and outputs
- Readily expandable in the bit dimensions
- Structured pinouts. Output pins directly opposite corresponding input pins
- Asynchronous operation
- Pin compatible with Fairchild's F3341 MOS FIFO and much faster

Description

The 67L401 is a low-power First-In First-Out (FIFO) memory device with TTL speed. This device is organized in a 64x4-bit structure and easily expandable to any width. A 5 MHz data rate with fast "fall through" time allows usage in tape and disc controllers, printers and communications buffer applications. This data rate is much faster than a comparable MOS device. The FIFO is a register-based device. Data entered at the inputs "falls through" to the empty space closest to the output. Data is shifted out in the same sequence it is shifted in. Also, the width can be increased by putting the Input Ready signals through an AND gate to give a composite Input Ready. Similarly, the Output Ready signals should be gated to form a composite Output Ready.

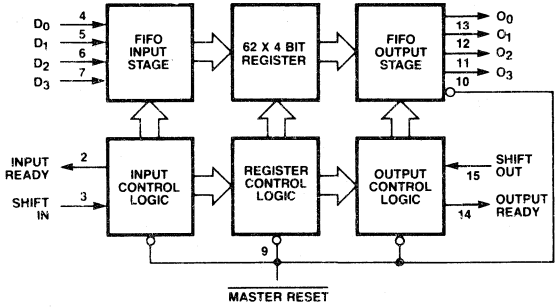
Generally, FIFOs are used in digital systems performing data transfers when source and receiver are not operating at the same data rate. FIFOs are also used as data buffers where the source and receiver are not operating at the same time. The 67L401 is particularly useful where low-power consumption is critical.

Ordering Information

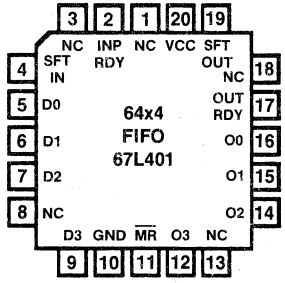
PART NUMBER	PKG	TEMP	DESCRIPTION
67L401	N, NL	COM	5 MHz 64x4 FIFO
67L401	J, NL	COM	5 MHz 64x4 FIFO

Block Diagram

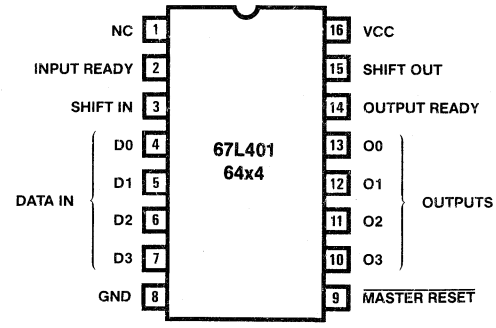
67L401 64x4



Pin Configurations



Plastic Chip Carrier



2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories

Absolute Maximum Ratings

Supply voltage V_{CC} ..... −0.5 V to 7 V
Input voltage ..... −1.5 V to 7 V
Off-state output voltage ..... −0.5 V to 5.5 V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		75	°C
t_{SIH}†	Shift in HIGH time	1	55			ns
t_{SIL}	Shift in LOW time	1	55			ns
t_{IDS}	Input data setup	1	10			ns
t_{IDH}	Input data hold time	1	80			ns
t_{SOH}†	Shift Out HIGH time	5	55			ns
t_{SOL}	Shift Out LOW time	5	55			ns
t_{MRW}	Master Reset pulse	10	40			ns
t_{MRS}	Master Reset to SI	10	35			ns

8

Switching Characteristics Over Operating Conditions

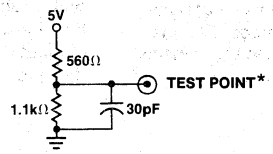
SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{IN}	Shift in rate	1	5			MHz
t_{IRL}†	Shift in to Input Ready LOW	1			75	ns
t_{IRH}†	Shift in to Input Ready HIGH	1			75	ns
f_{OUT}	Shift Out rate	5	5			MHz
t_{ORL}†	Shift Out to Output Ready LOW	5			75	ns
t_{ORH}†	Shift Out to Output Ready HIGH	5			80	ns
t_{ODH}	Output Data Hold (previous word)	5	8			ns
t_{ODS}	Output Data Shift (next word)	5			70	ns
t_{PT}	Data throughput or "fall through"	4, 8			4	μs
t_{MRORL}	Master Reset to OR LOW	10			85	ns
t_{MRIRH}	Master Reset to IR HIGH	10			85	ns
t_{IPH}*	Input Ready pulse HIGH	4	20			ns
t_{OPH}*	Output Ready pulse HIGH	8	20			ns

† See AC test and application note.

* This parameter applies to FIFOs communicating with each other in a cascade mode.

Test Load

* The "TEST POINT" is driven by the output under test, and observed by instrumentation.



Input Pulse 0 to 3 V
Input Rise and Fall Time (10% - 90%)
5 ns minimum
Measurements made at 1.5 V

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2†			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = -18mA			-1.5	V
I_{IL1}	Low-level	D_0-D_3 MR	V_{CC} = MAX	V_I = 0.45V			-0.8	mA
I_{IL2}	input current	SI, SO					-1.6	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.4V			50	μA
I_I	Maximum input current		V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN	I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN	I_{OH} = -0.9mA	2.4			V
I_{OS}	Output short-circuit current*		V_{CC} = MAX	V_O = 0V	-20		-90	mA
I_{CC}	Supply Current		V_{CC} = MAX	Inputs Low, Outputs Open		95	110	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† This is an absolute voltage with respect to device GND (Pin 8 or 9) and includes all overshoots due to test equipment.

Functional Description

Data Input

After power up the Master Reset is pulsed low (Fig. 11) to prepare the FIFO to accept data in the first location. When Input Ready (IR) is HIGH the location is ready to accept data from the D_X inputs. Data then present at the data inputs is entered into the first location when the Shift In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. The first word is present at the outputs before a shift out is applied. If the memory is full, IR will remain LOW.

Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device.

Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW, and O_X remains as before, (i.e. data does not change if FIFO is empty).

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

AC Test and Application Note

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing. Though the external data rate is 5 MHz internally the device is several times as fast. Device grounding and decoupling is crucial to correct operation, as the FIFO will respond to very small glitches caused by long reflective lines, high capacitances and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1 μF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in timing set up and measurement of parameters. For example, since an AND gate function is associated with both the Shift In-Input Ready Combination, as well as the Shift Out-Output Ready Combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input-Ready is High.If Input-Ready is not high due to too high a frequency, or the FIFO being full or affected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Time (t_{IDH}) and the next activity of Input Ready (t_{IRL}) to be extended relative to Shift-In going High.

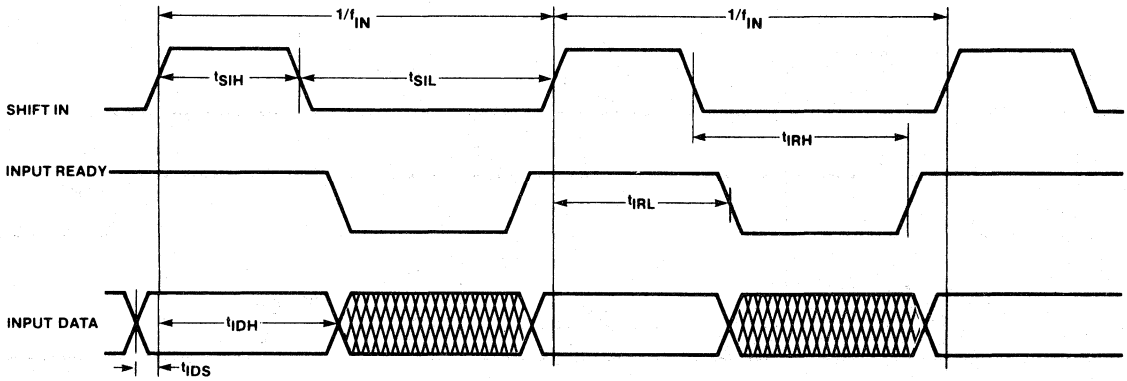


Figure 1. Input Timing

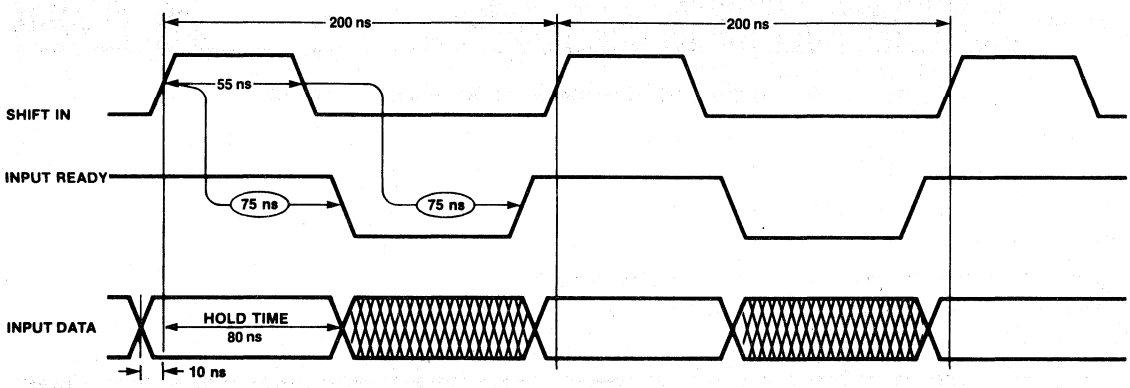


Figure 2. Typical Waveforms for 5-MHz Shift In Data Rate

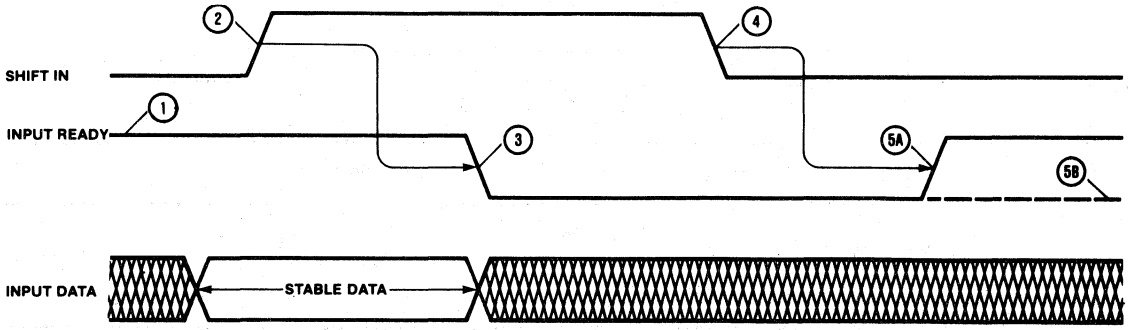


Figure 3. The Mechanism of Shifting Data Into the FIFO

(1) Input Ready HIGH indicates space is available and a Shift In pulse may be applied.

(2) Input Data is loaded into the first word.

(3) Input Ready goes LOW indicating the first word is full.

(4) The Data from the first word is released for "fall-through" to second word.

(5A) The Data from the first word is transferred to second word. The first word is now empty as indicated by Input Ready HIGH.

(5B) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

NOTE: Shift In pulses applied while Input Ready is LOW will be ignored (See Figure 5).

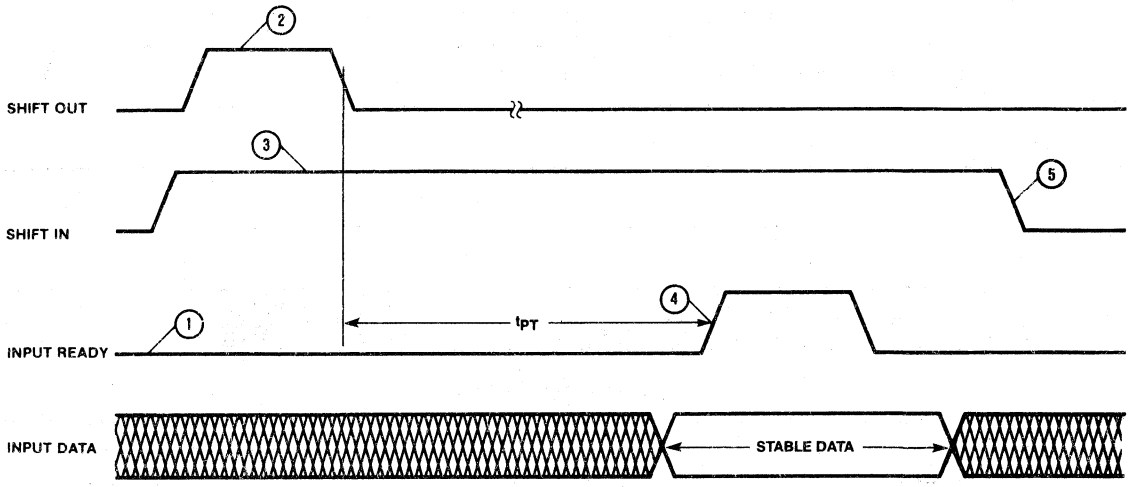


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

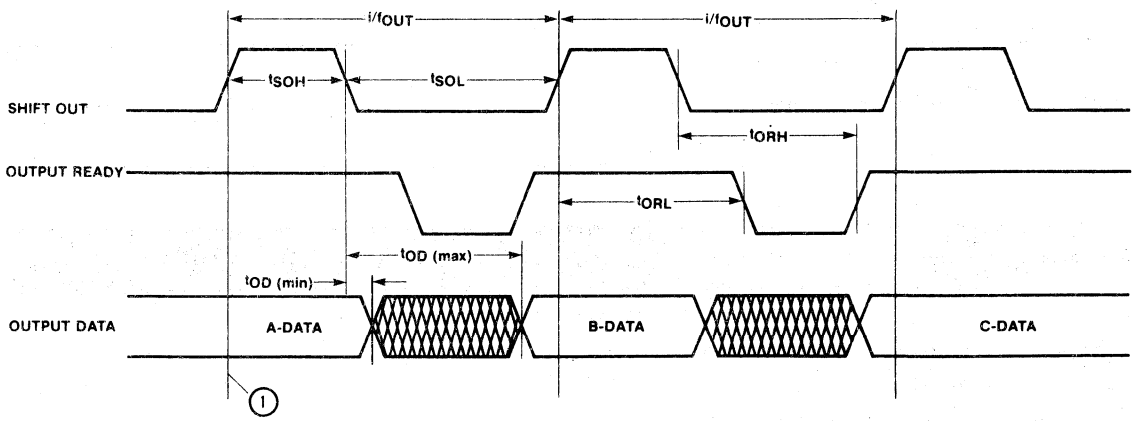
(1) FIFO is initially full.

(2) Shift Out pulse is applied. An empty location start "bubbling" to the front.

(3) Shift In is held HIGH.

(4) As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.

(5) The Data from the first word is released for "fall through" to second word.



(1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively

Figure 5. Output Timing

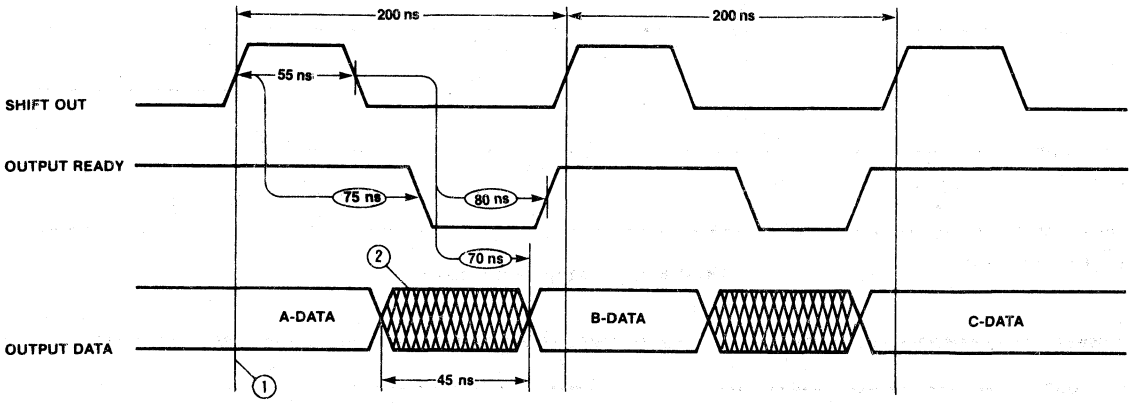


Figure 6. Typical Waveform for 5 MHz Shift Out Data Rate

(1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively.

(2) Data in the crosshatched region may be A or B Data.

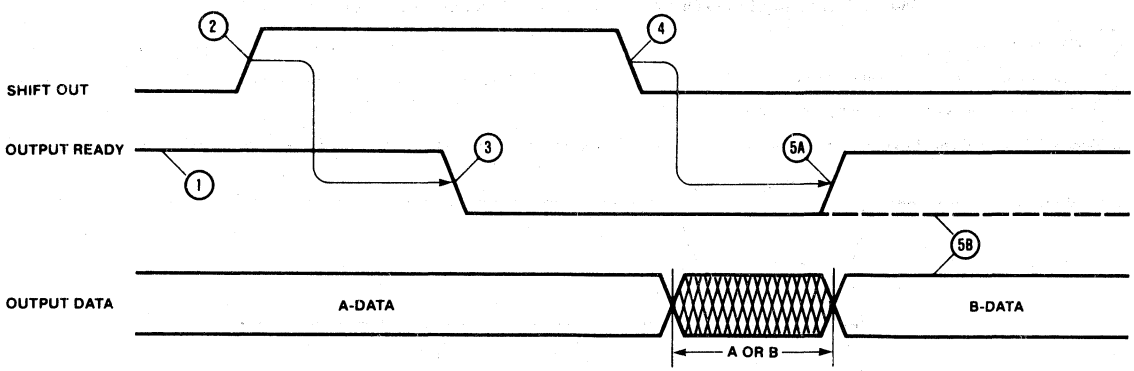


Figure 7. The Mechanism of Shifting Data Out of the FIFO

(1) Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.

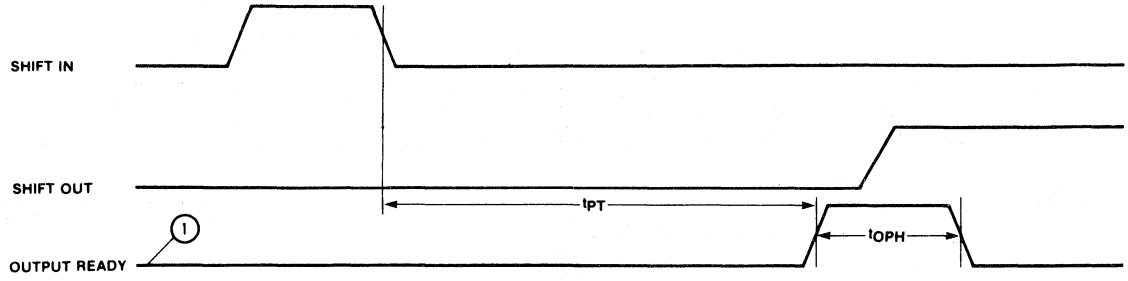
(2) Shift Out goes HIGH causing the next step.

(3) Output Ready goes LOW.

(4) Contents of word 62 (B-DATA) is released for "fall through" to word 63.

(5A) Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.

(5B) If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs.



1 FIFO initially empty.

Figure 8. t_{PT} and t_{OPH} Specification

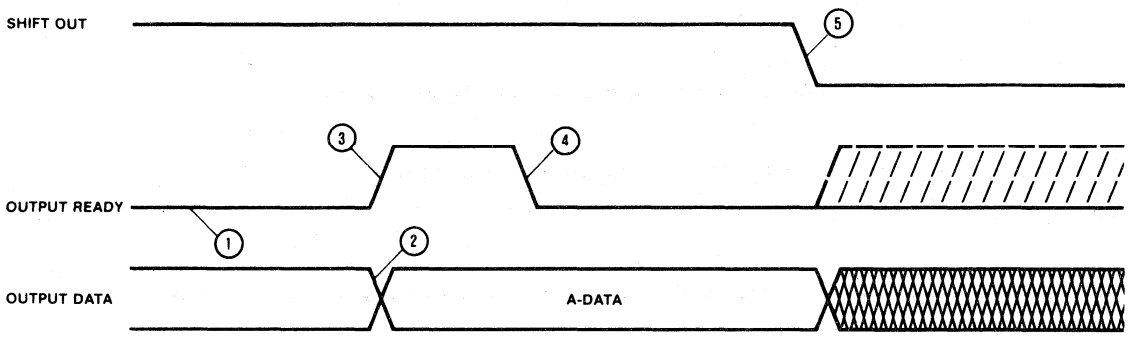
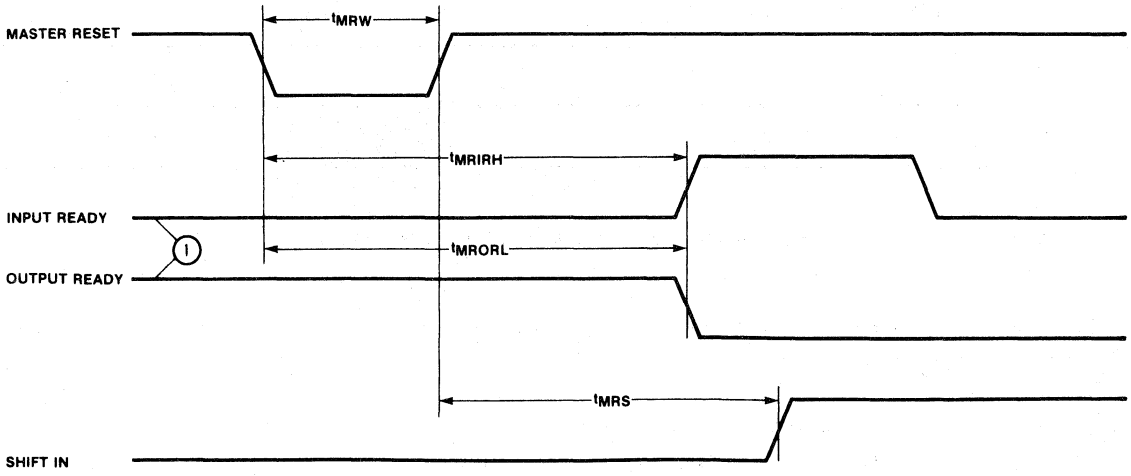


Figure 9. Data is ,Shifted Out Whenever Shift Out and Output Ready are Both HIGH

1. Word 63 is empty.
2. New data (A) arrives at the outputs (word 63).
3. Output Ready goes HIGH indicating the arrival of the new data.
4. Since Shift Out is held HIGH, Output Ready goes immediately LOW.
5. As soon as Shift Out goes LOW the Output Data is subject to change as shown by the dashed line on Output Ready.



1 FIFO initially full.

Figure 10. Master Reset Timing

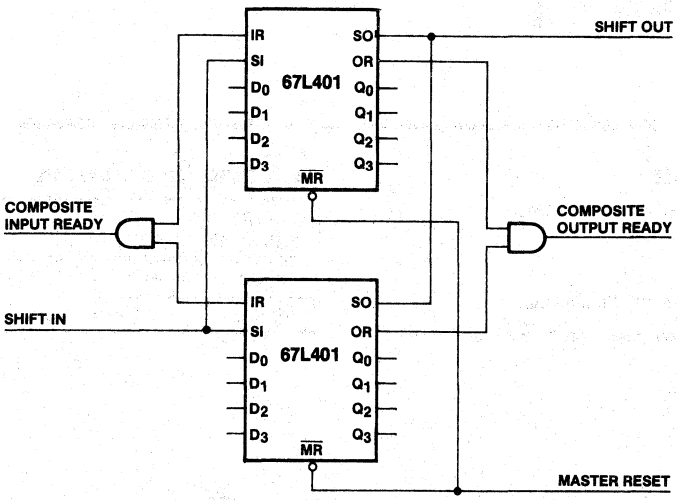


Figure 12. 64x8 FIFO With Two 67L401's

FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This need is due to the different fall through times of the FIFOs.

Applications

FIFOs are typically used as temporary data buffers between mismatching data rates. Such an application is shown in Figure 13.

The 67L401 can also be used in a bidirectional operation as shown in Figure 14.

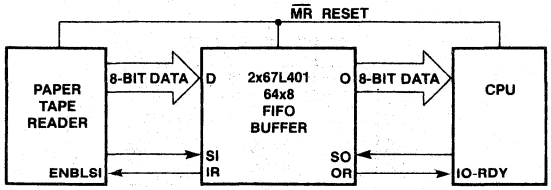
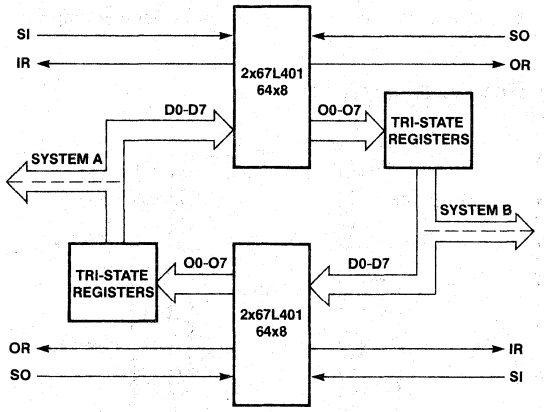


Figure 13. FIFO As Data Buffer Between Slow Steady Rate and Fast 'Burst' Rate



NOTE: Both depth and width expansion can be used in this mode.

Figure 14. Bidirectional FIFO Application

Low Power First-In First-Out (FIFO) 64x5 Memory
67L402

Features/Benefits

- Guaranteed 5 MHz shift-out/shift-in rates
- Low power consumption
- TTL inputs and outputs
- Readily expandable in the bit dimensions
- Structured pinouts. Output pins directly opposite corresponding input pins
- Asynchronous operation

Ordering Information

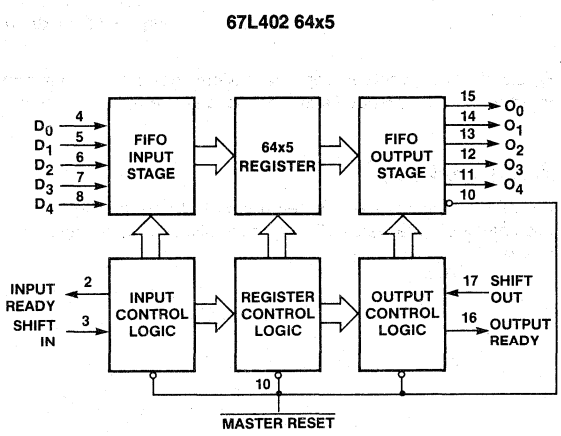
PART PACKAGE	PKG	TEMP	DESCRIPTION
67L402	N, NL	Com	5 MHz 64x5 FIFO
67L402	J, NL	Com	5 MHz 64x5 FIFO

Description

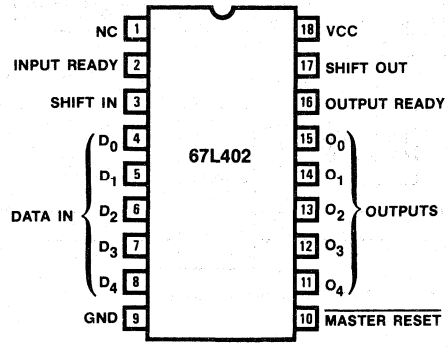
The 67L402 is a low-power First-In First-Out (FIFO) memory device with TTL speed. This device is organized in a 64x5-bit structure and easily expandable to any width. A 5 MHz data rate with fast "fall through" time allows usage in tape and disc controllers, printers and communications buffer applications. This data rate is much faster than a comparable MOS device. The FIFO is a register-based device. Data entered at the inputs "falls through" to the empty space closest to the output. Data is shifted out in the same sequence it is shifted in. Also, the width can be increased by putting the Input Ready signals through an AND gate to give a composite Input Ready. Similarly, the Output Ready signals should be gated to form a composite Output Ready.

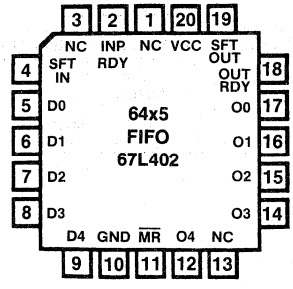
Generally, FIFOs are used in digital systems performing data transfers when source and receiver are not operating at the same data rate. FIFOs are also used as data buffers where the source and receiver are not operating at the same time. The 67L402 is particularly useful where low-power consumption is critical.

Block Diagram



Pin Configurations





Plastic Chip Carrier

TWX: 910-338-2376
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374

Monolithic Memories

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65° to +150° C

Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		75	°C
t_{SIH}†	Shift in HIGH time	1	55			ns
t_{SIL}	Shift in LOW time	1	55			ns
t_{IDS}	Input data setup	1	10			ns
t_{IDH}	Input data hold time	1	80			ns
t_{SOH}†	Shift Out HIGH time	5	55			ns
t_{SOL}	Shift Out LOW time	5	55			ns
t_{MRW}	Master Reset pulse	10	40			ns
t_{MRS}	Master Reset to SI	10	35			ns

8

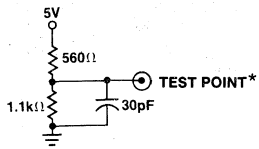
Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{IN}	Shift in rate	1	5			MHz
t_{IRL}†	Shift in to Input Ready LOW	1			75	ns
t_{IRH}†	Shift in to Input Ready HIGH	1			75	ns
f_{OUT}	Shift Out rate	5	5			MHz
t_{ORL}†	Shift Out to Output Ready LOW	5			75	ns
t_{ORH}†	Shift Out to Output Ready HIGH	5			80	ns
t_{ODH}	Output Data Hold (previous word)	5	8			ns
t_{ODS}	Output Data Shift (next word)	5			70	ns
t_{PT}	Data throughput or "fall through"	4, 8			4	μs
t_{MRORL}	Master Reset to OR LOW	10			85	ns
t_{MRIRH}	Master Reset to IR HIGH	10			85	ns
t_{IPH}	Input Ready pulse HIGH	4	20			ns
t_{OPH}	Output Ready pulse HIGH	8	20			ns

† See AC test and application note.

Test Load

* The "TEST POINT" is driven by the output under test, and observed by instrumentation.



Input Pulse 0 to 3 V
Input Rise and Fall Time (10% - 90%)
5 ns minimum
Measurements made at 1.5 V

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2†			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18mA			−1.5	V
I_{IL1}	Low-level input current	D_0–D_3 MR	V_{CC} = MAX	V_I = 0.45V			−0.8	mA
I_{IL2}		SI, SO					−1.6	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.4V			50	μA
I_I	Maximum input current		V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN	I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN	I_{OH} = −0.9mA	2.4			V
I_{OS}	Output short-circuit current*		V_{CC} = MAX	V_O = 0V	−20		−90	mA
I_{CC}	Supply Current		V_{CC} = MAX	Inputs Low, Outputs Open		113	130	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† This is an absolute voltage with respect to device GND (Pin 8 or 9) and includes all overshoots due to test equipment.

Functional Description

Data Input

After power up the Master Reset is pulsed low (Fig. 11) to prepare the FIFO to accept data in the first location. When Input Ready (IR) is HIGH the location is ready to accept data from the D_X inputs. Data then present at the data inputs is entered into the first location when the Shift In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. The first word is present at the outputs before a shift out is applied. If the memory is full, IR will remain LOW.

Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device.

Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW, and O_X remains as before, (i.e. data does not change if FIFO is empty).

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

AC Test and Application Note

Since the FIFO is a high-speed device, care must be exercised in design of the hardware and the timing. Though the external data rate is 5 MHz, internally the device is several times as fast. Device grounding and decoupling is crucial to correct operation, as the FIFO is sensitive to very small glitches caused by long reflective lines, high capacitances, and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1 μF directly between V_{CC} and GND with a very short lead length. In addition, care must be exercised in timing setup and measurement of parameters. For example, since an AND gate function is associated with both the Shift In-Input Ready Combination as well as the Shift Out-Output Ready Combination, timing measurements may be misleading. i.e., rising edge of the Shift-In pulse is not recognized until Input-Ready is High. If Input-Ready is not high due to too high a frequency, or the FIFO being full or affected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Time (t_{IDH}) and the next activity of Input Ready (t_{IRL}) to be extended relative to Shift-In going High.

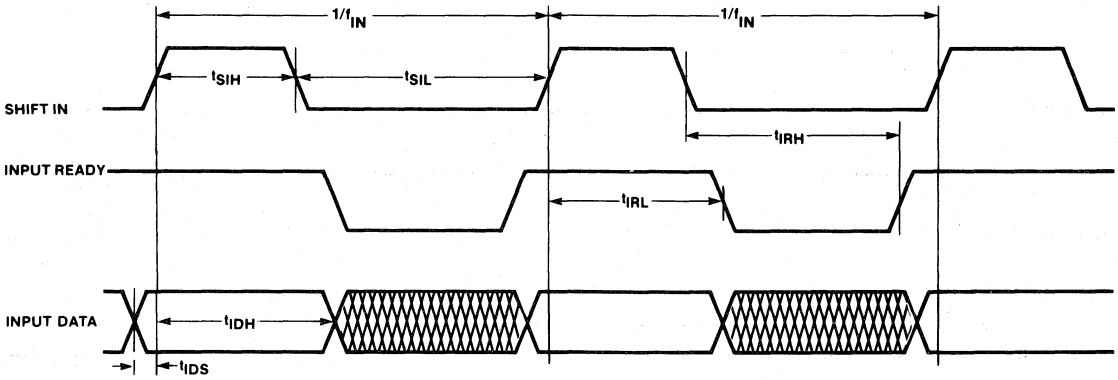


Figure 1. Input Timing

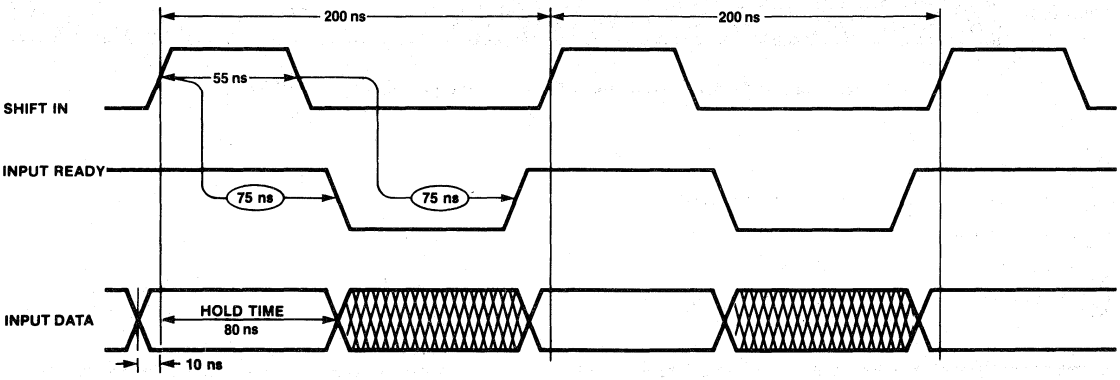


Figure 2. Typical Waveforms for 5 MHz Shift in Data Rate

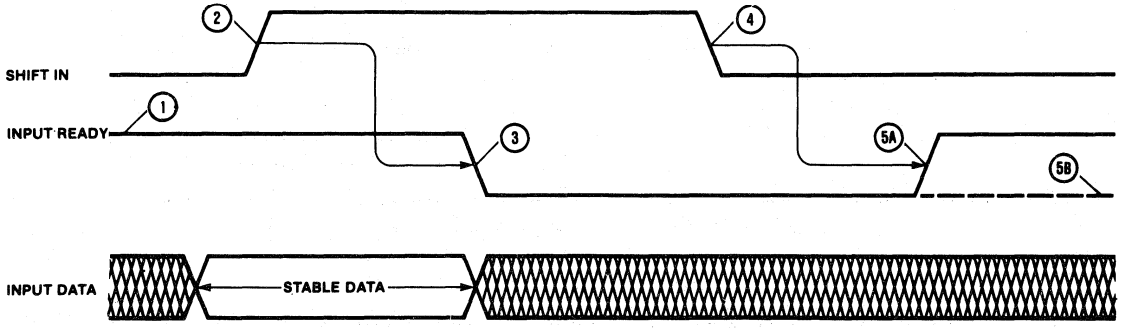


Figure 3. The Mechanism of Shifting Data into the FIFO

(1) Input Ready HIGH indicates space is available and a Shift In pulse may be applied.

(2) Input Data is loaded into the first word.

(3) Input Ready goes LOW indicating the first word is full.

(4) The Data from the first word is released for "fall-through" to second word.

(5A) The Data from the first word is transferred to second word. The first word is now empty as indicated by Input Ready HIGH.

(5B) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

NOTE: Shift In pulses applied while Input Ready is LOW will be ignored (See Figure 5).

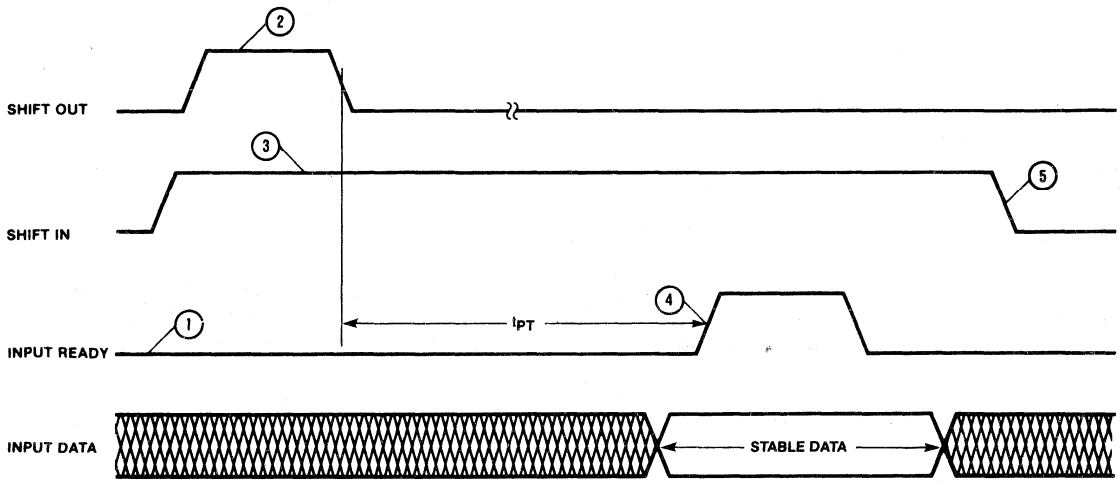
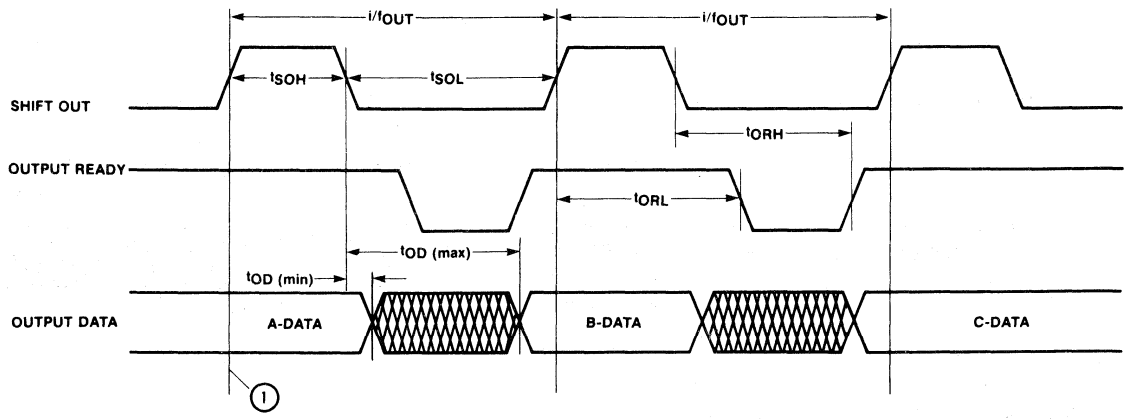


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

(1) FIFO is initially full.
(2) Shift Out pulse is applied. An empty location start "bubbling" to the front.
(3) Shift In is held HIGH.
(4) As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.
(5) The Data from the first word is released for "fall through" to second word.



(1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively

Figure 5. Output Timing

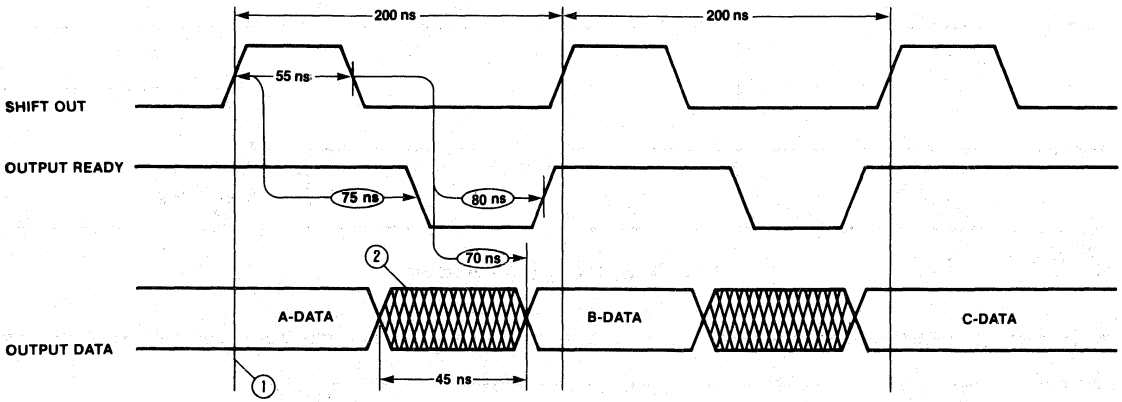


Figure 6. Typical Waveform for 5 MHz Shift Out Data Rate

(1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively.

(2) Data in the crosshatched region may be A or B Data.

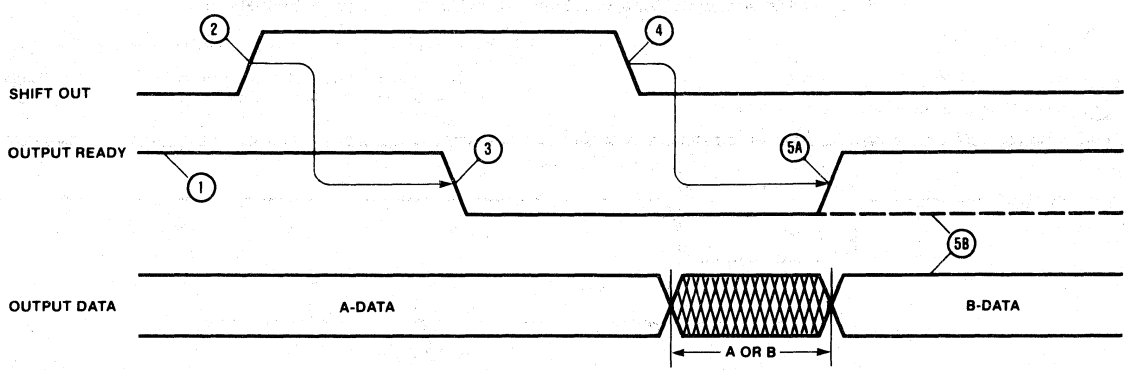


Figure 7. The Mechanism of Shifting Data Out of the FIFO

(1) Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.

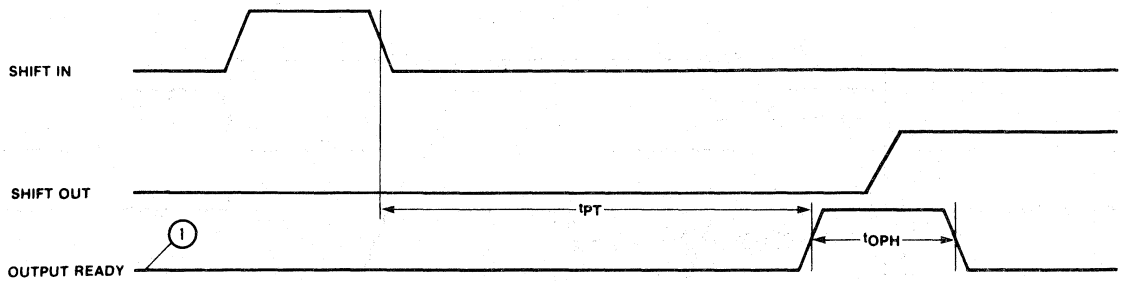
(2) Shift Out goes HIGH causing the next step.

(3) Output Ready goes LOW.

(4) Contents of word 62 (B-DATA) is released for "fall through" to word 63.

(5A) Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.

(5B) If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs.



1 FIFO initially empty.

Figure 8. t_{PT} and t_{OPH} Specification

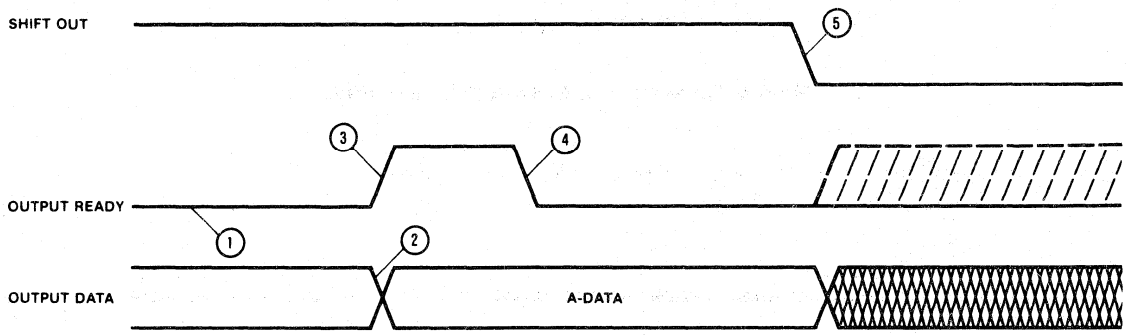
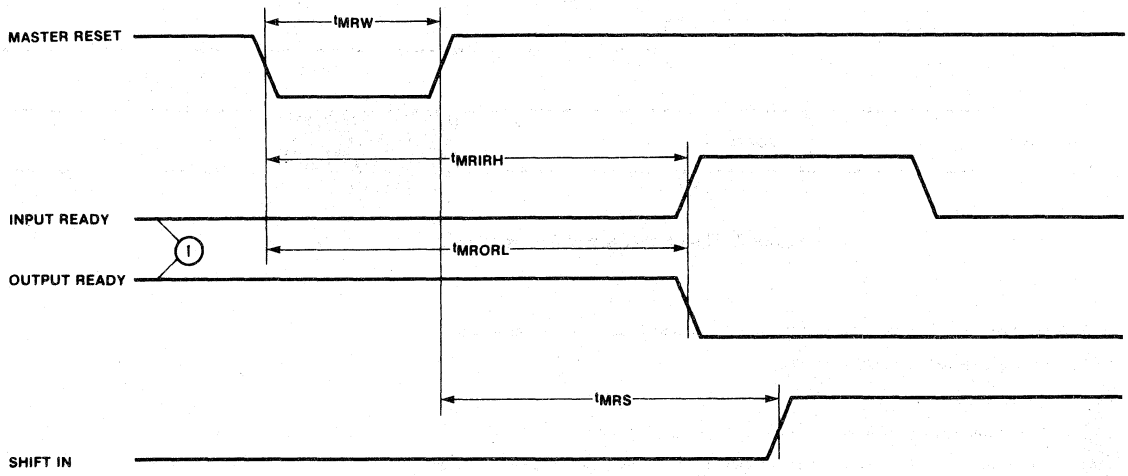


Figure 9. Data is ,Shifted Out Whenever Shift Out and Output Ready are Both HIGH

1. Word 63 is empty.
2. New data (A) arrives at the outputs (word 63).
3. Output Ready goes HIGH indicating the arrival of the new data.
4. Since Shift Out is held HIGH, Output Ready goes immediately LOW.
5. As soon as Shift Out goes LOW the Output Data is subject to change as shown by the dashed line on Output Ready.



1 FIFO initially full.

Figure 10. Master Reset Timing

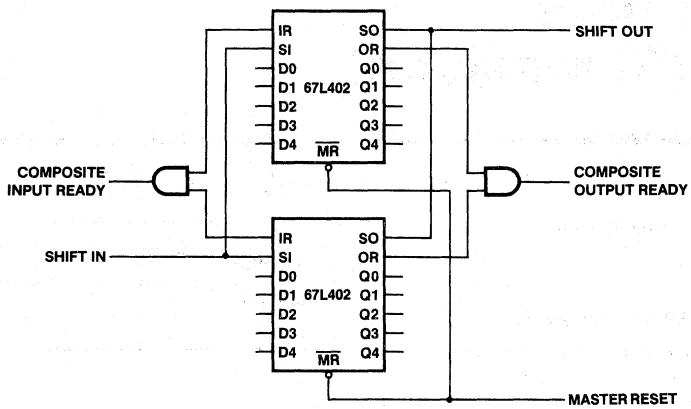


Figure 11. 64x8 FIFO With 67L402's

FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This need is due to the different fall through times of the FIFOs.

8

Applications

FIFOs are typically used as temporary data buffers between mismatching data rates. Such an application is shown in Figure 12.

The 67LS402 can also be used in a bidirectional operation as shown in Figure 13.

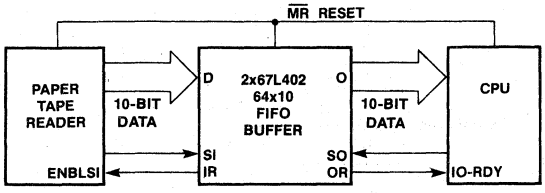
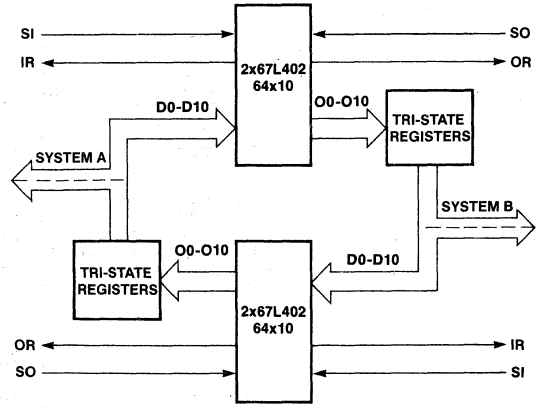


Figure 12. FIFO As Data Buffer Between Slow Steady Rate and Fast 'Burst' Rate



NOTE: Both depth and width expansion can be used in this mode.

Figure 13. Bidirectional FIFO Application

First-In First-Out (FIFO) 64x5 Memory 35 MHz (Standalone)

67413A 67413

Features/Benefits

- **High-speed 35 MHz shift-in/shift-out rates**
- **High-drive capability**
- **Three-state outputs**
- **Half-full and Almost-full/Empty status flags**
- **Structured pinouts. Output pins directly opposite corresponding input pins.**
- **Asynchronous operation**
- **TTL-compatible inputs and outputs**

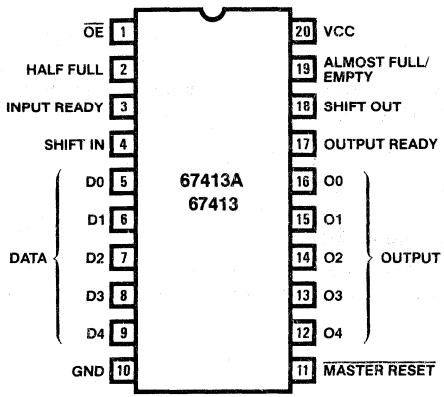
Description

The 67413A is a high-speed, 64x5 First-In-First-Out (FIFO) memory which operates at 35-MHz input/output rates (67413 operates at 25-MHz in-out). The data is loaded and emptied on a first-in-first-out basis. It is a three-state device with high-drive (I_{OL} = 24 mA) data outputs. These devices can be connected in parallel to give FIFOs of any word length. It has a Half-full flag (thirty-two or more words full) and an almost full/empty flag (fifty-six or more words or eight or less words). The main applications of 67413A, 67413 are rate buffers; sourcing and absorbing data at different rates. Other applications are high-speed tape and disk controllers, data communications systems and plotter control systems.

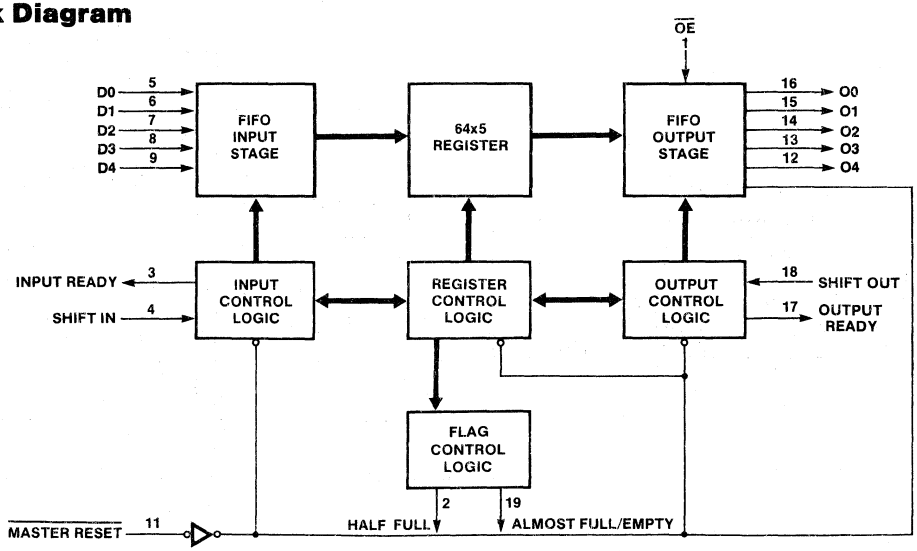
Ordering Information

PART NUMBER	PKG	TEMP	DESCRIPTION
67413A	J	Com	35 MHz-in/out
57413	J	Com	25 MHz-in/out

Pin Configuration



Block Diagram



2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Monolithic Memories

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 to 7 V
Input voltage ..... -1.5 to 7 V
Off-state output voltage ..... -0.5 to 5.5 V
Storage temperature ..... -65°C to +150°C

67413A Operating Conditions Over Temperature Range

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		75	°C
t_{SIH}†	Shift in HIGH time	1	9			ns
t_{SIL}†	Shift in LOW time	1	17			ns
t_{IDS}	Input data set up	1	2			ns
t_{IDH}	Input data hold time	1	15			ns
t_{SOH}†	Shift Out HIGH time	5	9			ns
t_{SOL}	Shift Out LOW time	5	17			ns
t_{MRW}	Master Reset pulse †	10	30			ns
t_{MRS}	Master Reset to SI	10	35			ns

67413A Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{IN}	Shift in rate	1	DC DC		††30 †††35	MHz
t_{IRL}†	Shift In ↑ to Input Ready LOW	1		12	18	ns
t_{IRH}†	Shift In ↓ to Input Ready HIGH	1		14	20	ns
f_{OUT}	Shift Out rate	5	DC DC		††30 †††35	MHz
t_{ORL}†	Shift Out ↑ to Output Ready LOW	5		12	18	ns
t_{ORH}†	Shift Out ↓ to Output Ready HIGH	5		14	20	ns
t_{ODH}†	Output Data Hold (previous word)	5	12			ns
t_{ODS}	Output Data Shift (next word)	5			34	ns
t_{PT}	Data throughput or "fall through"	4,8		510	650	ns
t_{MRORL}	Master Reset ↓ to Output Ready LOW	10		18	28	ns
t_{MRIRH}	Master Reset ↑ to Input Ready HIGH	10		21	28	ns
t_{MRIRL}	Master Reset ↓ Input Ready LOW*	10		18	28	ns
t_{MRO}	Master Reset ↓ to Outputs LOW	10		32	45	ns

Note: Typicals at 5 V V_{CC} and 25°C T_A.
* If the FIFO is not full (IR High), $\overline{MR}$ low forces IR low, followed by IR returning high when $\overline{MR}$ goes high.
† See AC test and high-speed application note.
†† Tested
††† Guaranteed by design (see test load).

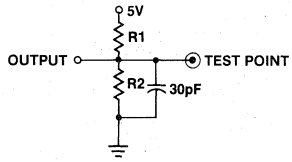
67413A Switching Characteristics Over Operating Conditions (continued)

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	TYP	MAX	UNIT
t_{IPH}	Input ready pulse HIGH	4	5	12		ns
t_{OPH}	Output ready pulse HIGH	8	5	12		ns
t_{ORD}	Output ready ↑ HIGH to Data Valid	5			18	ns
t_{AEH}*	Shift Out ↑ to AF/E HIGH	11		100	135	ns
t_{AEL}*	Shift In ↑ to AF/E LOW	11		450	600	ns
t_{AFL}*	Shift Out ↑ to AF/E LOW	12		450	600	ns
t_{AFH}*	Shift In ↑ to AF/E HIGH	12		100	135	ns
t_{HFH}*	Shift In ↑ to HF HIGH	13		280	360	ns
t_{HFL}*	Shift Out ↑ to HF LOW	13		280	360	s
t_{PHZ}	Output Disable Delay	A		14	25	ns
t_{PLZ}		A		14	25	ns
t_{PZL}	Output Enable Delay	A		14	25	ns
t_{PZH}		A		24	38	ns

Note: Input rise and fall time (10%-90%) = 2.5 ns. * See timing diagram for explanation of parameters.

67413A/67413

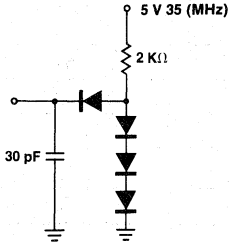
Standard Test Load



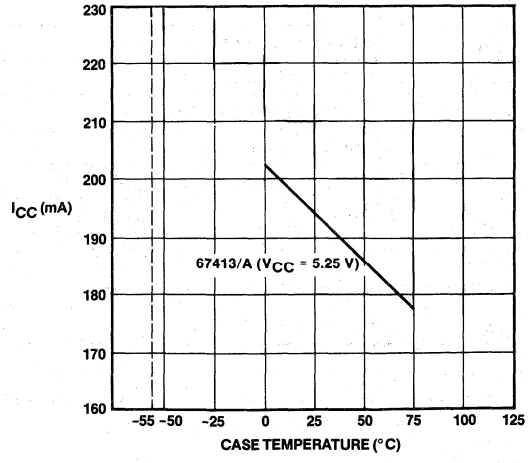
i_{OL}	R1	R2
24 mA	200 Ω	300 Ω
8 mA	600 Ω	1200 Ω

Input Pulse Amplitude = 3V
Input Rise and Fall Time (10%-90%) = 2.5 ns
Measurements made at 1.5 V

Design Test Load



Typical I_{CC} vs Temperature (V_{CC} = MAX)



Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65° to +150°C

67413 Operating Conditions Over Temperature Range

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		75	°C
t_{SIH}†	Shift in HIGH time	1	16			ns
t_{SIL}†	Shift in LOW time	1	20			ns
t_{IDS}	Input data set up	1	3			ns
t_{IDH}	Input data hold time	1	25			ns
t_{SOH}†	Shift Out HIGH time	5	16			ns
t_{SOL}	Shift Out LOW time	5	20			ns
t_{MRW}	Master Reset pulse †	10	35			ns
t_{MRS}	Master Reset to SI	10	35			ns

67413 Switching Characteristics Over Temperature Range

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{IN}	Shift in rate	1	DC		25	MHz
t_{IRL}†	Shift In ↑ to Input Ready LOW	1		12	28	ns
t_{IRH}†	Shift In ↑ to Input Ready HIGH	1		14	25	ns
f_{OUT}	Shift Out rate	5	DC		25	MHz
t_{ORL}†	Shift Out ↑ to Output Ready LOW	5		12	28	ns
t_{ORH}†	Shift Out ↓ to Output Ready HIGH	5		14	25	ns
t_{ODH}†	Output Data Hold (previous word)	5	10			ns
t_{ODS}	Output Data Shift (next word)	5			40	ns
t_{PT}	Data throughput or "fall through"	4,8		510	750	ns
t_{MRORL}	Master Reset ↓ to Output Ready LOW	10		18	30	ns
t_{MRIRH}	Master Reset ↑ to Input Ready HIGH	10		21	30	ns
t_{MRIRL}	Master Reset ↓ Input Ready LOW*	10		18	30	ns
t_{MRO}	Master Reset ↓ to Outputs LOW	10		32	55	ns

Note: Typicals at 5 V V_{CC} and 25°C T_A.

* If the FIFO is not full (IR High), $\overline{MR}$ low forces IR low, followed by IR returning high when $\overline{MR}$ goes high.

† See AC test and high-speed application note.

67413 Switching Characteristics Over Operating Conditions (continued)

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{IPH}	Input ready pulse HIGH	4	5	12		ns
t_{OPH}	Output ready pulse HIGH	8	5	12		ns
t_{ORD}	Output ready ↑ HIGH to Data Valid	5			20	ns
t_{AEH}*	Shift Out ↑ to AF/E HIGH	11		100	145	ns
t_{AEL}*	Shift In ↑ to AF/E LOW	11		450	650	ns
t_{AFL}*	Shift Out ↑ to AF/E LOW	12		450	650	ns
t_{AFH}*	Shift In ↑ to AF/E HIGH	12		100	145	ns
t_{HFH}*	Shift In ↑ to HF HIGH	13		280	380	ns
t_{HFL}*	Shift Out ↑ to HF LOW	13		280	380	ns
t_{PHZ}	Output Disable Delay	A		14	30	ns
t_{PLZ}		A		14	30	ns
t_{PZL}	Output Enable Delay	A		14	30	ns
t_{PZH}		A		24	50	ns

Note: Input rise and fall time (10%-90%) = 2.5 ns.

* See timing diagram for explanation of parameters.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION				MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage							0.8†	V
V_{IH}	High-level input voltage					2†			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA					−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.45 V					−250	μA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4 V					50	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V					1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} (Data outputs)	67413A 67413	24 mA			0.5	V
			I_{OL} (IR, OR)	67413A 67413	8 mA††				
			I_{OL} (Flag outputs)	67413A 67413	8 mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} (Data outputs)	67413A 67413	−3.0 mA	2.4			V
			I_{OH} (IR,OR)		−0.9 mA				
			I_{OH} (Flag outputs)		−0.9 mA				
I_{OS}	Output short-circuit current*	V_{CC} = MAX	V_O = 0 V			−20		−90	mA
I_{HZ}	Off-state output current	V_{CC} = MAX	V_O = 2.4 V					+20	μA
I_{LZ}		V_{CC} = MAX	V_O = 0.4 V					−20	μA
I_{CC}	Supply current	V_{CC} = MAX. All inputs low. All outputs open. (67413A/67413)						**240	mA

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

** See curve for I_{CC} vs. temp.

† There are absolute voltages with respect to GND (PIN 8 or 9) and includes all overshoots due to test equipment.

†† Care should be taken to minimize as much as possible the DC and capacitive load on IR and OR when operating at frequencies above 25 MHz.

Functional Description

Data Input

After power up the Master Reset is pulsed low (Figure 10) to prepare the FIFO to accept data in the first location. Master Reset must be applied prior to use to ensure proper operation. When Input Ready (IR) is HIGH the first location is ready to accept data from the D_X inputs. Data then present at the data inputs is entered into the first location when the Shift-In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Once data is entered into the first cell, the transfer of data in any full cell to the adjacent (downstream) empty cell is automatically activated by an on-chip control. Thus data will stack up at the end of the device (while empty locations will "bubble" to the front when data is shifted out). t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating more room is available. If the memory is full, IR will remain LOW.

Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that there is valid upstream data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW and Data output will not be valid.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

AC Test and High-Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 60 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. Monolithic Memories recommends a monolithic ceramic capacitor of 0.1 μF directly between V_{CC} and GND with very short lead length. In addition,

care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input Ready combination, as well as the Shift-Out-Output Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input Ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or effected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a funcitonal standpoint, and will also cause the "effective" timing of Input Data Hold time (T_{IDH}) and the next activity of Input Ready (T_{IRL}) to be extended relative to Shift-ingoing HIGH. This same type of problem is also related to T_{IRH}, T_{ORL} and T_{ORH} as related to Shift-Out. Data outputs driving a bus should be limited to 10 MHz frequency. For high-speed applications, proper grounding technique is essential.

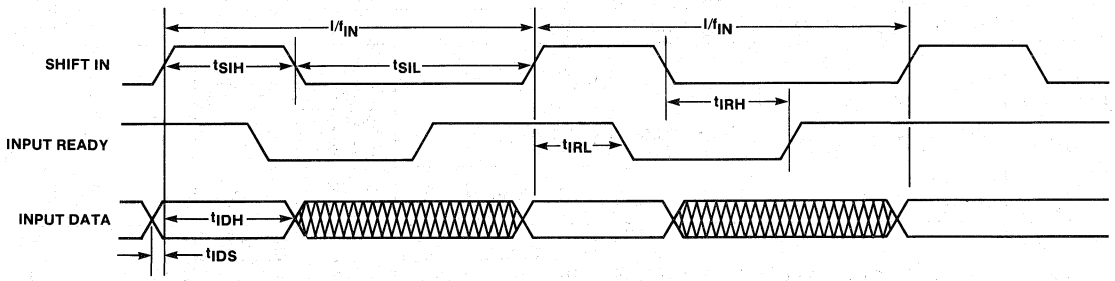


Figure 1. Input Timing

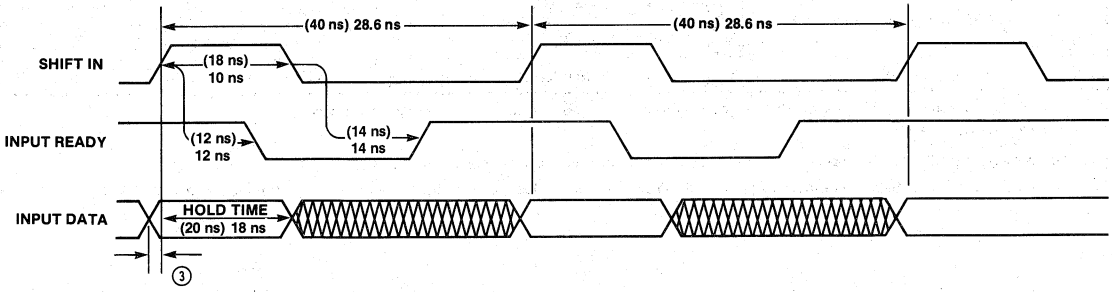


Figure 2. Typical Waveforms for 35 MHz Shift-In Data Rate (67413A)

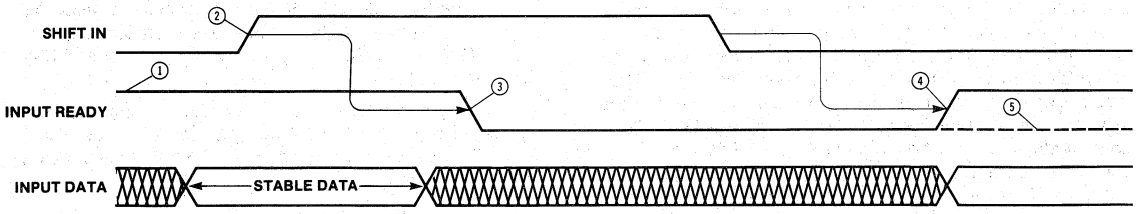


Figure 3. The Mechanism of Shifting Data into the FIFO

1. Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.
2. Input Data is loaded into the first word. The Data from the first word is released for "fall-through" to second word.
3. Input Ready goes LOW indicating the first word is full.
4. Shift-In going LOW allows Input Ready to sense the status of first word. The first word is now empty as indicated by Input Ready HIGH.
5. If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

Note: Shift-In pulses applied while Input Ready is LOW will be ignored (See Figure 5).

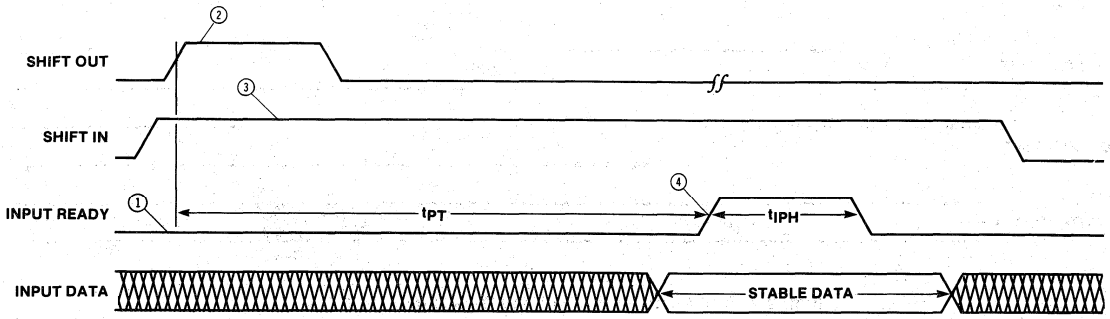


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

① FIFO is initially full.

② Shift Out pulse is applied. An empty location starts "bubbling" to the front.

③ Shift In is held HIGH

④ As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.

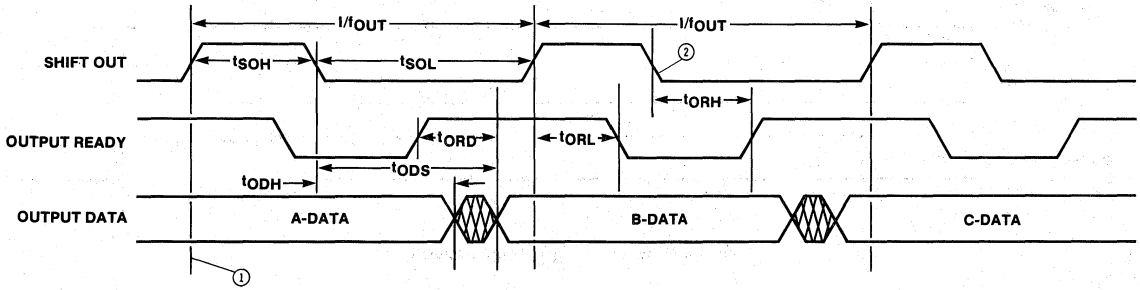


Figure 5. Output Timing

① The diagram assumes that at this time, words 63, 62 and 61 are loaded with A, B and C Data, respectively.

② Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e. OR and SO are both high together.

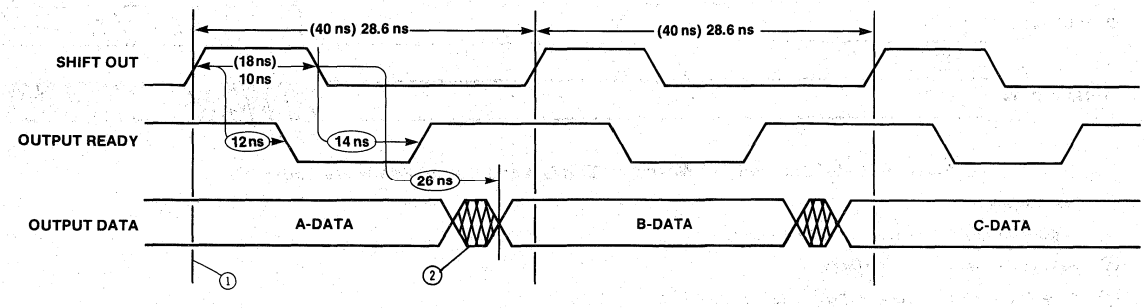


Figure 6. Typical Waveforms for 35 MHz Shift-Out Data Rate (67413A)

① The diagram assumes that at this time words 63, 62 and 61 are loaded with A, B and C Data, respectively.

② Data in the first crosshatched region may be A or B Data.

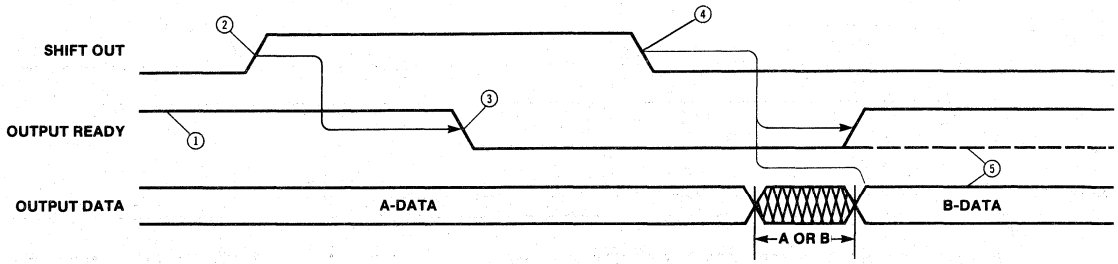


Figure 7. The Mechanism of Shifting Data Out of the FIFO

① Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.

② Shift-Out goes HIGH causing the contents of word 62 (B-Data) to be released for fall-through to word 63. Output data remains as valid A-Data while Shift-Out is HIGH.

③ Output Ready goes LOW.

④ Shift-out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.

⑤ If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data becomes invalid.

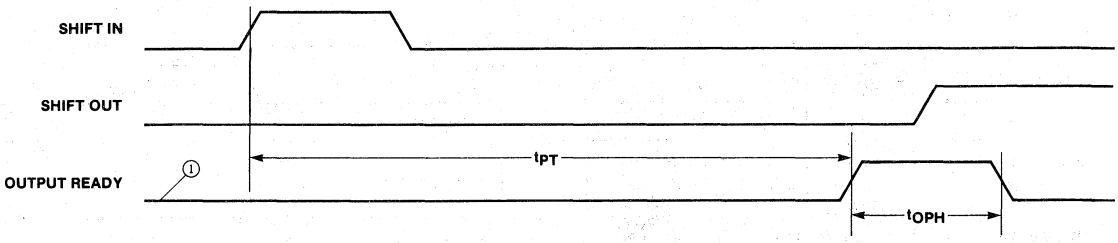


Figure 8. t_{PT} and t_{OPH} Specification

① FIFO initially empty.

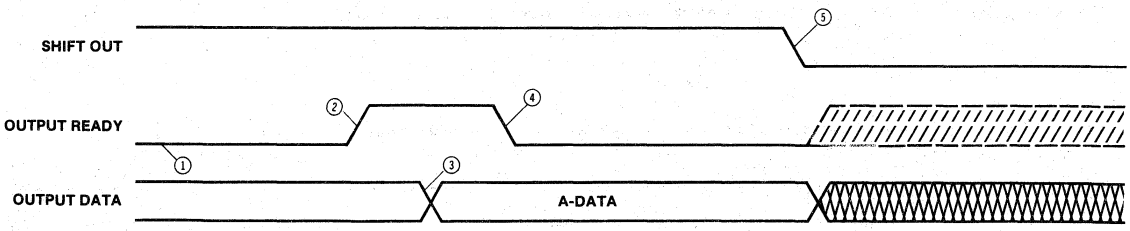


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH

① Word 63 is empty.

② Output Ready goes HIGH indicating arrival of the new data.

③ New data (A) arrives at the outputs (word 63).

④ Since Shift Out is held HIGH, Output Ready goes immediately LOW.

⑤ As soon as Shift Out goes LOW the Output Data is subject to change. Output Ready will go HIGH or LOW depending on whether there are any additional upstream words in the FIFO.

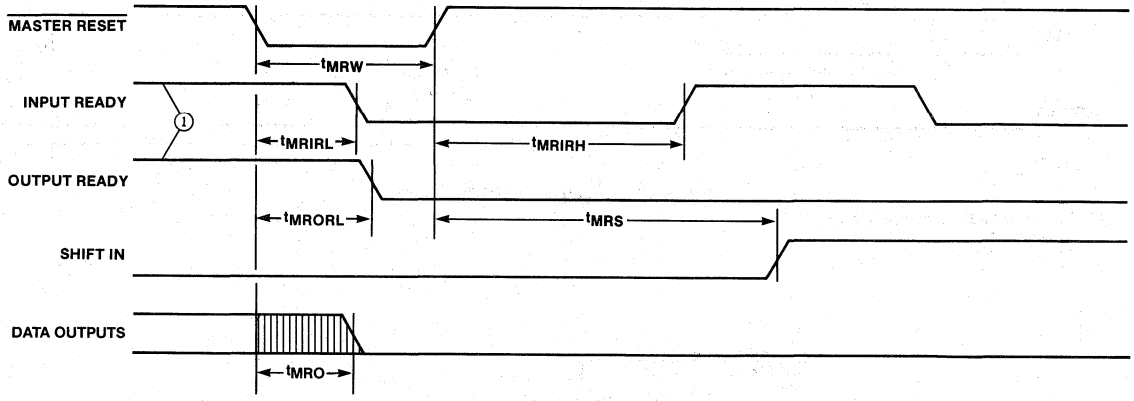


Figure 10. Master Reset Timing

① FIFO is partially full.

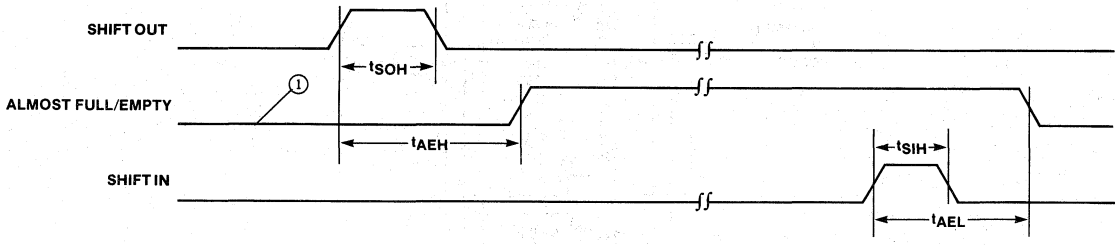


Figure 11. t_{AEH}, t_{AEL} Specifications

① FIFO contains 9 words (one more than almost empty).

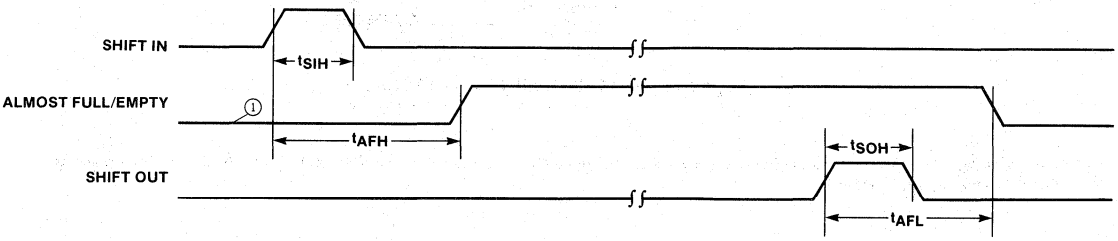


Figure 12. t_{AFH}, t_{AFL} Specifications

① FIFO contains 55 words (one short of almost full)

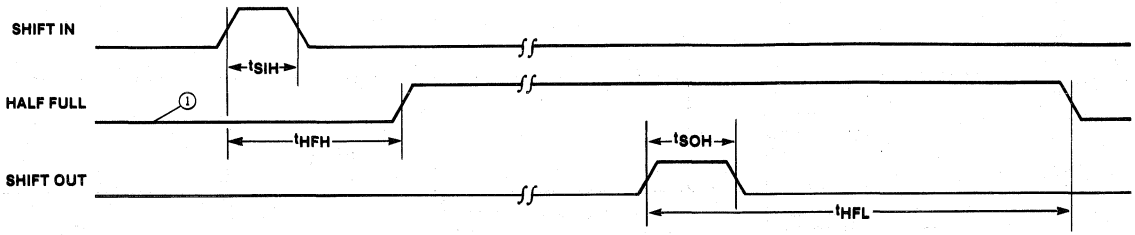


Figure 13. t_{HFL}, t_{HFH} Specifications

① FIFO contains 31 words (one short of half full).

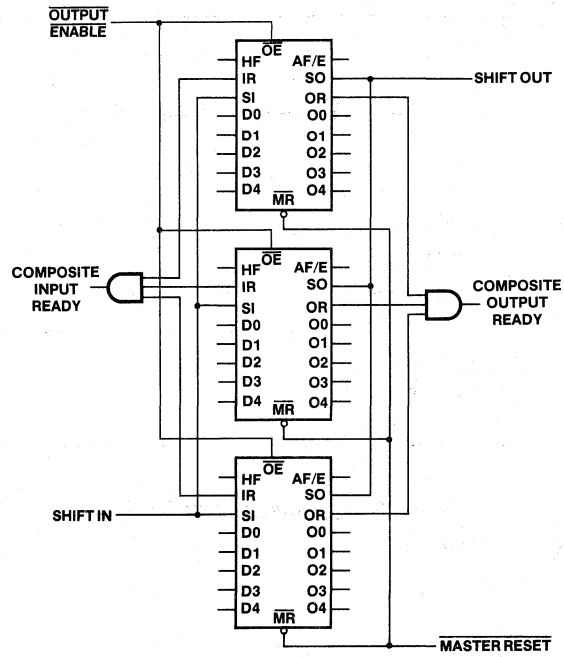


Figure 14. 64x15 FIFO with 67413A/67413

FIFOs are expandable in width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This requirement is due to the different fall through times of the FIFOs.

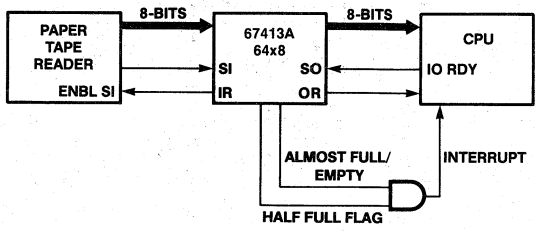
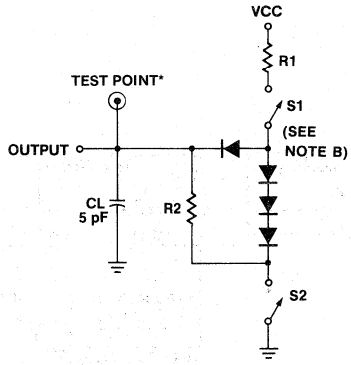


Figure 15. Application for 67413A "Slow and Steady Rate to Fast 'Blocked Rate' "

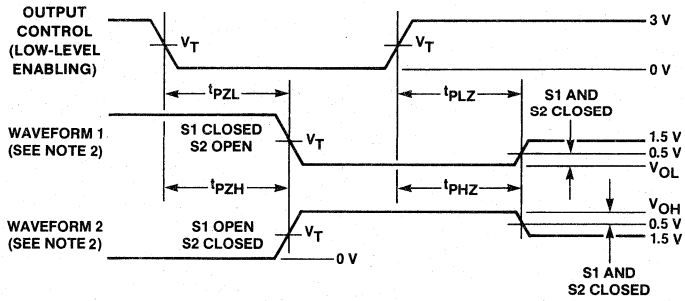
8

Note: Cascading the FIFO's in word width is done by ANDing the IR and OR as shown in Figure 14.

Three-State Test Load



Design Test Load



Enable and Disable

Notes: A. All diodes are 1N916 or 1N3064.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

D. When measuring propagation delay times of three-state outputs, switches S1 and S2 are closed.

First-In First-Out (FIFO) 64x4 64x5 Memory

67411A 67412A

35 MHz (Standalone)

Features/Benefits

- High-speed 35-MHz shift-in/shift-out rates
- Choice of 4-bit or 5-bit data width
- TTL inputs and outputs
- Readily expandable in word width
- Structured pinouts. Output pins directly opposite corresponding input pins
- Asynchronous operation
- Pin-compatible with Fairchild's F3341 MOS FIFO and many times faster

Ordering Information

PART NUMBER	PKG	TEMP	DESCRIPTION
67411A	J	Com	35 MHz 64x4 FIFO
67412A	J	Com	35 MHz 64x5 FIFO

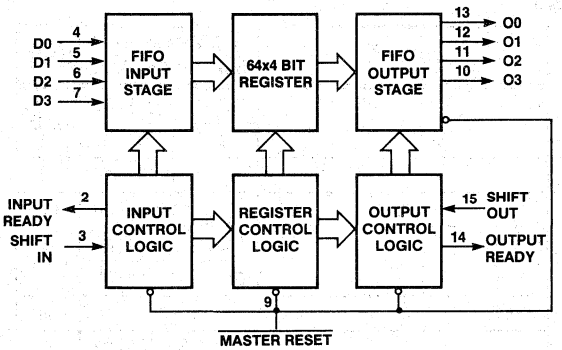
Description

The 67411/2A are "fall-through" high-speed First-In First-Out (FIFO) memory organized 64 words by 4 bits and 64 words by 5 bits respectively. The FIFO is expandable in word width only. It is the fastest FIFO available on the market. The FIFO is attractive for many applications such as disk controllers, communication buffers, rate buffers, etc.

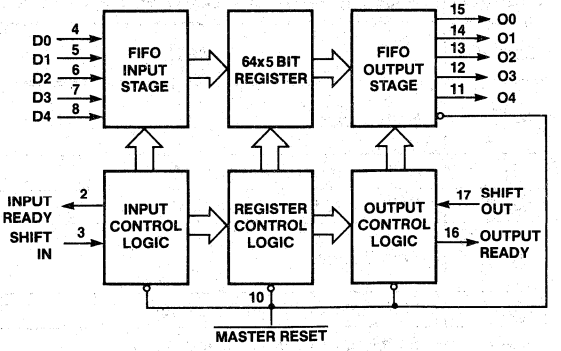
8

Block Diagrams

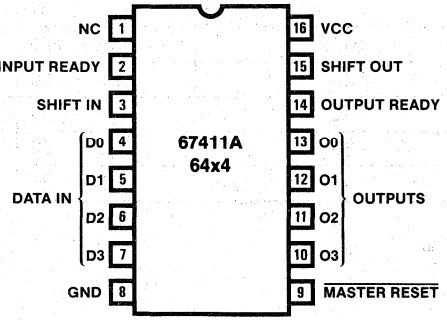
67411A

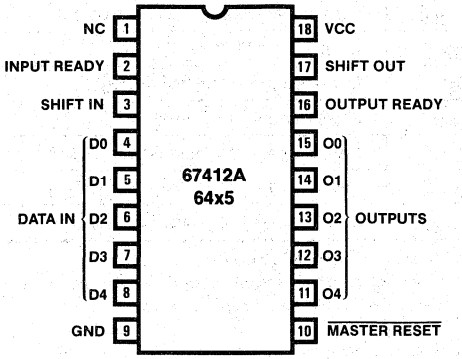


67412A



Pin Configurations





TWX: 910-338-2376
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
Monolithic Memories

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -.5 V to 5.5 V
Storage temperature ..... -65°C to +150°C

Operating Conditions Over Temperature Range

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		75	°C
t_{SIH}†	Shift in HIGH time	1	9			ns
t_{IDS}	Input data set up	1	2			ns
t_{IDH}	Input data hold time	1	14			ns
t_{SOH}†	Shift Out HIGH time	5	11			ns
t_{MRW}	Master Reset pulse †	10	30			ns
t_{MRS}	Master Reset to SI*	10	35			ns

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	TYP	MAX	UNIT
f_{IN}	Shift In rate	1	DC		††30	MHz
			DC		†††35	
t_{IRL}†	Shift In ↑ to Input Ready LOW	1		12	18	ns
t_{IRH}†	Shift In ↓ to Input Ready HIGH	1		14	20	ns
f_{OUT}	Shift Out rate	5	DC		††30	MHz
			DC		†††35	
t_{ORL}†	Shift Out ↑ to Output Ready LOW	5		12	18	ns
t_{ORH}†	Shift Out ↓ to Output Ready HIGH	5		14	20	ns
t_{ODH}†	Output Data Hold (previous word)	5	9			ns
t_{ODS}	Output Data Shift (next word)	5			31	ns
t_{PT}	Data throughput or "fall through"	4,8		510	650	ns
t_{MRORL}	Master Reset ↓ to Output Ready LOW	10		18	28	ns
t_{MRIRH}	Master Reset ↑ to Input Ready HIGH*	10		21	35	ns
t_{MRIRL}	Master Reset ↓ Input Ready LOW*	10		18	28	ns
t_{MRO}	Master Reset ↓ to Outputs LOW	10		32	45	ns

Note: Typical at 5 V V_{CC} and 25°C T_{AA}.
* If the FIFO is not full (IR High), $\overline{MR}$ low forces IR low returning high when $\overline{MR}$ goes high.
† See AC test and high-speed application note.
†† Tested.
††† Guaranteed by design (see test load).

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION				MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage							0.8 †	V
V_{IH}	High-level input voltage					2 †			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA					-1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.45 V					-50	μA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4 V					50	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V					1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} (Data Outputs)	67411/2A = 24 mA				0.5	V
			I_{OL} (IR, OR)	67411/2A = 8 mA ††					
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} (Data Out)	67411/2A	-3.0 mA	2.4			V
			I_{OH} (IR,OR)		-0.9 mA				
I_{OS}	Output short-circuit current*	V_{CC} = MAX	V_O = 0 V			-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX. Inputs low, outputs open (67411/2A)						**240	mA

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

** See curve for I_{CC} vs. temp.

† These are absolute voltages with respect to GND (Pin 8 or 9) and includes all overshoots due to test equipment.

†† Care should be taken to minimize as much as possible the DC and capacitive load on IR and OR when operating at frequencies above 25 MHz.

8

Functional Description

Data Input

After power up the Master Reset is pulsed low (Fig. 10) to prepare the FIFO to accept data in the first location. Master reset must be applied prior to use to ensure proper operation. When Input Ready (IR) is HIGH the first location is ready to accept data from the D_X inputs. Data then present at the data inputs is entered into the first location when the Shift-In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Once data is entered into the first cell, the transfer of data from any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating more room is available. If the memory is full, IR will remain LOW.

Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided the upstream stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW and Data output will not be valid.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

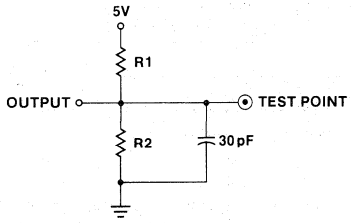
AC Test and High-Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 60 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. Monolithic Memories recommends a monolithic ceramic capacitor of 0.1 μF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input-Ready combination, as well as the Shift-Out-Output-Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input Ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or effected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input

Switching Characteristics Over Operating Conditions (continued)

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	TYP	MAX	UNIT
t_{IPH}	Input ready pulse HIGH	4	5	12		ns
t_{OPH}	Output ready pulse HIGH	8	5	12		ns
t_{ORD}	Ouput ready ↑ to Data Valid	5			18	ns

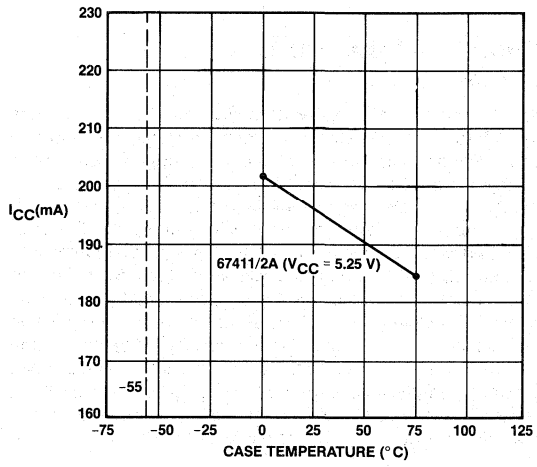
Standard Test Load



Input Pulse Amplitude = 3 V
Input Rise and Fall Time (10%-90%) = 2.5 ns
Measurements made at 1.5 V

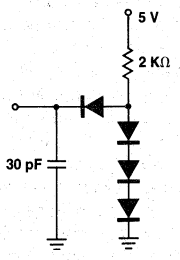
I_{OL}	R1	R2
24 mA	200 Ω	300 Ω
8 mA	600 Ω	1200 Ω

Typical I_{CC} vs Temperature (V_{CC} + MAX)



Test Load

Design Test Load (35 MHz)



Data Hold time (T_{IDH}) and the next activity of Input Ready (T_{IRL}) to be extended relative to shift-in going HIGH. This same type of situation occurs with T_{ORL} and T_{ORH} as related to Shift-Out. Data outputs driving a bus should be limited to 10 MHz frequency. For high-speed applications, proper grounding technique is essential.

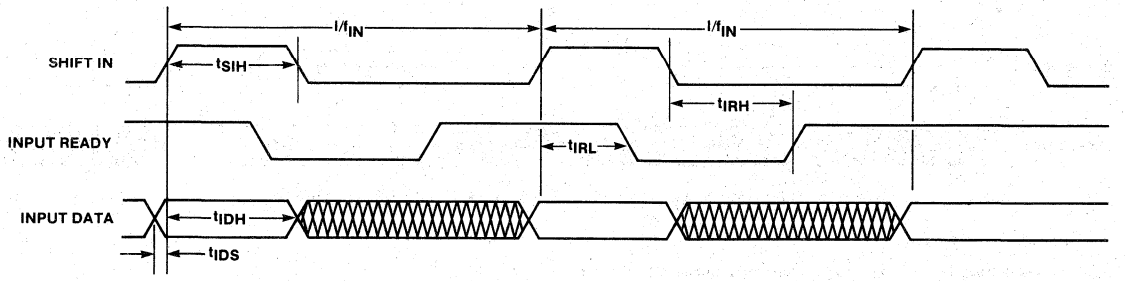


Figure 1. Input Timing

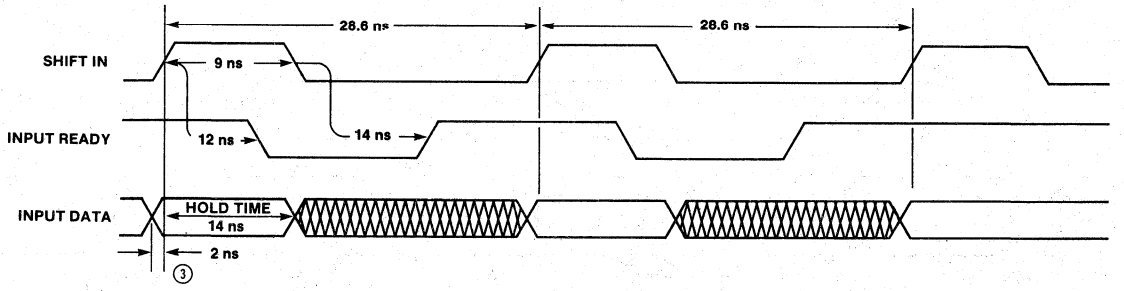


Figure 2. Typical Waveforms for 35 MHz Shift-In Data Rate

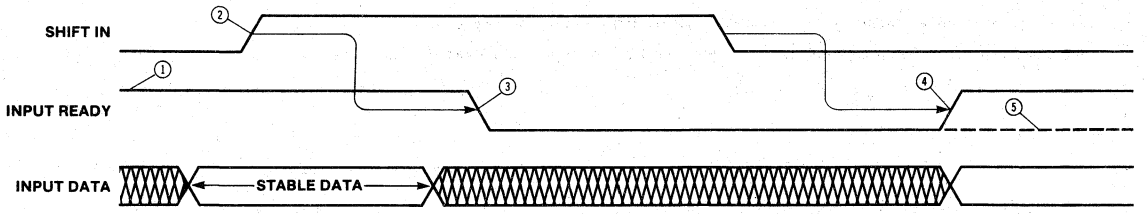


Figure 3. The Mechanism of Shifting Data into the FIFO

(1) Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.
(2) Input Data is loaded into the first word. The Data from the first word is released for "fall-through" to second word.
(3) Input Ready goes LOW indicating the first word is full.
(4) Shift-In going LOW allows Input Ready to sense the status of first word. The first word is now empty as indicated by Input Ready HIGH.
(5) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.
NOTE: Shift-In pulses applied while Input Ready is LOW will be ignored (See Figure 5).

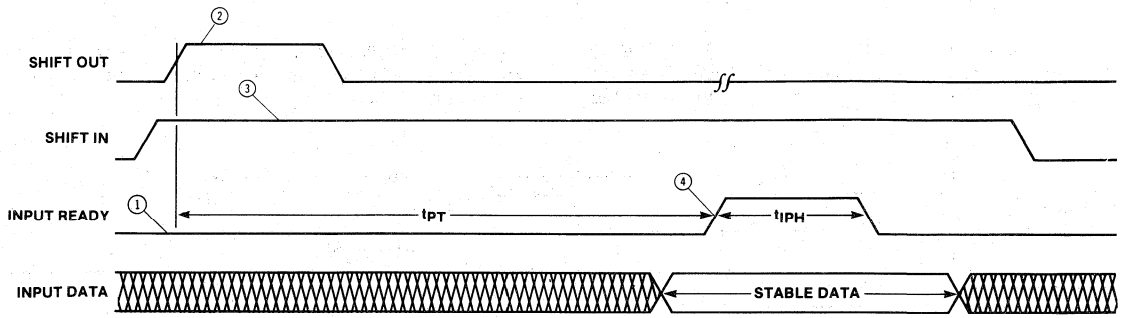


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

① FIFO is initially full.

② Shift Out pulse is applied. An empty location starts "bubbling" to the front.

③ Shift In is held HIGH

④ As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.

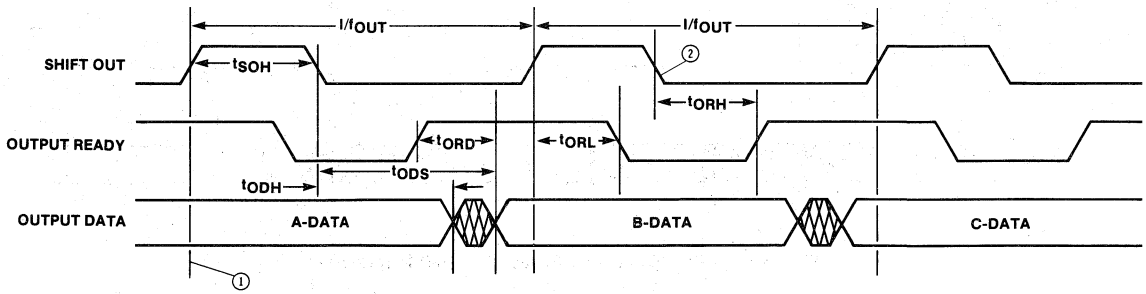


Figure 5. Output Timing

① The diagram assumes that at this time, words 63, 62 and 61 are loaded with A, B and C Data, respectively.

② Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e. OR and SO are both high together.

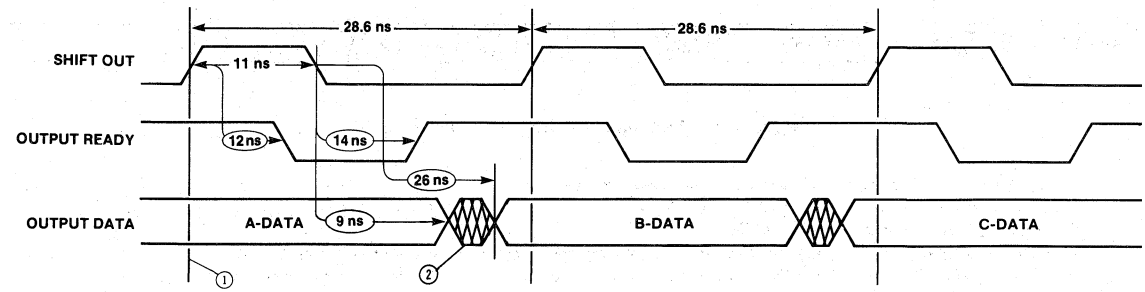


Figure 6. Typical Waveforms for 35 MHz Shift-Out Data Rate

① The diagram assumes that at this time words 63, 62 and 61 are loaded with A, B and C Data, respectively.

② Data in the first crosshatched region may be A or B Data.

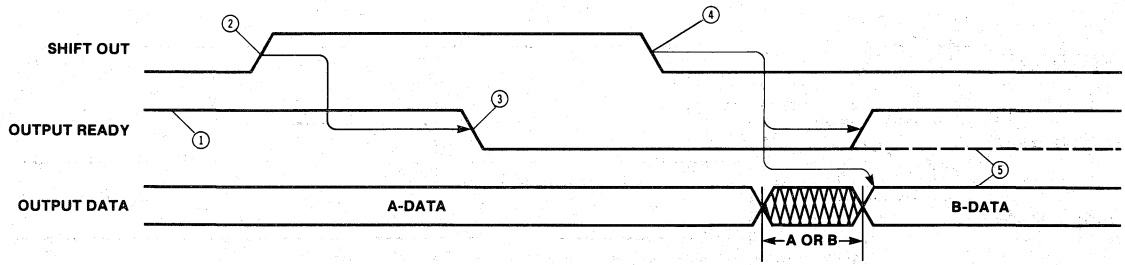


Figure 7. The Mechanism of Shifting Data Out of the FIFO

(1) Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.

(2) Shift-Out goes HIGH causing the contents of word 62 (B-Data) to be released for fall-through to word 63. Output data remains as valid A-Data while Shift-Out is HIGH.

(3) Output Ready goes LOW.

(4) Shift-out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.

(5) If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data becomes invalid.

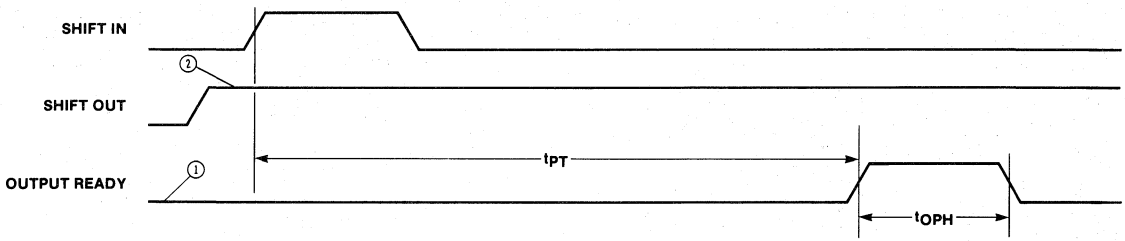


Figure 8. t_{PT} and t_{OPH} Specification

(1) FIFO initially empty.

(2) Shift Out held HIGH

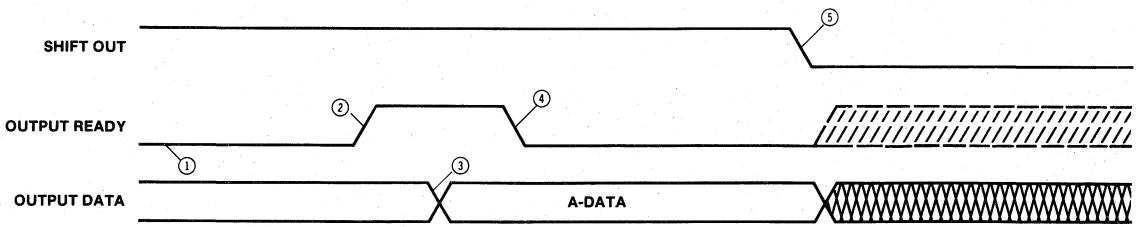


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH.

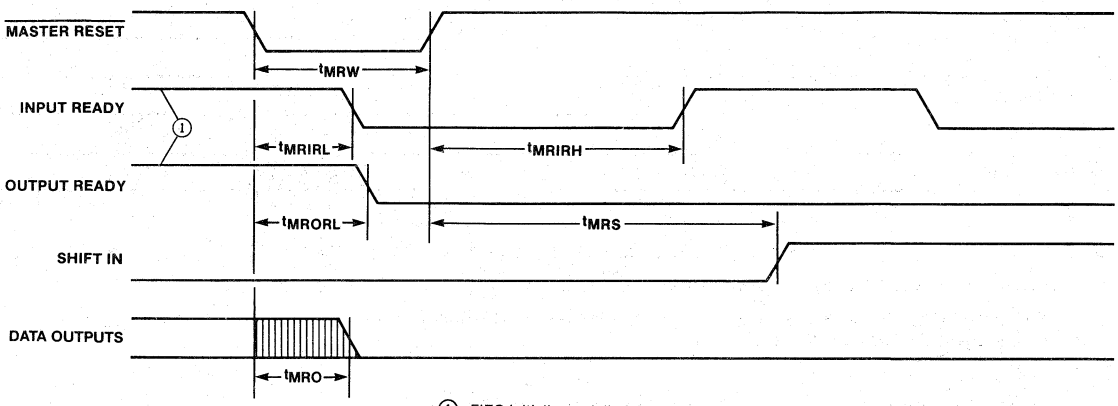
(1) Word 63 is empty.

(2) Output Ready goes HIGH indicating arrival of the new data.

(3) New data (A) arrives at the outputs (word 63).

(4) Since Shift Out is held HIGH, Output Ready goes immediately LOW.

(5) As soon as Shift Out goes LOW the Output Data is subject to change. Output Ready will go HIGH or LOW depending on whether there are any additional upstream words in the FIFO.



1 FIFO initially partially full.

Figure 10. Master Reset Timing

Serializing First-In-First-Out (FIFO) 64x8/9 Memory

67417

Features/Benefits

- High-speed 28-MHz serial shift-in/shift-out rate
- 10-MHz parallel shift-in/shift-out rate
- Three-state outputs with Hi-current drive
- Cascadable at parallel port only
- Half-full flag (32 or more)
- Selectable 64x8 or 64x9 FIFO configuration thus providing "frame mark bit"

Typical Applications

- LAN equipment
- Data communication
- Office automation
- Microcomputers
- Minicomputers
- Disk/tape controllers

Description

The 67417 is a serializing/deserializing FIFO. This FIFO, the first one of its type in the industry, is organized 64 words x 8/9 bits wide. Like traditional Monolithic Memories' FIFOs it is cascadable, but only at the parallel port.

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE	DESCRIPTION
67417	J	Com	64x8/9

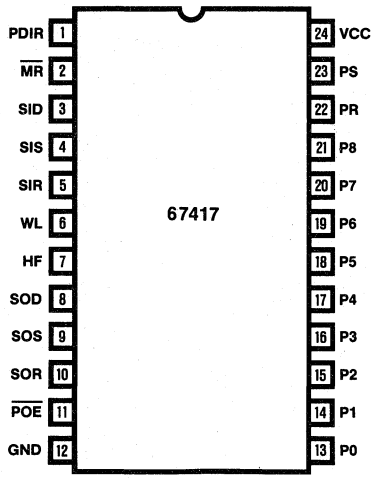
In addition, the device has the ability to connect directly to a system bus. These features make it a complete "sub-system on a chip."

The FIFO basically has three modes of operation;

1. Serial in to parallel out
2. Parallel in to serial out
3. Serial in to serial out (requires non-standard logic level on PDIR).

In the first mode, serial data can be accepted at up to 28 MHz and the FIFO outputs parallel data at up to 10 MHz. Similarly, in the alternate mode parallel data can be transformed into serial data. Please refer to appendix for detailed description.

Pin Configuration



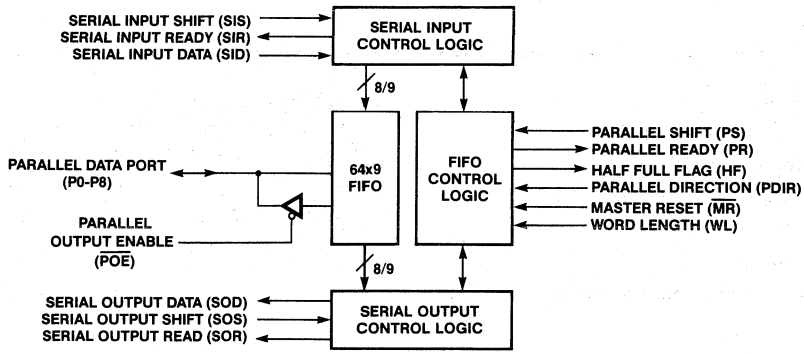
Pin Names

P0-P8	Parallel Data
PS	Parallel Shift In/Out
PR	Parallel Input/Output Ready
$\overline{POE}$	Parallel Output Enable
SID	Serial Input Data
SIS	Serial Input Shift
SIR	Serial Input Ready
SOD	Serial Output Data
SOS	Serial Output Shift
SOR	Serial Output Ready
PDIR	Parallel Port Direction
WL	Word Length
$\overline{MR}$	Master Reset
HF	Half Full Flag
VCC	VCC
GND	Ground

NOTE: Please call Monolithic Memories for introduction dates.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories MMI

Block Diagram



Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		75	°C
	SERIAL INPUT PARAMETERS					
f_{SIN}	Max. Serial Shift-In Rate	1			28	MHz
t_{SISH}	Serial Shift-In HIGH time	1	23			ns
t_{SISL}	Serial Shift-In LOW time	1	12			ns
t_{SIDS}	Serial Input Data Setup time	1	14			ns
t_{SIDH}	Serial Input Data Hold time	1	0			ns
t_{SIRHS}	Recovery Time Serial Input Ready ↑ to Serial Input Shift ↑	1	0			ns
	SERIAL OUTPUT PARAMETERS					
f_{SOUT}	Max. Serial Shift-Out Rate	1			28	MHz
t_{SOSH}	Serial Shift-Out HIGH time	3	15			ns
t_{SOSL}	Serial Shift-Out LOW time	3	15			ns
t_{ORHS}	Recovery time Serial Output Ready ↑ to Serial Output Shift ↑	3	5			ns
	WORD LENGTH PARAMETERS					
t_{SWL}	Setup SIS, SOS	1,3	18			ns
t_{HWL}	Hold SIS, SOS	1,3	3			ns
	PARALLEL PORT PARAMETERS					
f_P	Parallel shift-in/shift-out rate	8			10	MHz
t_{PSH}	Parallel Shift-In/Out HIGH time	5/8	30			ns
t_{PSL}	Parallel Shift-In/Out LOW time	5/8	30			ns
t_{PIDS}	Parallel Input Data Setup time	5	-5			ns
t_{PIDH}	Parallel Input Data hold time	5	35			ns
t_{PDIRSL}	Shift LOW to parallel direction transition	14	50			ns
t_{PDIRSH}	Parallel direction transition to Shift HIGH	14	50			ns
t_{PRHS}	Parallel Ready ↑ to Parallel Shift Low	10/11	30			ns
	MASTER RESET PARAMETER					
t_{MRW}	Master Reset LOW time	12/13	40			ns

8

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
	SERIAL INPUT PARAMETERS					
t_{SIRL}	Serial Input Shift ↑ to Serial Input Ready LOW	2			23	ns
t_{SIHFH}	Serial Input Shift ↑ to Half-Full Flag HIGH	7			1.3	µs
	SERIAL OUTPUT PARAMETERS					
t_{SORL}	Serial Output Shift ↑ to Serial Output Ready LOW	4			23	ns
t_{SOD}	Serial Output Shift ↑ to Serial Output data	3			23	ns
t_{ODRH}	Serial Output Data valid to Serial Output Ready HIGH	3	0	25		ns
t_{SOHFL}	Serial Output Shift ↑ to Half-Full LOW	7			1.3	µs
	PARALLEL INPUT/OUTPUT PARAMETERS					
t_{PSPRL}	Parallel Shift ↑ to Parallel Ready LOW	5/8			65	ns
t_{PSPRH}	Parallel Shift ↓ to Parallel Ready HIGH	5/8/10			80	ns
t_{PSHFH}	Parallel Shift-In ↓ to Half-Full HIGH	6			1.3	µs
t_{PSHFL}	Parallel Shift-Out ↓ to Half-Full LOW	9			1.3	µs
	PARALLEL OUTPUT PARAMETERS					
t_{PODH}	Minimum Parallel Shift ↓ to Ouput data	8	20			ns
t_{POD}	Maximum Parallel Shift ↓ to Output data	8			60	ns
t_{PODV}	Minimum Output data valid to parallel ready HIGH	8	0	15		ns
	OTHER PARAMETERS					
t_{PT}	Fall-through time	10/11/16/17			2.6	µs
t_{IPH}	Parallel Input Ready pulse HIGH	11	30			ns
t_{OPH}	Parallel Output Ready pulse HIGH	10	30			ns
t_{MRO}	$\overline{\text{Master Reset}}$ ↓ to Data Out LOW	12			65	ns
t_{MRSIRL}	$\overline{\text{Master Reset}}$ ↓ to Serial Input Ready LOW	12			40	ns
t_{MRSIRH}	$\overline{\text{Master Reset}}$ ↑ to Serial Input Ready HIGH	12			40	ns
t_{MRPRL}	$\overline{\text{Master Reset}}$ ↓ to Parallel Ready LOW	12/13			40	ns
t_{MRPRH}	$\overline{\text{Master Reset}}$ ↑ to Parallel Ready HIGH	13			30	ns
t_{MRSORL}	$\overline{\text{Master Reset}}$ ↓ to Serial Output Ready LOW	13			40	ns
t_{MRHFL}	Master Reset ↓ to Half-Full LOW	12/13			60	ns
t_{PDIROR}	Parallel Direction change to new Output Ready	14			60	ns
t_{PDIROD}	Parallel Direction change to Output data valid	14			60	ns
t_{PDIRPZ}	Parallel Direction change to Parallel Output data Hi-Z	14			35	ns
t_{PDIRSZ}	Parallel Direction changes to Serial Output-data Hi-Z	14			80	ns
t_{PZX}	Output enable time $\overline{\text{POE}}$ to P0-8	15			30	ns
t_{PXZ}	Output disable time $\overline{\text{POE}}$ to P0-8	15			35	ns

Electrical Characteristics Over Operating Conditions

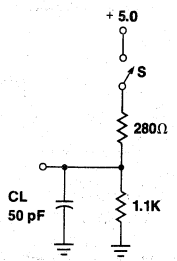
SYMBOL	PARAMETER		TEST CONDITIONS				COM MIN	COM TYP	COM MAX	UNIT
V_{IL}	Low-level input voltage								0.8†	V
V_{IH}	High-level input voltage						2†			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18 mA					−1.5	V
I_{IL}	Low-level input current		V_{CC} = MAX	V_I = 0.4 V					−0.4	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.4 V					0.1	mA
I_I	Maximum input current		V_{CC} = MAX	V_I = 5.5 V					0.4	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN	Data Outputs P0-P8, SOD	I_{OL} = 24 mA	0-80°C			0.58	V
						25°C			0.55	
					I_{OL} = 16 mA	0-80°C			0.5	
				All other outputs	I_{OL} = 8 mA				0.5	
V_{OH}	High-level output voltage		V_{CC} = MIN	I_{OH} = −3 mA			2.4			V
I_{OS}	Output short-circuit current*		V_{CC} = MAX	V_O = 0 V			−20		−90	mA
I_{LZ}	Off-state output current*	SOD P0 to P8	V_{CC} = MAX	V_O = 0.4 V					−100	μA
I_{HZ}				V_O = 2.4 V					100	mA
I_{CC}	Supply current		V_{CC} = MAX						350	mA
O_V	PDIR non-standard over voltage		Serial-In, Serial-Out				10		16	V

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

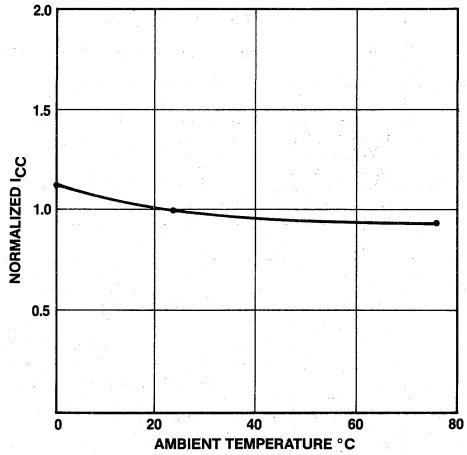
† This is an absolute voltage with respect to device GND (pin 12) and includes all overshoots due to test equipment.

Test Waveforms

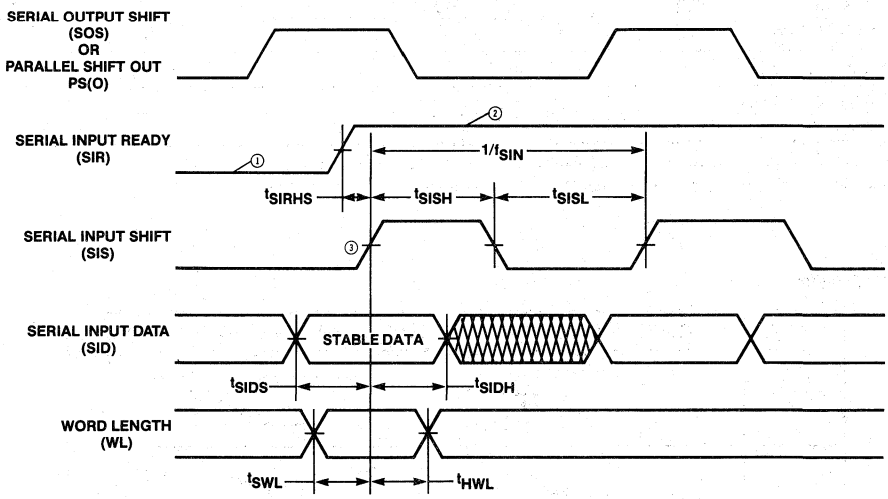
TEST	S = OPEN	S = CLOSED	OUTPUT WAVEFORM-MEAS-LEVEL
All t_{PD}		All t_{PD}	V_{OH}, V_{OL}, 1.5 V
t_{PXZ}	t_{PHZ}	t_{PLZ}	V_{OH} 0.5 V, V_{OL} 0.5 V, 2.8 V, 0.0 V
t_{PZX}	t_{PZH}	t_{PZL}	2.8 V, 0.0 V, 1.5 V, V_{OH}, V_{OL}



I_{CC} VS Temperature

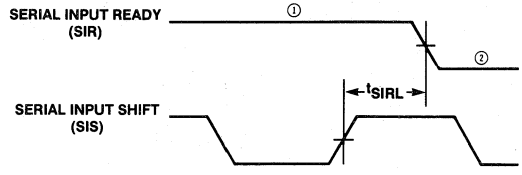


Definition of Waveforms



① FIFO is full.
② Shift-out (serial or parallel) is asserted, SIR goes High.
③ SIS can be asserted t_{SIRHS} after serial input ready changes from low-to-high.

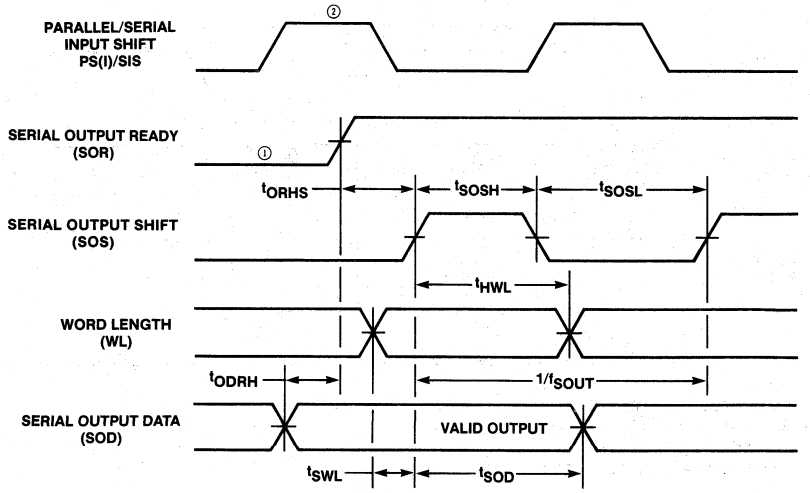
Figure 1. Serial Input Timing



① FIFO is not full.
② FIFO is full.

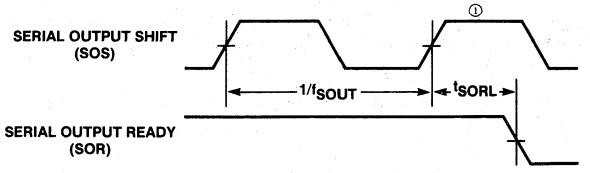
Figure 2. FIFO Full Specification (t_{SIRL})

Definition of Waveforms (cont'd)



① FIFO is empty, output ready remains Low and shift-out cannot be applied.
② After a word is shifted in, output ready goes High and shift-out can be applied.
③ The first serial bit is P0.

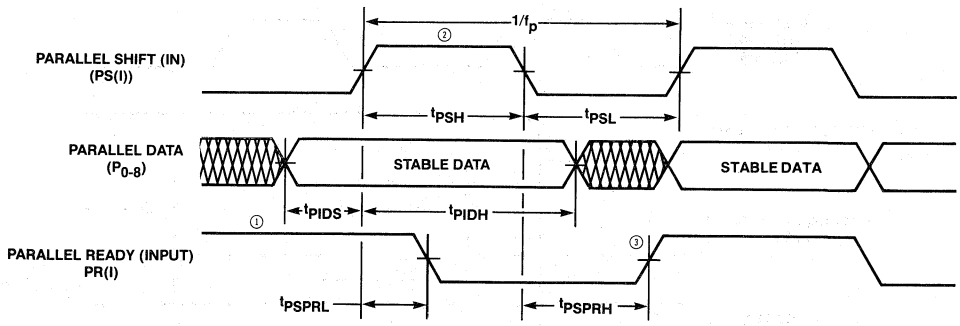
Figure 3. Serial Output Timing



① After the last shift-out, output ready goes Low indicating FIFO is empty.

Figure 4. FIFO Empty Specifications (t_{SORL})

Definition of Waveforms (cont'd)



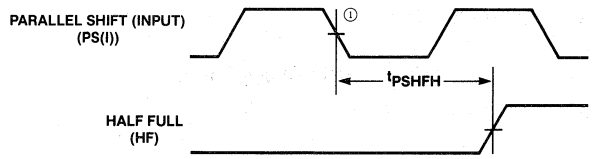
NOTE: P_{DIR} = High for the mode parallel-in to serial-out. Parallel ready is an output flag from the FIFO indicating that a word can be loaded into the FIFO.

① FIFO is not full and ready for input.

② PS (In) is asserted, shifting in parallel data P0-8.
PR (In) goes Low indicating parallel port is in use and no longer ready.
PR (In) will remain Low as long as PS (In) remains High.

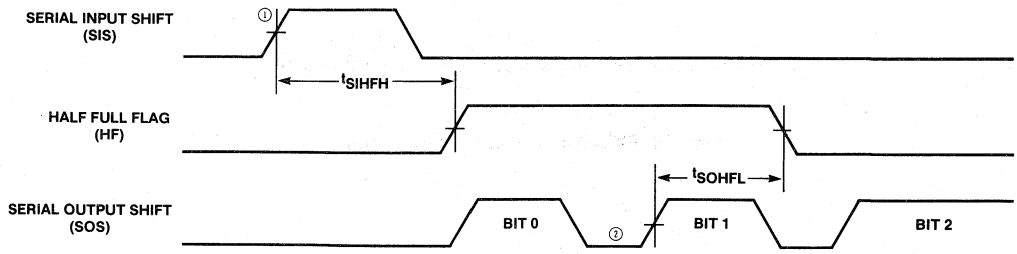
③ PS (In) has gone Low, allowing recent word to propagate through FIFO, PR (In) returns High when ready for more input.

Figure 5. Parallel Input Shift Timing



① for P_{DIR} = High, the direction is parallel-in to serial-out. After the 32nd shift-in, the half-full flag is set to High, and remains High, indicating the presence of 32 or more words.

Figure 6. Half-full Flag Specifications on Parallel (t_{PSHFH})

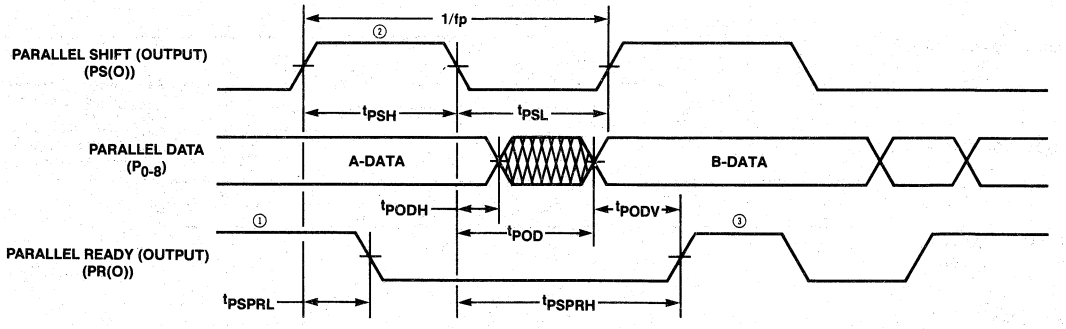


① When there are 31 words in the FIFO, the next shift-in on the 32nd word sets the half-full flag (HF) High indicating that there are 32 or more words.

② As soon as one word is partially shifted out, HF goes Low indicating there are less than 32 words.

Figure 7. Half-full Flag Specification on Serial Operation (t_{SIHFH}, t_{SOHFL})

Definition of Waveforms (cont'd)



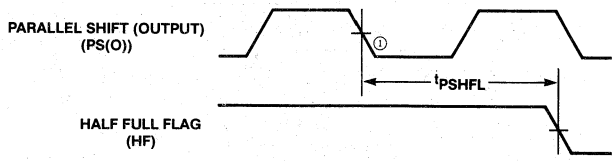
NOTE: For above conditions P_{DIR} = Low indicating that the direction is from serial-in to parallel-out. Thus parallel ready indicates the output status.

① FIFO is not empty and at least one word is valid and ready at P0-8 outputs.

② PS (Out) is asserted, shifting out parallel data. Data remains valid, but:
PR (Out) goes Low to indicate parallel port is in use and no longer ready.
PR (Out) will remain Low as long as PS (Out) remains High.

③ PS (Out) has gone Low, allowing data word to be shifted out. Next data word appears at output and PR (Out) is asserted to indicate valid data ready.

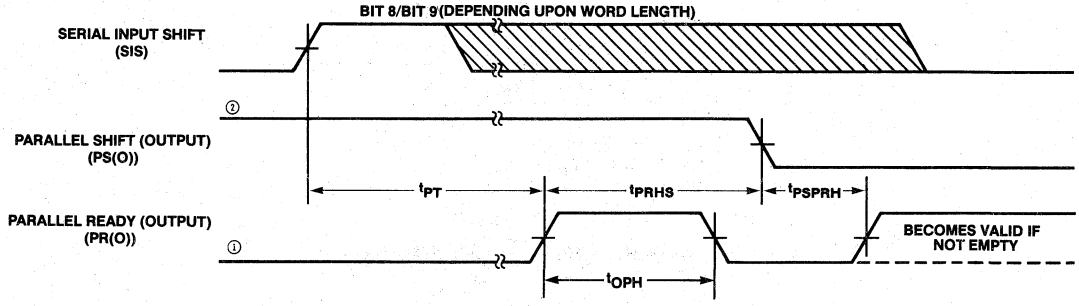
Figure 8. Serial-in to Parallel-out Specifications (t_{POD}, t_{PODH}, t_{ODV})



NOTE: For P_{DIR} = Low the direction is serial-in to parallel-out.

① When a word is shifted out and the half-full flag goes Low, 31 words or less are in the FIFO.

Figure 9. Half-full Flag Specification on Parallel Shift-out (t_{PSHFL})



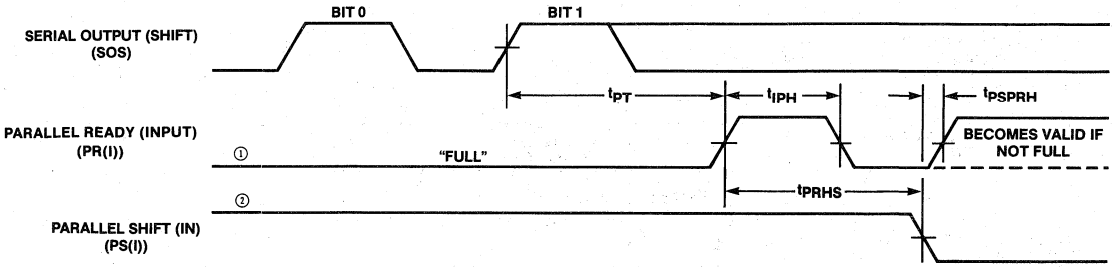
NOTE: P_{DIR} = Low indicating serial-in to parallel-out.

① FIFO initially empty.

② PS (Out) held High.

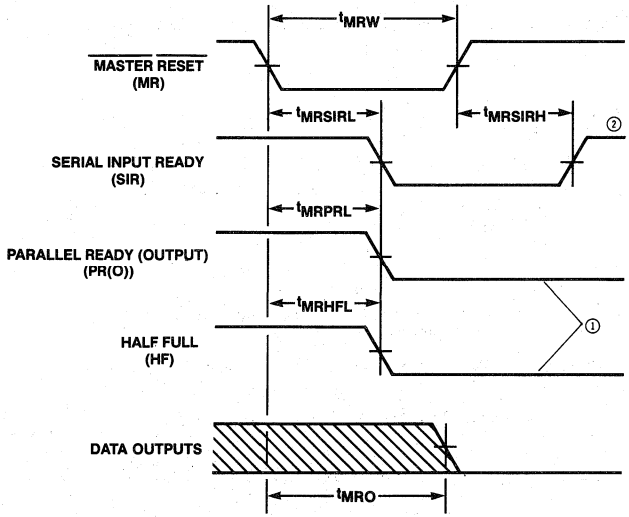
Figure 10. t_{PSPRH}, t_{PT}, t_{POH} Specifications (Serial Input Mode)

Definition of Waveforms (cont'd)



NOTE: P_{DIR} = High (parallel-in to serial-out).
① FIFO is full.
② PS (I) held High.

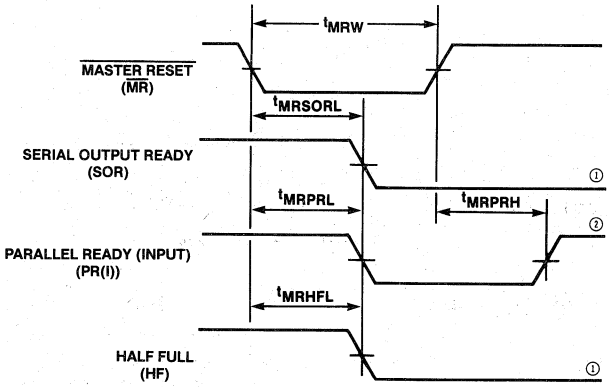
Figure 11. Fall-through Specifications



NOTE: P_{DIR} = Low.
① PR (O) and HF go Low.
② After $\overline{MR}$ goes High, SIR goes High.

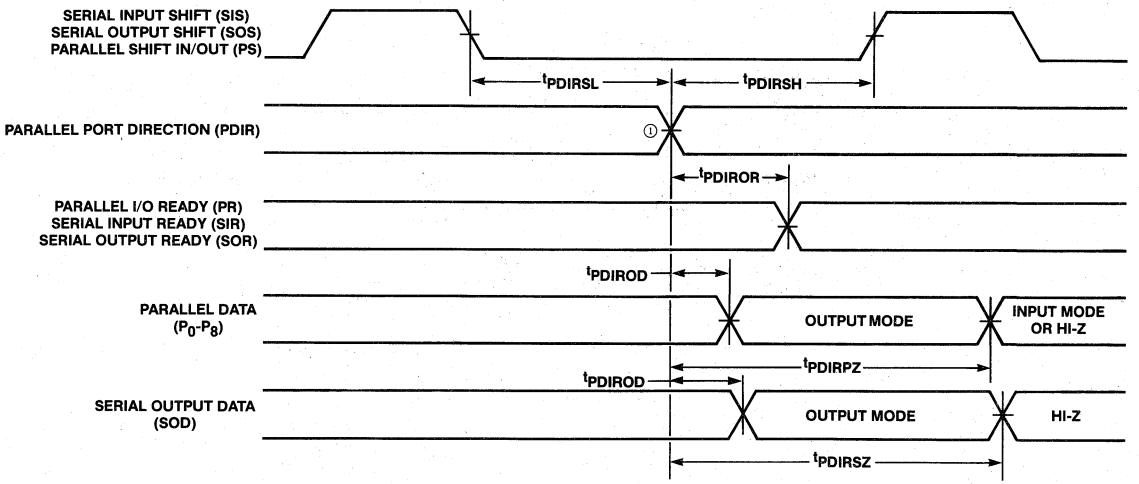
Figure 12. Master Reset Timing Serial-in to Parallel-out

Definition of Waveforms (cont'd)



NOTE: P_{DIR} = High.
① SOR and HF go Low.
② Affter $\overline{MR}$ goes High, PR(I) goes High.

Figure 13. Master Reset Timing (Parallel-in to Serial-out)



NOTE: When the FIFO is used as a stack, change the port direction before the FIFO is full; otherwise, data may be lost.

Figure 14. P_{DIR} Transition Parameters

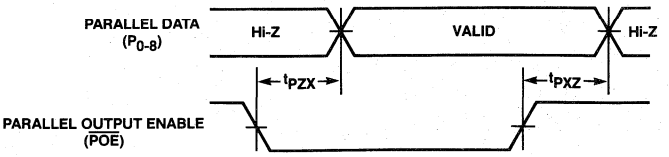


Figure 15. Parallel Port Enable and Disable Timing

Definition of Waveforms (cont'd)

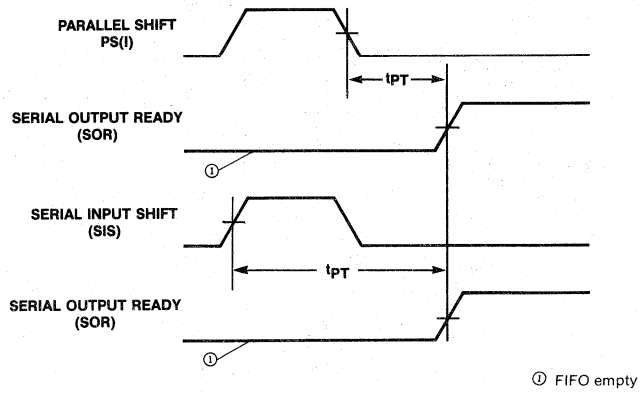


Figure 16. t_{PT} Specification (Shift-in to Serial Output Ready)

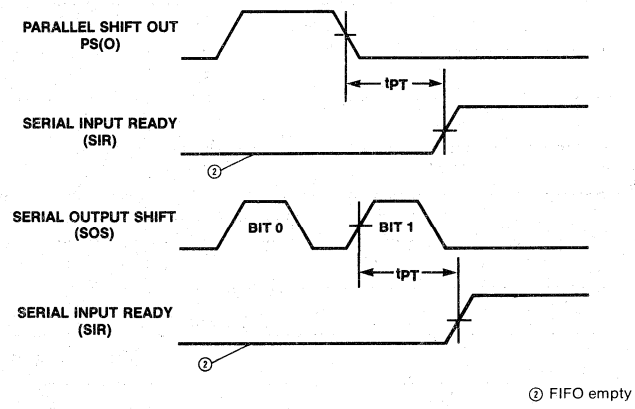
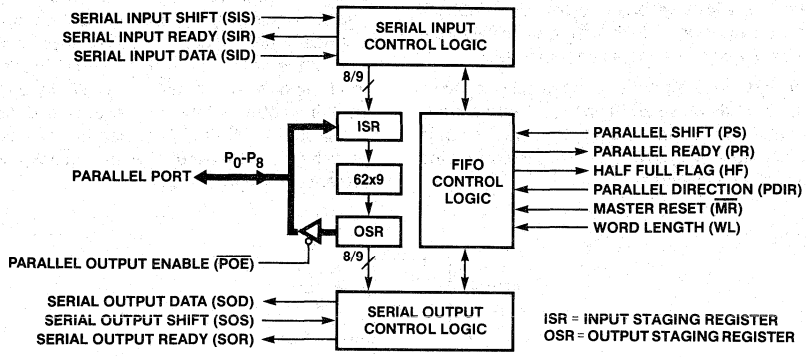


Figure 17. t_{PT} Specification (Shift-in to Serial Input Ready)

Appendix
Detailed Functional/Description for 67417

The 67417 is a serializing FIFO intended as a one-chip solution for data buffering and serializing/deserializing. It can be successfully used for interfacing parallel-format computing equipment to serial-format data communications and mass-memory equipment. The 67417 is a word-oriented device. It is meant to function with complete 8- or 9-bit words of data.



Basically the major internal subsystems of the 67417 are:

(i) The serial input port
(ii) The serial output port
(iii) The parallel port
(iv) The FIFO control logic and
(v) The cell array

Serial Port

The two serial ports (input and output) are entirely separate which allows a high-speed data rate of 28 MHz. These serial ports do not share data pins, control pins, or internal circuits. However, since the serial output data is a three-state output, the serial data ports could be connected together in the normal serial-parallel operation mode with separate SOR and SIR status signals.

The serial input port interface consists of the Serial Input Ready (SIR) output, Serial Input Data (SID) input, and the Serial Input Shift (SIS) clock input. Unlike the analogous SI and IR signals on the 67401/2, SIS and SIR do not accomplish a "handshake" with the rest of the logic of the system which incorporates the 67417; rather SIR is asserted whenever the 67417 is still capable of receiving at least one more bit. SIS is a positive edge-triggered input which sequences the serial input control logic. This logic in turn controls SIR and the 8/9-bit Input Staging Register (ISR).

The serial output port interface is the dual of the above, with a Serial Output Data (SOD) output, a Serial Output Shift (SOS) clock input, and a Serial Output Ready (SOR) status output. SOR is asserted whenever at least one more bit is available at the output. SOS is a positive edge-triggered input which sequences the 8/9-bit Output Staging Register (OSR). Serial Output Data is automatically three-stated whenever the serial output port is disabled (during Master Reset) and PDIR = Low. The parallel port is controlled by Parallel Shift (PS) input and Parallel Direction Input (PDIR). Parallel Ready (PR) is the handshake/status output. At the Parallel Port PS and PR *do* accomplish a handshake with the outside world as SI, IR, SO and OR on the 67401/2.

Parallel Port

This is a fully bidirectional port, and it operates at a more conservative data rate of 10 MHz. The input-staging register (ISR) internally controls the parallel input data port bus signals. Likewise the OSR internally controls the parallel output data port. The ISR data outputs drive the parallel data inputs to the cell array, and the OSR inputs are likewise driven by the final parallel data stage of the cell array

Modes of Operation

There are three modes in which the 67417 can operate

(i) Parallel-in to serial-out
(ii) Serial-in to parallel-out and
(iii) Serial-in to serial-out.

In the parallel-in to serial-out mode, PDIR = HIGH. Thus Parallel Shift (PS) acts as a Shift In (SI) and similarly, Parallel Ready (PR) as Input Ready (IR). The first bit shifted out of the serial port will be bit 0 of the parallel word input.

Similarly for serial-in to parallel-out mode, PDIR = LOW, and Parallel Shift (PS) acts as a Shift Out(SO) and Parallel Ready (PR) as Output Ready (OR). The first bit shifted into the serial port will be bit 0 of the parallel word output.

If the direction mode for a particular application of the 67417 is not intended to change during system operation, the PDIR input should be strapped to a logic LOW or HGH.

In the serial-in to serial-out mode, PDIR = 10 V minimum.

The parallel port does not function during this mode and is three-stated. The direction operating mode should not be changed if the FIFO is FULL otherwise stored data will be lost.

Cell Array

The 67417 cell array can function *either* as a 64x8 FIFO (with the 9th bit padded to a zero) or as a 64x9 FIFO, according to the setting of the word length (WL) control input. Like the PDIR

control input, WL can be switched at electronic speeds during system operations; but if the word length of a particular 67417 is *never* to change during system operation, WL for that part can be strapped to ground or V_{CC}.

It is a permissible 67417 mode of operation to almost fill the FIFO (there should be at least two empty locations) with WL set to 8-bit operation, then switch WL to 9-bit operation (WL = HIGH) to load one more word plus a frame marker in the last bit, and then switch PDIR and unload the 67417 in a 9-bit mode. This sequence of operations has the effect of providing a "frame marker bit" in the ninth bit of the last word loaded. The corresponding 9th bits will have been zeroed by the 67417 internal logic for all the other words in the frame since they were loaded while the 67417 was operating as an 8-bit device.

It is, however, the system designer's responsibility to avoid changing PDIR inputs when only part of an 8- or 9-bit word has been received or transmitted. In general, if such a change occurs, the part in general will try to add zero bits to pad out the impacted word to assume full length.

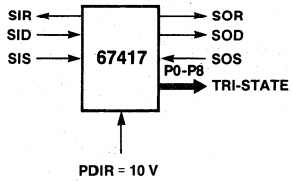
Half-Full Flag

This status output indicates when the 67417 statically contains 32 words or more. This provides an indication to send in more data if the device is operated in a mostly-empty mode or send out more data if the 67417 is operated in a mostly-full mode.

Cascading

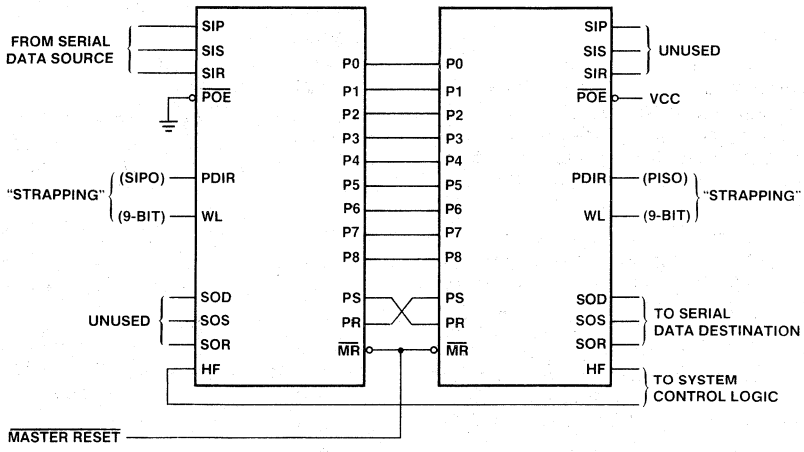
The 67417 is designed to be cascaded at the parallel port only, due to very high data transfer rates at the serial ports. Cascading two 67417's is accomplished by connecting Parallel Input/Output Ready (PR) of each part to control the Parallel Shift In/Out (PS) of the other part, with one FIFO in serial-in to parallel-out mode, and the other FIFO in parallel-in to serial-out mode. The combined effect of this is a reversible 128x8 or 128x9 serial-in serial-out FIFO. The 67417 can not be cascaded at the serial ports because SIR and SOR are not acknowledged signals but rather status signals only.

Applications



NOTE: It can shift in data serially in the multiples of 8- or 9-bit according to WL.

Figure 18. 512/576x1 Serial-in to Serial-out Mode



* SIPO = Serial-in to Parallel-out.
** PISO = Parallel-in to Serial-out.

Figure 19. Cascading of Two 'S417s for Serial-in to Serial-out Operation as a 128x9 (1152x1) FIFO

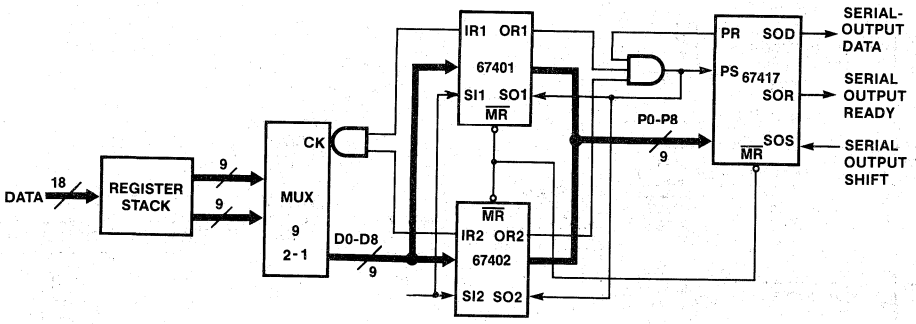


Figure 20. An Example of an Expansion Scheme for a 64x18 Parallel-to-Serial FIFO

An 18-bit data word is multiplexed into the two 67401/2 FIFOs. Since the 67417 FIFO is cascadable at the parallel port only, two 67401/2 FIFOs were used along with the 67417 to obtain the appropriate organization.

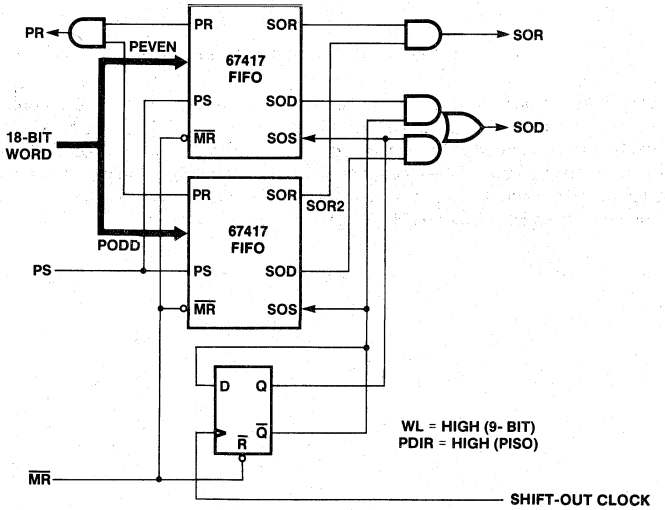


Figure 21. Another Example of an Expansion Scheme for a 64x18 Parallel-in to Serial-out FIFO Two 67417 FIFOs Are Used to Implement a 64x18 Parallel-in to Serial-out FIFO

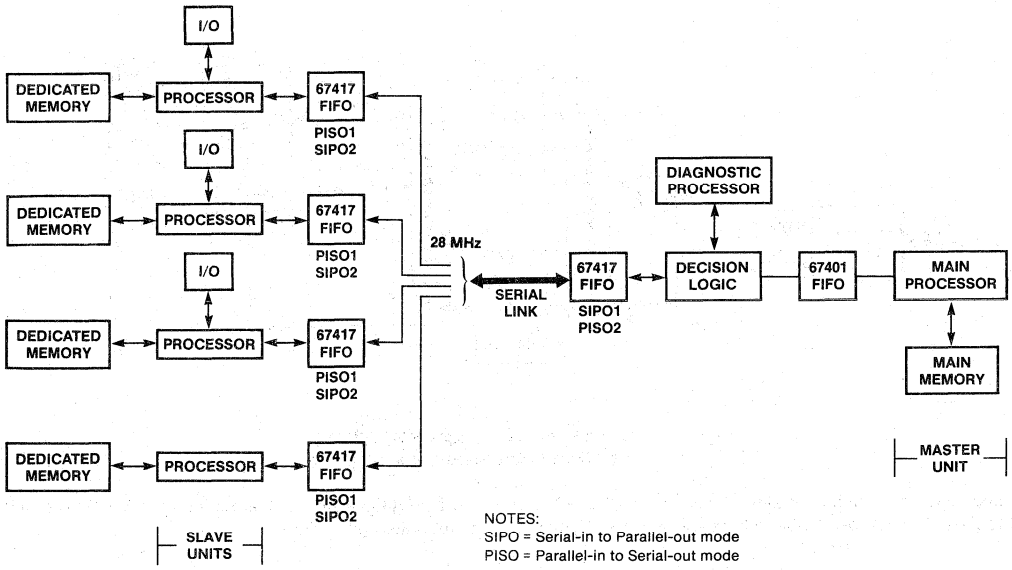


Figure 22. A Multiprocessing System

Each processor unit on the left has its own communication interface which consists of a serializing FIFO. The serial data link can operate in either direction 1 or direction 2 which is decided by the Decision logic. In direction 1 either of the slave units send the data to the master over the serial link, with its respective 67417 operating in parallel-in to serial-out mode (PISO1). While the 67417 for the master unit operates in serial-in to parallel-out mode (SIPO1). The direction 2 has the FIFOs (67417) operating in the reverse direction from the above case. Decision logic determines the priority of the slave processors to use the serial link.

First-In First-Out (FIFO) 64x5 Memory 15 MHz (Cascadable)

C67L4033D

Features/Benefits

- **High-speed 15 MHz shift-in/shift-out rates**
- **High drive capability**
- **Low-power consumption**
- **Three-state outputs**
- **Fully expandable by word width and depth**
- **Half-Full and Almost-Full/Empty status flags**
- **Structured pinouts. Output pins directly opposite corresponding input pins.**
- **Asynchronous operation**
- **TTL-compatible inputs and outputs**

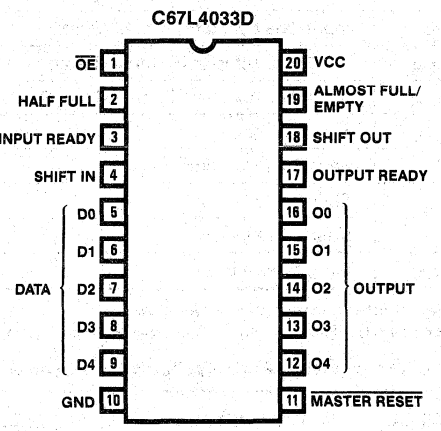
Ordering Information

PART NUMBER	PKG	TEMP	DESCRIPTION
C67L4033D	N,J	Com	15 MHz in/out

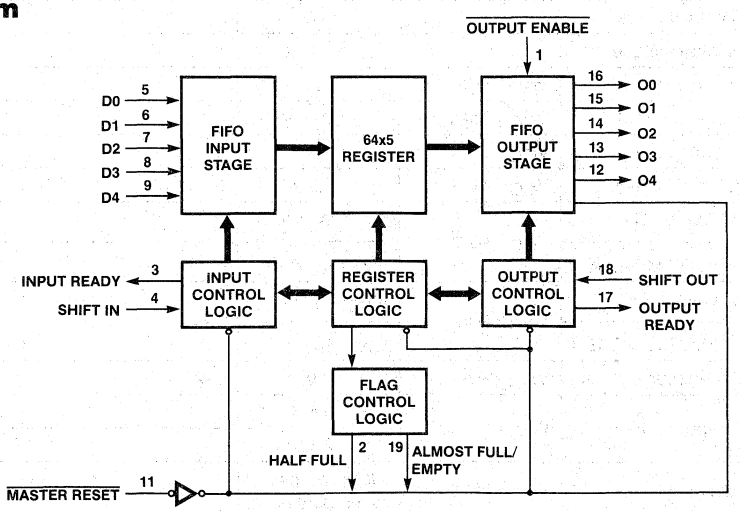
Description

The C67L4033D is a high-speed, 64x5 First-In-First-Out (FIFO) memory which operates at 15 MHz input/output rates. The data is loaded and emptied on a first-in-first-out basis. It is a three-state device with high-drive (I_{OL} = 24 mA) data outputs. These devices can be expanded to any word width and depth. It has a Half-Full flag (thirty-two or more words full) and an almost full/empty flag (fifty-six or more words or eight or less words). The main application of C67L4033D is as a rate buffer; sourcing and absorbing data at different rates. Other applications are high-speed tape and disk controllers, data communications systems and plotter control systems.

Pin Configuration



Block Diagram



Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65°C to +150°C

Operating Conditions Over Temperature Range

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		70	°C
f_{IN}	Shift In rate	1			15	MHz
t_{SIH}*	Shift in HIGH time	1	24			ns
t_{SIL}*	Shift in LOW time	1	15			ns
t_{IDS}	Input data setup to SI (Shift In)	1	0			ns
t_{IDH}	Input data hold time from SI (Shift In)	1	26			ns
t_{RIDS}	Input data setup to IR (Input Ready)	4	0			ns
t_{RIDH}	Input data hold time from IR (Input Ready)	4	26			ns
f_{OUT}	Shift Out rate	5			15	MHz
t_{SOH}**	Shift Out HIGH time	5	17			ns
t_{SOL}	Shift Out LOW time	5	15			ns
t_{MRW}*	Master Reset pulse	10	35			ns
t_{MRS}**	Master Reset to SI	10	35			ns

* See AC test and high-speed application note.
** If the FIFO is not full (IR High), $\overline{MR}$ low forces IR low, followed by IR returning high when $\overline{MR}$ goes high.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITION		COMMERCIAL MIN	COMMERCIAL MAX	UNIT
V_{IL}*	Low-level input voltage					0.8	V
V_{IH}*	High-level input voltage				2		V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = -18 mA		-1.5	V
I_{IL}	Low-level input current		V_{CC} = MAX	V_I = 0.45 V		-250	µA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.4 V		50	µA
I_I	Maximum input current		V_{CC} = MAX	V_I = 5.5 V		1	mA
V_{OL}	Low-level output voltage	Output, O	V_{CC} = MIN	I_{OL} = 24 mA		0.5	V
		IR,OR,HF,AF/E		I_{OL} = 8 mA		0.5	
V_{OH}	High-level output voltage	Output, O	V_{CC} = MIN	I_{OH} = - 3 mA	2.4		V
		IR,OR,HF,AF/E		I_{OH} = -0.9 mA			
I_{OS}**	Output short-circuit current		V_{CC} = MAX	V_O = 0 V	-20	-90	mA
I_{OZL}	Off-state output current		V_{CC} = MAX	V_O = 0.4 V		-50	µA
I_{OZH}				V_O = 2.4 V		50	
I_{CC}	Supply current		V_{CC} = MAX	All inputs low. All outputs open.		120	mA

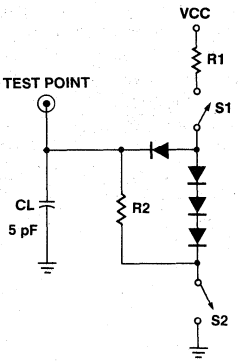
* These are absolute voltages with respect to GND (Pin 10) and include all overshoots due to system and/or tester noise.
** Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL MAX	UNIT
t_{IRL}	Shift In ↑ to Input Ready LOW	1		40	ns
t_{IRH}	Shift In ↓ to Input Ready HIGH	1		26	ns
t_{ORL}	Shift Out ↑ to Output Ready LOW	5		45	ns
t_{ORH}	Shift Out ↓ to Output Ready HIGH	5		50	ns
t_{ODH}	Output Data Hold (previous word)	5	12		ns
t_{ODS}	Output Data Shift (next word)	5		40	ns
t_{PT}	Data throughput	4,8		1600	ns
t_{MRORL}	Master Reset ↓ to Output Ready LOW	10		60	ns
t_{MRIRH}*	Master Reset ↑ to Input Ready HIGH	10		30	ns
t_{MRIRL}*	Master Reset ↓ to Input Ready LOW	10		50	ns
t_{MRO}	Master Reset ↓ to Outputs LOW	10		60	ns
t_{IPH}	Input ready pulse HIGH	4	17		ns
t_{OPH}	Output ready pulse HIGH	8	24		ns
t_{ORD}	Output ready ↑ to Data Valid	5		-3	ns
t_{AEH}*	Shift Out ↑ to AF/E HIGH	11		320	ns
t_{AEL}*	Shift In ↑ to AF/E LOW	11		1400	ns
t_{AFL}*	Shift Out ↑ to AF/E LOW	12		1400	ns
t_{AFH}*	Shift In ↑ to AF/E HIGH	12		320	ns
t_{HFH}*	Shift In ↑ to HF HIGH	13		800	ns
t_{HFL}*	Shift Out ↑ to HF LOW	13		800	ns
t_{PHZ}*	Output Disable Delay	A		30	ns
t_{PLZ}*				30	
t_{PZL}*	Output Enable Delay			30	ns
t_{PZH}*				40	

* See timing diagram for explanation of parameters.

Three-State Test Load



See table on following page for Resistor values

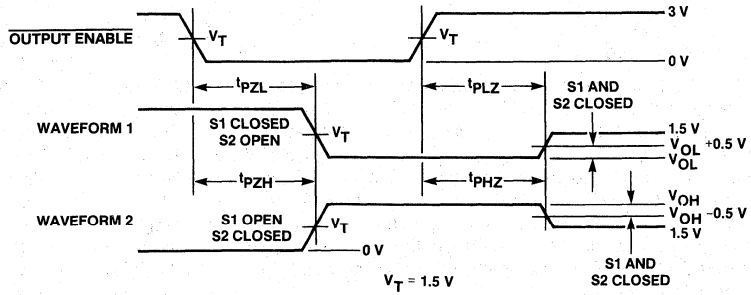
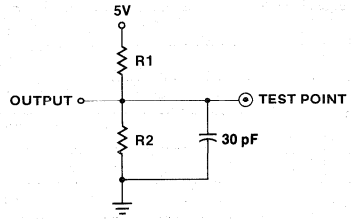


Figure A. Enable and Disable

Waveform 1 is for a data output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for a data output with internal conditions such that the output is high except when disabled by the output control.

Standard Test Load



I_{OL}	R1	R2
24 mA (Data)	200 Ω	300 Ω
8 mA (IR, OR, Flags)	600 Ω	1200 Ω

Input Pulse Amplitude = 3 V
Input Rise and Fall Time (10%-90%) = 2.5 ns
Measurements made at 1.5 V
All Diodes are 1N916 or 1N3064

Functional Description

Data Input

After power up the Master Reset is pulsed low (Figure 10) to prepare the FIFO to accept data in the first location. Master Reset must be applied prior to use to ensure proper operation. When Input Ready (IR) is HIGH the first location is ready to accept data from the D_X inputs. Data then present at the the data inputs is entered into the first location when the Shift-In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Once data is entered into the first cell, the transfer of data in any full cell to the adjacent (downstream) empty cell is automatically activated by an on-chip control. Thus data will stack up at the end of the device (while empty locations will "bubble" to the front when data is shifted out). t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating more room is available. If the memory is full, IR will remain LOW. The FIFO should always be cleared by using Master Reset before starting the operation.

Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that there is valid upstream data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW and Data output will not be valid.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

AC Test and High-Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 20 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. Monolithic Memories recommends a monolithic ceramic capacitor of 0.1 μF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input Ready combination, as well as the Shift-Out-Output Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or effected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time (T_{IDH}) and the next activity of Input Ready (T_{IRL}) to be extended relative to Shift-in going HIGH. This same type of problem is also related to T_{IRH}, T_{ORL} and T_{ORH} as related to Shift-Out. For high-speed applications, proper grounding technique is essential.

Timing Waveforms

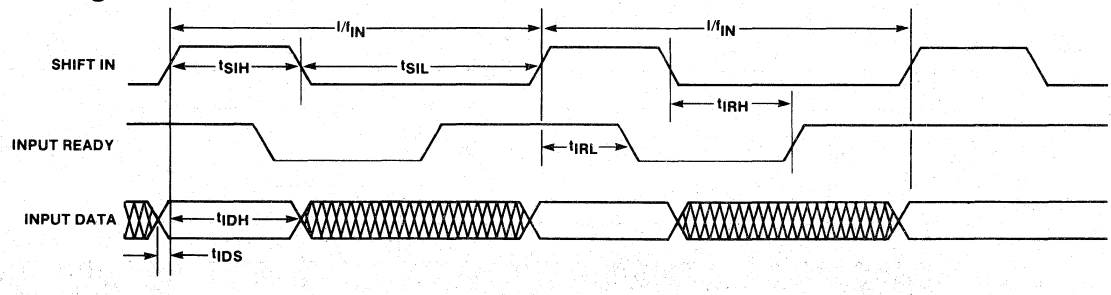


Figure 1. Input Timing

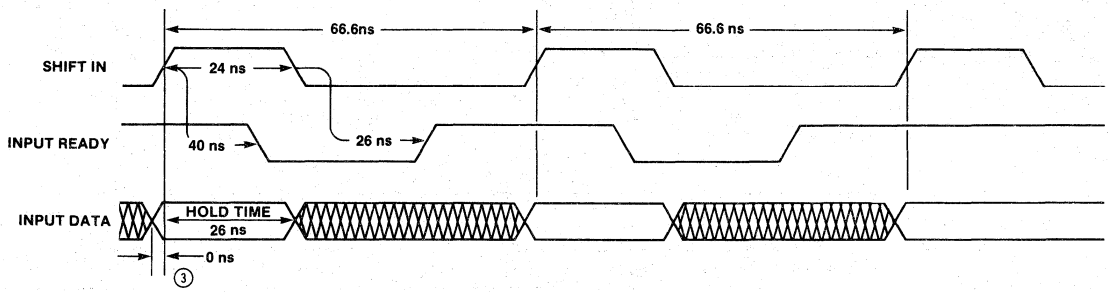


Figure 2. Typical Waveforms for 15 MHz Shift-In Data Rate

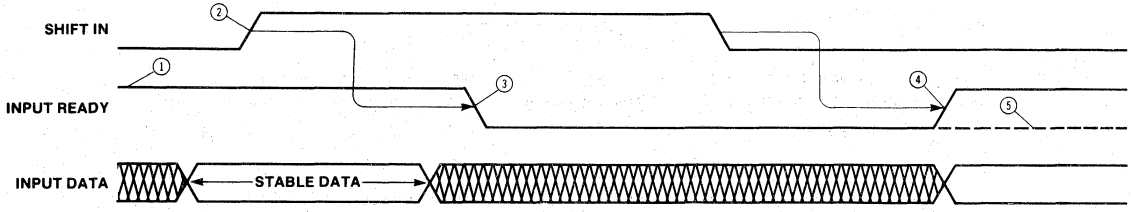


Figure 3. The Mechanism of Shifting Data into the FIFO

① Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.

② Input Data is loaded into the first word. The data from the first word is released for "fall-through" to second word.

③ Input Ready goes LOW indicating the first word is full.

④ Shift-In going LOW allows Input Ready to sense the status of first word. The first word is now empty as indicated by Input Ready HIGH.

⑤ If the second word is already full then data remains at the first word. Since the FIFO is now full Input Ready remains low.

Note: Shift-In pulses applied while Input Ready is LOW will be ignored (See Figure 5).

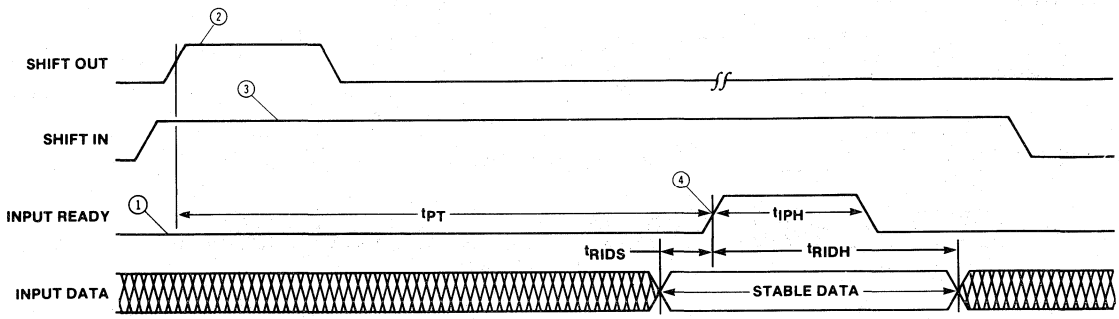


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

① FIFO is initially full.

② Shift Out pulse is applied. An empty location starts "bubbling" to the front.

③ Shift In is held HIGH.

④ As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.

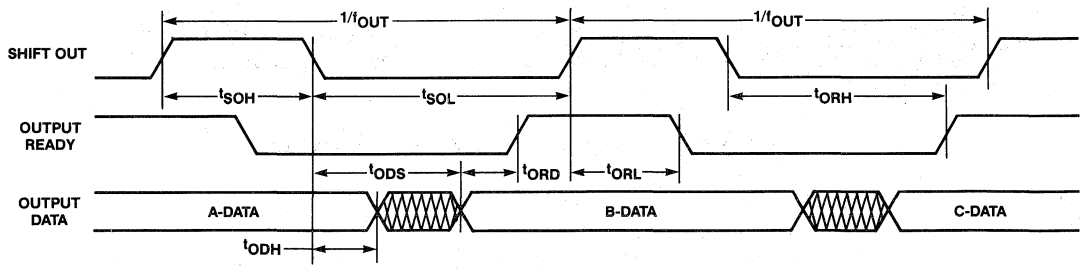


Figure 5. Output Timing

① The diagram assumes that at this time, words 64, 63 and 62 are loaded with A, B and C Data, respectively.

② Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e., OR and SO are both high together.

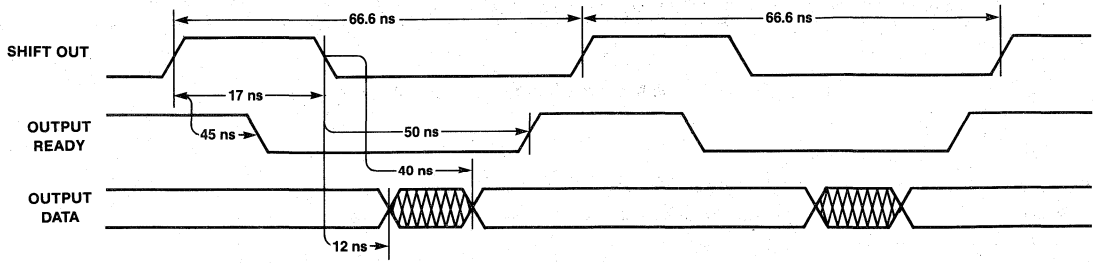


Figure 6. Typical Waveforms for 15 MHz Shift-Out Data Rate

① The diagram assumes that at this time words 64, 63 and 62 are loaded with A, B and C Data, respectively.

② Data in the first crosshatched region may be A or B Data.

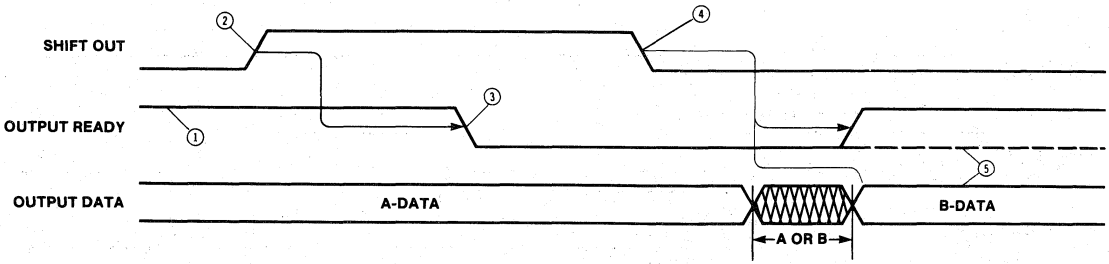


Figure 7. The Mechanism of Shifting Data Out of the FIFO

① Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.
② Shift-Out goes HIGH causing the contents of word 63 (B-Data) to be released for fall-through to word 64. Output data remains as valid A-Data while Shift-Out is HIGH.
③ Output Ready goes LOW.
④ Shift-out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.
⑤ If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data becomes invalid.

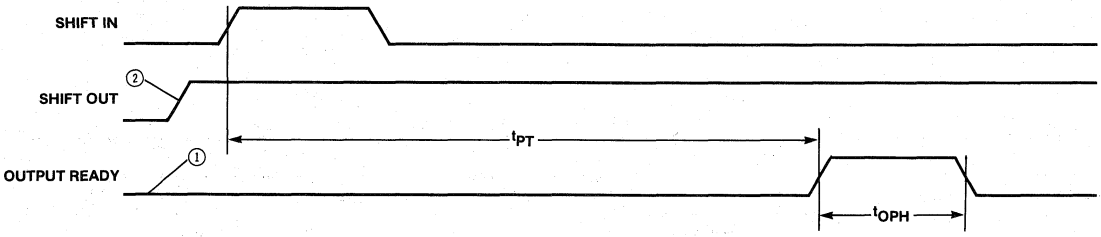


Figure 8. t_{PT} and t_{OPH} Specification

① FIFO initially empty.
② Shift-Out is held HIGH.

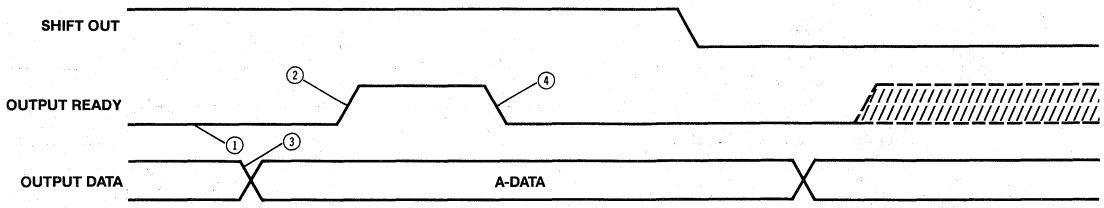


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH

① Word 64 is empty.
② Output Ready goes HIGH indicating arrival of the new data.
③ New data (A) arrives at the outputs (word 64).
④ Since Shift Out is held HIGH, Output Ready goes immediately LOW.
⑤ As soon as Shift Out goes LOW the Output Data is subject to change. Output Ready will go HIGH or LOW depending on whether there are any additional upstream words in the FIFO.

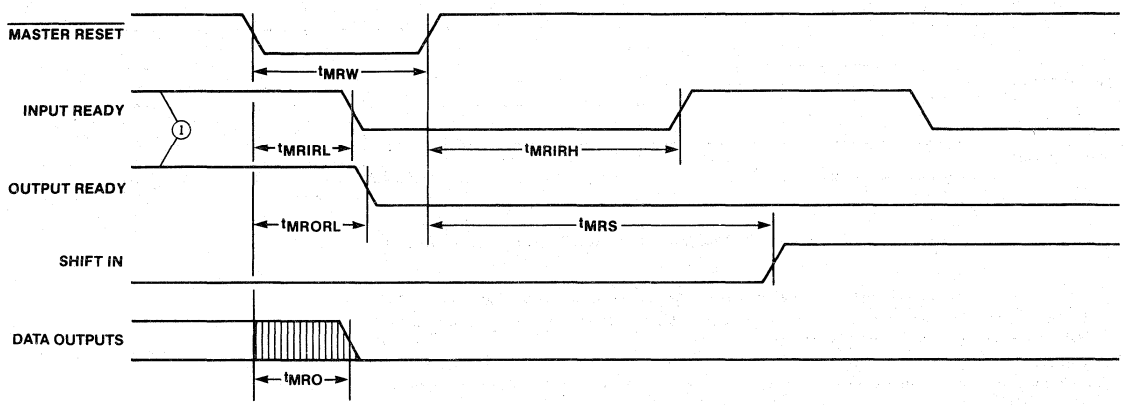


Figure 10. Master Reset Timing

① FIFO is partially full.

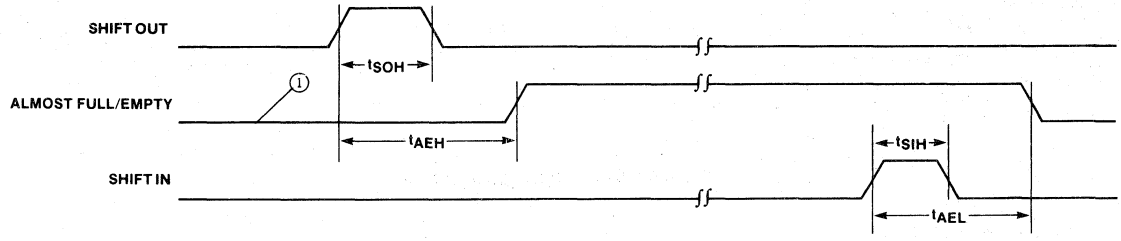


Figure 11. t_{AEH}, t_{AEL} Specifications

① FIFO contains 9 words (one more than almost empty).

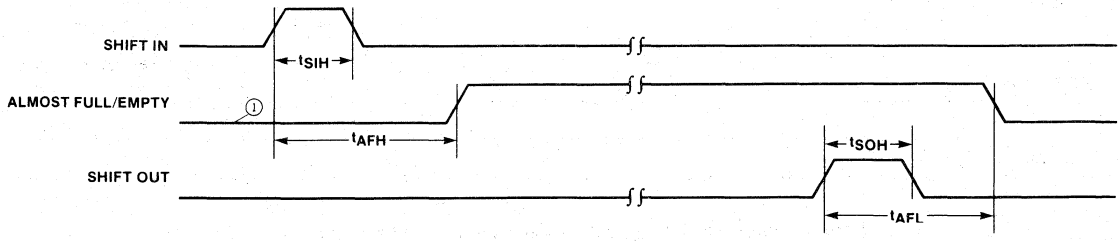


Figure 12. t_{AFH}, t_{AFL} Specifications

① FIFO contains 55 words (one short of almost full).

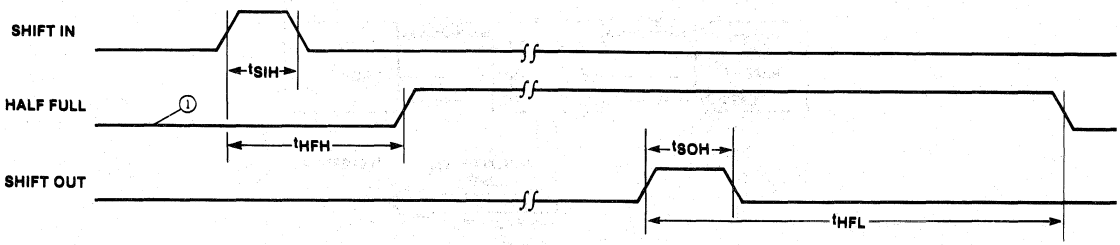
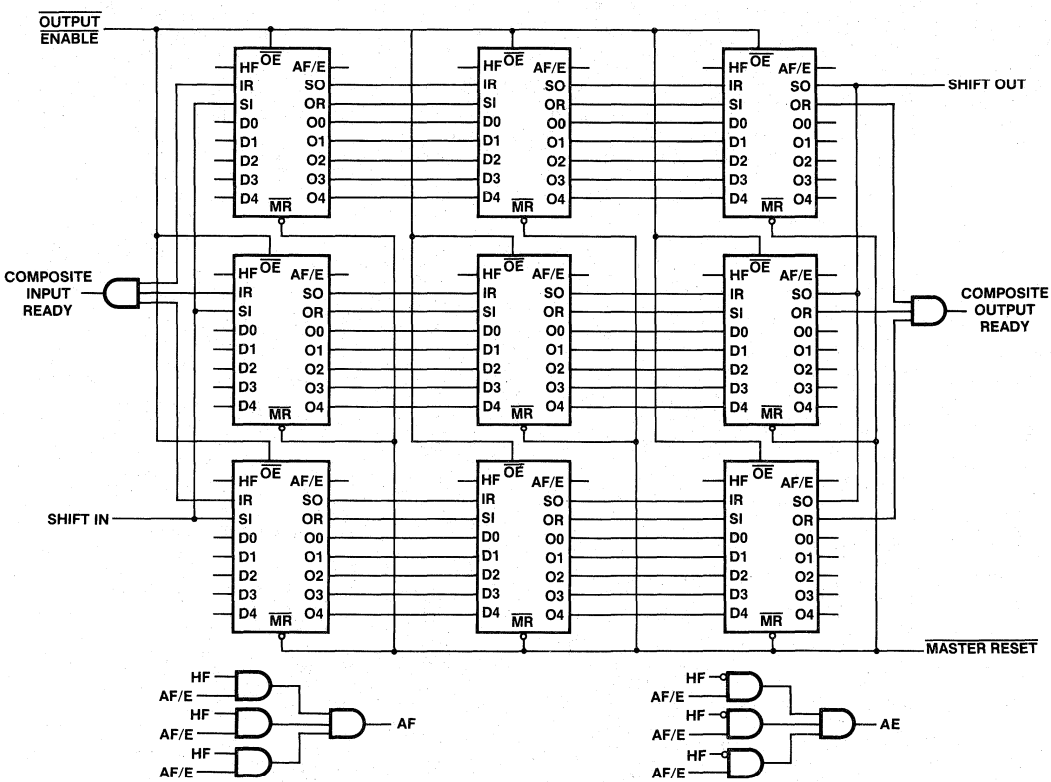


Figure 13. t_{HFL}, t_{HFH} Specifications

① FIFO contains 31 words (one short of half full).



The First Column of FIFOs **The Last Column of FIFOs**

Almost Full (AF) is eight words or less to FIFO full.
Almost Empty (AE) is eight words or less to FIFO empty

Figure 14. 192x15 FIFO with C67L4033D

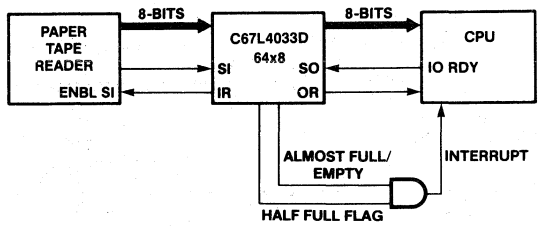


Figure 15. Application for C67L4033D "Slow and Steady Rate to Fast 'Blocked Rate' "

Note: Cascading the FIFO's in word width is done by ANDing the IR and OR as shown in Figure 14.

First-In First-Out (FIFO) 64x4 Memory 15 MHz (Cascadable) With Three-State Outputs

C67L4013D

Features/Benefits

- High-speed 15-MHz shift-in/shift-out rates
- Low power consumption
- TTL inputs and outputs
- Readily expandable in word width and depth
- Structured pinouts. Output pins directly opposite corresponding input pins
- High-drive capability
- Asynchronous operation
- Output Enable feature

Ordering Information

PART NUMBER	PKG	TEMP	O/P	DESCRIPTION
C67L4013D	N, J	Com	3-state	15 MHz 64x4 FIFO

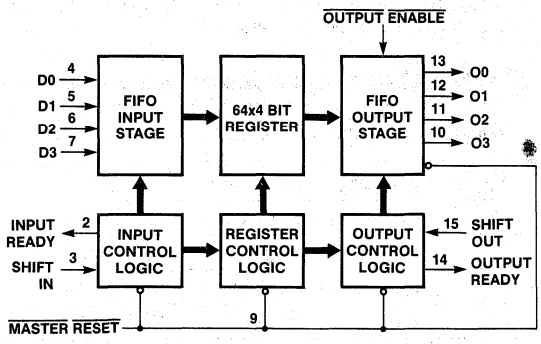
8

Description

The C67L4013D is a "fall-through" high-speed First-In First-Out (FIFO) memory organized 64 words by 4 bits. The FIFO is expandable in word width and depth. The FIFO is attractive for many applications such as disk controllers, communication buffers, rate buffers, etc. The C67L4013D has three-state, high-drive (I_{OL} = 24 mA) outputs.

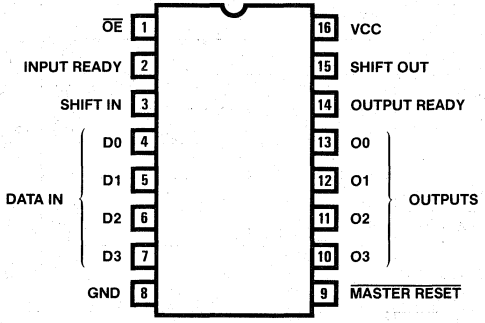
Block Diagram

C67L4013D



Pin Configuration

C67L4013D



Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65°C to +150°C

Operating Conditions Over Temperature Range

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		70	°C
f_{IN}	Shift in rate	1			15	MHz
t_{SIH}	Shift in High time	1	24			ns
t_{SIL}	Shift in Low time	1	15			ns
t_{IDS}	Input data setup to SI (Shift In)	1	0			ns
t_{IDH}	Input data hold time to SI (Shift In)	1	26			ns
t_{RIDS}	Input data setup to IR (Input Ready)	4	0			ns
t_{RIDH}	Input data hold time to IR (Input Ready)	4	26			ns
f_{OUT}	Shift out rate	5			15	MHz
t_{SOH}	Shift out High time	5	17			ns
t_{SOL}	Shift out Low time	5	15			ns
t_{MRW}	Master Reset pulse**	10	35			ns
t_{MRS}	Master Reset to SI*	10	35			ns

* If the FIFO is not full (IR High), $\overline{MR}$ low forces IR low, followed by IR returning high when $\overline{MR}$ goes high.
** See AC test and high-speed application note.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITION		COMMERCIAL MIN	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.8**	V
V_{IH}	High-level input voltage				2**		V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = -18 mA		-1.5	V
I_{IL}	Low-level input current		V_{CC} = MAX	V_I = 0.45 V		-250	μA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.4 V		50	μA
I_I	Maximum input current		V_{CC} = MAX	V_I = 5.5 V		1	mA
V_{OL}	Low-level Output voltage	Output, O	V_{CC} = MIN	I_{OL} = 24 mA		0.5	V
		IR, OR		I_{OL} = 8 mA			
V_{OH}	High-level Output voltage	Output, O	V_{CC} = MIN	I_{OH} = -3.0 mA	2.4		V
		IR, OR		I_{OH} = -0.9 mA			
I_{OS}	Output short-circuit current*		V_{CC} = MAX	V_O = 0V	-20	-90	mA
I_{OZL}	Off-state output current		V_{CC} = MAX	V_O = 0.4 V		-50	μA
I_{OZH}				V_O = 2.4 V		+50	
I_{CC}	Supply current		V_{CC} = MAX All inputs low. All outputs open.			110	mA

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
** These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL MAX	UNIT
t_{IRL}†	Shift In ↑ to Input Ready LOW	1		40	ns
t_{IRH}†	Shift In ↓ to Input Ready HIGH			26	ns
t_{ORL}†	Shift Out ↑ to Output Ready LOW	5		45	ns
t_{ORH}†	Shift Out ↓ to Output Ready HIGH			50	ns
t_{ODH}†	Output Data Hold (previous word)		12		ns
t_{ODS}	Output Data Shift (next word)			40	ns
t_{PT}	Data throughput	4,8		1600	ns
t_{MRORL}	Master Reset ↓ to Output Ready LOW	10		60	ns
t_{MRIRH}	Master Reset ↑ to Input Ready HIGH*			30	ns
t_{MRIRL}	Master Reset ↓ to Input Ready LOW*			50	ns
t_{MRO}	Master Reset ↓ to Outputs LOW			60	ns
t_{IPH}	Input ready pulse HIGH	4	17		ns
t_{OPH}	Output ready pulse HIGH	8	24		ns
t_{ORD}	Output ready ↑ to Data Valid	5		-3	ns
t_{PHZ}	Output Disable Delay, C67L4013D	A		30	ns
t_{PLZ}				30	
t_{PZL}	Output Enable Delay, C67L4013D			30	ns
t_{PZH}				40	

Note: Typicals at 5V V_{CC} and 25°C T_A.

* If the FIFO is not full (IR High), $\overline{MR}$ low forces IR low, followed by IR returning high when $\overline{MR}$ goes high.

† See AC test and high-speed application note.

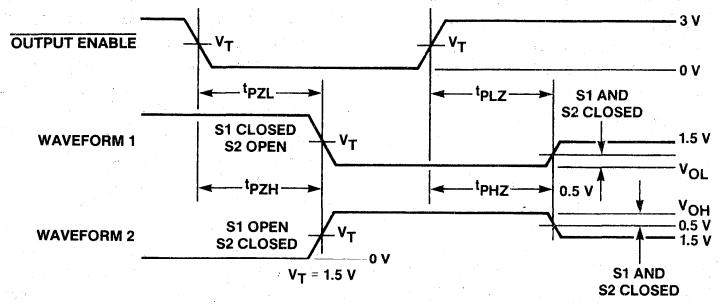
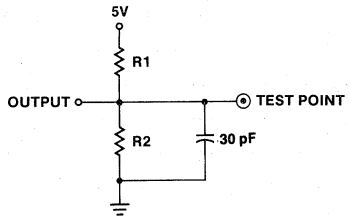


Figure A. Enable and Disable

Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

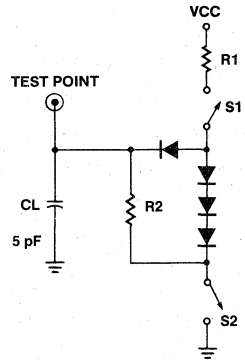
Standard Test Load



I_{OL}	R1	R2
24 mA	200 Ω	300 Ω
8 mA	600 Ω	1200 Ω

Input Pulse Amplitude = 3 V
Input Rise and Fall Time (10%-90%) = 2.5 ns
Measurements made at 1.5 V
All Diodes are 1N916 or 1N3064

Three-State Test Load



Functional Description

Data Input

After power up the Master Reset is pulsed low (Figure 10) to prepare the FIFO to accept data in the first location. Master reset must be applied prior to use to ensure proper operation. When Input Ready (IR) is HIGH the first location is ready to accept data from the D_X inputs. Data then present at the data inputs is entered into the first location when the Shift-In (SI) is brought HIGH. An SI HIGH signal causes the IR to go LOW. Once data is entered into the first cell, the transfer of data from any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating more room is available. If the memory is full, IR will remain LOW. The FIFO should always be cleared by using master reset.

Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided the upstream stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW and Data output will not be valid.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

AC Test and High-Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 20 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. Monolithic Memories recommends a monolithic ceramic capacitor of 0.1 μF directly between VCC and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input-Ready combination, as well as the Shift-Out-Output-Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input Ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or effected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time (T_{IDH}) and the next activity of Input Ready (T_{IRL}) to be extended relative to shift-in going HIGH. This same type of situation occurs with T_{ORL} and T_{ORH} as related to Shift-Out. For high-speed applications, proper grounding technique is essential.

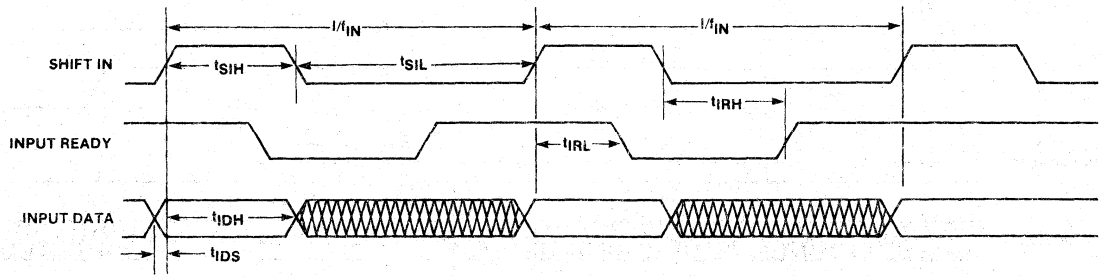


Figure 1. Input Timing

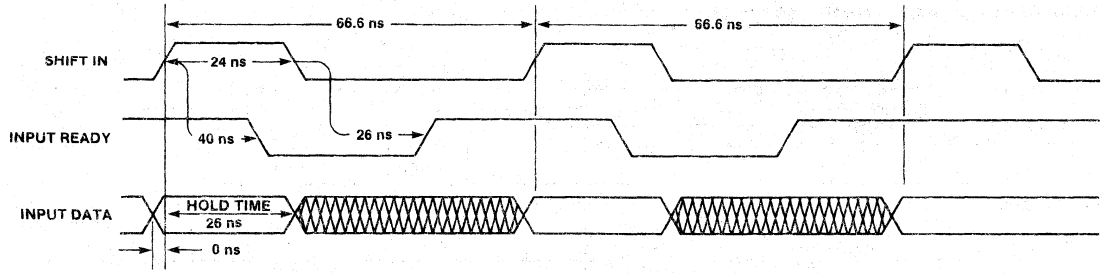


Figure 2. Typical Waveforms for 15 MHz Shift-In Rate

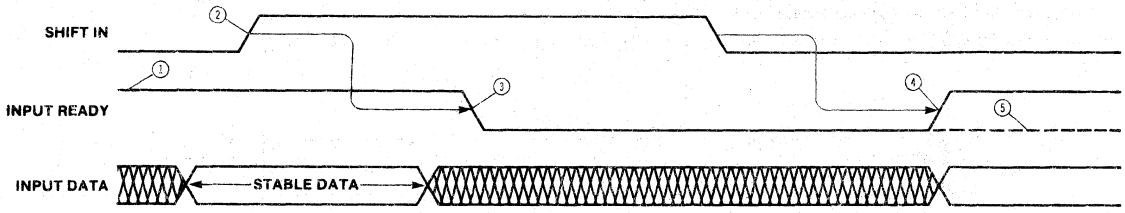


Figure 3. The Mechanism of Shifting Data into the FIFO

① Input Ready HIGH indicates space is avialable and a Shift-In pulse may be applied.

② Input Data is loaded into the first word. The Data from the first word is released for "fall-through" to second word.

③ Input Ready goes LOW indicating the first word is full.

④ Shift-In going LOW allows Input Ready to sense the status of first word. The first word is now empty as indicated by Input Ready HIGH.

⑤ If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

Note: Shift-In pulses applied while Input Ready is LOW will be ignored (See Figure 5).

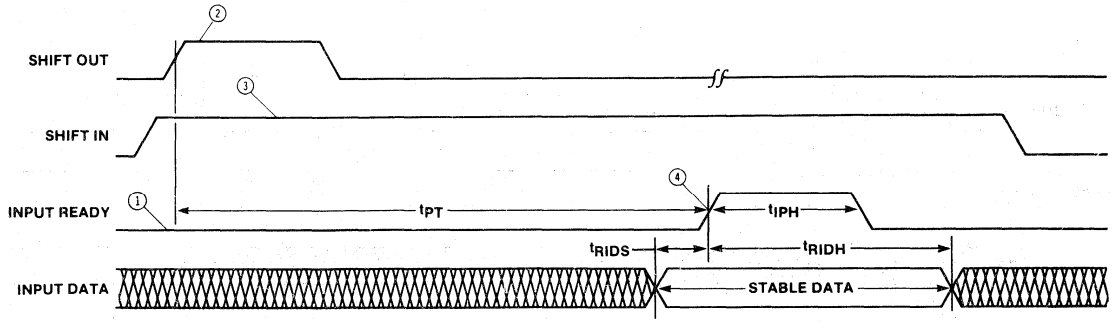


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

① FIFO is initially full.

② Shift Out pulsed is applied. An empty location starts "bubbling" to the front.

③ Shift In is held HIGH.

④ As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.

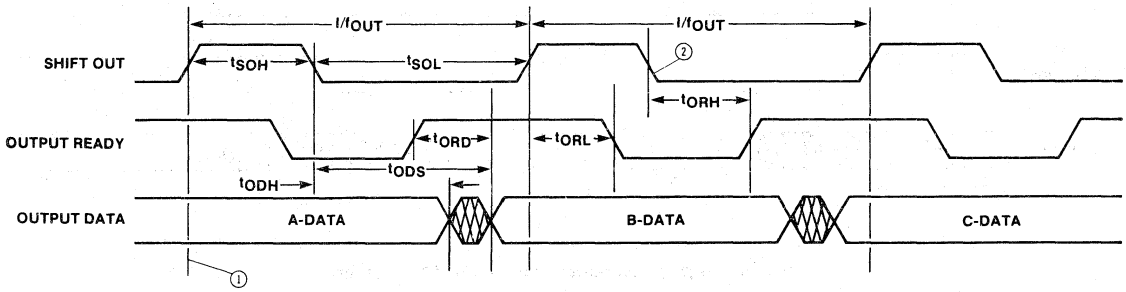


Figure 5. Output Timing

① The diagram assumes that at this time, words 63, 62 and 61 are loaded with A, B and C Data, respectively.

② Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e. OR and SO are both high together.

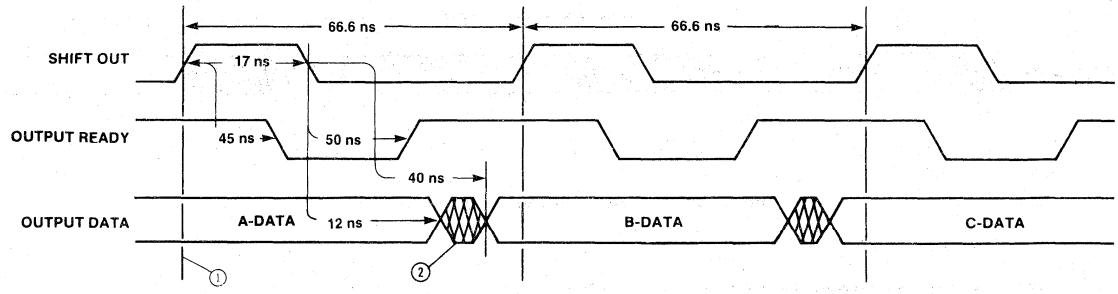


Figure 6. Waveforms for 15 MHz Shift-Out Data Rate

① The diagram assumes that at this time words 63, 62 and 61 are loaded with A, B and C Data, respectively.

② Data in the first crosshatched region may be A or B Data.

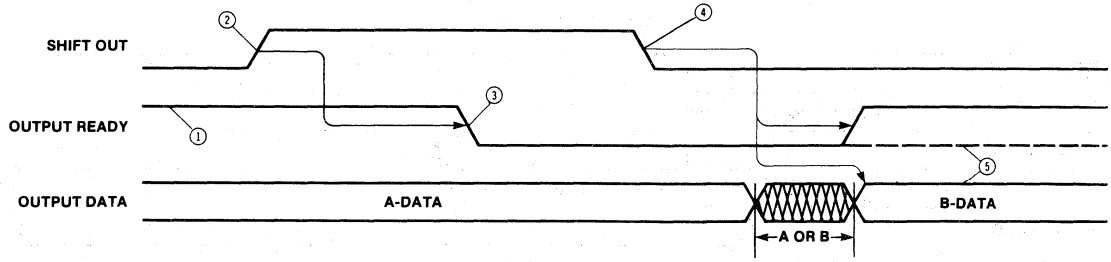


Figure 7. The Mechanism of Shifting Data Out of the FIFO

① Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.

② Shift-Out goes HIGH causing the contents of word 62 (B-Data) to be released for fall-through to word 63. Output data remains as valid A-Data while Shift-Out is HIGH.

③ Output Ready goes LOW.

④ Shift-Out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.

⑤ If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data becomes invalid.

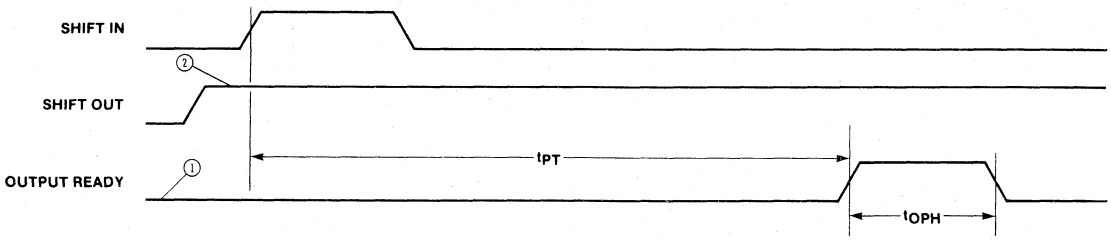


Figure 8. t_{PT} and t_{OPH} Specification

① FIFO initially empty.

② Shift Out held HIGH.

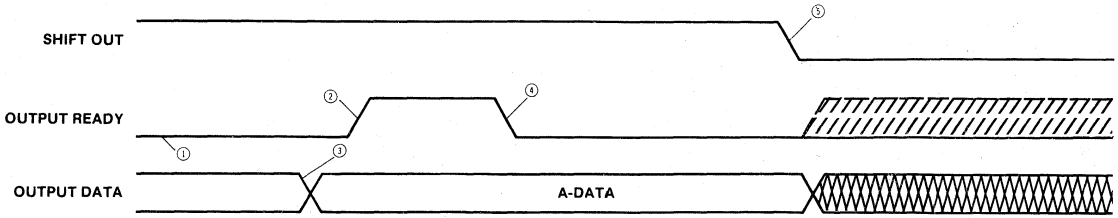


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH.

① Word 63 is empty.

② Output Ready goes HIGH indicating arrival of the new data.

③ New data (A) arrives at the outputs (word 63).

④ Since Shift Out is held HIGH, Output Ready goes immediately LOW.

⑤ As soon as Shift Out goes LOW the Output Data is subject to change. Output Ready will go HIGH or LOW depending on whether there are any additional upstream words in the FIFO.

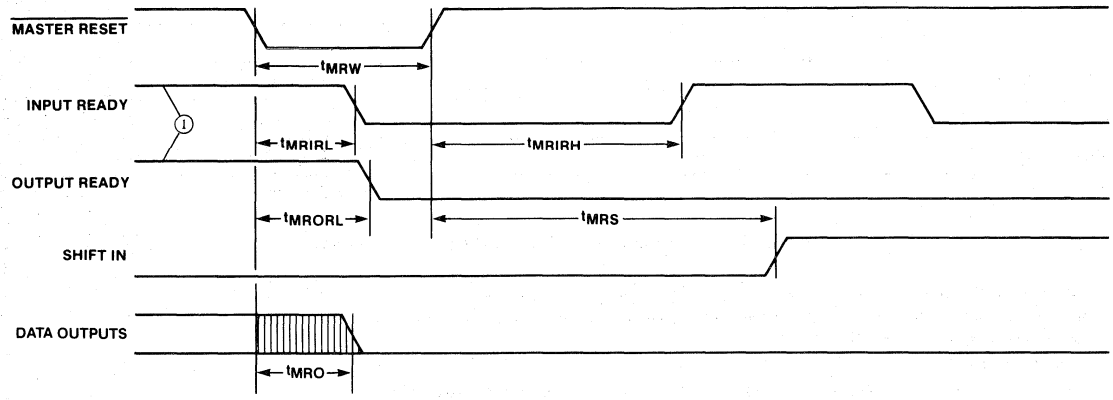


Figure 10. Master Reset Timing

① FIFO initially partially full.

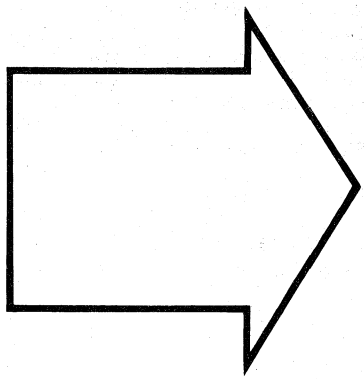


Table of Contents

MEMORY SUPPORT

8-Bit Dynamic-RAM Driver with Three-state Outputs

SN54/74S730/-1
SN54/74S734/-1

Features/Benefits

- **Provides MOS voltage levels for 16K and 64K DRAMs**
- **Undershoot of low-going output is less than -0.5 V**
- **Large capacitive drive capability**
- **Symmetric rise and fall times due to balanced output impedence**
- **Glitch-free outputs at power-up and power-down**
- **20-pin SKINNYDIP® saves space**
- **'S730/734 are exact replacement for the Am2965/66**
- **'S730/734 are pin-compatible with 'S240/244, and can replace them in many applications**
- **'S730-1/734-1 have a larger resistor in the output stage for better undershoot protection**
- **Commercial devices are specified at V_{CC} ± 10%**

Ordering Information

PART NUMBER	PKG	TEMP	ENABLE	POLARITY	POWER
SN54S730/-1	J,W,L	Mil	Low	Invert	S
SN74S730/-1	N,J,NL	Com			
SN54S734/-1	J,W,L	Mil	Low	Non-Invert	
SN74S734/-1	N,J,NL	Com			

Description

The 'S730 and 'S734 are buffers that can drive multiple address and control lines of MOS dynamic RAMs. The 'S730 is an inverting driver, and the 'S734 is a non-inverting driver. The 'S730 is pin-compatible with the 'S240 and an exact replacement for the Am2965. The 'S734 is pin-compatible with the 'S244 and an exact replacement for the Am2966.

These devices have been designed with an additional internal resistor in the lower output driver transistor circuit, unlike regular 8-bit buffers. This resistor serves two purposes: it causes a slower fall time for a high-to-low transition, and it limits the undershoot without the use of an external series resistor.

The 'S730 and 'S734 have been designed to drive the highly-capacitive input lines of dynamic RAMs. The drivers provide a guaranteed V_{OH} of V_{CC}-1.15 V, limit undershoot to 0.5 V, and exhibit a rise time symmetrical to their fall time by having balanced outputs. These features enhance dynamic RAM performance.

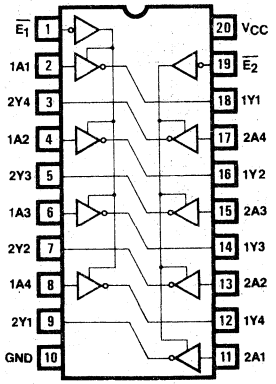
For a better-controlled undershoot for lightly capacitive-loaded circuits the 'S730-1 and 'S734-1 provide a larger resistor in the lower output stage. Also an improved undershoot voltage of -0.3 V is provided in the 'S730-1 and 'S734-1.

A typical fully-loaded-board dynamic-RAM array consists of four banks of dynamic-RAM memory. Each bank has its own $\overline{RAS}$ and $\overline{CAS}$, but has identical address lines. The $\overline{RAS}$ and $\overline{CAS}$ inputs to the array can come from one driver, reducing the skew between the $\overline{RAS}$ and $\overline{CAS}$ signals. Also, only one driver is needed to drive eight address lines of a dynamic RAM. The propagation delays are specified for 50 pF and 500 pF load capacitances, and the commercial-range specifications are extended to V_{CC} ±10%.

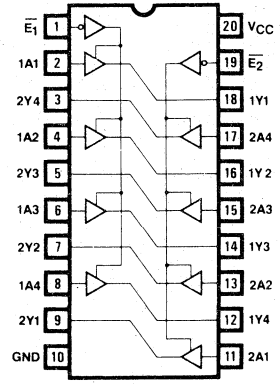
All of the drivers are available in 20-pin/DIP and 20-pin PLCC packages.

Logic Symbols

'S730 (Am2965)
'S730-1



'S734 (Am2966)
'S734-1



SKINNYDIP® is a registered trademarkof Monolithic Memories

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374
Monolithic Memories MMI

Function Tables

'S730/-1

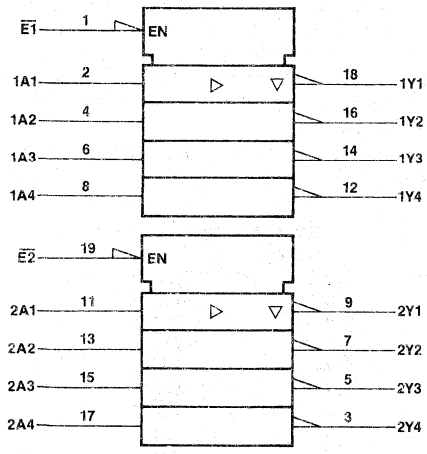
$\overline{E1}$	$\overline{E2}$	1A	2A	1Y	2Y
L	L	L	L	H	H
L	L	L	H	H	L
L	L	H	L	L	H
L	L	H	H	L	L
L	H	L	X	H	Z
L	H	H	X	L	Z
H	L	X	L	Z	H
H	L	X	H	Z	L
H	H	X	X	Z	Z

'S734/-1

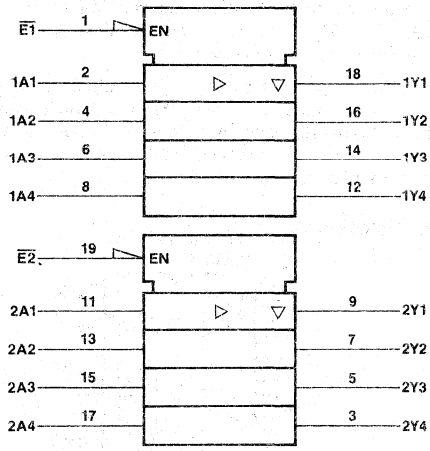
$\overline{E1}$	$\overline{E2}$	1A	2A	1Y	2Y
L	L	L	L	L	L
L	L	L	H	L	H
L	L	H	L	H	L
L	L	H	H	H	H
L	H	L	X	L	Z
L	H	H	X	H	Z
H	L	X	L	Z	L
H	L	X	H	Z	H
H	H	X	X	Z	Z

IEEE Symbol

'S730-1



'S734-1



Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to +V_{CC} max
Storage temperature range ..... -65°C to +150°C
Output current ..... 200 mA

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
T_A	Operating free-air temperature	-55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}*	Low-level input voltage						0.8			0.8	V
V_{IH}*	High-level input voltage				2			2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = -18 mA			-1.2			-1.2	V
I_{IL}	Low-level input current	Any A	V_{CC} = MAX	V_I = 0.4 V			-0.2			-0.2	mA
		Any E					-0.4			-0.4	
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7 V			20			20	μA
I_I	Maximum input current		V_{CC} = MAX	V_I = 7 V			0.1			0.1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V, V_{IH} = 2 V	I_{OL} = 1 mA			0.5			0.5	V
				I_{OL} = 12 mA			0.8			0.8	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V, V_{IH} = 2 V	I_{OH} = -1 mA	V_{CC} -1.15	V_{CC} -0.7		V_{CC} -1.15	V_{CC} -0.7		V
I_{OZL}	Off-state output current		V_{CC} = MAX, V_{IL} = 0.8 V, V_{IH} = 2 V	V_O = 0.4 V			-200			-200	μA
I_{OZH}				V_O = 2.7 V			100			100	μA
I_{OS}	Output short-circuit current †		V_{CC} = MAX		-60		-200	-60		-200	mA
I_{OL}	Output sink current		V_{OL} = 2.0 V	'S7XX	50			50			mA
				'S7XX-1	40			40			
I_{OH}	Output source current		V_{OH} = 2.0 V		-35			-35			mA
I_{CC}	Supply current	Outputs high	V_{CC} = MAX, Outputs open	'S730/-1		24	50		24	50	mA
				'S734/-1		53	75		53	75	
		Outputs low		'S730/-1		86	125		86	125	
				'S734/-1		92	130		92	130	
		Outputs disabled		'S730/-1		86	125		86	125	
				'S734/-1		116	150		116	150	

† Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

* These are absolute voltages with respect to pin 10 on the device and includes all overshoots due to system and/or test noise. Do not attempt to test these values without suitable equipment.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C For the 'S730 and 'S734

SYMBOL	PARAMETER	FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data to output delay	1 & 3	C_L = 50pf	6	9	15	ns
			C_L = 500pf	18	22	30	
t_{PHL}			C_L = 50pf	5	7	15	
			C_L = 500pf	18	22	30	
t_{PZL}	Output enable delay	2 & 4	S = 1		12	20	ns
t_{PZH}			S = 2		12	20	
t_{PLZ}	Output disable delay	2 & 4	S = 1		11	20	ns
t_{PHZ}			S = 2		6.5	12	
t_{SKEW}	Output-to-output skew	1 & 3	C_L = 50pf	*	±0.5	±3.0	ns
V_{ONP}	Output voltage undershoot	1 & 3	C_L = 50pf		0	−0.5	V

*The SKEW timing specification is guaranteed by design, but not tested.

Switching Characteristics Over Operating Range** For the 'S730 and 'S734

SYMBOL	PARAMETER	FIGURE	TEST CONDITIONS	MILITARY †† V_{CC} = 5.0V ±10%			COMMERCIAL V_{CC} = 5.0V ±10%			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Data to output delay	1 & 3	C_L = 50pf	4		20	4		17	ns
			C_L = 500pf	18		40	18		35	
t_{PHL}			C_L = 50pf	4		20	4		17	
			C_L = 500pf	18		40	18		35	
t_{PZL}	Output enable delay	2 & 4	S = 1†			28			28	ns
t_{PZH}			S = 2†			28			28	
t_{PLZ}	Output disable delay	2 & 4	S = 1†			24			24	ns
t_{PHZ}			S = 2†			16			16	
V_{ONP}	Output voltage undershoot	1 & 3	C_L = 50pf			−0.5			−0.5	V

**AC performance over the operating temperature is guaranteed by testing as defined in Group A, Subgroup 9, Mil Std 883B.

†"S = 1" and "S = 2" refer to the switch setting in Figure 2.

††T_C = -55 to + 125°C for flatpack versions.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C For the 'S730 and 'S734

SYMBOL	PARAMETER	FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data to output delay	1 & 3	C_L = 50pf	6	9	15	ns
			C_L = 500pf	18	22	30	
t_{PHL}			C_L = 50pf	5	7	15	
			C_L = 500pf	18	22	40	
t_{PZL}	Output enable delay	2 & 4	S = 1		12	20	ns
t_{PZH}			S = 2		12	20	
t_{PLZ}	Output disable delay	2 & 4	S = 1		11	20	ns
t_{PHZ}			S = 2		6.5	12	
t_{SKEW}	Output-to-output skew	1 & 3	C_L = 50pf	*	±0.5	±3.0	ns
V_{ONP}	Output voltage undershoot	1 & 3	C_L = 50pf		0	-0.3	V

*The SKEW timing specification is guaranteed by design, but not tested.

Switching Characteristics Over Operating Range** For the 'S730 and 'S734

SYMBOL	PARAMETER	FIGURE	TEST CONDITIONS	MILITARY †† V_{CC} = 5.0V ±10% MIN	TYP	MAX	COMMERCIAL V_{CC} = 5.0V ±10% MIN	TYP	MAX	UNIT
t_{PLH}	Data to output delay	1 & 3	C_L = 50pf	4		20	4		17	ns
			C_L = 500pf	18		40	18		35	
t_{PHL}			C_L = 50pf	4		20	4		17	
			C_L = 500pf	18		50	18		45	
t_{PZL}	Output enable delay	2 & 4	S = 1†			28			28	ns
t_{PZH}			S = 2†			28			28	
t_{PLZ}	Output disable delay	2 & 4	S = 1†			24			24	ns
t_{PHZ}			S = 2†			16			16	
V_{ONP}	Output voltage undershoot	1 & 3	C_L = 50pf			-0.3			-0.3	V

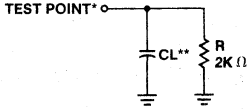
**AC performance over the operating temperature is guaranteed by testing as defined in Group A, Subgroup 9, Mil Std 883B.

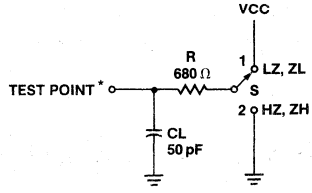
†"S = 1" and "S = 2" refer to the switch setting in Figure 2.

†† T_C = -55 to + 125° C for flatpack versions.

9

Test Loads





* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

** tpd specified at CL = 50 and 500pF

Figure 1. Capacitive Load Switching

Figure 2. Three-State Enable/Disable

Typical Switching Characteristics

VOLTAGE WAVEFORMS

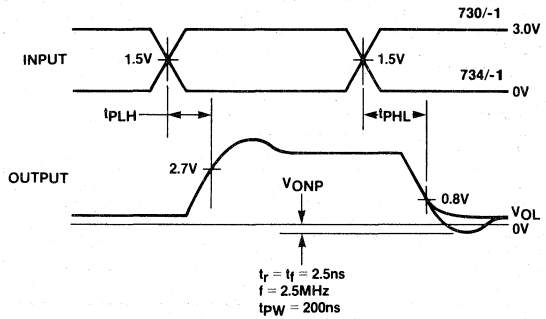


Figure 3. Output Voltage Levels

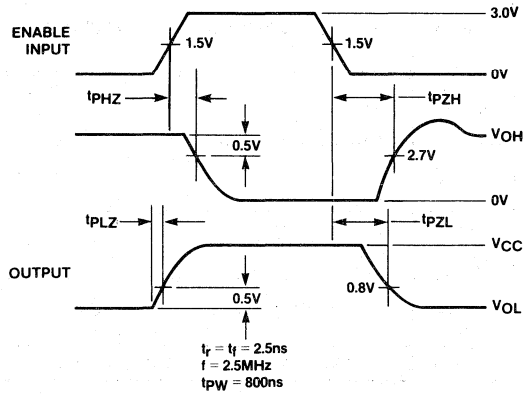
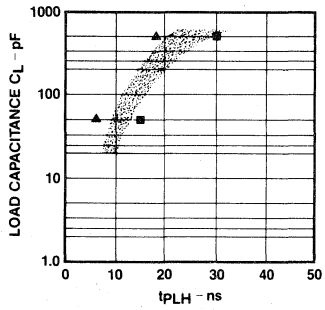
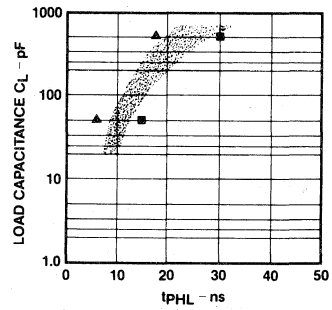


Figure 4. Three-State Control Levels

Typical Performance Characteristics:

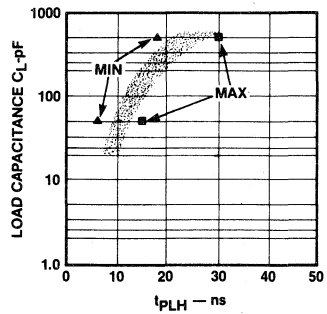


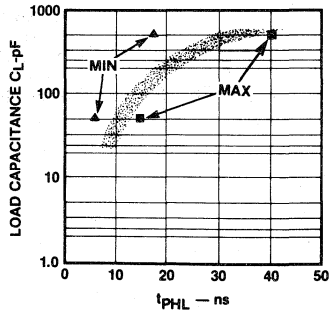


▲ INDICATE MINIMUM VALUES AT 25°C.
■ INDICATE MAXIMUM VALUE AT 25°C.

Figure 5a. t_{PLH} for V_{OH} = 2.7 V vs. C_L, for the 'S730 and 'S734

Figure 6a. t_{PHL} for V_{OL} = 0.8 V vs. C_L, for the 'S730 and 'S734





▲ INDICATE MINIMUM VALUES AT 25°C.
■ INDICATE MAXIMUM VALUE AT 25°C.

Figure 5b. t_{PLH} for V_{OH} = 2.7 V vs. C_L, for the 'S730-1 and 'S734-1

Figure 6b. t_{PHL} for V_{OL} = 0.8 V vs. C_L, for the 'S730-1 and 'S734-1

Applications

The 'S730 and 'S734 are 8-bit bipolar dynamic RAM drivers and are pin-compatible with the 'S240 and 'S244 respectively.

The actual circuit conditions that arise for driving dynamic RAM memories are as follows: Typically, in dynamic RAM arrays address lines and control lines, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ have a fair amount of "daisy chaining." The daisy chaining causes an inductive effect due to the traces in the printed circuit board; the dominant factor in the RAM loading is input capacitance, and these two conditions contribute to the actual driver conditions shown in Figure 7. The result is a transmission line with distributed inductance and capacitance connected to the driver outputs.

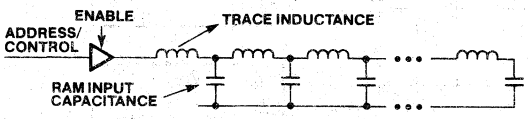


Figure 7. RAM Driver Output To Array

The transmission line effect can imply reflections, which in turn cause ringing, and it takes some time before the output settles from the low-to-high transition. On the high-to-low transition, along with ringing, a voltage undershoot can occur, and the circuit takes even longer to settle to an acceptable zero level. The main cause for the shorter high-to-low transition as compared to the low-to-high transition is the output impedance of typical Schottky drivers. Figure 8, shows a typical Schottky driver output stage and Figure 9 shows the output impedance for high and low output states.

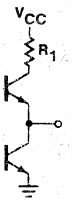


Figure 8. Typical Schottky Driver Output

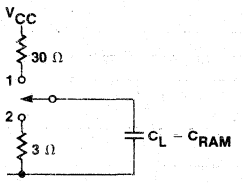


Figure 9. Driver Output Impedance

In Figure 9 when S=1, the output is high and the driver output impedance is approximately 30Ω. When S=2, the output is low and the driver output impedance is approximately 3Ω. There is a 10:1 ratio for the output impedances for the low and high states. The high-to-low transition causes a problem as the output transistor turns on fast due to the low impedance and undershoot results at the RAM inputs.

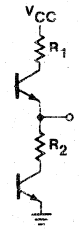


Figure 10. 'S730 and 'S734 Output Stage

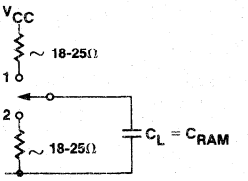


Figure 11. Driver Output Impedence For the 'S730 and 'S734

The 'S730 and 'S734 have a modification in their output stage, in that an internal resistor is added to the lower output stage as shown in Figure 10.

The 'S730-1 and 'S734-1 have a larger resistor, R2, comparted to the "non-dash" parts, which give better undershoot protection at a slightly slower switching performance.

The structure in Figure 10 provides a driver output impedence of approximately 18 Ω to 25 Ω in either high (S = 1) or low (S = 2) states as shown in Figure 11. In addition, this circuit limits undershoot to -0.5 V, essentially eliminating that problem; provides a symmetrical rise and fall time; and guarantees output levels of V_{CC}-1.15 V needed for MOS High levels. Also, when using the 'S730 asnd 'S734, no external resistors are needed. 'S240-series parts used with external resistors to provide drive capability, but the rise times and fall times are unsymmetrical due to higher impedance for low-to-high transitions.

Figure 12 shows the undershoot problem using a 'S240 without external resistors and the elimination of the problem by using the 'S730. Thus from a dynamic-RAM system-design viewpoint, the 'S730 and 'S734 are very effective RAM drivers.

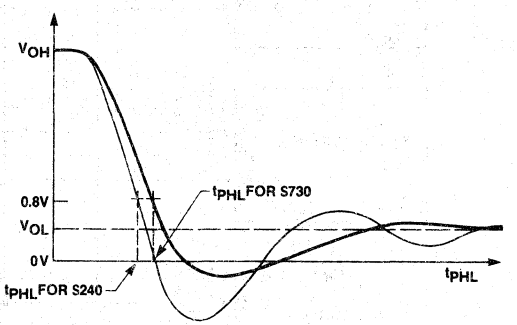


Figure 12. Comparison of Undershoots and t_{PHL}

An application using these 8-bit drivers to interface address and control lines (and data lines) to a dynamic RAM array using 64K DRAMs is discussed. The signals needed for the controls are $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$. The address lines are A0–A7 and the data lines are shown as the high and low byte. The array is shown in Figure 13. It consists of four rows of DRAMs; each row has individual $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ lines. However, all four rows have common address lines A0–A7. The RAM capacitive loading for $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ is about 10 pf per input. The loading of the address lines is about 5 to 7 pf per input. The loading of the $\overline{RAS}_i$, $\overline{CAS}_i$ and $\overline{WE}_i$ inputs to each row of memories is 160 pf. Note that $\overline{RAS}_i$ and $\overline{CAS}_i$ come from the same driver, which reduces timings skews which might arise if they were output from separate drivers. The address lines are outputs from another driver, and the loading on each line is 320 pf (5 pf loading times 64 DRAMs). At this point it is worth noting that if a 320-pf loading affects performance unduly, then the address lines can be split between two drivers with each having a load of 160 pf, reducing overall signal delay.

If an error-detection-and-correction scheme is used, then typically the row size expands to 22 bits from the 16 bits shown in the example. The 'S730 and 'S734 drivers lend themselves to such expansion, as their propagation delays are specified at 50 pF and also at 500 pF.

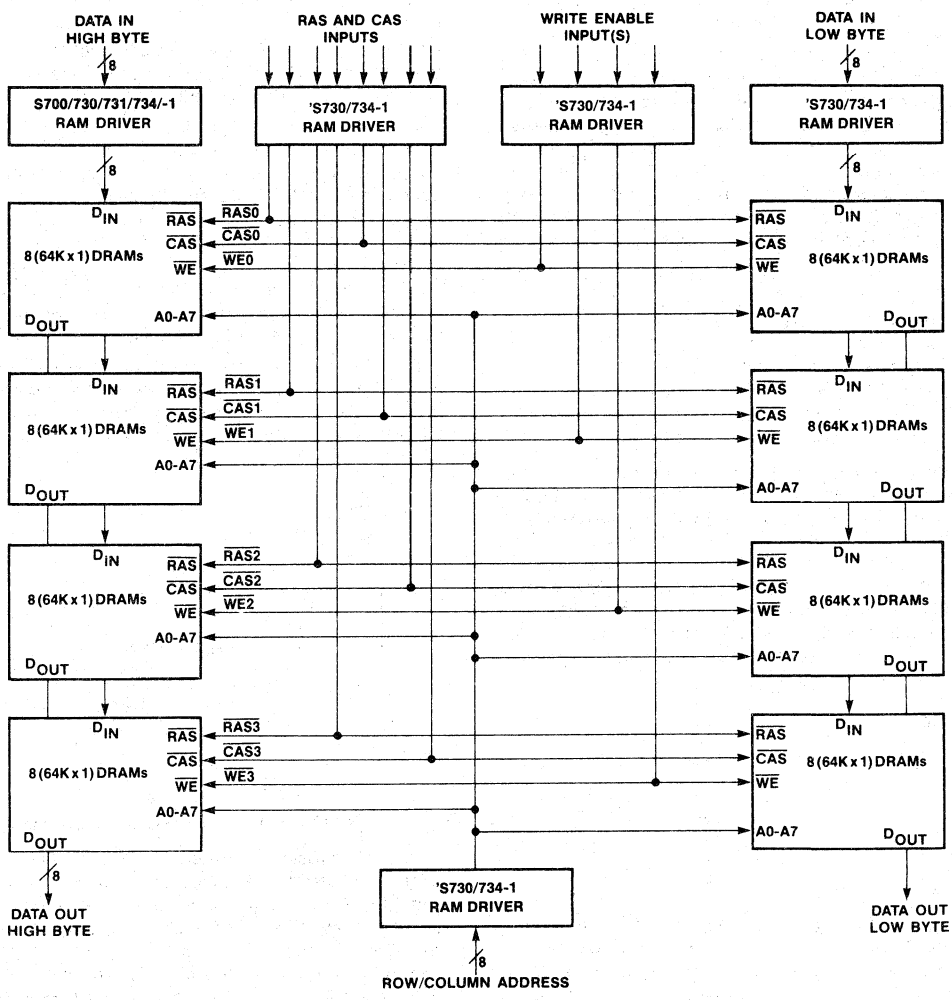


Figure 13. 256K X 16 Dynamic RAM Array with RAM Drivers

256K Dynamic RAM Controller/Driver

673102
673102A

Features/Benefits

- Supports 16K, 64K, and 256K DRAMs
- Capable of addressing up to 2 M 16-bit words or 2 M bytes
- On-chip capacitive-load drivers are capable of driving up to 88 DRAMs with 30-nsec typical address propagation delay and 128 DRAMs with 35-nsec typical address propagation delay
- $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ delay of 20 nsec max ($\overline{\text{RAS}}$ driving 22 DRAMs)
- Max and Min skews are specified to simplify system design
- Two $\overline{\text{CASIN}}$ inputs and two $\overline{\text{CAS}}$ outputs simplify byte addressing
- An Auto-Access mode with extended $\overline{\text{CAS}}$ capability takes advantage of full performance of 120 and 150 nsec DRAMs
- An output series resistor reduces undershoot

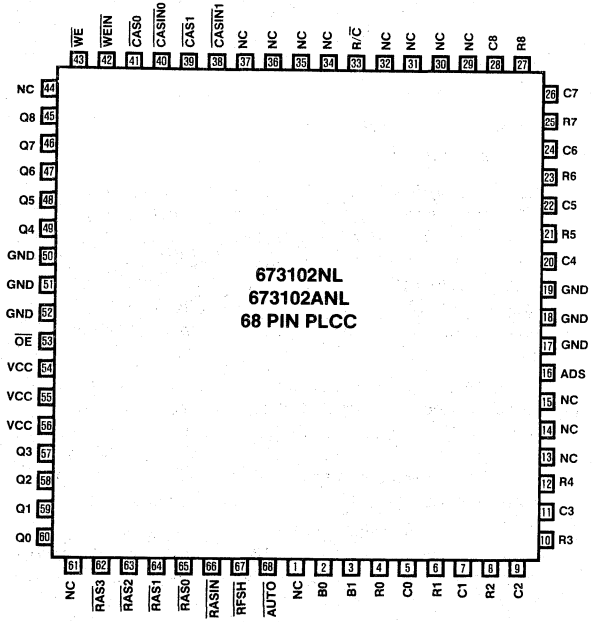
Modes of Operation

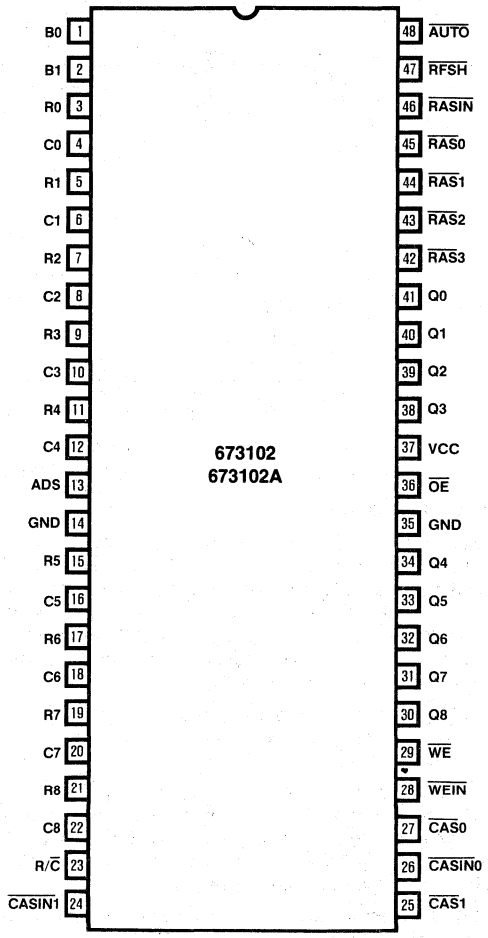
- Externally Controlled Access (ECA)
- Auto Access (AA)
- Refresh

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
673102	48D, 48N, 68NL, 68NP	Com
673102A		

Pin Configurations





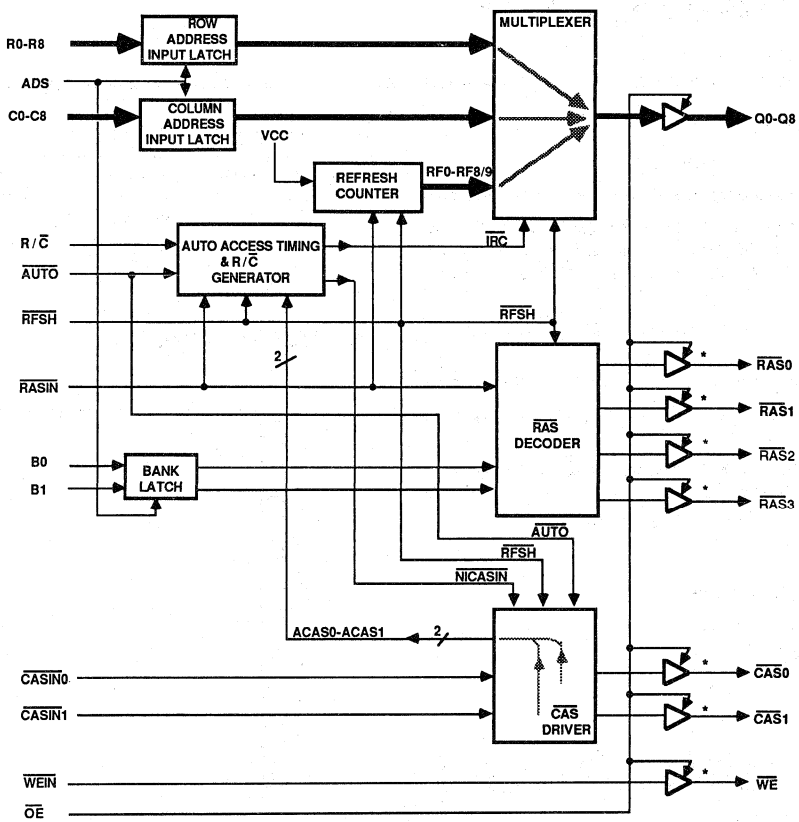
9

PAL® is a registered trademark of Monolithic Memories.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Monolithic Memories MMI

Block Diagram



* Indicates that there is a 3-KΩ pull-up resistor on these outputs when they are disabled

Figure 1. 673102 Functional Block Diagram

Description

The 673102 is a 48-pin LSI device which performs most of the functions needed to control and address Dynamic RAMs. Twenty address inputs, nine address outputs, four $\overline{RAS}$ outputs, and two $\overline{CASIN}$-$\overline{CAS}$ input-output pairs allow the 673102 to directly address 2 M 16-bit words or bytes. The two $\overline{CASIN}$n inputs and the two $\overline{CAS}$n outputs simplify individual byte access in 16-bit wide memory arrays (see Figure 2).

The 673102 has three operating modes:

- Externally Controlled Access (ECA)
- Auto Access (AA)
- Refresh (RFSH).

The Externally-Controlled-Access mode gives the system direct control over the $\overline{RAS}$m outputs, the $\overline{CAS}$n outputs, and Row/Column multiplexing. It also supports PAGE mode access, NIBBLE mode access, and static column mode access.

The Auto-Access mode provides on-chip delays that automatically control the timing delays between $\overline{RAS}$m signals, address multiplexing, and $\overline{CAS}$n signals. In the Auto-Access mode $\overline{CASIN}$0-1 inputs serve as enables for the respective $\overline{CAS}$0-1 outputs, allowing the access of either or both bytes of the memory array (for 16-bit wide memory arrays organized in two bytes). In this mode $\overline{CAS}$0-1 outputs go HIGH only when the respective $\overline{CASIN}$0-1 inputs go HIGH, and the address switches back to row address only when both $\overline{CASIN}$0 and $\overline{CASIN}$1 go HIGH. This feature allows extension of the $\overline{CAS}$0 or $\overline{CAS}$1 LOW time and column address time while $\overline{RASIN}$ and $\overline{RAS}$m can go HIGH to satisfy the precharge requirements of the dynamic RAMs.

When the Refresh mode is selected ($\overline{RFSH}$ is LOW) an on-chip refresh counter provides the refresh address; with $\overline{AUTO}$ HIGH and R/$\overline{C}$ LOW the column address is forced onto the address output multiplexer, facilitating an access of a particular memory location while refreshing a row. This feature may be useful when implementing error detection and correction scrubbing.

The 673102 can drive eight banks of DRAMs. $\overline{RAS}$m control signals are used to select a pair of banks, while leaving the other three pairs of banks in standby. The two $\overline{CAS}$n outputs enable the selection of one bank out of the pair. The address lines and the $\overline{WE}$ signal can be connected to all eight banks. In a 16-bit wide, byte-oriented, memory array the $\overline{RAS}$m signals select one out of four banks while the CASn signals select the bytes as shown in Figure 2.

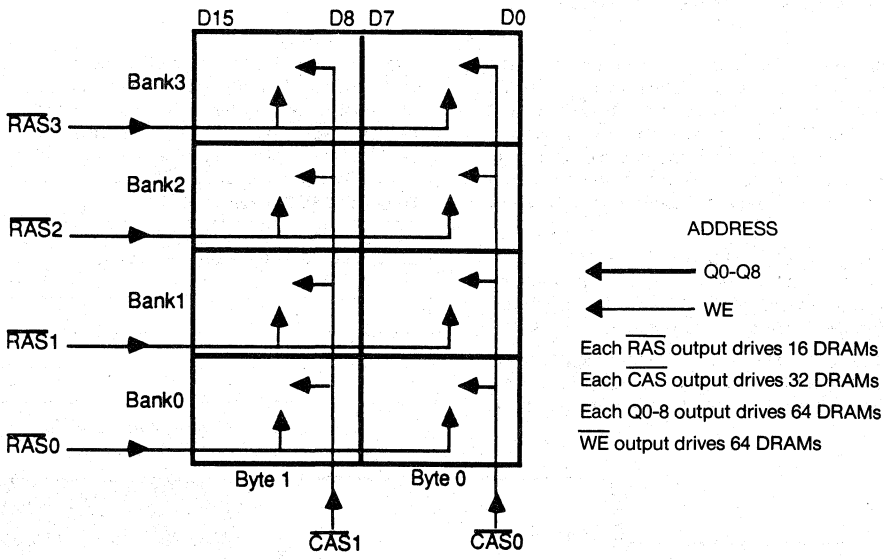


Figure 2. 673102 Addressing Four Banks of 16-bit Memory Array Organized in Two Bytes

9

Pin Definitions

VCC, GND: VCC-GND = 5 V ±10%. The supply pins have been assigned to the center of the package to reduce voltage drops, both DC and AC. A low-inductance connection between the ground pin and a solid ground plane will minimize fluctuations in the ground level of the device that may occur when the address outputs switch from HIGH to LOW simultaneously. A 1 μF multilayer ceramic capacitor in parallel with a low-voltage tantalum capacitor, both connected close to the VCC and GND pins, will properly decouple the device.

R0-R8: Row Address Inputs

C0-C8: Column Address Inputs

B0-B1: Bank-Pair Select Inputs — Strobed by ADS. Decoded to enable one of the $\overline{RAS}$ outputs when $\overline{RASIN}$ goes LOW in the access modes.

Q0-Q8: Multiplexed Address Outputs — Selected from the row address input latch, the column address input latch, or the refresh counter.

$\overline{RASIN}$: Row Address Strobe Input — Drives the selected $\overline{RAS}$m output in the access modes and all $\overline{RAS}$ outputs in the Refresh mode.

ADS: Address (Latch) Strobe Input — Strobes input row address, column address and Bank Select inputs into the respective latches when HIGH; latches on HIGH-to-LOW transition.

$\overline{OE}$: Output Enable — When $\overline{OE}$ is LOW the address and control outputs are enabled. When $\overline{OE}$ is HIGH the address outputs are in high-impedance and the control outputs are pulled HIGH.

R/$\overline{C}$: Row/Column Select Input — In the Externally-Controlled-Access mode it is used to select either the row address input latch or the column address input latch onto the address outputs. In the Refresh mode, when $\overline{AUTO}$ is HIGH, it is used to select between the refresh address (R/$\overline{C}$ HIGH) and the column address (R/$\overline{C}$ LOW). When $\overline{AUTO}$ is LOW R/$\overline{C}$ is disabled.

$\overline{CASIN}$0-1: Column Address Strobe Inputs — In the Externally-Controlled-Access mode the $\overline{CASIN}$n directly drives $\overline{CAS}$n output. In the Auto-Access mode each is used to enable the corresponding $\overline{CAS}$n output (See $\overline{CAS}$0-1 description).

$\overline{WEIN}$: Write Enable Input.

$\overline{WE}$: Write Enable Output.

$\overline{CAS}$0-1: Column Address Strobe Outputs — In the Externally-Controlled-Access mode the $\overline{CAS}$ outputs follow the $\overline{CASIN}$ inputs. In the Auto-Access mode the $\overline{CASIN}$ inputs are used to enable the $\overline{CAS}$ outputs. The $\overline{CAS}$ outputs are asserted LOW, with proper delay from the $\overline{RAS}$ output, by the $\overline{RASIN}$ signal via the Auto-Access timing generator. In the Auto-Access mode, the $\overline{CAS}$n goes HIGH only when the corresponding $\overline{CASIN}$n goes HIGH. Extending the $\overline{CAS}$n LOW duration while $\overline{RASIN}$ and $\overline{RAS}$m go HIGH satisfies the precharge requirement of the dynamic RAMs.

$\overline{RAS}$0-3: Row Address Strobe Outputs — When $\overline{RFSH}$ is HIGH the selected row address strobe output (decoded from signals B0, B1) follows the $\overline{RASIN}$ input. When $\overline{RFSH}$ is LOW all $\overline{RAS}$ outputs go LOW together following $\overline{RASIN}$ going LOW.

$\overline{AUTO}$: Auto-Access Input — When $\overline{AUTO}$ is LOW and $\overline{RFSH}$ is HIGH the Auto-Access mode is selected (see Auto-Access mode description).

$\overline{RFSH}$: Refresh Input — When $\overline{RFSH}$ is LOW the Refresh mode is selected (see Refresh mode description).

Externally-Controlled-Access Mode (ECA)

In this mode, selected when $\overline{AUTO}$ and $\overline{RFSH}$ are held HIGH, the 673102 serves as a straightforward multiplexer and driver for the address and control signals to the DRAMs. The $\overline{RAS}$m output selected by the B0 and B1 inputs follows the $\overline{RASIN}$ input, and each of the $\overline{CAS}$ outputs follows its corresponding $\overline{CASIN}$ input. When R/$\overline{C}$ is HIGH the row address is enabled onto the Q0-8 outputs. When R/$\overline{C}$ is LOW the column address latch is enabled onto Q0-8 outputs.

The $\overline{RASIN}$ — $\overline{RAS}$, $\overline{CASIN}$ — $\overline{CAS}$, and R/$\overline{C}$ — Q0-8 control paths are independent to allow the system designer maximum flexibility and support of special DRAM access and refresh modes such as NIBBLE mode, PAGE mode, $\overline{CAS}$ before $\overline{RAS}$, etc.

To allow tighter timing of the sequence of control signals to the Dynamic RAM, several difference timing parameters have been specified for the Externally Controlled Access mode. These parameters specify the maximum difference between the various "control channels" of the device. In particular, using switching characteristics t_{d7} and t_{d8} is very useful when designing the delay from $\overline{RASIN}$ going LOW to R/$\overline{C}$ and the delay between R/$\overline{C}$ going LOW to $\overline{CASIN}$ going LOW (see Applications).

BANK SELECT (STROBED BY ADS)		ENABLED $\overline{RAS}$n
B1	B0	
0	0	$\overline{RAS}$0
0	1	$\overline{RAS}$1
1	0	$\overline{RAS}$2
1	1	$\overline{RAS}$3

Table 1. Memory Bank Decode

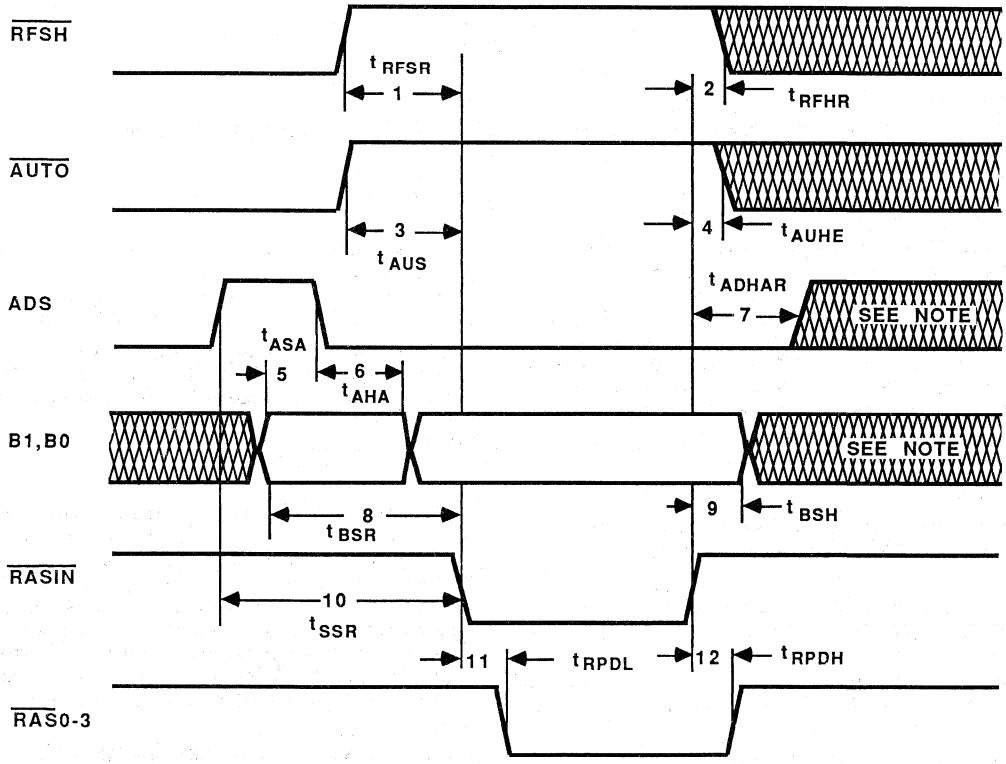


Figure 3. Externally-Controlled-Access—$\overline{RASIN}$-to-$\overline{RAS}$ Timing

Note: To prevent glitches on the $\overline{RAS}$0-3 outputs, operating conditions t_{BSH} or t_{ADHAR} must be satisfied.

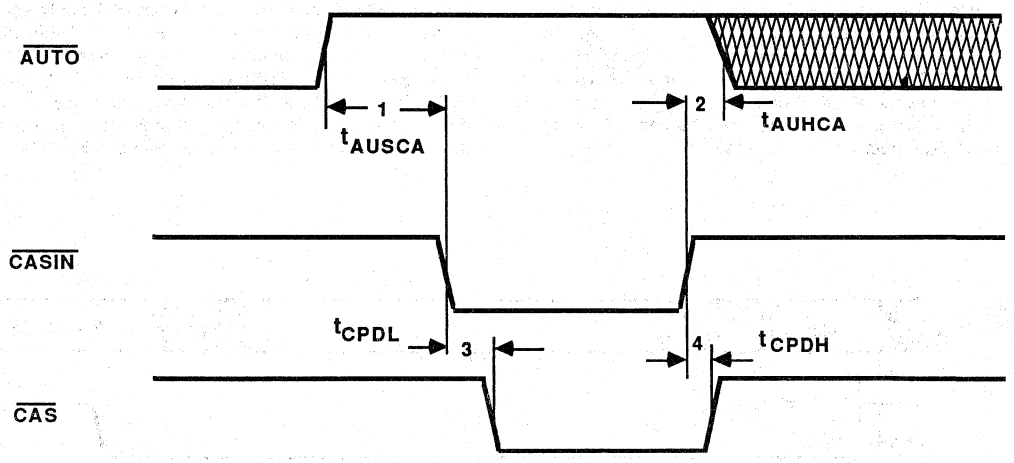


Figure 4. Externally-Controlled-Access-$\overline{\text{CASIN}}$ to $\overline{\text{CAS}}$ Timing

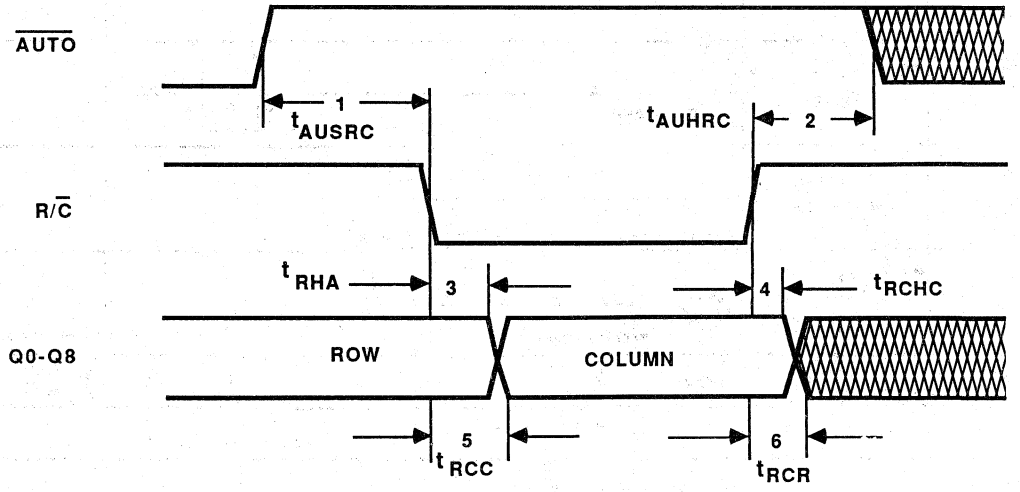


Figure 5. Externally-Controlled-Access R/$\overline{\text{C}}$ Timing

Note: t_{RCC} will be met only if the column address is available t_{APD} before it appears on Q0-8 outputs or if it is latched by ADS.

Auto-Access Mode (AA)

In the Auto-Access mode the 673102 provides the system designer with built-in delays and sequencing to accommodate DRAMs with 150 nanoseconds and faster access time. The Auto-Access mode is selected when $\overline{AUTO}$ is held LOW and $\overline{RFSH}$ is held HIGH. The R/$\overline{C}$ input is disabled, and $\overline{RASIN}$ going LOW initiates the sequence of control signals to access the DRAMs. The $\overline{CASIN}$0-1 inputs are used as enables for the respective $\overline{CAS}$ outputs. A LOW on a $\overline{CASIN}$n input enables the $\overline{CAS}$n output to be driven LOW with the internally generated delay from $\overline{RAS}$. Each $\overline{CAS}$n output goes HIGH only when the corresponding $\overline{CASIN}$n input goes HIGH, and the address switches back to row address only when both $\overline{CASIN}$0 and $\overline{CASIN}$1 go HIGH. This feature allows extension of the $\overline{CAS}$0 or $\overline{CAS}$1 LOW time and the column address time, while $\overline{RASIN}$ and $\overline{RAS}$m can go HIGH to satisfy precharge requirements of the dynamic RAMs. The R/$\overline{C}$ input is disabled in this mode.

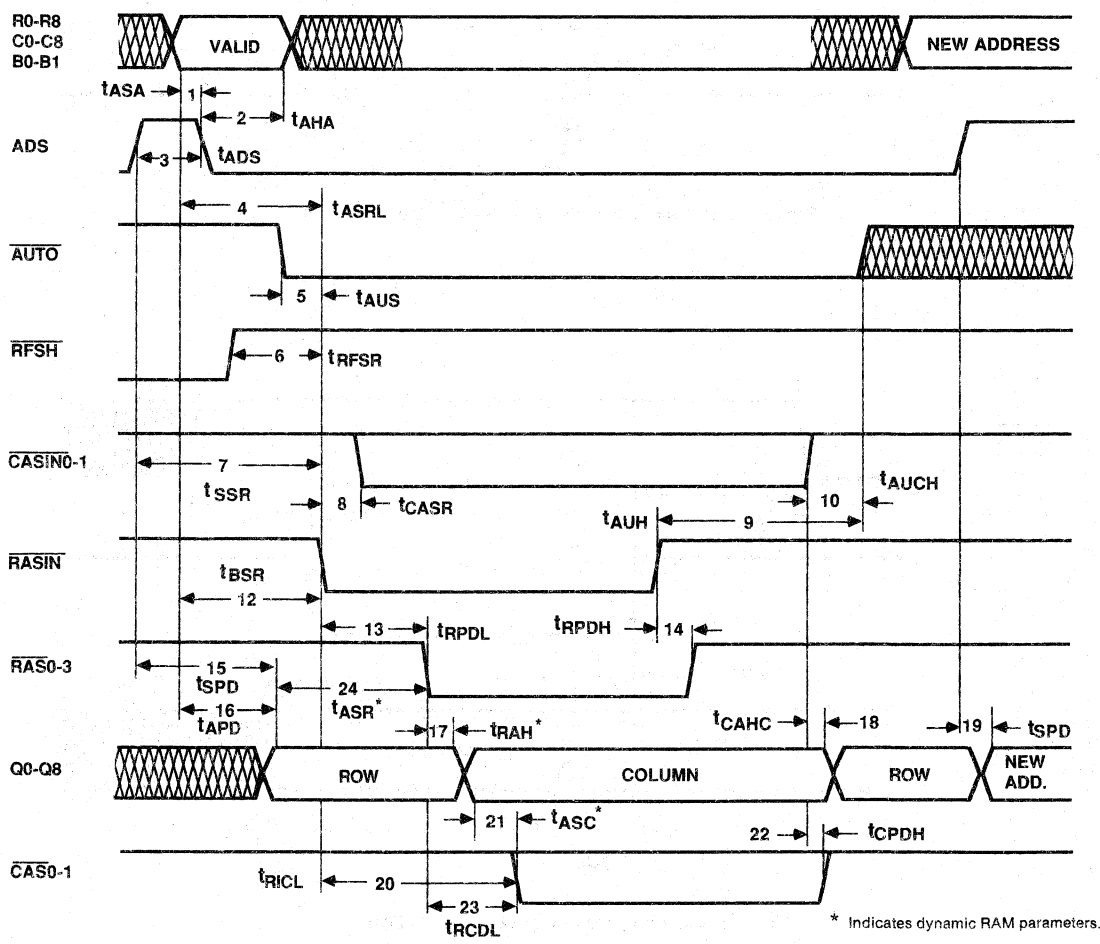


Figure 6. Auto-Access (AA) Timing

Refresh Mode (RFSH)

When $\overline{RFSH}$ is held LOW the refresh counter contents are enabled onto the Q0-8 address outputs, provided either R/$\overline{C}$ is held HIGH, or $\overline{AUTO}$ is held LOW, or both conditions exist. In this mode all four $\overline{RAS}$ outputs follow the $\overline{RASIN}$ input signal. The refresh counter increments the refresh address when either $\overline{RASIN}$ or $\overline{RFSH}$ goes HIGH while the other is LOW. When $\overline{AUTO}$ is LOW the $\overline{CASIN}$0-1 inputs are isolated and $\overline{CAS}$0-1 are held HIGH. Also, when $\overline{AUTO}$ is LOW the R/$\overline{C}$ input is isolated from the output multiplexer, and the refresh address appears at the Q0-8 outputs.

When $\overline{AUTO}$ is HIGH, pulling R/$\overline{C}$ LOW enables the column address onto the Q0-8 outputs. Also, each of the $\overline{CAS}$ outputs follows its corresponding $\overline{CASIN}$ input. This feature may be used when implementing error correction and detection "scrubbing" for two-bank memory array. "Scrubbing" is a term describing the cyclic error correction of soft errors in the memory array, done within the refresh cycles. On every refresh cycle one location of the memory array is accessed, and the data in that location goes, if necessary, through a correction cycle (a read-modify-write memory cycle). The 673102 provides the facilities to force a column address onto the Q0-8 address outputs and to assert the $\overline{CAS}$0-1 outputs within a refresh cycle to allow scrubbing. A column counter and a bank counter must be added externally to provide the column addresses for scrubbing.

The refresh counter is a 9-bit counter that resets to 0 on power-up and rolls over to 0 at 511.

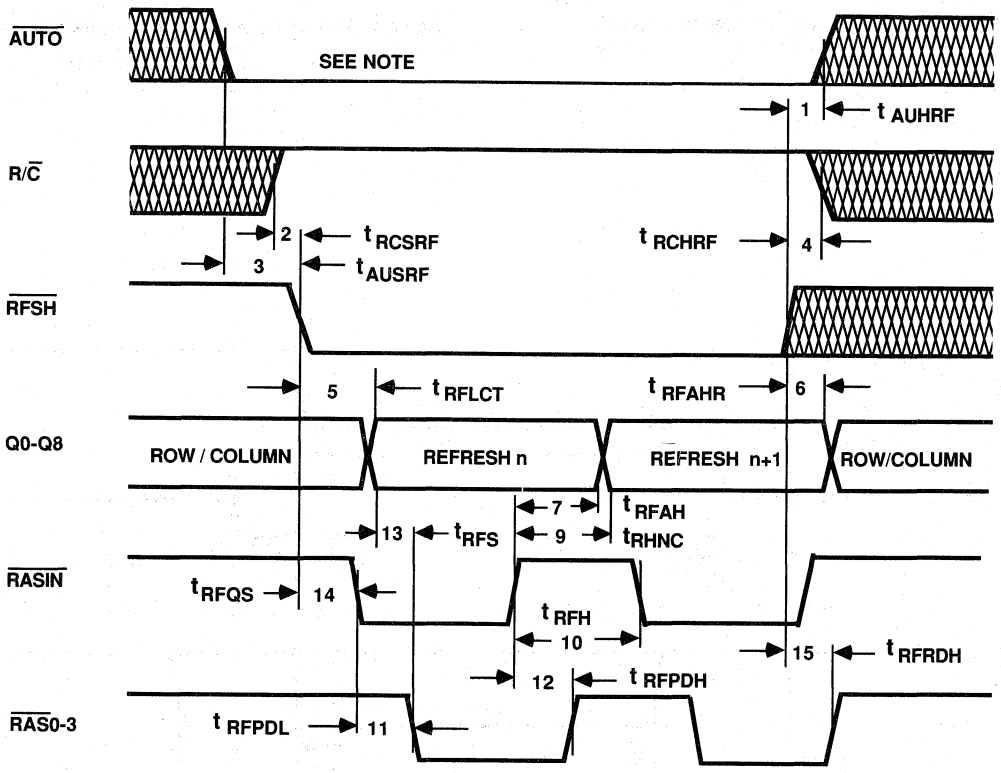


Figure 7. Refresh Timing

Note: In the REFRESH mode, $\overline{AUTO}$ must be LOW or R/$\overline{C}$ must be HIGH to guarantee the refresh address on the Q0-8 outputs.

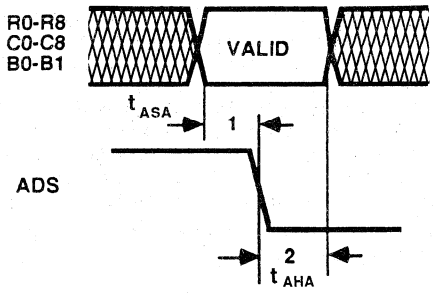


Figure 8. Address Setup and Hold Time to ADS

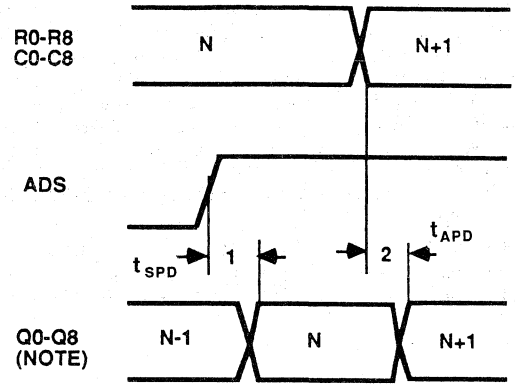


Figure 9. Address Input/Output Propagation Delay

Note: Row or Column address ($\overline{RFSH}$ = HIGH).

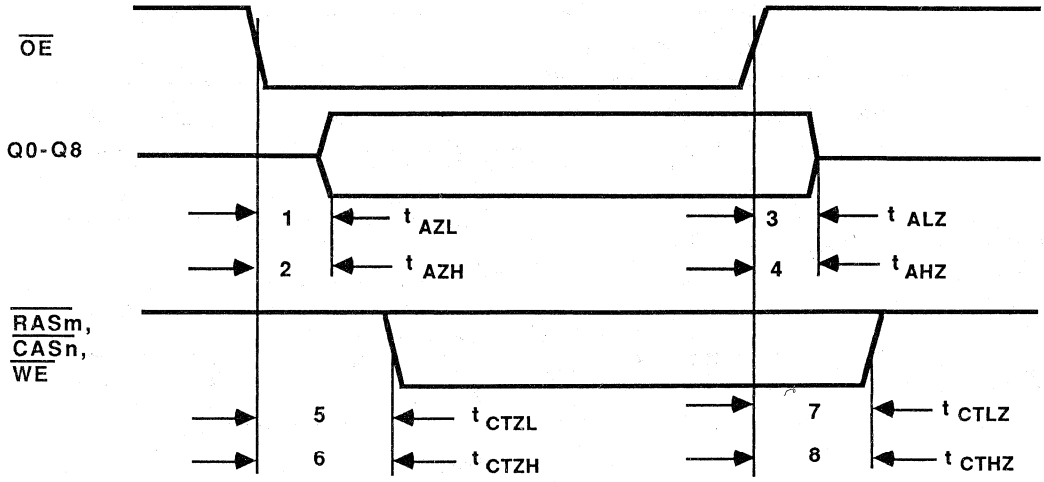


Figure 10. High-Z Timing

Electrical Characteristics V_{CC} = 5 V ±10%, 0°C ≤ T_A ≤ 75°C. Typicals are for V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	FIGURE/ NUMBER	MIN	TYP	MAX	UNIT
V_{IC}	Input clamp voltage	I_{IN} = −18 mA, V_{CC} = MIN			−0.8	−1.2	V
I_{IH}	Input high current	V_{IN} = 2.7 V, V_{CC} = MAX				50	μA
I_{CTL}	Output load current for $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	V_{OUT} = 0.4 V, V_{CC} = MAX Chip deselect			−1.5	−2.5	mA
I_{IL}	Input low current except for $\overline{RFSH}$	V_{IN} = 0.4 V, V_{CC} = MAX			−20	−250	μA
I_{ILRF}	Input low current for $\overline{RFSH}$	V_{IN} = 0.4 V, V_{CC} = MAX			−80	−500	μA
V_{IL}	Input low threshold (Note 1)					0.8	V
V_{IH}	Input high threshold (Note 1)			2.0			V
V_{OL1}	Output low voltage	I_{OUT} = 1 mA, V_{CC} = MIN				0.5	V
V_{OL2}	Output low voltage	I_{OUT} = 12 mA, V_{CC} = MIN				0.8	V
V_{OH}	Output high voltage	I_{OUT} = −1 mA, V_{CC} = MIN		2.4	3.0		V
I_{OH}	Output source current (Note 2)	V_{OUT} = 0.8 V, V_{CC} = MIN		−50	−140		mA
I_{OL}	Output sink current (Note 2)	V_{OUT} = 2.4 V, V_{CC} = MIN		40	100		mA
I_{OZ}	Three-state output current (address output)	0.4 V ≤ V_{OUT} ≤ 2.7 V V_{CC} = MAX, Chip deselect		−50		50	μA
I_{CC}	Supply current	V_{CC} = MAX			150	240	mA
C_{IN}	Input capacitance	T_A = 25°C			10		pF

9

Switching Characteristics (See Note 3)

SYMBOL	EXTERNALLY CONTROLLED ACCESS PARAMETER	FIGURE/ NUMBER	673102A MIN	673102A TYP	673102A MAX	673102 MIN	673102 TYP	673102 MAX	UNIT
t_{RHA}	Row addresses remaining valid from R/$\overline{C}$ LOW	5/3	0			0			ns
t_{RPDL}	$\overline{RASIN}$ to $\overline{RAS}$ LOW delay	3/11			20			20	ns
t_{RPDH}	$\overline{RASIN}$ to $\overline{RAS}$ HIGH delay	3/12			31			31	ns
t_{APD}	Address input to output delay	9/2			50			50	ns
t_{WPDL}	$\overline{WEIN}$ to $\overline{WE}$ LOW delay				45			45	ns
t_{WPDH}	$\overline{WEIN}$ to $\overline{WE}$ HIGH delay				40			40	ns
t_{CPDL}	$\overline{CASIN}$ to $\overline{CAS}$ LOW delay	4/3			28			28	ns
t_{CPDH}	$\overline{CASIN}$ to $\overline{CAS}$ HIGH delay	4/4			40			40	ns
t_{RCC}	Column select to column address valid	5/5			41			41	ns
t_{RCR}	Row select to row address valid	5/6			45			45	ns
t_{d1}	($\overline{CASIN}$ to $\overline{CAS}$ LOW delay)-($\overline{RASIN}$ to $\overline{RAS}$ LOW delay)		−2		13	−2		13	ns
t_{d2}	(Address input to output delay)-($\overline{RASIN}$ to $\overline{RAS}$ LOW delay)				30			30	ns
t_{d3}	(Address input to output delay)-($\overline{CASIN}$ to $\overline{CAS}$ LOW delay)		−5		23	−5		23	ns
t_{d4}	Skew between address output lines				10			10	ns
t_{d5}	($\overline{RASIN}$ to $\overline{RAS}$ HIGH delay)-($\overline{RASIN}$ to $\overline{RAS}$ LOW delay)		−7		13	−7		13	ns
t_{d6}	($\overline{CASIN}$ to $\overline{CAS}$ HIGH delay)-($\overline{CASIN}$ to $\overline{CAS}$ LOW delay)		−12		12	−12		12	ns
t_{SPD}	ADS HIGH to address output valid	9/1			55			55	ns
t_{RCHC}	Column addresses remaining valid from R/$\overline{C}$ HIGH	5/4	0			0			ns
t_{d7}	t_{RPDL} - t_{RHA}				13			13	ns
t_{d8}	t_{RCC} - t_{CPDL}				20			20	ns

Switching Characteristics (Continued)

SYMBOL	AUTO ACCESS PARAMETER	FIGURE/ NUMBER	673102A MIN	673102A TYP	673102A MAX	673102 MIN	673102 TYP	673102 MAX	UNIT
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ LOW delay	6/20			75			85	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ LOW delay	6/23	30		65	30		75	ns
t_{RPDL}	$\overline{RASIN}$ to $\overline{RAS}$ LOW delay	6/13			20			20	ns
t_{RPDH}	$\overline{RASIN}$ to $\overline{RAS}$ HIGH delay	6/14			31			31	ns
t_{APD}	Address input to output delay	6/16			50			50	ns
t_{WPDL}	$\overline{WEIN}$ to $\overline{WE}$ LOW delay				45			45	ns
t_{WPDH}	$\overline{WEIN}$ to $\overline{WE}$ HIGH delay				40			40	ns
t_{CPDH}	$\overline{CASIN}$ to $\overline{CAS}$ HIGH delay	6/22			40			40	ns
t_{RAH}	Row address hold time from $\overline{RAS}$ LOW	6/17	15			15			ns
t_{d2}	(Address input to output delay)-($\overline{RASIN}$ to $\overline{RAS}$ LOW delay)				30			30	ns
t_{SPD}	ADS HIGH to address output valid	6/19			55			55	ns
t_{ASC}	Column address setup to $\overline{CAS}$ LOW	6/21	0			0			ns
t_{CAHC}	Column address remaining valid from $\overline{CASIN0}$-1 HIGH	6/18	5			5			ns
t_{ASR}	Row address valid before $\overline{RAS}$ LOW	6/24	0			0			ns
t_{d5}	($\overline{RASIN}$ to $\overline{RAS}$ HIGH delay)-($\overline{RASIN}$ to $\overline{RAS}$ LOW delay)		-7		13	-7		13	ns
	REFRESH PARAMETER								
t_{RFLCT}	$\overline{RFSH}$ LOW to refresh address valid ($\overline{AUTO}$ LOW or R/$\overline{C}$ HIGH)	7/5			40			40	ns
t_{RFPDL}	$\overline{RASIN}$ LOW to $\overline{RAS}$ LOW delay during refresh	7/11			23			23	ns
t_{RFPDH}	$\overline{RASIN}$ HIGH to $\overline{RAS}$ HIGH delay during refresh	7/12			38			38	ns
t_{RFAH}	Refresh address held from $\overline{RASIN}$ HIGH ($\overline{RFSH}$ LOW)	7/7	0			0			ns
t_{RHNC}	$\overline{RASIN}$ HIGH to new refresh address valid	7/9			66			66	ns
t_{RFAHR}	Refresh address held from $\overline{RFSH}$ HIGH	7/6	0			0			ns
t_{RFS}	Refresh address valid to $\overline{RAS}$ LOW (provided t_{RFQS} is satisfied)	7/13	0			0			ns
t_{RFRDH}	$\overline{RFSH}$ HIGH to $\overline{RAS}$ HIGH (for 3 banks, $\overline{RASIN}$ = LOW)	7/15			40			40	ns
t_{d9}	($\overline{RASIN}$ to $\overline{RAS}$ HIGH delay)-($\overline{RASIN}$ to $\overline{RAS}$ LOW delay)		-9		16	-9		16	ns
	THREE-STATE PARAMETER								
t_{AZL}	$\overline{OE}$ LOW to address output LOW	10/1			45			45	ns
t_{AZH}	$\overline{OE}$ LOW to address output HIGH	10/2			60			60	ns
t_{ALZ}	$\overline{OE}$ HIGH to address output HI-Z from LOW	10/3			35			35	ns
t_{AHZ}	$\overline{OE}$ HIGH to address output HI-Z from HIGH	10/4			25			25	ns
t_{CTZL}	$\overline{OE}$ LOW to control output LOW	10/5			40			40	ns
t_{CTZH}	$\overline{OE}$ LOW to control output HIGH	10/6			50			50	ns
t_{CTLZ}	$\overline{OE}$ HIGH to control output HI-Z from LOW	10/7			30			30	ns
t_{CTHZ}	$\overline{OE}$ HIGH to control output HI-Z from HIGH	10/8			25			25	ns

Note 1: These are absolute voltage levels with respect to the ground pins on the device and includes all overshoots due to system or tester noise. Do not attempt to test these values without suitable equipment.

Note 2: This test is provided as a monitor of driver output source and sink current capability. Caution should be exercised in testing this parameter. One output should be tested at a time and test duration should not exceed one second.

Note 3: Output load capacitance is typical for four banks of 22 DRAMs with trace capacitance. The values are: Q0-8 C_L = 500 pF, $\overline{RAS}$0-3 C_L = 150 pF, $\overline{WE}$ C_L = 500 pF, $\overline{CAS}$0-1 C_L = 300 pF.

Absolute Maximum Ratings (See Note)

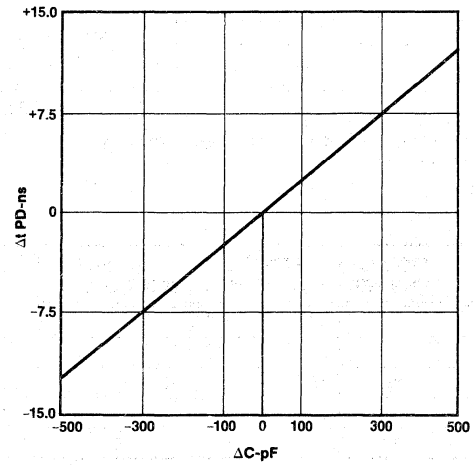
Supply voltage, V_{CC} ..... -0.5 V to 7 V
Storage temperature range ..... -65°C to +150°C
Input voltage ..... -1.5 V to 5.5 V
Output current ..... 150 mA
Lead temperature (soldering, 10 seconds) ..... 300°C

Note: "Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of operating conditions provides conditions for actual device operation.

Operating Conditions

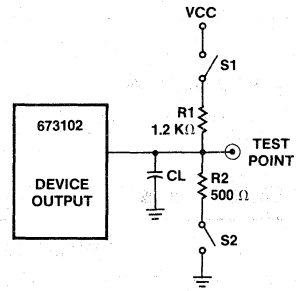
SYMBOL	PARAMETER	FIGURE/ NUMBER	673102A MIN	673102A TYP	673102A MAX	673102 MIN	673102 TYP	673102 MAX	UNIT
V_{CC}	Supply voltage		4.5		5.5	4.5		5.5	V
T_A	Ambient temperature		0		75	0		75	C
t_{ASA}	Address setup time to ADS LOW	8/1	18			18			ns
t_{ADS}	Address strobe pulse width HIGH		26			26			ns
t_{AHA}	Address hold time from ADS LOW	8/2	10			10			ns
	EXTERNALLY CONTROLLED ACCESS PARAMETER								
t_{ADHAR}	ADS LOW hold from $\overline{RASIN}$ HIGH	3/7	0			0			ns
t_{BSR}	Bank select setup to $\overline{RASIN}$ LOW (ADS = HIGH)	3/8	10			10			ns
t_{BSH}	Bank select hold from $\overline{RASIN}$ HIGH (ADS = HIGH)	3/9	10			10			ns
t_{SSR}	Address strobe HIGH setup to $\overline{RASIN}$ LOW (B0, B1 STABLE)	3/10	20			20			ns
t_{AUHE}	$\overline{AUTO}$ hold from $\overline{RASIN}$ HIGH	3/4	55			55			ns
t_{AUSRC}	$\overline{AUTO}$ HIGH setup to R/$\overline{C}$ LOW	5/1	25			25			ns
t_{AUHRC}	$\overline{AUTO}$ HIGH hold from R/$\overline{C}$ HIGH	5/2	10			10			ns
t_{AUSCA}	$\overline{AUTO}$ HIGH setup to $\overline{CASIN}$ LOW	4/1	45			45			ns
t_{AUHCA}	$\overline{AUTO}$ HIGH hold from $\overline{CASIN}$ HIGH	4/2	0			0			ns
t_{AUS}	$\overline{AUTO}$ setup to $\overline{RASIN}$ LOW	3/3	0			0			ns
t_{RFSR}	$\overline{RFSH}$ HIGH setup to $\overline{RASIN}$ LOW (to guarantee t_{ASR})	3/1	10			10			ns
t_{RFHR}	$\overline{RFSH}$ HIGH hold from $\overline{RASIN}$ HIGH	3/2	10			10			ns
	AUTOMATIC ACCESS PARAMETER								
t_{ADHAR}	ADS LOW hold from $\overline{RASIN}$ HIGH	3/7	0			0			ns
t_{BSR}	Bank select setup to $\overline{RASIN}$ LOW (ADS = HIGH)	6/12	10			10			ns
t_{BSH}	Bank select hold from $\overline{RASIN}$ HIGH (ADS = HIGH)	3/9	10			10			ns
t_{ASRL}	Address setup to $\overline{RASIN}$ LOW (ADS = HIGH) ($t_{ASRL} = t_{d2}$ max to guarantee t_{ASR})	6/4	30			30			ns
t_{AUS}	$\overline{AUTO}$ setup to $\overline{RASIN}$ LOW	6/5	0			0			ns
t_{RFSR}	$\overline{RFSH}$ HIGH setup to $\overline{RASIN}$ LOW (to guarantee t_{ASR})	6/6	10			10			ns
t_{SSR}	Address strobe HIGH to $\overline{RASIN}$ LOW (B0, B1 STABLE)	6/7	20			20			ns
t_{CASR}	$\overline{CASIN}$0-1 setup to $\overline{RASIN}$ LOW	6/8	-30			-30			ns
t_{AUH}	$\overline{AUTO}$ hold from $\overline{RASIN}$ HIGH	6/9	50			50			ns
t_{AUCH}	$\overline{AUTO}$ LOW hold from $\overline{CASIN}$ HIGH	6/10	0			0			ns
	REFRESH PARAMETER								
t_{AUHRF}	$\overline{AUTO}$ LOW hold from $\overline{RFSH}$ HIGH (R/$\overline{C}$ LOW)	7/1	10			10			ns
t_{RCSRF}	R/$\overline{C}$ HIGH setup to $\overline{RFSH}$ LOW ($\overline{AUTO}$ HIGH)	7/2	20			20			ns
t_{AUSRF}	$\overline{AUTO}$ LOW setup to $\overline{RFSH}$ LOW (R/$\overline{C}$ LOW)	7/3	20			20			ns
t_{RCHRF}	R/$\overline{C}$ HIGH hold from $\overline{RFSH}$ HIGH ($\overline{AUTO}$ HIGH)	7/4	10			10			ns
t_{RFH}	$\overline{RASIN}$ HIGH during refresh	7/10	30			30			ns
t_{RFQS}	$\overline{RFSH}$ LOW setup to $\overline{RASIN}$ LOW (to guarantee t_{RFS})	7/14	30			30			ns

9



Change in Propagation Delays vs. Change in Loading Capacitance Relative to the Specified Load

673102 Test Loads (See Note)



Note: Input pulse 0 V to 3.0 V, $t_R = t_F$ = 2.5 ns, f = 1 MHz, t_{PW} = 200 ns.
Input reference point on AC measurements is 1.5 V.
Output reference points are 2.4 V for HIGH and 0.8 V for LOW.

Address Outputs

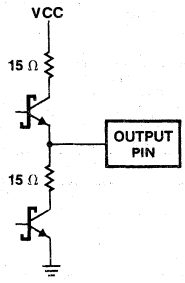
TEST	S1	S2	CL	MEASURED AT
t_{PD}	Open	Closed	500 pF	0.8 V, 2.4 V
t_{PZH}	Closed	Closed	500 pF	2.4 V
t_{PHZ}	Open	Closed	15 pF	V_{OH} -0.5 V
t_{PZL}	Closed	Closed	500 pF	0.8 V
t_{PLZ}	Closed	Open	15 pF	V_{OL} +0.5 V

Control Outputs

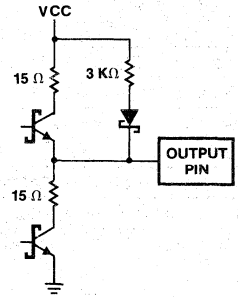
TEST	S1	S2	CL	MEASURED AT
t_{PD}	Open	Closed	CL	0.8 V, 2.4 V
t_{PZH}	Open	Closed	CL	2.4 V
t_{PHZ}	Open	Closed	15 pF	V_{OH} -0.5 V
t_{PZL}	Open	Open	CL	0.8 V
t_{PLZ}	Open	Open	15 pF	V_{OL} +0.5 V

Where CL = 150 pF for $\overline{RAS}$, 300 pF for $\overline{CAS}$, and 500 pF for $\overline{WE}$.

Address Driver Output Stage



Control Driver Output Stage



Applications

Microprocessor Interface

The 673102 Dynamic RAM Controller provides the address and control signals required to access and refresh dynamic RAMs. When interfaced to a 16-bit microprocessor, some external logic is required to generate a refresh clock as well as to perform access/refresh arbitration and interface handshake functions. Two PAL® devices may be used to perform these functions, as shown in Figure 1. One PAL device is used to generate the refresh clock, while the other performs all arbitration and handshake functions. A hidden refresh (refresh which is transparent to the system) scheme is implemented in the interface PAL device which takes advantage of "free" system time to refresh the memory, and falls back to "forced" refresh when hidden refresh cannot be performed.

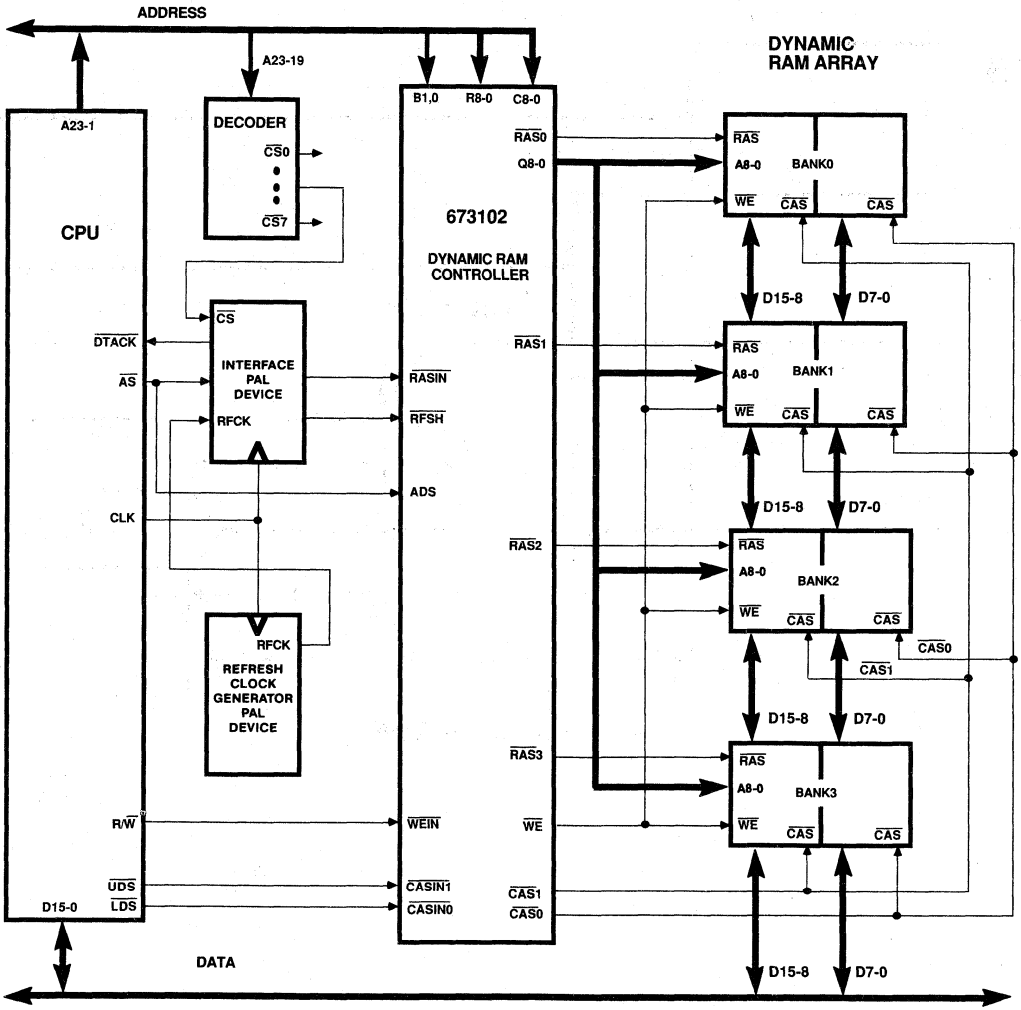


Figure 1. A CPU Interfaced to the 673102 Driving 2 M Bytes of Dynamic Memory

Determining System Performance (Auto-Access)

When determining system performance the dynamic RAM parameters must be considered as well as the controller's propagation delays. For both read and write cycles the access time for the dynamic RAM is t_{RAC} (Data access time from $\overline{RAS}$ going LOW) or t_{CAC} (Data access time from $\overline{CAS}$ going LOW), whichever results in the later appearance of Data at the dynamic RAM output. Since the $\overline{RAS}$ and $\overline{CAS}$ coming out of the controller are initiated by the $\overline{RASIN}$, the controller-memory performance is measured from the $\overline{RASIN}$ HIGH-to-LOW transition (See Figure 2).

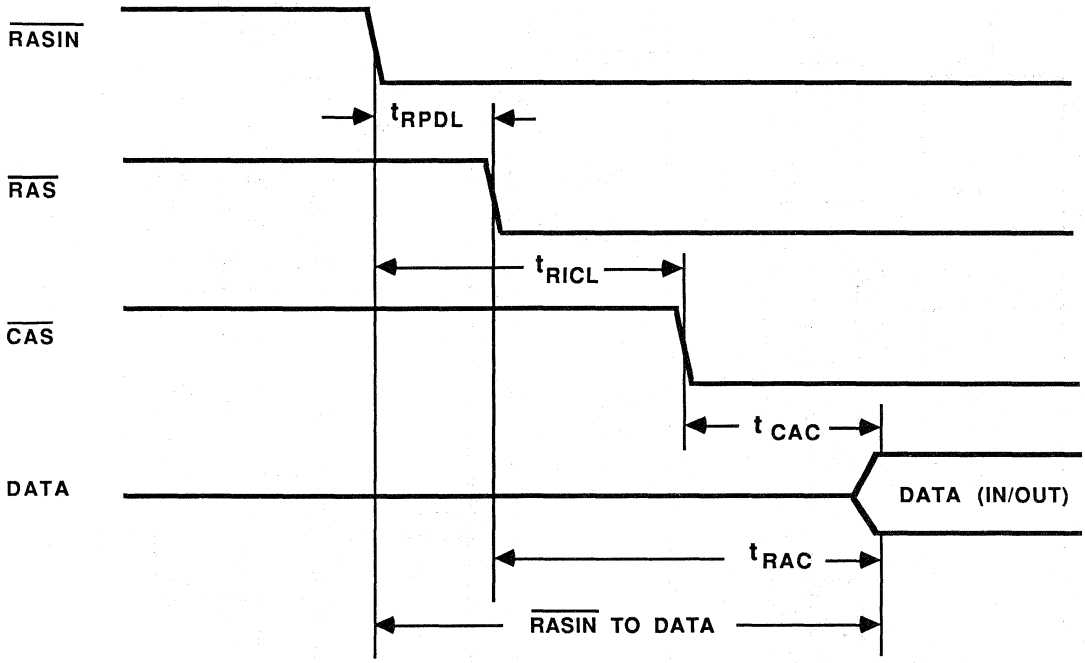


Figure 2. Access Time from $\overline{RASIN}$

The time from $\overline{RASIN}$ to data is calculated to be the longer of:

$t_{RICL} + t_{CAC}$ ($\overline{RASIN}$ to $\overline{CAS}$ + $\overline{CAS}$ to data)

$t_{RPDL} + t_{RAC}$ ($\overline{RASIN}$ to $\overline{RAS}$ + $\overline{RAS}$ to data)

Table 1 illustrates the access times from $\overline{RASIN}$ achieved for various dynamic RAM speeds.

CONTROLLER/MEMORY	PARAMETER				
	t_{RAC}	t_{RPDL}	t_{CAC}	t_{RICL}	ACCESS TIME FROM $\overline{RASIN}$
673102/HM256-12	120	20	60	85	145
673102A/HM256-12	120	20	60	75	140
673102/HM256-15	150	20	75	85	170
673102A/HM256-15	150	20	75	75	170
673102/MB8265A-10	100	20	50	85	135
673102A/MB8265A-10	100	20	50	75	125
673102/MB8265A-12	120	20	60	85	145
673102A/MB8265A-12	120	20	60	75	140
673102/IMS2620-10	100	20	60	85	145
673102A/IMS2620-10	100	20	60	75	135
673102/IMS2620-12	120	20	70	85	155
673102A/IMS2620-12	120	20	70	75	145

Table 1. Access Times from $\overline{RASIN}$ for Various Memory Speeds

673102 Parameters

t_{RPDL} — $\overline{RASIN}$ LOW to $\overline{RAS}$ LOW delay

t_{RICL} — $\overline{RASIN}$ TO $\overline{CAS}$ LOW delay

DRAM Parameters

t_{RAC} — Access time from $\overline{RAS}$ LOW

t_{CAC} — Access time from $\overline{CAS}$ LOW

Using the Externally Controlled Access

In the Externally Controlled Access mode $\overline{RASIN}$ controls the selected $\overline{RAS}$ output, and the $\overline{CASIN0}$, 1 inputs control $\overline{CAS0}$, 1 outputs respectively. The R/$\overline{C}$ input controls the address multiplexer. The system designer may create, using the $\overline{RASIN}$, $\overline{CASIN}$ and R/$\overline{C}$ inputs, the required control signal sequence for the specific system being designed. Special dynamic RAM access modes such as Nibble mode, Page mode, and static column mode access cycles may be performed simply by toggling the appropriate control inputs. Special skew timing specifications have been specified to allow tighter timing control as outlined in the following examples. Both following examples relate to the scheme depicted in Figure 3.

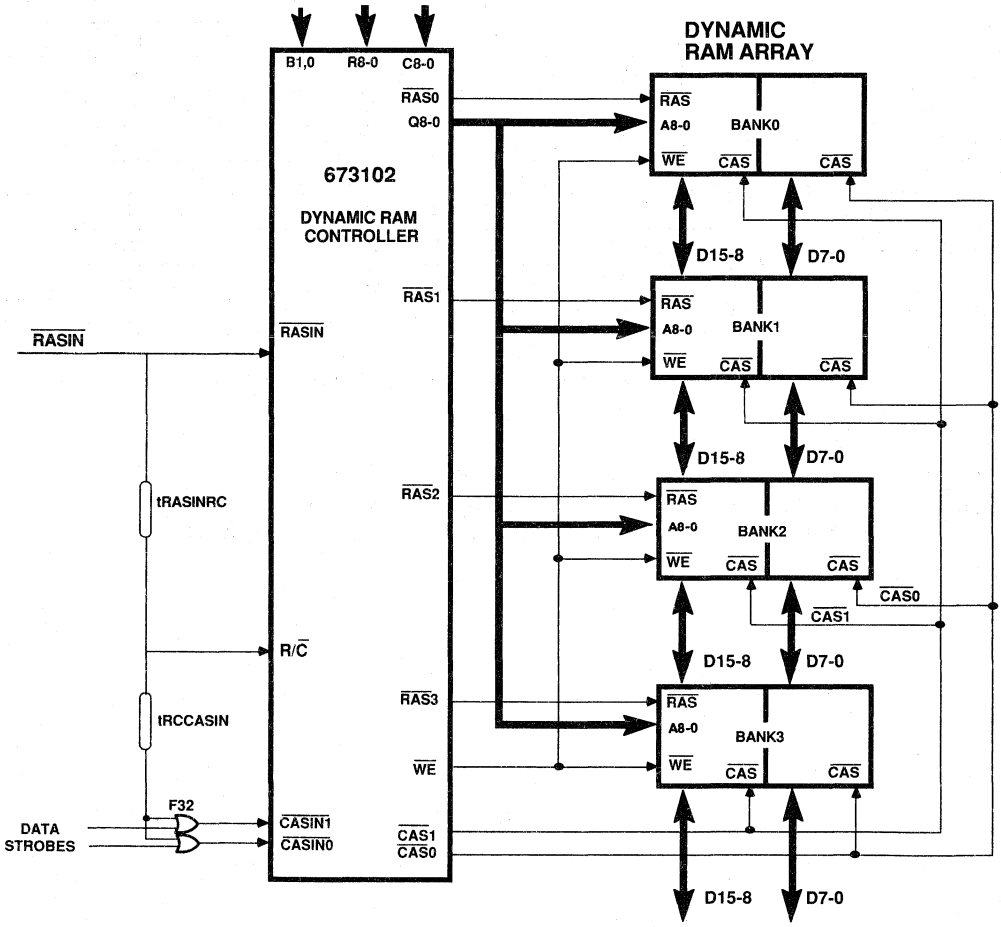


Figure 3. The 673102 in the Externally-Controlled Access Mode

Externally Controlled Access (ECA)
(Continued)

Example 1: Computing $\overline{RASIN}$ to R/$\overline{C}$ Delay

The delay between $\overline{RASIN}$ going LOW to R/$\overline{C}$ going LOW ($t_{RASINRC}$) which is required in order to satisfy the dynamic RAMs' row address hold time (t_{RAH}) is computed as follows:

$t_{RASINRC} = t_{RAH}(min) + t_{d7}$

Where:

$t_{RAH}(min)$ — Row address hold time (dynamic RAM parameter)

$t_{d7}(max) = t_{RPDL} - t_{RHA}$

t_{RPDL} — $\overline{RASIN}$ to $\overline{RAS}$ LOW delay

t_{RHA} — Row address held valid from R/$\overline{C}$ LOW

Example 2: Computing R/$\overline{C}$ to $\overline{CASIN}$ Delay

The delay between R/$\overline{C}$ going LOW and $\overline{CASIN}$ going LOW ($t_{RCCASIN}$) which is required in order to satisfy the dynamic RAMs' column address setup (t_{ASC}) is computed as follows:

$t_{RCCASIN} = t_{ASC}(min) + t_{d8} + t_{PD}F32(max)$

Where:

$t_{ASC}(min)$ — Column address setup (dynamic RAM parameter)

$t_{d8}(max) = t_{RCC} - t_{CPDL}$

t_{RCC} — R/$\overline{C}$ low to column address valid

t_{CPDL} — $\overline{CASIN}$ to $\overline{CAS}$ LOW delay

$t_{PD}F32(max)$ — Propagation delay of the OR gate used to validate $\overline{CASIN}$

Better system performance may be achieved using the t_{d7}, t_{d8} switching parameters to calculate $t_{RASINRC}$ and $t_{RCCASIN}$ than when using the t_{RPDL}, t_{RCDL}, t_{RCC} and t_{RHA} parameters (see t_{d7}, t_{d8} in Externally Controlled Access switching parameters).

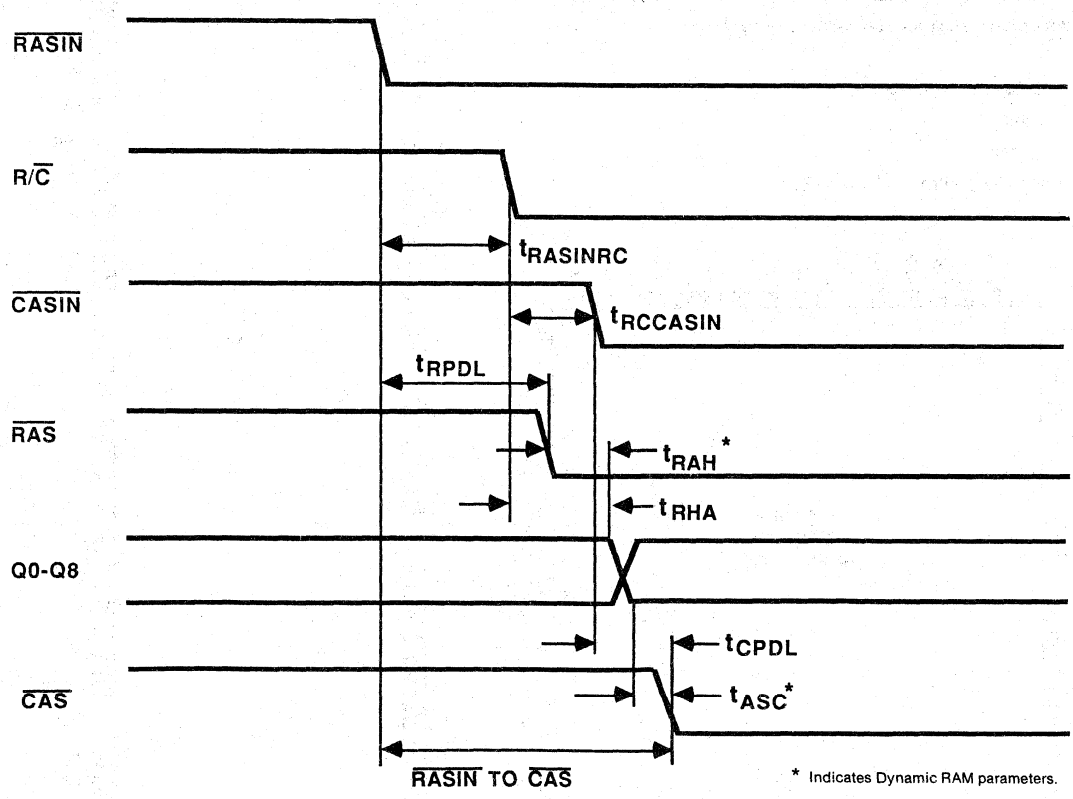


Figure 4. Externally Controlled Access Timing

1-Megabit Dynamic RAM Controller/Driver

673103
673103A

Features/Benefits

- Supports up to 1 M DRAMs
- Capable of addressing up to 8 M 16-bit words or 8 M bytes
- On-chip capacitive-load drivers capable of driving up to 88 DRAMs with 30-nsec typical address propagation delay and 128 DRAMs with 35-nsec typical address propagation delay
- $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ delay of 20 nsec max ($\overline{\text{RAS}}$ driving 22 DRAMs)
- Max and Min skews are specified to simplify system design
- Two $\overline{\text{CASIN}}$ inputs and two $\overline{\text{CAS}}$ outputs simplify byte addressing
- An Auto-Access mode with extended $\overline{\text{CAS}}$ capability takes advantage of full performance of 120 and 150 nsec DRAMs
- An output series resistor reduces undershoot

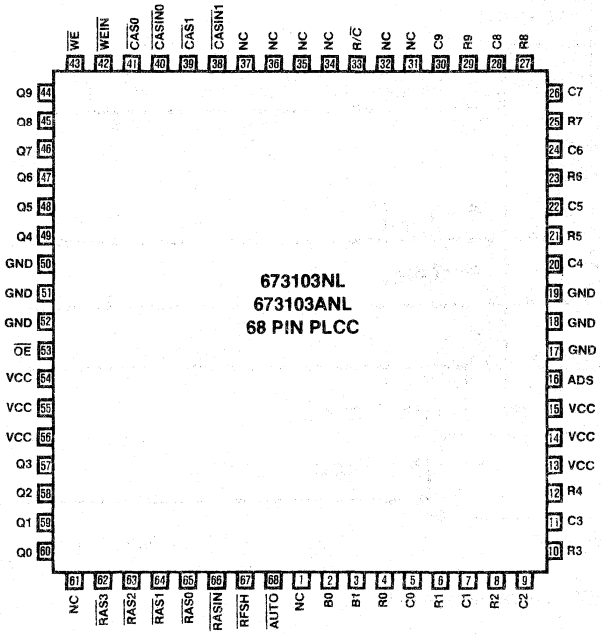
Modes of Operation

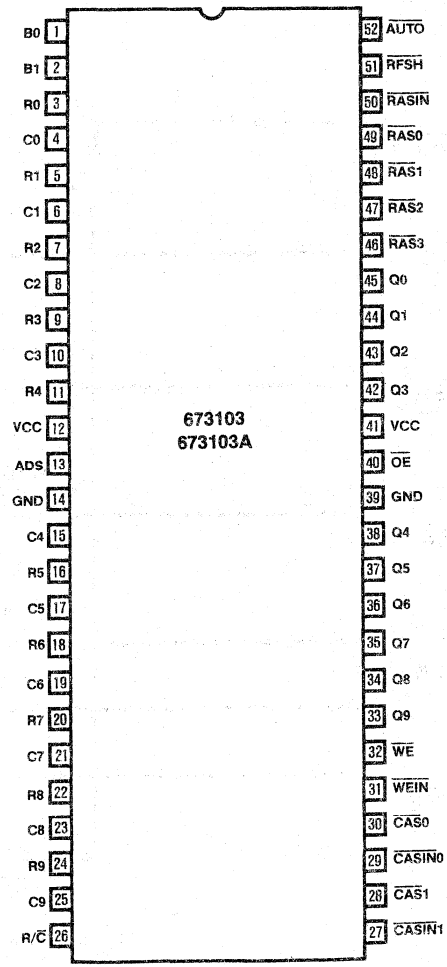
- Refresh
- Auto Access (AA)
- Externally Controlled Access (ECA)

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
673103	52D, 68NL, 68NP	Com
673103A		

Pin Configurations





2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories

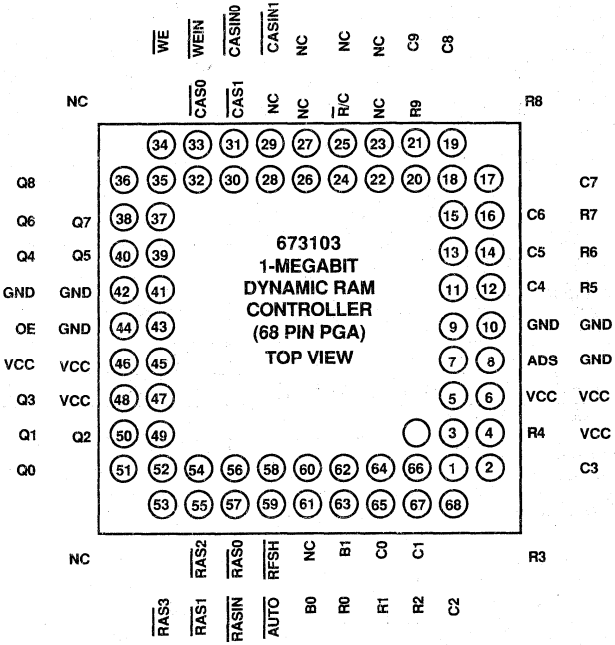
Switching Characteristics (Continued)

SYMBOL	AUTO ACCESS PARAMETER	FIGURE/ NUMBER	673103A MIN	673103A TYP	673103A MAX	673103 MIN	673103 TYP	673103 MAX	UNIT
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ LOW delay	6/20			75			85	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ LOW delay	6/23	30		65	30		75	ns
t_{RPDL}	$\overline{RASIN}$ to $\overline{RAS}$ LOW delay	6/13			20			20	ns
t_{RPDH}	$\overline{RASIN}$ to $\overline{RAS}$ HIGH delay	6/14			31			31	ns
t_{APD}	Address input to output delay	6/16			50			50	ns
t_{WPDL}	$\overline{WEIN}$ to $\overline{WE}$ LOW delay				45			45	ns
t_{WPDH}	$\overline{WEIN}$ to $\overline{WE}$ HIGH delay				40			40	ns
t_{CPDH}	$\overline{CASIN}$ to $\overline{CAS}$ HIGH delay	6/22			40			40	ns
t_{RAH}	Row address hold time from $\overline{RAS}$ LOW	6/17	15			15			ns
t_{d2}	(Address input to output delay)-($\overline{RASIN}$ to $\overline{RAS}$ LOW delay)				30			30	ns
t_{SPD}	ADS HIGH to address output valid	6/19			55			55	ns
t_{ASC}	Column address setup to $\overline{CAS}$ LOW	6/21	0			0		5	ns
t_{CAHC}	Column address remaining valid from $\overline{CASIN}$0-1 HIGH	6/18	5			5			ns
t_{ASR}	Row address valid before $\overline{RAS}$ LOW	6/24	0			0			ns
t_{d5}	($\overline{RASIN}$ to $\overline{RAS}$ HIGH delay)-($\overline{RASIN}$ to $\overline{RAS}$ LOW delay)		-7		13	-7		13	ns
	REFRESH PARAMETER								
t_{RFLCT}	$\overline{RFSH}$ LOW to refresh address valid ($\overline{AUTO}$ LOW or R/$\overline{C}$ HIGH)	7/5			40			40	ns
t_{RFPDL}	$\overline{RASIN}$ LOW to $\overline{RAS}$ LOW delay during refresh	7/11			23			23	ns
t_{RFPDH}	$\overline{RASIN}$ HIGH to $\overline{RAS}$ HIGH delay during refresh	7/12			38			38	ns
t_{RFAH}	Refresh address held from $\overline{RASIN}$ HIGH ($\overline{RFSH}$ LOW)	7/7	0			0			ns
t_{RHNC}	RASIN HIGH to new refresh address valid	7/9			66			66	ns
t_{RFAHR}	Refresh address held from $\overline{RFSH}$ HIGH	7/6	0			0			ns
t_{RFS}	Refresh address valid to $\overline{RAS}$ LOW (provided t_{RFQS} is satisfied)	7/13	0			0			ns
t_{RFRDH}	$\overline{RFSH}$ HIGH to $\overline{RAS}$ HIGH (for 3 banks, $\overline{RASIN}$ = LOW)	7/15			40			40	ns
t_{d9}	($\overline{RASIN}$ to $\overline{RAS}$ HIGH delay)-($\overline{RASIN}$ to $\overline{RAS}$ LOW delay)		-9		16	-9		16	ns
	THREE-STATE PARAMETER								
t_{AZL}	$\overline{OE}$ LOW to address output LOW	10/1			45			45	ns
t_{AZH}	$\overline{OE}$ LOW to address output HIGH	10/2			60			60	ns
t_{ALZ}	$\overline{OE}$ HIGH to address output HI-Z from LOW	10/3			35			35	ns
t_{AHZ}	$\overline{OE}$ HIGH to address output HI-Z from HIGH	10/4			25			25	ns
t_{CTZL}	$\overline{OE}$ LOW to control output LOW	10/5			40			40	ns
t_{CTZH}	$\overline{OE}$ LOW to control output HIGH	10/6			50			50	ns
t_{CTLZ}	$\overline{OE}$ HIGH to control output HI-Z from LOW	10/7			30			30	ns
t_{CTHZ}	$\overline{OE}$ HIGH to control output HI-Z from HIGH	10/8			25			25	ns

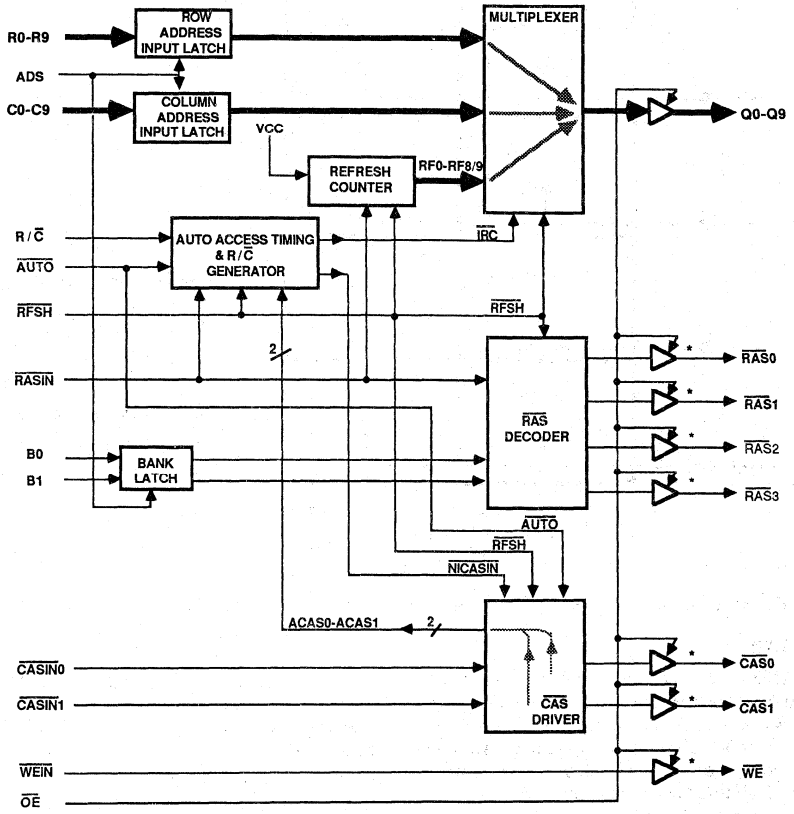
Note 1: These are absolute voltage levels with respect to the ground pins on the device and includes all overshoots due to system or tester noise. Do not attempt to test these values without suitable equipment.

Note 2: This test is provided as a monitor of driver output source and sink current capability. Caution should be exercised in testing this parameter. One output should be tested at a time and test duration should not exceed one second.

Note 3: Output load capacitance is typical for four banks of 22 DRAMs with trace capacitance. The values are: Q0-8 C_L = 500 pF, $\overline{RAS}$0-3 C_L = 150 pF, $\overline{WE}$ C_L = 500 pF, $\overline{CAS}$0-1 C_L = 300 pF.


673103
1-MEGABIT
DYNAMIC RAM
CONTROLLER
(68 PIN PGA)
TOP VIEW
WE
WEIN
CASIN0
CASIN1
NC
NC
NC
C9
C8
NC
CAS0
CAS1
NC
NC
R/C
NC
R9
R8
34 33 31 29 27 25 23 21 19
Q8 36 35 32 30 28 26 24 22 20 18 17 C7
Q6 Q7 38 37 15 16 C6 R7
Q4 Q5 40 39 13 14 C5 R6
GND GND 42 41 11 12 C4 R5
OE GND 44 43 9 10 GND GND
VCC VCC 46 45 7 8 ADS GND
Q3 VCC 48 47 5 6 VCC VCC
Q1 Q2 50 49 3 4 R4 VCC
Q0 51 52 54 56 58 60 62 64 66 1 2 C3
53 55 57 59 61 63 65 67 68
NC
RAS2
RAS0
RFSH
NC
B1
C0
C1
R3
RAS3
RAS1
RASIN
AUTO
B0
R0
R1
R2
C2

Block Diagram



* Indicates that there is a 3-KΩ pull-up resistor on these outputs when they are disabled

Figure 1. 673103 Functional Block Diagram

Description

The 673103 is an LSI device, provided in 52-pin and 68-pin packages, which performs most of the functions needed to control and address Dynamic RAMs. Twenty-two address inputs, ten address outputs, four RAS outputs, and two CASIN-CAS input-output pairs allow the 673103 to directly address 8 M 16-bit words or bytes. The CASINn inputs and the CASn outputs simplify individual byte access in 16-bit wide memory arrays (see Figure 2).

The 673103 has three operating modes:

- Externally Controlled Access (ECA)
- Auto Access (AA)
- Refresh (RFSH).

The Externally-Controlled-Access mode gives the system direct control over the RASm outputs, the CASn outputs, and Row/Column multiplexing. It also supports PAGE mode access, NIBBLE mode access, and static column mode access.

The Auto-Access mode provides on-chip delays that automatically control the timing delays between RASm signals, address multiplexing, and CASn signals. In the Auto-Access mode CASIN0-1 inputs serve as enables for the respective CAS0-1 outputs, allowing the access of any byte of the memory array (for 16-bit wide memory arrays organized in two bytes). In this mode CAS0-1 outputs go HIGH only when the respective CASIN0-1 inputs go HIGH, and the address switches back to row address only when both CASIN0-1 go HIGH. This feature allows extension of the CAS LOW time, and column address time while RASIN and RASm can go HIGH to satisfy the precharge requirements of the dynamic RAMs.

When the Refresh mode is selected (RFSH is LOW) an on-chip refresh counter provides the refresh address; with AUTO HIGH and R/C LOW the column address is forced onto the address output multiplexer, facilitating an access of a particular memory location while refreshing a row. This feature may be useful when implementing error detection and correction scrubbing.

The 673103 can drive eight banks of DRAMs. RASm control signals are used to select a pair of banks, while leaving the other banks in standby. The two CASn outputs enable the selection of one bank out of two. The address lines and the WE signal can be connected to all eight banks. In a 16-bit wide, byte-oriented, memory array the RASm signals select the banks while the CASn signals select the bytes, as shown in Figure 2.

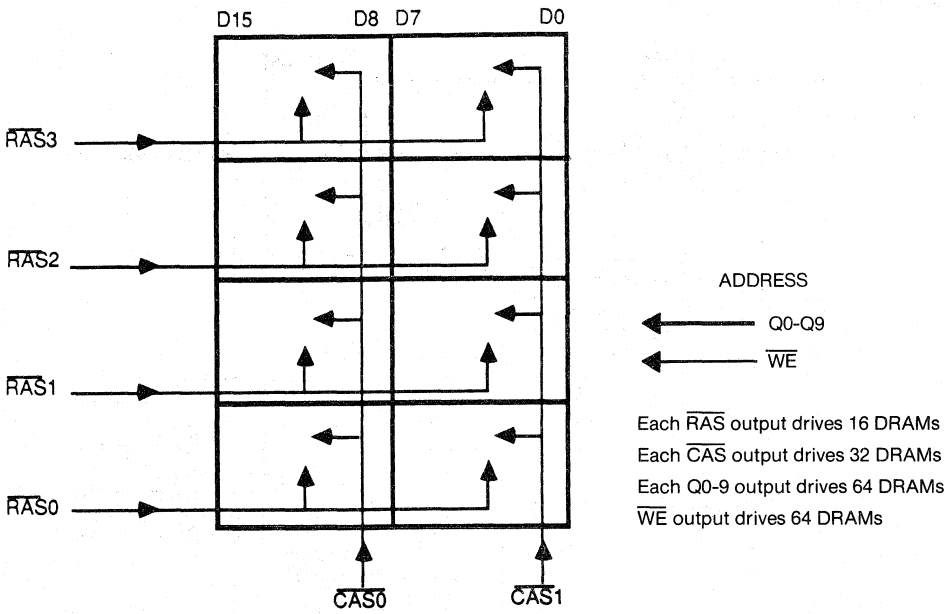


Figure 2. 673103 Addressing Four Banks of 16-bit Memory Array Organized in Two Bytes

Pin Definitions

VCC, GND: VCC-GND = 5 V ±10%. The supply pins have been assigned to the center of the package to reduce voltage drops, both DC and AC. A low-inductance connection between the ground pin and a solid ground plane will minimize fluctuations in the ground level of the device that may occur when the address outputs switch from HIGH to LOW simultaneously. A 1-μF multilayer ceramic capacitor in parallel with a low-voltage tantalum capacitor, both connected close to the VCC and GND pins, will properly decouple the device.

R0-R9: Row Address Inputs

C0-C9: Column Address Inputs

B0-B1: Bank-Pair Select Inputs — Strobed by ADS. Decoded to enable one of the $\overline{RAS}$ outputs when $\overline{RASIN}$ goes LOW in the access modes.

Q0-Q9: Multiplexed Address Outputs — Selected from the row address input latch, the column address input latch, or the refresh counter.

$\overline{RASIN}$: Row Address Strobe Input — Drives the selected $\overline{RAS}$m output in the access modes, and all $\overline{RAS}$ outputs in the Refresh mode.

ADS: Address (Latch) Strobe Input — Strobes input row address, column address, and Bank Select inputs into the respective latches when HIGH; latches on HIGH-to-LOW transition.

$\overline{OE}$: Output Enable — When $\overline{OE}$ is LOW the address and control outputs are enabled. When $\overline{OE}$ is HIGH the address outputs are in high-impedance and the control outputs are pulled HIGH.

R/$\overline{C}$: Row/Column Select Input — In the Externally-Controlled-Access mode, it is used to select either the row address input latch or the column address input latch onto the address outputs. In the Refresh mode, when $\overline{AUTO}$ is HIGH, it is used to select between the refresh address (R/$\overline{C}$ HIGH) and the column address (R/$\overline{C}$ LOW). When $\overline{AUTO}$ is LOW R/$\overline{C}$ is disabled.

$\overline{CASIN}$0-1: Column Address Strobe Inputs — In the Externally-Controlled-Access mode, the $\overline{CASIN}$n directly drives the $\overline{CAS}$n output. In the Auto-Access mode, it is used to enable the corresponding $\overline{CAS}$n output (See $\overline{CAS}$0-1 description).

$\overline{WEIN}$: Write Enable Input.

$\overline{WE}$: Write Enable Output.

$\overline{CAS}$0-1: Column Address Strobe Outputs — In the Externally-Controlled-Access mode the $\overline{CAS}$ outputs follow the $\overline{CASIN}$ inputs. In the Auto-Access mode the $\overline{CASIN}$ inputs are used to enable the $\overline{CAS}$ outputs. The $\overline{CAS}$ outputs are asserted LOW, with proper delay from the $\overline{RAS}$ output, by the $\overline{RASIN}$ signal via the Auto-Access timing generator. In the Auto-Access mode, the $\overline{CAS}$n goes HIGH only when the corresponding $\overline{CASIN}$n goes HIGH. Extending the $\overline{CAS}$n LOW duration while $\overline{RASIN}$ and $\overline{RAS}$m go HIGH to satisfy precharge requirements of the dynamic RAMs.

$\overline{RAS}$0-3: Row Address Strobe Outputs — When $\overline{RFSH}$ is HIGH the selected row address strobe output (decoded from signals B0, B1) follows the $\overline{RASIN}$ input. When $\overline{RFSH}$ is LOW all $\overline{RAS}$ outputs go LOW together following $\overline{RASIN}$ going LOW.

$\overline{AUTO}$: Auto-Access Input — When AUTO is LOW and $\overline{RFSH}$ is HIGH the Auto-Access mode is selected (see Auto-Access mode description).

$\overline{RFSH}$: Refresh Input — When $\overline{RFSH}$ is LOW the Refresh mode is selected (see Refresh mode description).

Externally-Controlled-Access Mode (ECA)

In this mode, selected when $\overline{AUTO}$ and $\overline{RFSH}$ are held HIGH, the 673103 serves as a straightforward multiplexer and driver for the address and control signals to the DRAMs. The $\overline{RAS}$m output selected by the B0 and B1 inputs follows the $\overline{RASIN}$ input, and each of the $\overline{CAS}$ outputs follows its corresponding $\overline{CASIN}$ input. When R/$\overline{C}$ is HIGH the row address is enabled onto the Q0-9 outputs. When R/$\overline{C}$ is LOW the column address latch is enabled onto Q0-9 outputs.

The $\overline{RASIN}$ — $\overline{RAS}$, $\overline{CASIN}$ — $\overline{CAS}$, and R/$\overline{C}$ — Q0-9 control paths are independent to allow the system designer maximum flexibility and support of special DRAM access and refresh modes such as NIBBLE mode, PAGE mode, $\overline{CAS}$ before $\overline{RAS}$, etc.

To allow tighter timing of the sequence of control signals to the Dynamic RAM, several difference timing parameters have been specified for the Externally Controlled Access mode. These parameters specify the maximum difference between the various "control channels" of the device. In particular, using switching characteristics t_{d7} and t_{d8} is very useful when designing the delay from $\overline{RASIN}$ going LOW to R/$\overline{C}$ and the delay between R/$\overline{C}$ going LOW to $\overline{CASIN}$ going LOW (see Applications).

BANK SELECT (STROBED BY ADS)		ENABLED $\overline{RAS}$n
B1	B0	
0	0	$\overline{RAS0}$
0	1	$\overline{RAS1}$
1	0	$\overline{RAS2}$
1	1	$\overline{RAS3}$

Table 1. Memory Bank Decode

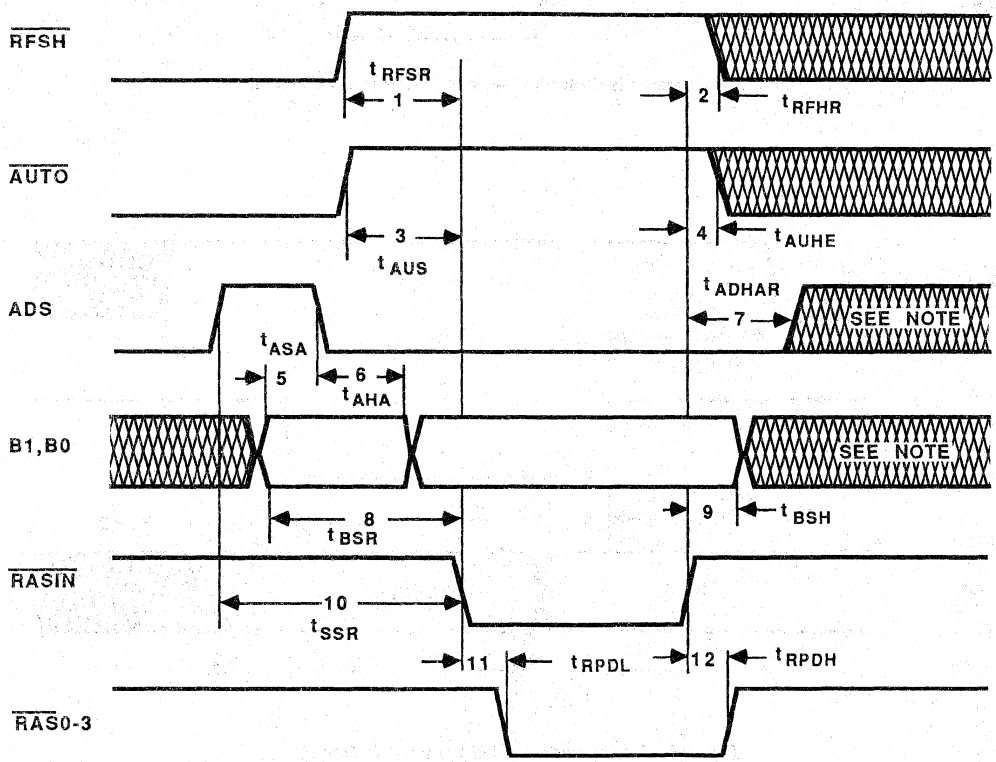


Figure 3. Externally Controlled Access—$\overline{RASIN}$-to-$\overline{RAS}$ Timing

Note: To prevent glitches on the $\overline{RAS}$0-3 outputs, operating conditions t_{BSH} or t_{ADHAR} must be satisfied.

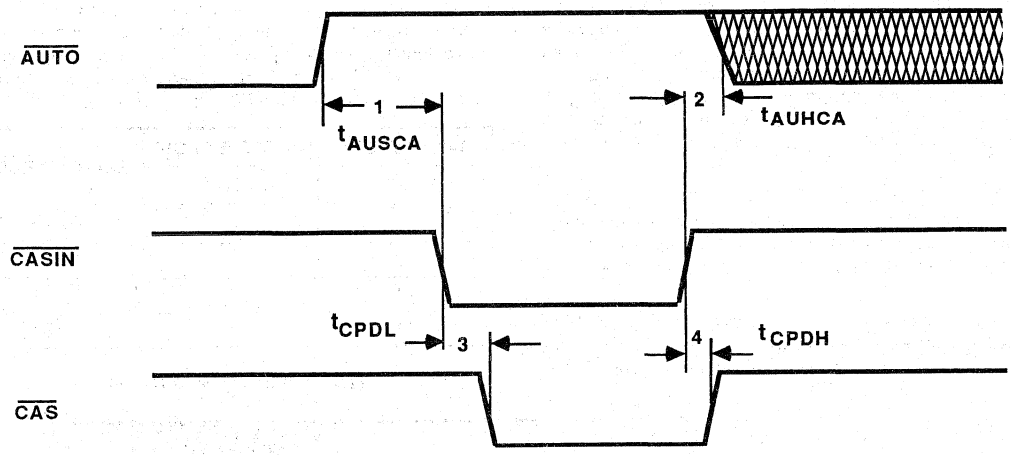


Figure 4. Externally Controlled Access-$\overline{\text{CASIN}}$ to $\overline{\text{CAS}}$ Timing

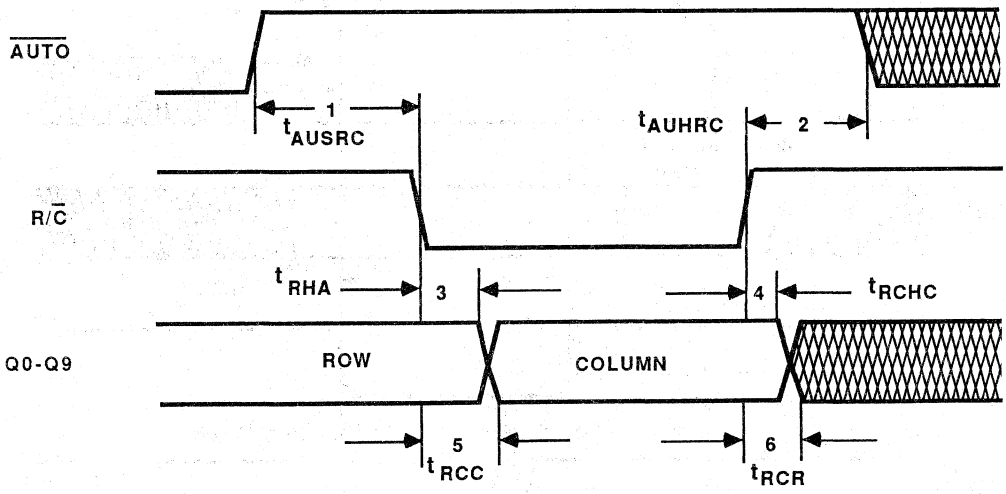


Figure 5. Externally Controlled Access R/$\overline{\text{C}}$ Timing

Note: t_{RCC} will be met only if the column address is available t_{APD} before it appears on Q0-9 outputs or if it is latched by ADS.

Auto-Access Mode (AA)

In the Auto-Access mode the 673103 provides the system designer with built-in delays and sequencing to accommodate DRAMs with 150 nanoseconds and faster access time. The Auto-Access mode is selected when $\overline{AUTO}$ is held LOW and $\overline{RFSH}$ pin is held HIGH. The R/$\overline{C}$ input is disabled, and $\overline{RASIN}$ goes LOW initiating the sequence of control signals to access the DRAMs. The $\overline{CASIN}$0-1 inputs are used as enables for the respective $\overline{CAS}$ outputs. A LOW on a $\overline{CASIN}$n input enables the $\overline{CAS}$n output to be driven LOW with the internally-generated delay from $\overline{RAS}$. Each $\overline{CAS}$n output goes HIGH only when the corresponding $\overline{CASIN}$n input goes HIGH, and the address switches back to row address only when all $\overline{CASIN}$ go HIGH. This feature allows extension of the $\overline{CAS}$ LOW time and the column address time, while $\overline{RASIN}$ and $\overline{RAS}$m can go HIGH to satisfy precharge requirements of the dynamic RAMs. The R/$\overline{C}$ input is disabled in this mode.

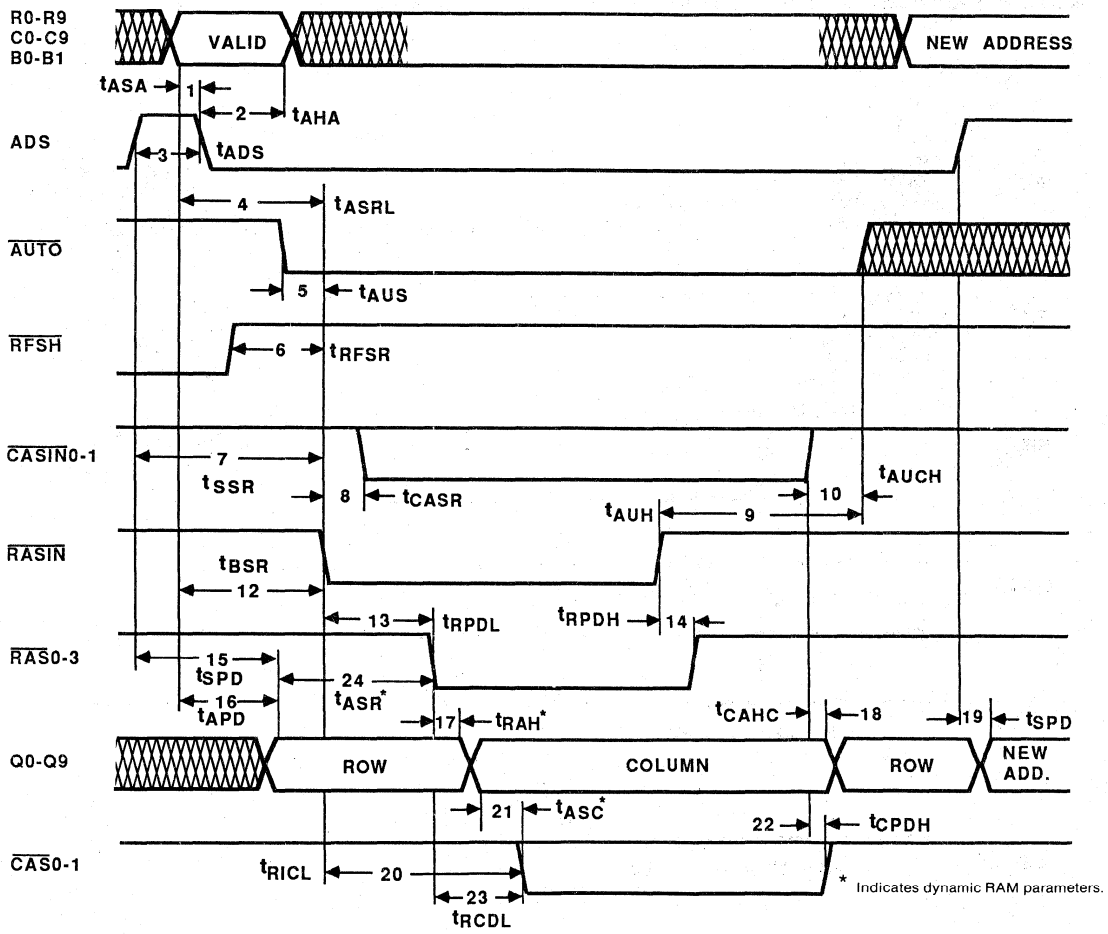


Figure 6. Auto-Access (AA) Timing

Refresh Mode (RFSH)

When $\overline{RFSH}$ is held LOW the refresh counter contents are enabled onto the Q0-9 address outputs, provided either R/$\overline{C}$ is held HIGH, or $\overline{AUTO}$ is held LOW, or both conditions exist. In this mode all four $\overline{RAS}$ outputs follow the $\overline{RASIN}$ input signal. The refresh counter increments the refresh address when either $\overline{RASIN}$ or $\overline{RFSH}$ goes HIGH while the other is LOW. When $\overline{AUTO}$ is LOW the $\overline{CASIN}$0-1 inputs are isolated and $\overline{CAS}$0-1 are held HIGH. Also, when $\overline{AUTO}$ is LOW the R/$\overline{C}$ input is isolated from the output multiplexer, and the refresh address appears at the Q0-9 outputs.

When $\overline{AUTO}$ is HIGH, pulling R/$\overline{C}$ LOW enables the column address onto the Q0-9 outputs. Also, each of the $\overline{CAS}$ outputs follows its respective $\overline{CASIN}$ input. This feature may be used when implementing error correction and detection "scrubbing" for two-bank memory arrays. "Scrubbing" is a term describing a cyclic error correction of soft errors in the memory array, done within the refresh cycles. On every refresh cycle one location of the memory array is accessed, and the data in that location goes, if necessary, through a correction cycle (a read-modify-write memory cycle). The 673103 provides the facilities to force a column address onto the Q0-9 address outputs and to assert the $\overline{CAS}$0-1 outputs within a refresh cycle to allow scrubbing. A column counter and a bank counter need to be added externally to provide the column address for scrubbing.

The refresh counter is a 10-bit counter that resets to 0 on power-up and rolls over to 0 at 1023.

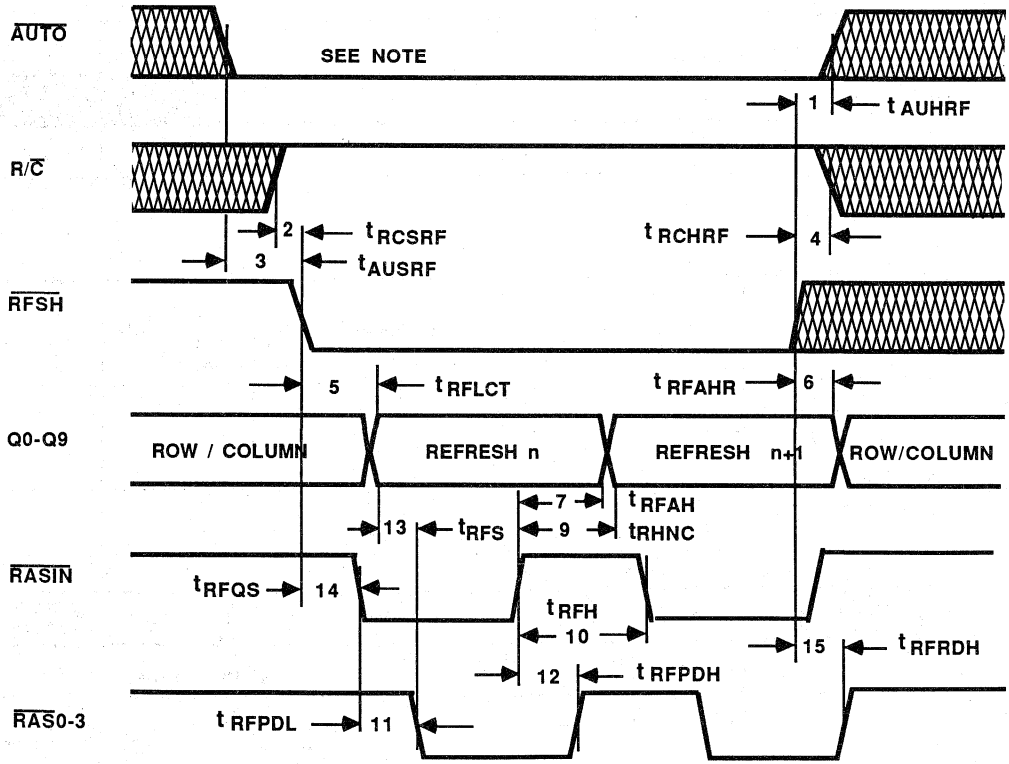


Figure 7. Refresh Timing

Note: In the REFRESH mode, $\overline{AUTO}$ must be LOW or R/$\overline{C}$ must be HIGH to guarantee the refresh address on the Q0-8 outputs.

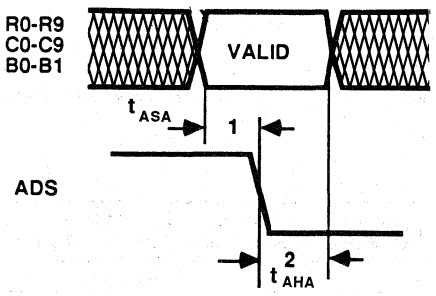
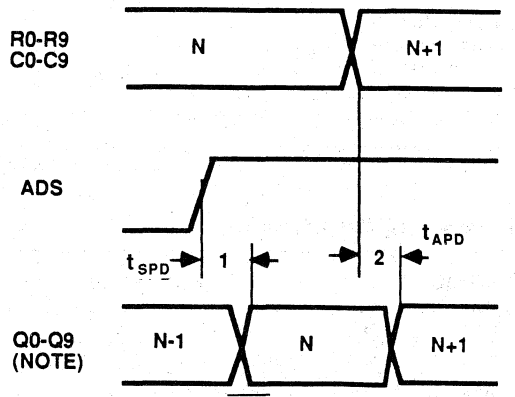


Figure 8. Address Setup and Hold Time to ADS



Note: Row or Column address ($\overline{RFSH}$ = HIGH).

Figure 9. Address Input/Output Propagation Delay

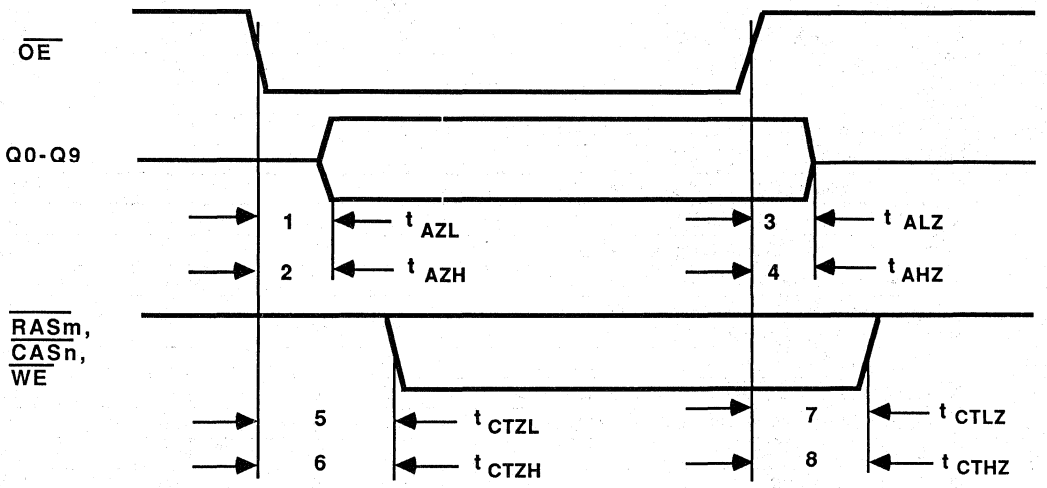


Figure 10. High-Z Timing

Absolute Maximum Ratings (See Note)

Supply voltage, V_{CC} ..... -0.5 V to 7 V
Storage temperature range ..... -65°C to +150°C
Input voltage ..... -1.5 V to 5.5 V
Output current ..... 150 mA
Lead temperature (soldering, 10 seconds) ..... 300°C

Note: "Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of operating conditions provides conditions for actual device operation.

Operating Conditions

SYMBOL	PARAMETER	FIGURE/ NUMBER	673103A MIN	673103A TYP	673103A MAX	673103 MIN	673103 TYP	673103 MAX	UNIT
V_{CC}	Supply voltage		4.5		5.5	4.5		5.5	V
T_A	Ambient temperature		0		75	0		75	C
t_{ASA}	Address setup time to ADS LOW	8/1	18			18			ns
t_{ADS}	Address strobe pulse width HIGH		26			26			ns
t_{AHA}	Address hold time from ADS LOW	8/2	10			10			ns
	EXTERNALLY CONTROLLED ACCESS PARAMETER								
t_{ADHAR}	ADS LOW hold from $\overline{RASIN}$ HIGH	3/7	0			0			ns
t_{BSR}	Bank select setup to $\overline{RASIN}$ LOW (ADS = HIGH)	3/8	10			10			ns
t_{BSH}	Bank select hold from $\overline{RASIN}$ HIGH (ADS = HIGH)	3/9	10			10			ns
t_{SSR}	Address strobe HIGH setup to $\overline{RASIN}$ LOW (B0, B1 STABLE)	3/10	20			20			ns
t_{AUHE}	$\overline{AUTO}$ hold from $\overline{RASIN}$ HIGH	3/4	55			55			ns
t_{AUSRC}	$\overline{AUTO}$ HIGH setup to R/$\overline{C}$ LOW	5/1	25			25			ns
t_{AUHRC}	$\overline{AUTO}$ HIGH hold from R/$\overline{C}$ HIGH	5/2	10			10			ns
t_{AUSCA}	$\overline{AUTO}$ HIGH setup to $\overline{CASIN}$ LOW	4/1	45			45			ns
t_{AUHCA}	$\overline{AUTO}$ HIGH hold from $\overline{CASIN}$ HIGH	4/2	0			0			ns
t_{AUS}	$\overline{AUTO}$ setup to $\overline{RASIN}$ LOW	3/3	0			0			ns
t_{RFSR}	$\overline{RFSH}$ HIGH setup to $\overline{RASIN}$ LOW (to guarantee t_{ASR})	3/1	10			10			ns
t_{RFHR}	$\overline{RFSH}$ HIGH hold from $\overline{RASIN}$ HIGH	3/2	10			10			ns
	AUTOMATIC ACCESS PARAMETER								
t_{ADHAR}	ADS LOW hold from $\overline{RASIN}$ HIGH	3/7	0			0			ns
t_{BSR}	Bank select setup to $\overline{RASIN}$ LOW (ADS = HIGH)	6/12	10			10			ns
t_{BSH}	Bank select hold from $\overline{RASIN}$ HIGH (ADS = HIGH)	3/9	10			10			ns
t_{ASRL}	Address setup to $\overline{RASIN}$ LOW (ADS = HIGH) ($t_{ASRL} = t_{d2}$ max to guarantee t_{ASR})	6/4	30			30			ns
t_{AUS}	$\overline{AUTO}$ setup to $\overline{RASIN}$ LOW	6/5	0			0			ns
t_{RFSR}	$\overline{RFSH}$ HIGH setup to $\overline{RASIN}$ LOW (to guarantee t_{ASR})	6/6	10			10			ns
t_{SSR}	Address strobe HIGH to $\overline{RASIN}$ LOW (B0, B1 STABLE)	6/7	20			20			ns
t_{CASR}	$\overline{CASIN}$0-1 setup to $\overline{RASIN}$ LOW	6/8	-30			-30			ns
t_{AUH}	$\overline{AUTO}$ hold from $\overline{RASIN}$ HIGH	6/9	50			50			ns
t_{AUCH}	$\overline{AUTO}$ LOW hold from $\overline{CASIN}$ HIGH	6/10	0			0			ns
	REFRESH PARAMETER								
t_{AUHRF}	$\overline{AUTO}$ LOW hold from $\overline{RFSH}$ HIGH (R/$\overline{C}$ LOW)	7/1	10			10			ns
t_{RCSRF}	R/$\overline{C}$ HIGH setup to $\overline{RFSH}$ LOW ($\overline{AUTO}$ HIGH)	7/2	20			20			ns
t_{AUSRF}	$\overline{AUTO}$ LOW setup to $\overline{RFSH}$ LOW (R/$\overline{C}$ LOW)	7/3	20			20			ns
t_{RCHRF}	R/$\overline{C}$ HIGH hold from $\overline{RFSH}$ HIGH ($\overline{AUTO}$ HIGH)	7/4	10			10			ns
t_{RFH}	$\overline{RASIN}$ HIGH during refresh	7/10	30			30			ns
t_{RFQS}	$\overline{RFSH}$ LOW setup to $\overline{RASIN}$ LOW (to guarantee t_{RFS})	7/14	30			30			ns

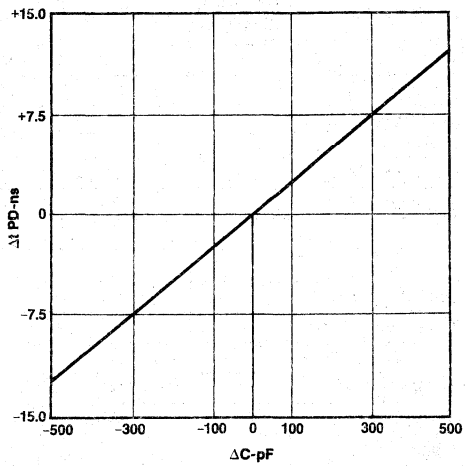
Electrical Characteristics V_{CC} = 5 V ±10%, 0°C ≤ T_A ≤ 75°C. Typicals are for V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	FIGURE/ NUMBER	MIN	TYP	MAX	UNIT
V_{IC}	Input clamp voltage	I_{IN} = -18 mA, V_{CC} = MIN			-0.8	-1.2	V
I_{IH}	Input high current	V_{IN} = 2.7 V, V_{CC} = MAX				50	μA
I_{CTL}	Output load current for $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	V_{OUT} = 0.4 V, V_{CC} = MAX Chip deselect			-1.5	-2.5	mA
I_{IL}	Input low current except for $\overline{RFSH}$	V_{IN} = 0.4 V, V_{CC} = MAX			-20	-250	μA
I_{ILRF}	Input low current for $\overline{RFSH}$	V_{IN} = 0.4 V, V_{CC} = MAX			-80	-500	μA
V_{IL}	Input low threshold (Note 1)					0.8	V
V_{IH}	Input high threshold (Note 1)			2.0			V
V_{OL1}	Output low voltage	I_{OUT} = 1 mA, V_{CC} = MIN				0.5	V
V_{OL2}	Output low voltage	I_{OUT} = 12 mA, V_{CC} = MIN				0.8	V
V_{OH}	Output high voltage	I_{OUT} = -1 mA, V_{CC} = MIN		2.4	3.0		V
I_{OH}	Output source current (Note 2)	V_{OUT} = 0.8 V, V_{CC} = MIN		-50	-140		mA
I_{OL}	Output sink current (Note 2)	V_{OUT} = 2.4 V, V_{CC} = MIN		40	100		mA
I_{OZ}	Three-state output current (address output)	0.4 V ≤ V_{OUT} ≤ 2.7 V V_{CC} = MAX, Chip deselect		-50		50	μA
I_{CC}	Supply current	V_{CC} = MAX			170	260	mA
C_{IN}	Input capacitance	T_A = 25°C			10		pF

9

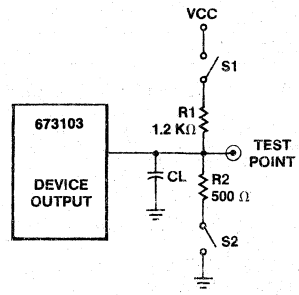
Switching Characteristics (See Note 3)

SYMBOL	EXTERNALLY CONTROLLED ACCESS PARAMETER	FIGURE/ NUMBER	673103A MIN	673103A MAX	673103 MIN	673103 MAX	UNIT
t_{RHA}	Row addresses remaining valid from R/$\overline{C}$ LOW	5/3	0		0		ns
t_{RPDL}	$\overline{RASIN}$ to $\overline{RAS}$ LOW delay	3/11		20		20	ns
t_{RPDH}	$\overline{RASIN}$ to $\overline{RAS}$ HIGH delay	3/12		31		31	ns
t_{APD}	Address input to output delay	9/2		50		50	ns
t_{WPDL}	$\overline{WEIN}$ to $\overline{WE}$ LOW delay			45		45	ns
t_{WPDH}	$\overline{WEIN}$ to $\overline{WE}$ HIGH delay			40		40	ns
t_{CPDL}	$\overline{CASIN}$ to $\overline{CAS}$ LOW delay	4/3		28		28	ns
t_{CPDH}	$\overline{CASIN}$ to $\overline{CAS}$ HIGH delay	4/4		40		40	ns
t_{RCC}	Column select to column address valid	5/5		41		41	ns
t_{RCR}	Row select to row address valid	5/6		45		45	ns
t_{d1}	($\overline{CASIN}$ to $\overline{CAS}$ LOW delay)-($\overline{RASIN}$ to $\overline{RAS}$ LOW delay)		-2	13	-2	13	ns
t_{d2}	(Address input to output delay)-($\overline{RASIN}$ to $\overline{RAS}$ LOW delay)			30		30	ns
t_{d3}	(Address input to output delay)-($\overline{CASIN}$ to $\overline{CAS}$ LOW delay)		-5	23	-5	23	ns
t_{d4}	Skew between address output lines			10		10	ns
t_{d5}	($\overline{RASIN}$ to $\overline{RAS}$ HIGH delay)-($\overline{RASIN}$ to $\overline{RAS}$ LOW delay)		-7	13	-7	13	ns
t_{d6}	($\overline{CASIN}$ to $\overline{CAS}$ HIGH delay)-($\overline{CASIN}$ to $\overline{CAS}$ LOW delay)		-12	12	-12	12	ns
t_{SPD}	ADS HIGH to address output valid	9/1		55		55	ns
t_{RCHC}	Column addresses remaining valid from R/$\overline{C}$ HIGH	5/4	0		0		ns
t_{d7}	t_{RPDL} - t_{RHA}			13		13	ns
t_{d8}	t_{RCC} - t_{CPDL}			20		20	ns



Change in Propagation Delays vs. Change in Loading Capacitance Relative to the Specified Load

673103 Test Loads (See Note)



Note: Input pulse 0 V to 3.0 V, $t_R = t_F = 2.5$ ns, f = 1 MHz, $t_{PW} = 200$ ns
Input reference point on AC measurements is 1.5 V.
Output reference points are 2.4 V for HIGH and 0.8 V for LOW.

Address Outputs

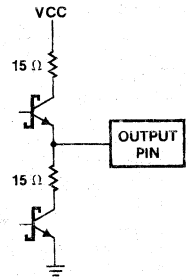
TEST	S1	S2	CL	MEASURED AT
t_{PD}	Open	Closed	500 pF	0.8 V, 2.4 V
t_{PZH}	Closed	Closed	500 pF	2.4 V
t_{PHZ}	Open	Closed	15 pF	V_{OH} -0.5 V
t_{PZL}	Closed	Closed	500 pF	0.8 V
t_{PLZ}	Closed	Open	15 pF	V_{OL} +0.5 V

Control Outputs

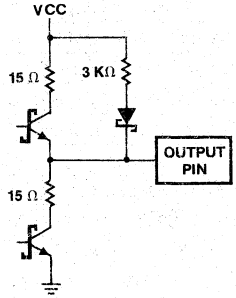
TEST	S1	S2	CL	MEASURED AT
t_{PD}	Open	Closed	CL	0.8 V, 2.4 V
t_{PZH}	Open	Closed	CL	2.4 V
t_{PHZ}	Open	Closed	15 pF	V_{OH} -0.5 V
t_{PZL}	Open	Open	CL	0.8 V
t_{PLZ}	Open	Open	15 pF	V_{OL} +0.5 V

Where C_L = 150 pF for $\overline{RAS}$, 300 pF for $\overline{CAS}$, and 500 pF for $\overline{WE}$.

Address Driver Output Stage



Control Driver Output Stage



Applications

Microprocessor Interface

The 673103 Dynamic RAM controller provides the address and control signals required to access and refresh dynamic RAMs. When interfaced to a 16-bit microprocessor, some external logic is required to generate a refresh clock as well as to perform access/refresh arbitration and interface handshake functions. Two PAL® devices may be used to perform these functions, as shown in Figure 1. One PAL device is used to generate the refresh clock, while the other performs all arbitration and handshake functions. A hidden refresh (refresh which is transparent to the system) scheme is implemented in the interface PAL device which takes advantage of "free" system time to refresh the memory, and falls back to "forced" refresh when hidden refresh cannot be performed.

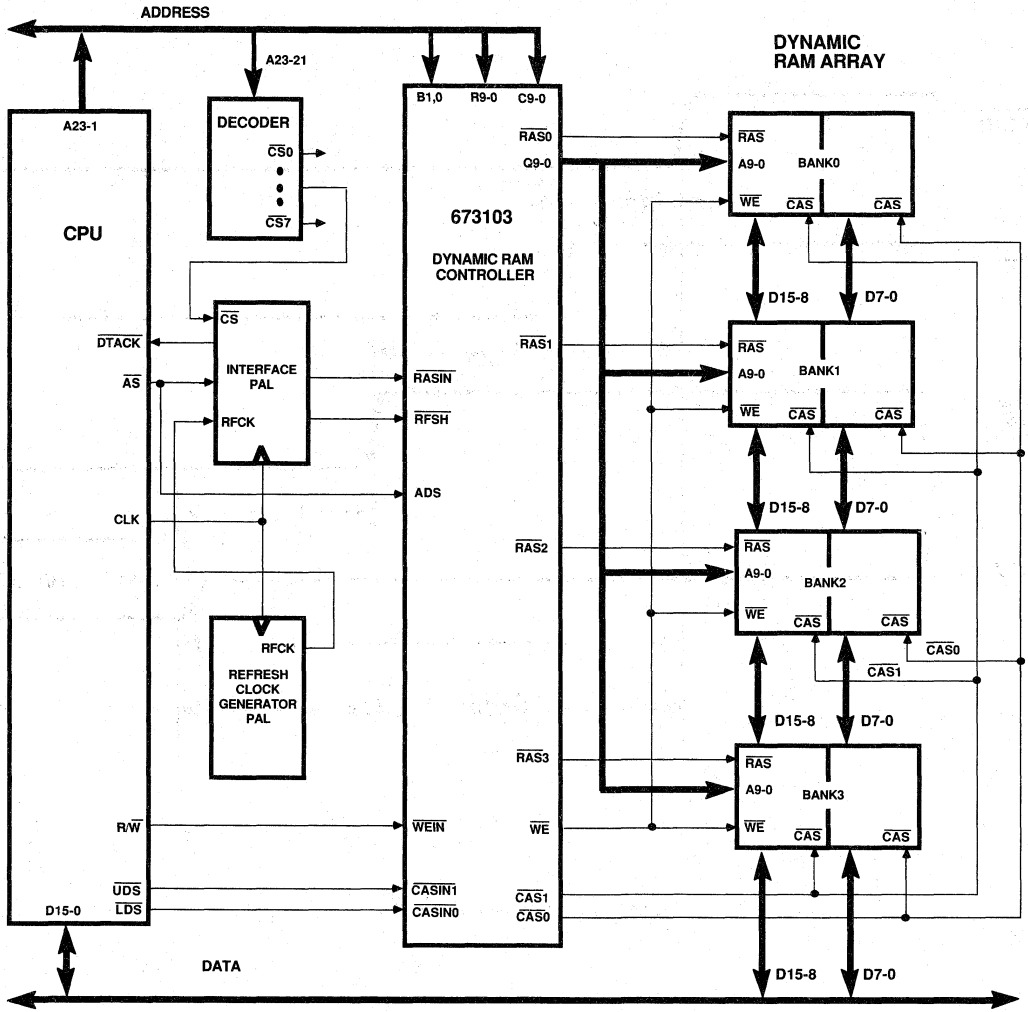


Figure 1. A CPU Interfaced to the 673103 Driving 8 M Bytes of Dynamic Memory

Determining System Performance (Auto-Access)

When determining system performance the dynamic RAM parameters must be considered as well as the controller's propagation delays. For both read and write cycles the access time for the dynamic RAM is t_{RAC} (Data access time from $\overline{RAS}$ going LOW) or t_{CAC} (Data access time from $\overline{CAS}$ going LOW), whichever results in the later appearance of data at the Dynamic RAM output. Since the $\overline{RAS}$ and $\overline{CAS}$ coming out of the controller are initiated by the $\overline{RASIN}$, the controller-memory performance is measured from the $\overline{RASIN}$ HIGH-to-LOW transition (see Figure 2).

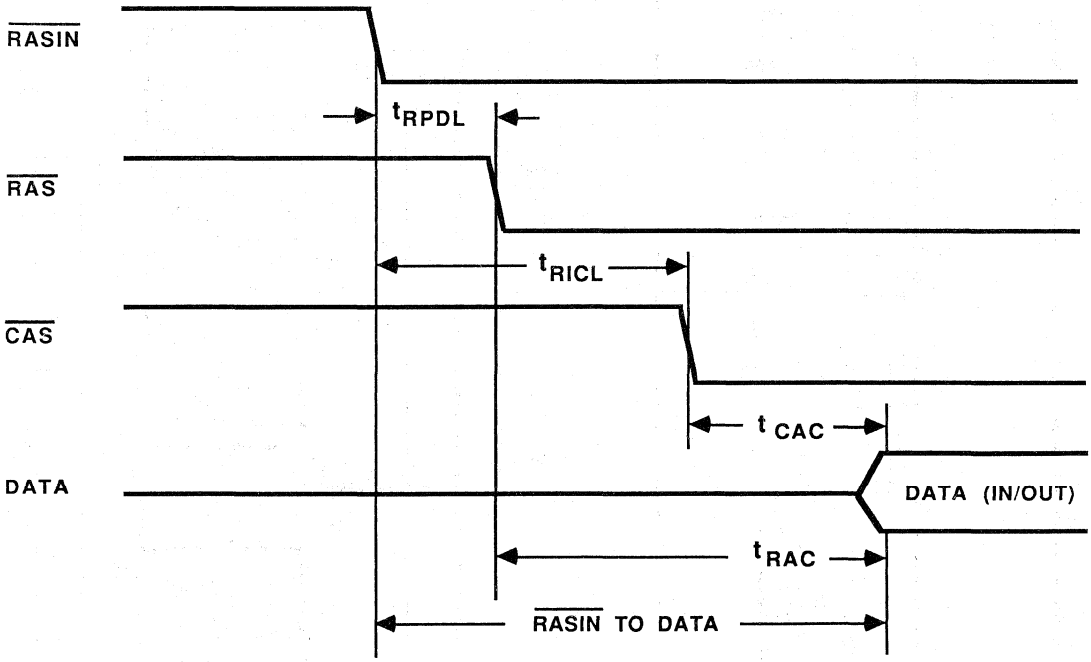


Figure 2. Access Time from $\overline{RASIN}$

The time from $\overline{\text{RASIN}}$ to data is calculated to be the longer of:

$t_{RICL} + t_{CAC}$ ($\overline{\text{RASIN}}$ to $\overline{\text{CAS}}$ + $\overline{\text{CAS}}$ to data)

$t_{RPDL} + t_{RAC}$ ($\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ + $\overline{\text{RAS}}$ to data)

Table 1 illustrates the access times from $\overline{\text{RASIN}}$ achieved for various dynamic RAM speeds.

CONTROLLER/MEMORY	PARAMETER				
	t_{RAC}	t_{RPDL}	t_{CAC}	t_{RICL}	ACCESS TIME FROM $\overline{\text{RASIN}}$
673103/HM256-12	120	20	60	85	145
673103A/HM256-12	120	20	60	75	140
673103/HM256-15	150	20	75	85	170
673103A/HM256-15	150	20	75	75	170
673103/MB8265A-10	100	20	50	85	135
673103A/MB8265A-10	100	20	50	75	125
673103/MB8265A-12	120	20	60	85	145
673103A/MB8265A-12	120	20	60	75	140
673103/IMS2620-10	100	20	60	85	145
673103A/IMS2620-10	100	20	60	75	135
673103/IMS2620-12	120	20	70	85	155
673103A/IMS2620-12	120	20	70	75	145

Table 1. Access Times from $\overline{\text{RASIN}}$ for Various Memory Speeds

673103 Parameters

t_{RPDL} — $\overline{\text{RASIN}}$ LOW to $\overline{\text{RAS}}$ LOW delay

t_{RICL} — $\overline{\text{RASIN}}$ TO $\overline{\text{CAS}}$ LOW delay

DRAM Parameters

t_{RAC} — Access time from $\overline{\text{RAS}}$ LOW

t_{CAC} — Access time from $\overline{\text{CAS}}$ LOW

Using the Externally Controlled Access

In the Externally Controlled Access mode $\overline{RASIN}$ controls the selected $\overline{RAS}$ output, $\overline{CASIN}$0-1 control $\overline{CAS}$0-1 outputs respectively and R/$\overline{C}$ controls the address multiplexer. The system designer may create, using the $\overline{RASIN}$, $\overline{CASIN}$ and R/$\overline{C}$ inputs, the required control signal sequence for the specific system being designed. Special dynamic RAM access modes such as Nibble mode and Page mode access cycles may be performed simply by toggling the appropriate control inputs. Special skew timing specifications have been specified to allow tighter timing control as outlined in the following examples. Both following examples relate to the scheme depicted in Figure 3.

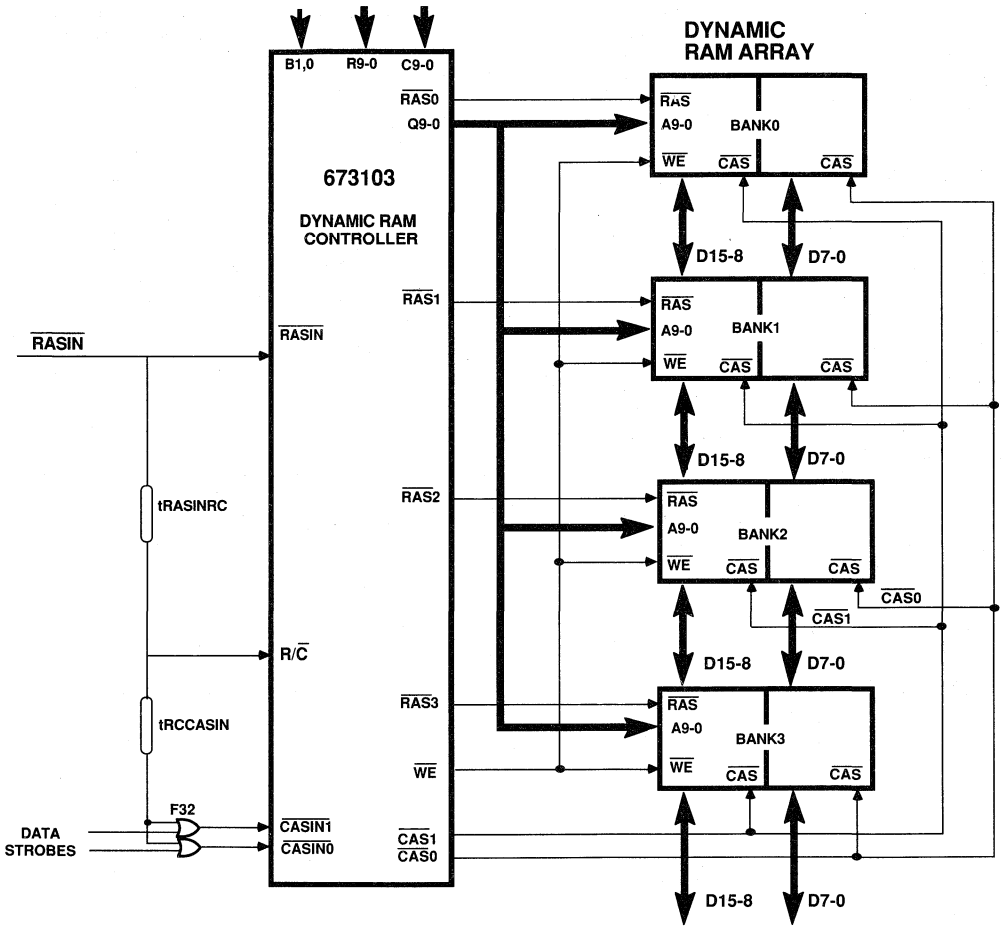


Figure 3. The 673103 in the Externally-Controlled Access Mode

Externally Controlled Access (ECA)
(Continued)

Example 1: Computing $\overline{RASIN}$ to R/$\overline{C}$ Delay

The delay between $\overline{RASIN}$ going LOW to R/$\overline{C}$ going LOW ($t_{RASINRC}$) which is required in order to satisfy the dynamic RAMs' row address hold time (t_{RAH}) is computed as follows:

$t_{RASINRC} = t_{RAH}(min) + t_{d7}$

Where:

$t_{RAH}(min)$ — Row address hold time (dynamic RAM parameter)

$t_{d7}(max) = t_{RPDL} - t_{RHA}$

t_{RPDL} — $\overline{RASIN}$ to $\overline{RAS}$ LOW delay

t_{RHA} — Row address held valid from R/$\overline{C}$ LOW

Example 2: Computing R/$\overline{C}$ to $\overline{CASIN}$ Delay

The delay between R/$\overline{C}$ going LOW to going $\overline{CASIN}$ LOW ($t_{RCCASIN}$) which is required in order to satisfy the dynamic RAMs' column address setup (t_{ASC}) is computed as follows:

$t_{RCCASIN} = t_{ASC}(min) + t_{d8} + t_{PD}F32(max)$

Where:

$t_{ASC}(min)$ — Column address setup (dynamic RAM parameter)

$t_{d8}(max) = t_{RCC} - t_{CPDL}$

t_{RCC} — R/C low to column address valid

t_{CPDL} — $\overline{CASIN}$ to $\overline{CAS}$ LOW delay

$t_{PD}F32(max)$ — Propagation delay of the OR gate used to validate $\overline{CASIN}$

Better system performance may be achieved using the t_{d7}, t_{d8} switching parameters to calculate $t_{RASINRC}$ and $t_{RCCASIN}$ than when using the t_{RPDL}, t_{RCDL}, t_{RCC} and t_{RHA} parameters (see t_{d7}, t_{d8} in Externally Controlled Access switching parameters).

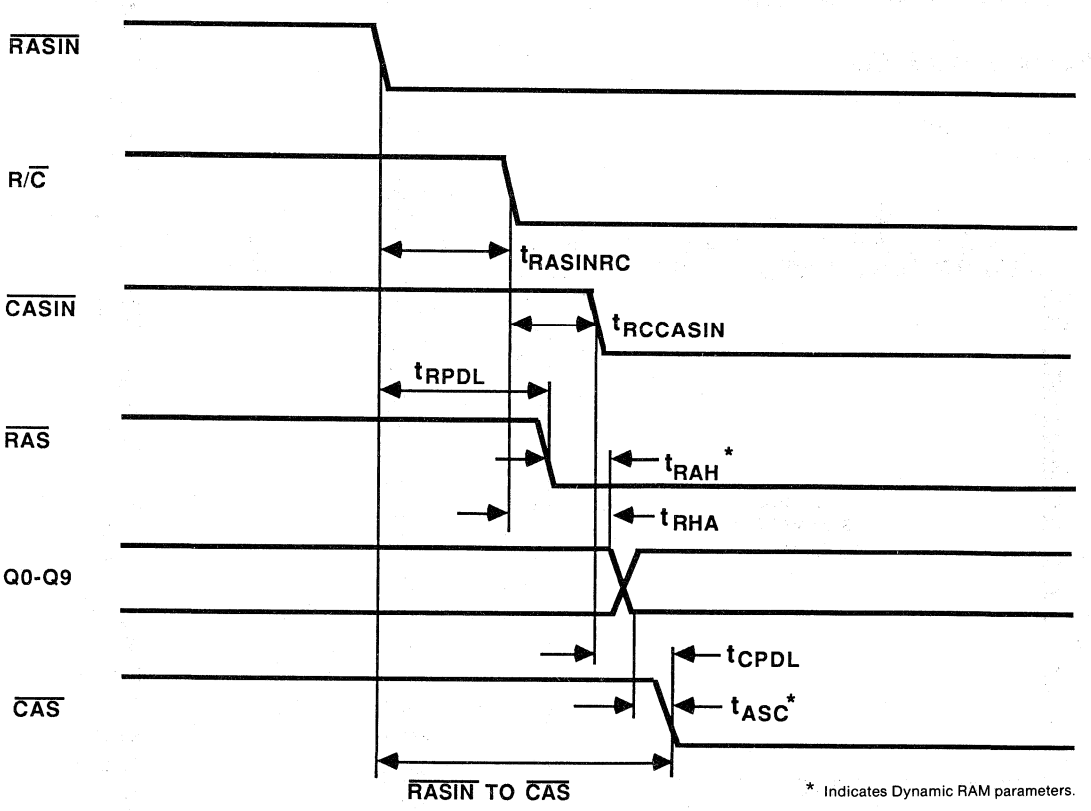


Figure 4. Externally Controlled Access Timing

1-Megabit Dynamic RAM Controller/Driver

673104
673104A

Features/Benefits

- Supports up to 1 M DRAMs
- Capable of addressing up to 16 M bytes
- On-chip capacitive-load drivers capable of driving up to 88 DRAMs with 30-nsec typical address propagation delay and 128 DRAMs with 35-nsec typical address propagation delay
- $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ delay of 23 nsec max ($\overline{\text{RAS}}$ driving 32 DRAMs)
- Max and Min skews are specified to simplify system design
- Four $\overline{\text{CASIN}}$ inputs and four $\overline{\text{CAS}}$ outputs simplify byte addressing
- An Auto-Access mode with extended $\overline{\text{CAS}}$ capability takes advantage of full performance of 120- and 150-nsec DRAMs
- An output series resistor reduces undershoot

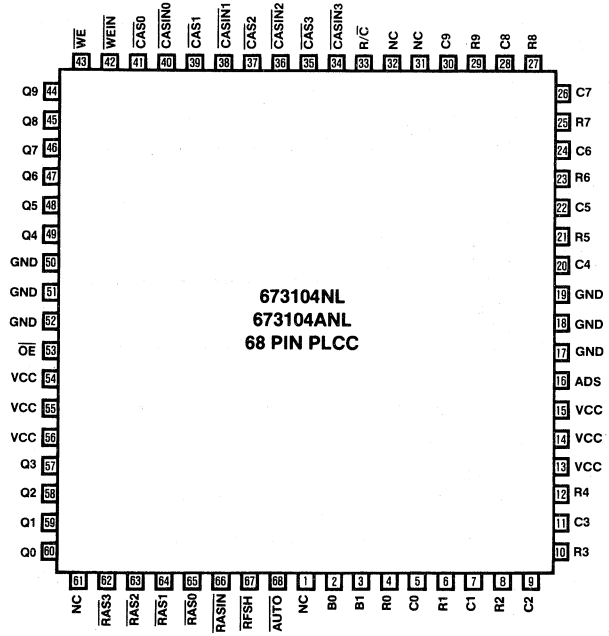
Modes of Operation

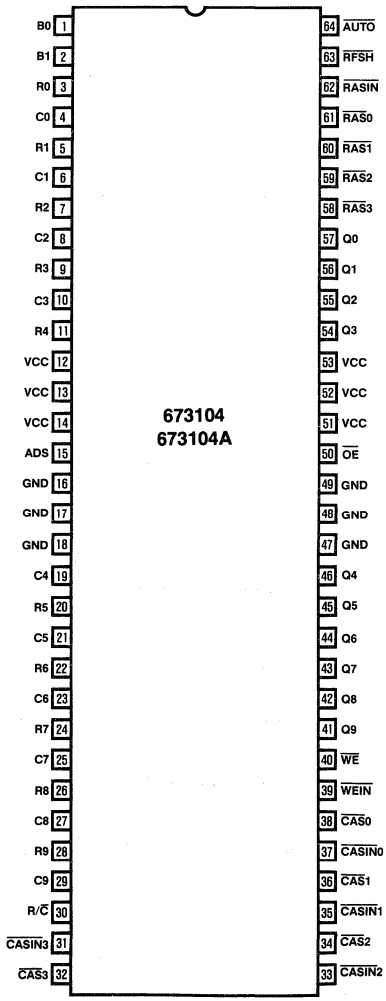
- Externally Controlled Access (ECA)
- Auto Access (AA)
- Refresh

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
673104	64D, 68NL, 68NP	Com
673104A		

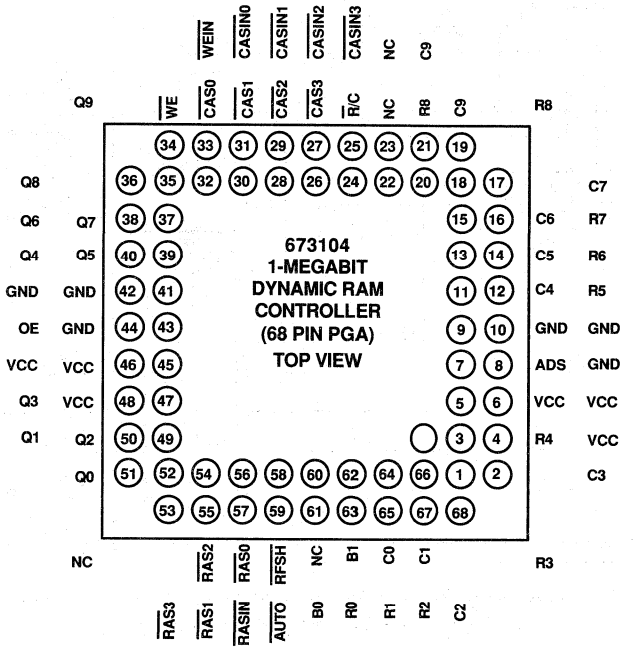
Pin Configurations





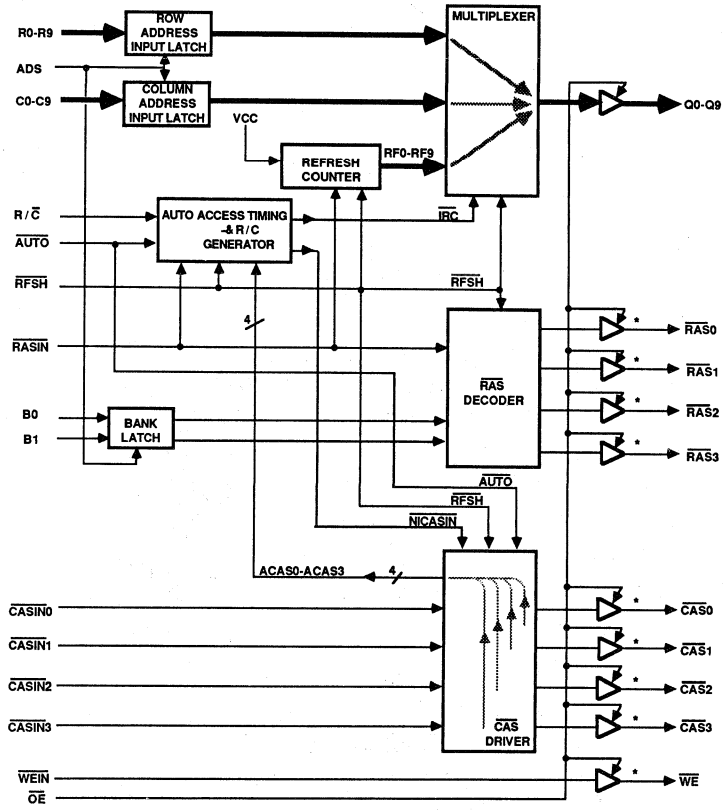
PAL® is a registered trademark of Monolithic Memories.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories


673104
1-MEGABIT
DYNAMIC RAM
CONTROLLER
(68 PIN PGA)
TOP VIEW
WEIN
CASIN0
CASIN1
CASIN2
CASIN3
NC
C9
Q9
WE
CAS0
CAS1
CAS2
CAS3
R/C
NC
R8
C9
R8
Q8
C7
Q6
Q7
C6
R7
Q4
Q5
C5
R6
GND
GND
C4
R5
OE
GND
GND
GND
VCC
VCC
ADS
GND
Q3
VCC
VCC
VCC
Q1
Q2
R4
VCC
Q0
C3
NC
R3
RAS3
RAS1
RASIN
AUTO
B0
R0
R1
R2
C2
RAS2
RAS0
RFSH
NC
B1
C0
C1

9

Block Diagram



* Indicates that there is a 3-KΩ pull-up resistor on these outputs when they are disabled

Figure 1. 673104 Functional Block Diagram

Description

The 673104 is an LSI device, provided in 64-pin and 68-pin packages, which performs most of the functions needed to control and address Dynamic RAMs. Twenty-two address inputs, ten address outputs, four $\overline{RAS}$ outputs, and four $\overline{CASIN}$-$\overline{CAS}$ input-output pairs allow the 673104 to directly address 16 M bytes. The four $\overline{CASIN}$n inputs and the four $\overline{CAS}$n outputs simplify individual byte access in 32-bit wide memory arrays (see Figure 2).

The 673104 has three operating modes:

- Externally Controlled Access (ECA)
- Auto Access (AA)
- Refresh (RFSH).

The Externally-Controlled-Access mode gives the system direct control over the $\overline{RAS}$m outputs, the $\overline{CAS}$n outputs, and Row/Column multiplexing. It also supports PAGE mode access, NIBBLE mode access and static column mode access.

The Auto-Access mode provides on-chip delays that automatically control the timing delays between $\overline{RAS}$m signals, address multiplexing, and $\overline{CAS}$n signals. In the Auto-Access mode $\overline{CASIN}$0-3 inputs serve as enables for the respective $\overline{CAS}$0-3 outputs, allowing the access of any byte of the memory array (for 32-bit wide memory arrays organized in four bytes). In this mode $\overline{CAS}$0-3 outputs go HIGH only when the respective $\overline{CASIN}$0-3 inputs go HIGH, and the address switches back to row address only when $\overline{CASIN}$0-3 go HIGH. This feature allows extension of the $\overline{CAS}$ LOW time and column address time while $\overline{RASIN}$ and $\overline{RAS}$m can go HIGH to satisfy the precharge requirements of the dynamic RAMs.

When the Refresh mode is selected ($\overline{RFSH}$ is LOW) an on-chip refresh counter provides the refresh address; with $\overline{AUTO}$ HIGH and R/$\overline{C}$ LOW the column address is forced onto the address output multiplexer, facilitating an access of a particular memory location while refreshing a row. This feature may be useful when implementing error detection and correction scrubbing.

The 673104 can drive sixteen banks of DRAMs. $\overline{RAS}$m control signals are used to select four banks, while leaving the other twelve banks in standby. The four $\overline{CAS}$n outputs enable the selection of one bank out of four. The address lines and the $\overline{WE}$ signal can be connected to all sixteen banks. In a 32-bit wide, byte-oriented, memory array the $\overline{RAS}$m signals select one out of four banks while the $\overline{CAS}$n signals select the bytes, as shown in Figure 2.

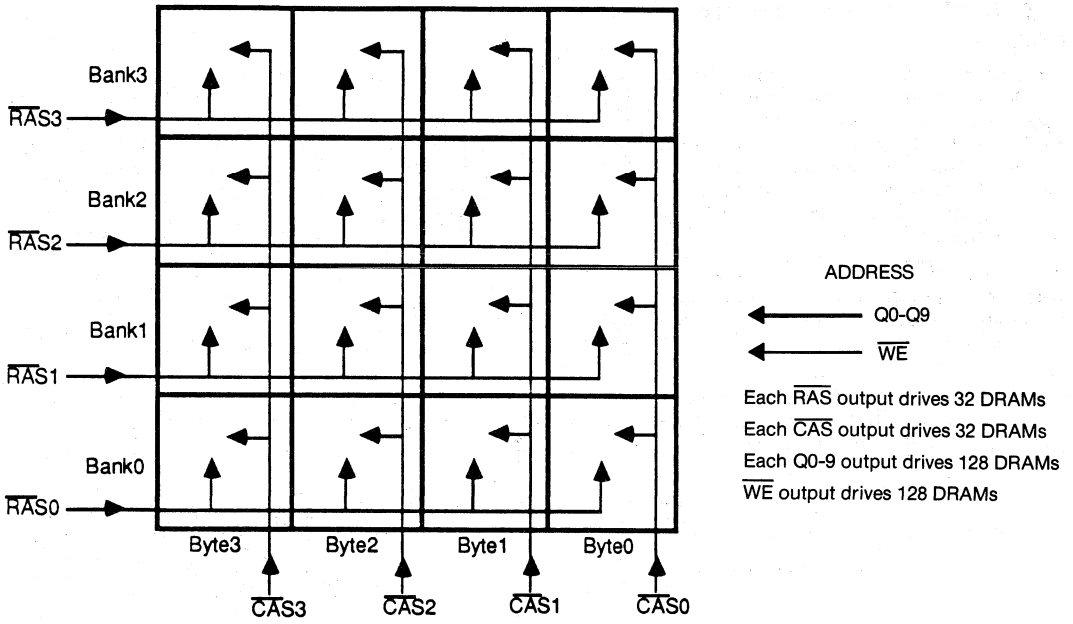


Figure 2. 673104 Addressing Four Banks of 32-bit Memory Array Organized in Four Bytes

Pin Definitions

VCC, GND: VCC-GND = 5 V ±10%. The supply pins have been assigned to the center of the package to reduce voltage drops, both DC and AC. A low inductance connection between the ground pin and a solid ground plane will minimize fluctuations in the ground level of the device that may occur when the address outputs switch from HIGH to LOW simultaneously. A 1-μF multilayer ceramic capacitor in parallel with a low voltage tantalum capacitor, both connected close to the VCC and GND pins, will properly decouple the device.

R0-R9: Row Address Inputs

C0-C9: Column Address Inputs

B0-B1: Bank-Pair Select Inputs — Strobed by ADS. Decoded to enable one of the $\overline{RAS}$ outputs when $\overline{RASIN}$ goes LOW in the access modes.

Q0-Q9: Multiplexed Address Outputs — Selected from the row address input latch, the column address input latch, or the refresh counter.

$\overline{RASIN}$: Row Address Strobe Input — Drives the selected $\overline{RAS}$m output in the access modes and all $\overline{RAS}$ outputs in the Refresh mode.

ADS: Address (Latch) Strobe Input — Strobes input row address, column address, and Bank Select inputs into the respective latches when HIGH; latches on HIGH-to-LOW transition.

$\overline{OE}$: Output Enable — When $\overline{OE}$ is LOW the address and control outputs are enabled. When $\overline{OE}$ is HIGH the address outputs are in high-impedance and the control outputs are pulled HIGH.

R/$\overline{C}$: Row/Column Select Input — In the Externally-Controlled-Access, it is used to select either the row address input latch or the column address input latch onto the address outputs. In the Refresh mode, when $\overline{AUTO}$ is HIGH, it is used to select between the refresh address (R/$\overline{C}$ HIGH) and the column address (R/$\overline{C}$ LOW). When $\overline{AUTO}$ is LOW R/$\overline{C}$ is disabled.

$\overline{CASIN}$0-3: Column Address Strobe Inputs — In the Externally-Controlled-Access mode the $\overline{CASIN}$n directly drives $\overline{CAS}$n output. In the Auto-Access mode, it is used to enable the corresponding $\overline{CAS}$n output (See $\overline{CAS}$0-3 description).

$\overline{WEIN}$: Write Enable Input.

$\overline{WE}$: Write Enable Output.

$\overline{CAS}$0-3: Column Address Strobe Outputs — In the Externally-Controlled-Access mode the $\overline{CAS}$ outputs follow the $\overline{CASIN}$ inputs. In the Auto-Access mode the $\overline{CASIN}$ inputs are used to enable the $\overline{CAS}$ outputs, but the $\overline{CAS}$ outputs are asserted LOW, with proper delay from the $\overline{RAS}$ output, by the $\overline{RASIN}$ signal via the Auto-Access timing generator. In the Auto-Access mode, the $\overline{CAS}$n goes HIGH only when the corresponding $\overline{CASIN}$n goes HIGH. Extending the $\overline{CAS}$n LOW duration while $\overline{RASIN}$ and $\overline{RAS}$m go HIGH satisfies the precharge requirement of the dynamic RAMs.

$\overline{RAS}$0-3: Row Address Strobe Outputs — When $\overline{RFSH}$ is HIGH the selected row address strobe output (decoded from signals B0, B1) follows the $\overline{RASIN}$ input. When $\overline{RFSH}$ is LOW all $\overline{RAS}$ outputs go LOW together following $\overline{RASIN}$ going LOW.

$\overline{AUTO}$: Auto-Access Input — When $\overline{AUTO}$ is LOW the Auto-Access mode is selected (see Auto-Access mode description).

$\overline{RFSH}$: Refresh Input — When $\overline{RFSH}$ is LOW the Refresh mode is selected (see Refresh mode description).

Externally-Controlled-Access Mode (ECA)

In this mode, selected when $\overline{AUTO}$ and $\overline{RFSH}$ are held HIGH, the 673104 serves as a straightforward multiplexer and driver for the address and control signals to the DRAMs. The $\overline{RAS}$m output selected by the B0 and B1 inputs follows the $\overline{RASIN}$ input, and each of the $\overline{CAS}$ outputs follows its corresponding $\overline{CASIN}$ input. When R/$\overline{C}$ is HIGH the row address is enabled onto the Q0-9 outputs. When R/$\overline{C}$ is LOW the column address latch is enabled onto Q0-9 outputs.

The $\overline{RASIN}$ — $\overline{RAS}$, $\overline{CASIN}$ — $\overline{CAS}$, and R/$\overline{C}$ — Q0-9 control paths are independent to allow the system designer maximum flexibility and support of special DRAM access and refresh modes such as NIBBLE mode, PAGE mode, $\overline{CAS}$ before $\overline{RAS}$, etc.

To allow tighter timing of the sequence of control signals to the Dynamic RAM, several difference timing parameters have been specified for the Externally Controlled Access mode. These parameters specify the maximum difference between the various "control channels" of the device. In particular, using switching characteristics t_{d7} and t_{d8} is very useful when designing the delay from $\overline{RASIN}$ going LOW to R/$\overline{C}$ and the delay between R/$\overline{C}$ going LOW to $\overline{CASIN}$ going LOW (see Applications).

BANK SELECT (STROBED BY ADS)		ENABLED $\overline{RAS}$n
B1	B0	
0	0	$\overline{RAS}$0
0	1	$\overline{RAS}$1
1	0	$\overline{RAS}$2
1	1	$\overline{RAS}$3

Table 1. Memory Bank Decode

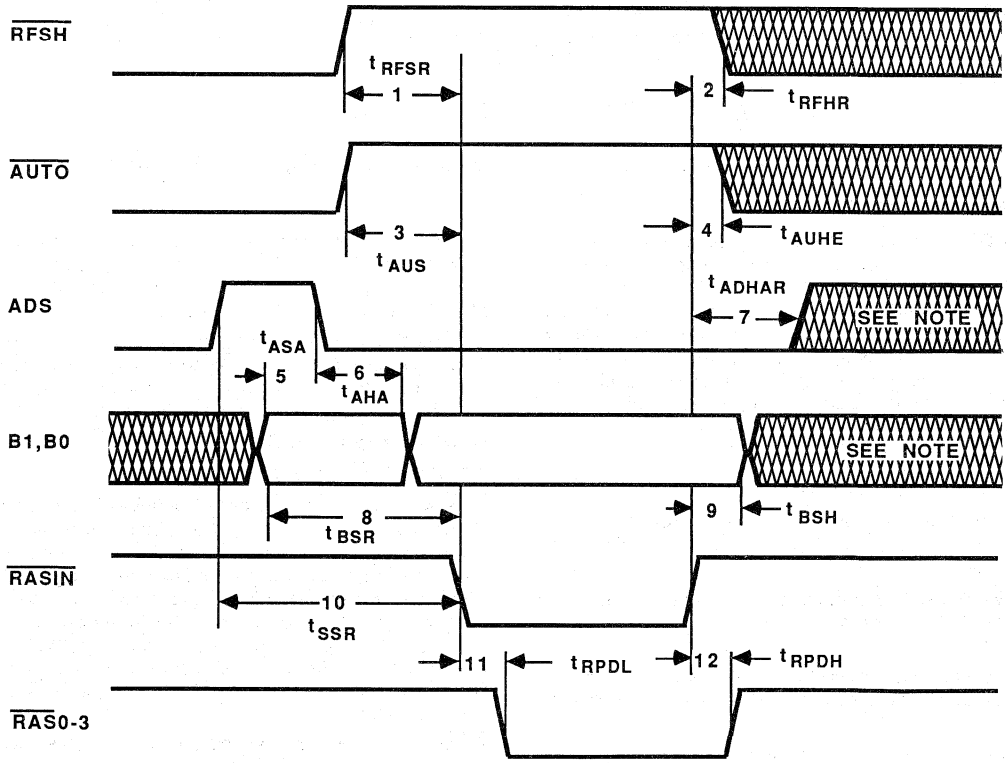


Figure 3. Externally-Controlled-Access—$\overline{RASIN}$-to-$\overline{RAS}$ Timing

Note: To prevent glitches on the $\overline{RAS}$0-3 outputs, operating conditions t_{BSH} or t_{ADHAR} must be satisfied.

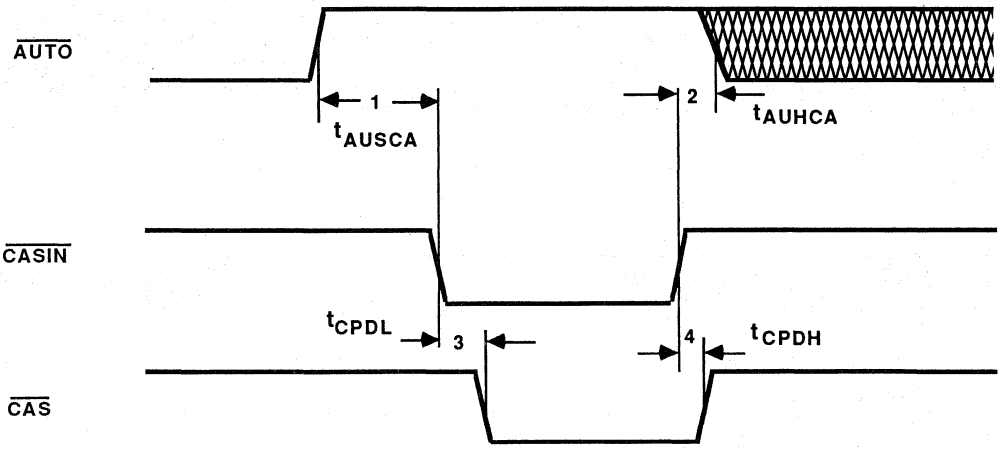


Figure 4. Externally-Controlled-Access-$\overline{\text{CASIN}}$ to $\overline{\text{CAS}}$ Timing

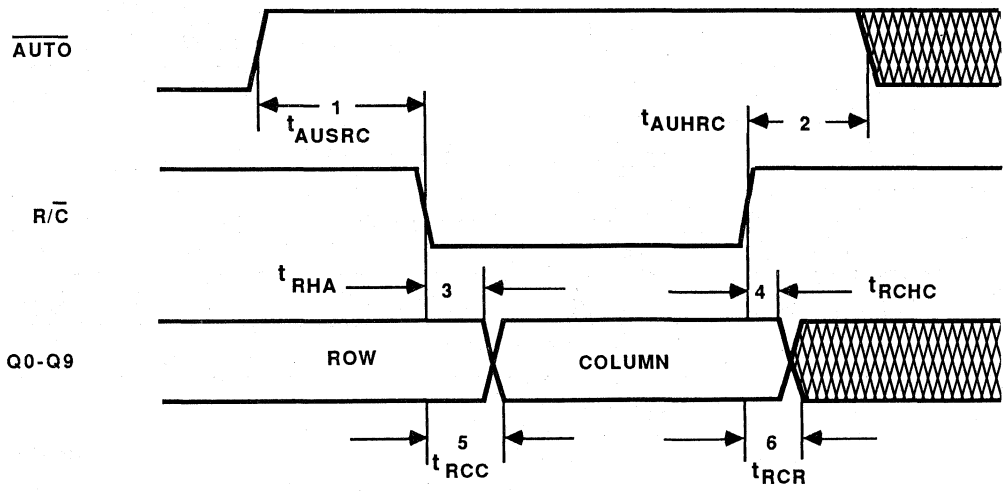


Figure 5. Externally-Controlled-Access R/$\overline{\text{C}}$ Timing

Note: t_{RCC} will be met only if the column address is available t_{APD} before it appears on Q0-9 outputs or if it is latched by ADS.

Auto-Access Mode (AA)

In the Auto-Access mode the 673104 provides the system designer with built-in delays and sequencing to accommodate DRAMs with 150 nanoseconds and faster access time. The Auto-Access mode is selected when AUTO is held LOW and RFSH is held HIGH. The R/C input is disabled, and RASIN going LOW initiates the sequence of control signals to access the DRAMs. The CASIN0-3 inputs are used as enables for the respective CAS outputs. A LOW on a CASINn input enables the CASn output to be driven LOW with the internally generated delay from RAS. Each CASn output goes HIGH only when the corresponding CASINn input goes HIGH, and the address switches back to row address only when all CASIN go HIGH. This feature allows extension of the CAS LOW time and the column address time, while RASIN and RASm can go HIGH to satisfy precharge requirements of the dynamic RAMs. The R/C input is disabled in this mode.

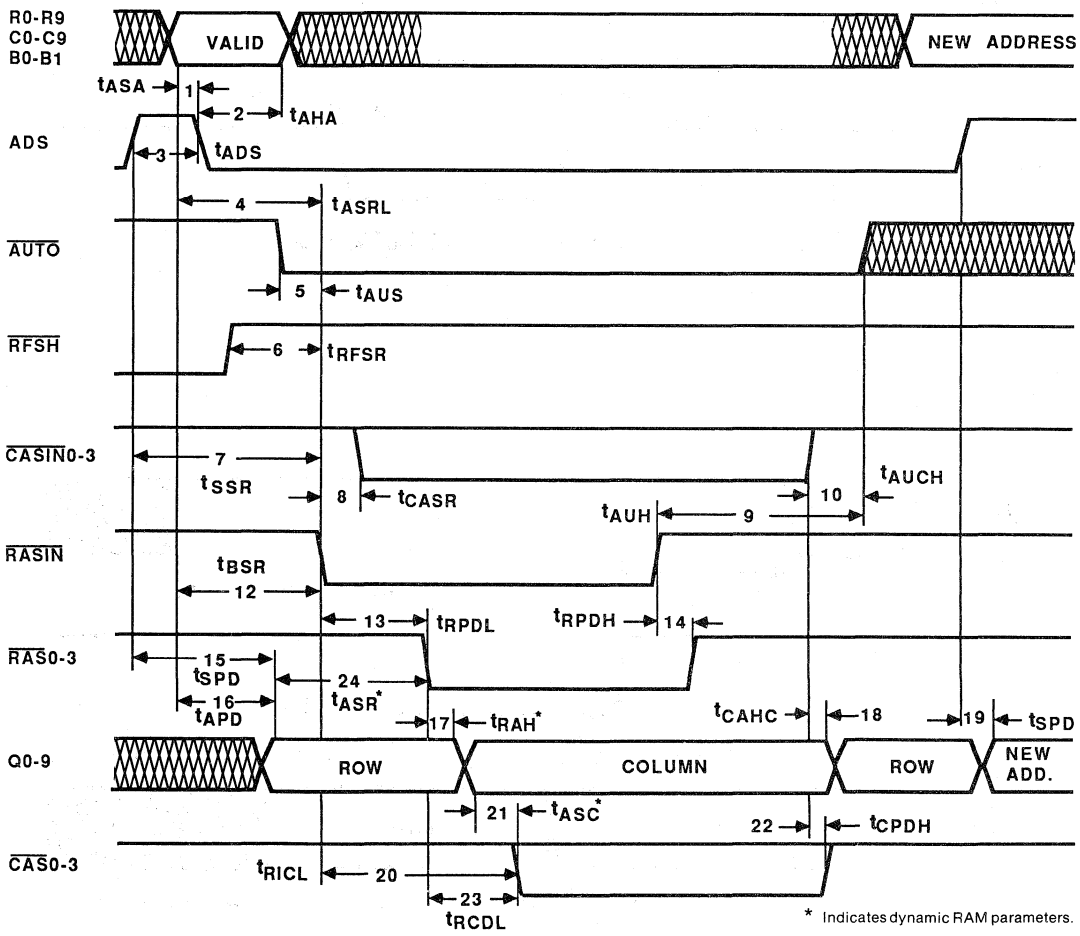


Figure 6. Auto-Access (AA) Timing

Refresh Mode (RFSH)

When $\overline{RFSH}$ is held LOW the refresh counter contents are enabled onto the Q0-9 address outputs, provided either R/$\overline{C}$ is held HIGH, or $\overline{AUTO}$ is held LOW, or both conditions exist. In this mode all four $\overline{RAS}$ outputs follow the $\overline{RASIN}$ input signal. The refresh counter increments the refresh address when either $\overline{RASIN}$ or $\overline{RFSH}$ goes HIGH while the other is LOW. When $\overline{AUTO}$ is LOW the $\overline{CASIN}$0-3 inputs are isolated and $\overline{CAS}$0-3 are held HIGH. Also, when $\overline{AUTO}$ is LOW the R/$\overline{C}$ input is isolated from the output multiplexer, and the refresh address appears at the Q0-9 outputs.

When $\overline{AUTO}$ is HIGH, pulling R/$\overline{C}$ LOW enables the column address onto the Q0-9 outputs. Also, each of the $\overline{CAS}$ outputs follows its respective $\overline{CASIN}$ input. This feature may be used when implementing error correction and detection "scrubbing" for four-bank memory arrays. "Scrubbing" is a term describing a cyclic error correction of soft errors in the memory array, done within the refresh cycles. On every refresh cycle one location of the memory array is accessed and the data in that location goes, if necessary, through a correction cycle (a read-modify-write memory cycle). The 673104 provides the facilities to force a column address onto the Q0-9 address outputs and to assert the $\overline{CAS}$0-3 outputs within a refresh cycle to allow scrubbing. A column counter and a bank counter need to be added externally to provide the column addresses for scrubbing.

The refresh counter is a 10-bit counter that resets to 0 on power-up and rolls-over to 0 at 1023.

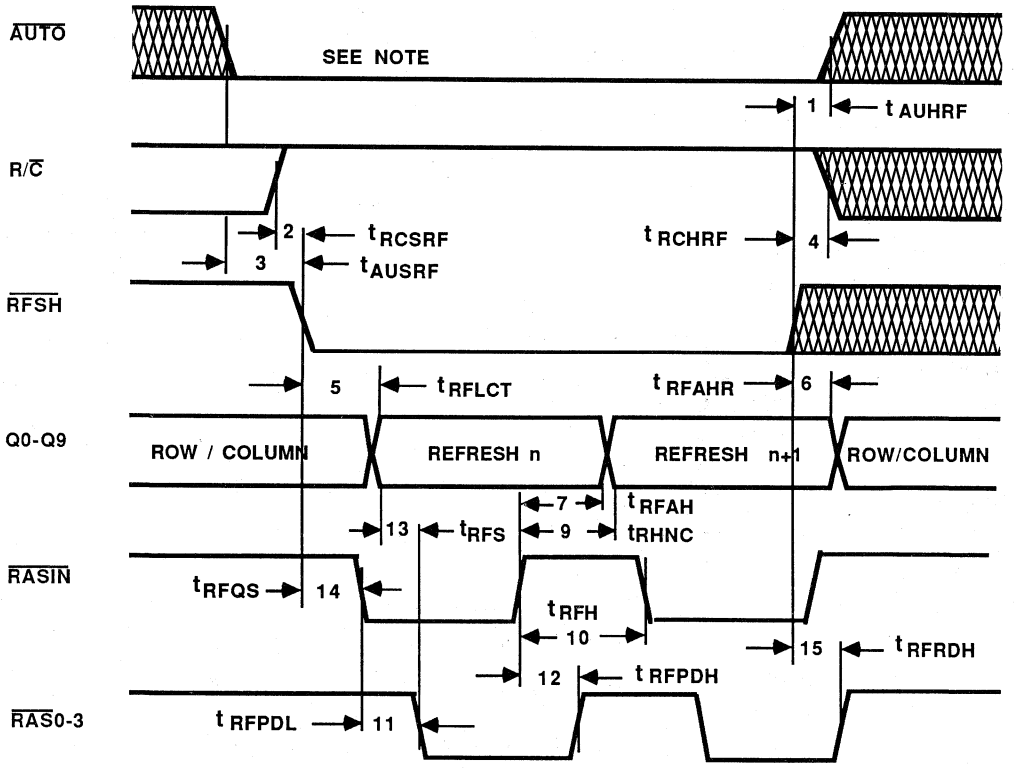


Figure 7. Refresh Timing

Note: In the REFRESH mode, $\overline{AUTO}$ must be LOW or R/$\overline{C}$ must be HIGH to guarantee the refresh address on the Q0-9 outputs.

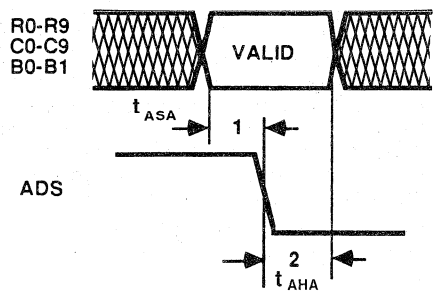


Figure 8. Address Setup and Hold Time to ADS

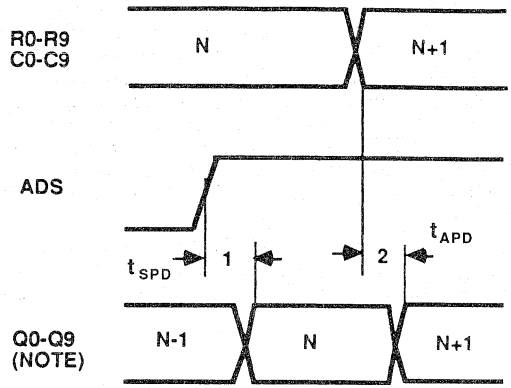


Figure 9. Address Input/Output Propagation Delay

Note: Row or Column address ($\overline{RFSH}$ = HIGH).

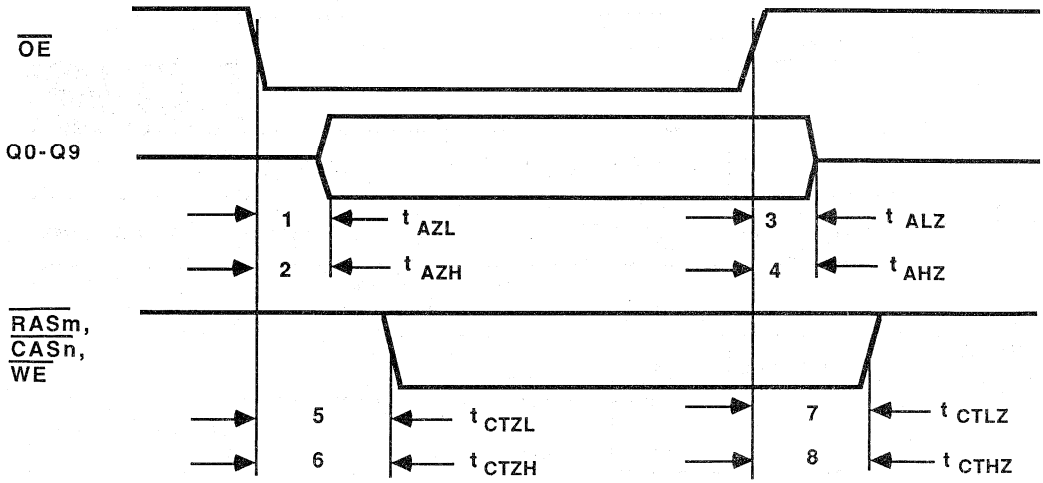


Figure 10. High-Z Timing

Absolute Maximum Ratings (See Note)

Supply voltage, V_{CC} ..... -0.5 V to 7 V
Storage temperature range ..... -65°C to +150°C
Input voltage ..... -1.5 V to 5.5 V
Output current ..... 150 mA
Lead temperature (soldering, 10 seconds) ..... 300°C

Note: "Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of operating conditions provides conditions for actual device operation.

Operating Conditions

SYMBOL	PARAMETER	FIGURE/ NUMBER	673104A MIN	673104A TYP	673104A MAX	673104 MIN	673104 TYP	673104 MAX	UNIT
V_{CC}	Supply voltage		4.5		5.5	4.5		5.5	V
T_A	Ambient temperature		0		75	0		75	C
t_{ASA}	Address setup time to ADS LOW	8/1	18			18			ns
t_{ADS}	Address strobe pulse width HIGH		26			26			ns
t_{AHA}	Address hold time from ADS LOW	8/2	10			10			ns
	EXTERNALLY CONTROLLED ACCESS PARAMETER								
t_{ADHAR}	ADS LOW hold from $\overline{RASIN}$ HIGH	3/7	0			0			ns
t_{BSR}	Bank select setup to $\overline{RASIN}$ LOW (ADS = HIGH)	3/8	10			10			ns
t_{BSH}	Bank select hold from $\overline{RASIN}$ HIGH (ADS = HIGH)	3/9	10			10			ns
t_{SSR}	Address strobe HIGH setup to $\overline{RASIN}$ LOW (B0, B1 STABLE)	3/10	20			20			ns
t_{AUHE}	$\overline{AUTO}$ hold from $\overline{RASIN}$ HIGH	3/4	55			55			ns
t_{AUSRC}	$\overline{AUTO}$ HIGH setup to R/$\overline{C}$ LOW	5/1	25			25			ns
t_{AUHRC}	$\overline{AUTO}$ HIGH hold from R/$\overline{C}$ HIGH	5/2	10			10			ns
t_{AUSCA}	$\overline{AUTO}$ HIGH setup to $\overline{CASIN}$ LOW	4/1	45			45			ns
t_{AUHCA}	$\overline{AUTO}$ HIGH hold from $\overline{CASIN}$ HIGH	4/2	0			0			ns
t_{AUS}	$\overline{AUTO}$ setup to $\overline{RASIN}$ LOW	3/3	0			0			ns
t_{RFSR}	$\overline{RFSH}$ HIGH setup to $\overline{RASIN}$ LOW (to guarantee t_{ASR} = 0)	3/1	10			10			ns
t_{RFHR}	$\overline{RFSH}$ HIGH hold from $\overline{RASIN}$ HIGH	3/2	10			10			ns
	AUTOMATIC ACCESS PARAMETER								
t_{ADHAR}	ADS LOW hold from $\overline{RASIN}$ HIGH	3/7	0			0			ns
t_{BSR}	Bank select setup to $\overline{RASIN}$ LOW (ADS = HIGH)	6/12	10			10			ns
t_{BSH}	Bank select hold from $\overline{RASIN}$ HIGH (ADS = HIGH)	3/9	10			10			ns
t_{ASRL}	Address setup to $\overline{RASIN}$ LOW (ADS = HIGH) (t_{ASRL} = t_{d2} max to guarantee t_{ASR} = 0)	6/4	34			34			ns
t_{AUS}	$\overline{AUTO}$ setup to $\overline{RASIN}$ LOW	6/5	0			0			ns
t_{RFSR}	$\overline{RFSH}$ HIGH setup to $\overline{RASIN}$ LOW (to guarantee t_{ASR} = 0)	6/6	10			10			ns
t_{SSR}	Address strobe HIGH to $\overline{RASIN}$ LOW (B0, B1 STABLE)	6/7	20			20			ns
t_{CASR}	$\overline{CASIN}$0-1 setup to $\overline{RASIN}$ LOW	6/8	-30			-30			ns
t_{AUH}	$\overline{AUTO}$ hold from $\overline{RASIN}$ HIGH	6/9	50			50			ns
t_{AUCH}	$\overline{AUTO}$ LOW hold from $\overline{CASIN}$ HIGH	6/10	0			0			ns
	REFRESH PARAMETER								
t_{AUHRF}	$\overline{AUTO}$ LOW hold from $\overline{RFSH}$ HIGH (R/$\overline{C}$ LOW)	7/1	10			10			ns
t_{RCSRF}	R/$\overline{C}$ HIGH setup to $\overline{RFSH}$ LOW ($\overline{AUTO}$ HIGH)	7/2	20			20			ns
t_{AUSRF}	$\overline{AUTO}$ LOW setup to $\overline{RFSH}$ LOW (R/$\overline{C}$ LOW)	7/3	20			20			ns
t_{RCHRF}	R/$\overline{C}$ HIGH hold from $\overline{RFSH}$ HIGH ($\overline{AUTO}$ HIGH)	7/4	10			10			ns
t_{RFH}	$\overline{RASIN}$ HIGH during refresh	7/10	30			30			ns
t_{RFQS}	$\overline{RFSH}$ LOW setup to $\overline{RASIN}$ LOW (to guarantee t_{RFS})	7/14	34			34			ns

Electrical Characteristics V_{CC} = 5 V ±10%, 0°C ≤ T_A ≤ 75°C. Typicals are for V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	FIGURE/ NUMBER	MIN	TYP	MAX	UNIT
V_{IC}	Input clamp voltage	I_{IN} = -18 mA, V_{CC} = MIN			-0.8	-1.2	V
I_{IH}	Input high current	V_{IN} = 2.7 V, V_{CC} = MAX				50	μA
I_{CTL}	Output load current for $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	V_{OUT} = 0.4 V, V_{CC} = MAX Chip deselect			-1.5	-2.5	mA
I_{IL}	Input low current except for $\overline{RFSH}$	V_{IN} = 0.4 V, V_{CC} = MAX			-20	-250	μA
I_{ILRF}	Input low current for RFSH	V_{IN} = 0.4 V, V_{CC} = MAX			-80	-500	μA
V_{IL}	Input low threshold (Note 1)					0.8	V
V_{IH}	Input high threshold (Note 1)			2.0			V
V_{OL1}	Output low voltage	I_{OUT} = 1 mA, V_{CC} = MIN				0.5	V
V_{OL2}	Output low voltage	I_{OUT} = 12 mA, V_{CC} = MIN				0.8	V
V_{OH}	Output high voltage	I_{OUT} = -1 mA, V_{CC} = MIN		2.4	3.0		V
I_{OH}	Output source current (Note 2)	V_{OUT} = 0.8 V, V_{CC} = MIN		-50	-140		mA
I_{OL}	Output sink current (Note 2)	V_{OUT} = 2.4 V, V_{CC} = MIN		40	100		mA
I_{OZ}	Three-state output current (address output)	0.4 V ≤ V_{OUT} ≤ 2.7 V V_{CC} = MAX, Chip deselect		-50		50	μA
I_{CC}	Supply current	V_{CC} = MAX			190	280	mA
C_{IN}	Input capacitance	T_A = 25°C			10		pF

Switching Characteristics (See Note 3)

SYMBOL	EXTERNALLY CONTROLLED ACCESS PARAMETER	FIGURE/ NUMBER	673104A MIN	673104A TYP	673104A MAX	673104 MIN	673104 TYP	673104 MAX	UNIT
t_{RHA}	Row addresses remaining valid from R/$\overline{C}$ LOW	5/3	0			0			ns
t_{RPDL}	$\overline{RASIN}$ to $\overline{RAS}$ LOW delay	3/11			23			23	ns
t_{RPDH}	$\overline{RASIN}$ to $\overline{RAS}$ HIGH delay	3/12			33			33	ns
t_{APD}	Address input to output delay	9/2			60			60	ns
t_{WPDL}	$\overline{WEIN}$ to $\overline{WE}$ LOW delay				50			50	ns
t_{WPDH}	$\overline{WEIN}$ to $\overline{WE}$ HIGH delay				45			45	ns
t_{CPDL}	$\overline{CASIN}$ to $\overline{CAS}$ LOW delay	4/3			28			28	ns
t_{CPDH}	$\overline{CASIN}$ to $\overline{CAS}$ HIGH delay	4/4			40			40	ns
t_{RCC}	Column select to column address valid	5/5			50			50	ns
t_{RCR}	Row select to row address valid	5/6			53			53	ns
t_{d1}	($\overline{CASIN}$ to $\overline{CAS}$ LOW delay)-($\overline{RASIN}$ to $\overline{RAS}$ LOW delay)		-5		10	-5		10	ns
t_{d2}	(Address input to output delay)-($\overline{RASIN}$ to $\overline{RAS}$ LOW delay)				34			34	ns
t_{d3}	(Address input to output delay)-($\overline{CASIN}$ to $\overline{CAS}$ LOW delay)		0		28	0		28	ns
t_{d4}	Skew between address output lines				12			12	ns
t_{d5}	($\overline{RASIN}$ to $\overline{RAS}$ HIGH delay)-($\overline{RASIN}$ to $\overline{RAS}$ LOW delay)		-10		10	-10		10	ns
t_{d6}	($\overline{CASIN}$ to $\overline{CAS}$ LOW delay)-($\overline{CASIN}$ to $\overline{CAS}$ HIGH delay)		-12		12	-12		12	ns
t_{SPD}	ADS HIGH to address output valid	9/1			64			64	ns
t_{RCHC}	Column addresses remaining valid from R/$\overline{C}$ HIGH	5/4	0			0			ns
t_{d7}	t_{RPDL} - t_{RHA}				16			16	ns
t_{d8}	t_{RCC} - t_{CPDL}				27			27	ns

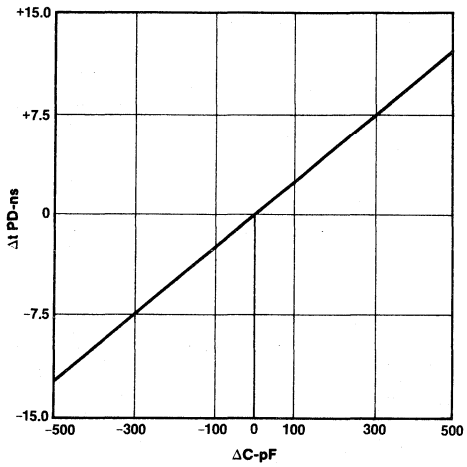
Switching Characteristics (Continued)

SYMBOL	AUTO ACCESS PARAMETER	FIGURE/ NUMBER	673104A MIN	673104A TYP	673104A MAX	673104 MIN	673104 TYP	673104 MAX	UNIT
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ LOW delay	6/20			83			90	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ LOW delay	6/23	30		73	30		80	ns
t_{RPDL}	$\overline{RASIN}$ to $\overline{RAS}$ LOW delay	6/13			23			23	ns
t_{RPDH}	$\overline{RASIN}$ to $\overline{RAS}$ HIGH delay	6/14			33			33	ns
t_{APD}	Address input to output delay	6/16			60			60	ns
t_{WPDL}	$\overline{WEIN}$ to $\overline{WE}$ LOW delay				50			50	ns
t_{WPDH}	$\overline{WEIN}$ to $\overline{WE}$ HIGH delay				45			45	ns
t_{CPDH}	$\overline{CASIN}$ to $\overline{CAS}$ HIGH delay	6/22			40			40	ns
t_{RAH}	Row address hold time from $\overline{RAS}$ LOW	6/17	15			15			ns
t_{d2}	(Address input to output delay)-($\overline{RASIN}$ to $\overline{RAS}$ LOW delay)				34			34	ns
t_{SPD}	ADS HIGH to address output valid	6/19			64			64	ns
t_{ASC}	Column address setup to $\overline{CAS}$ LOW	6/21	0			0			ns
t_{CAHC}	Column address remaining valid from $\overline{CASIN}$0-3 HIGH	6/18	5			5			ns
t_{ASR}	Row address valid before $\overline{RAS}$ LOW	6/24	0			0			ns
t_{d5}	($\overline{RASIN}$ to $\overline{RAS}$ HIGH delay)-($\overline{RASIN}$ to $\overline{RAS}$ LOW delay)		-10		10	-10		10	ns
	REFRESH PARAMETER								
t_{RFLCT}	$\overline{RFSH}$ LOW to refresh address valid ($\overline{AUTO}$ LOW or R/$\overline{C}$ HIGH)	7/5			50			50	ns
t_{RFPDL}	$\overline{RASIN}$ LOW to $\overline{RAS}$ LOW delay during refresh	7/11			26			26	ns
t_{RFPDH}	$\overline{RASIN}$ HIGH to $\overline{RAS}$ HIGH delay during refresh	7/12			38			38	ns
t_{RFAH}	Refresh address held from $\overline{RASIN}$ HIGH ($\overline{RFSH}$ LOW)	7/7	0			0			ns
t_{RHNC}	$\overline{RASIN}$ HIGH to new refresh address valid	7/9			72			72	ns
t_{RFAHR}	Refresh address held from $\overline{RFSH}$ HIGH	7/6	0			0			ns
t_{RFS}	Refresh address valid to $\overline{RAS}$ LOW (provided t_{RFQS} is satisfied)	7/13	0			0			ns
t_{RFRDH}	$\overline{RFSH}$ HIGH to $\overline{RAS}$ HIGH (for three banks, $\overline{RASIN}$ = LOW)	7/15			45			45	ns
t_{d9}	($\overline{RASIN}$ to $\overline{RAS}$ HIGH delay)-($\overline{RASIN}$ to $\overline{RAS}$ LOW delay)		-9		16	-9		16	ns
	THREE-STATE PARAMETER								
t_{AZL}	$\overline{OE}$ LOW to address output LOW	10/1			50			50	ns
t_{AZH}	$\overline{OE}$ LOW to address output HIGH	10/2			60			60	ns
t_{ALZ}	$\overline{OE}$ HIGH to address output HI-Z from LOW	10/3			35			35	ns
t_{AHZ}	$\overline{OE}$ HIGH to address output HI-Z from HIGH	10/4			25			25	ns
t_{CTZL}	$\overline{OE}$ LOW to control output LOW	10/5			50			50	ns
t_{CTZH}	$\overline{OE}$ LOW to control output HIGH	10/6			50			50	ns
t_{CTLZ}	$\overline{OE}$ HIGH to control output HI-Z from LOW	10/7			35			35	ns
t_{CTHZ}	$\overline{OE}$ HIGH to control output HI-Z from HIGH	10/8			30			30	ns

Note 1: These are absolute voltage levels with respect to the ground pins on the device and includes all overshoots due to system or tester noise. Do not attempt to test these values without suitable equipment.

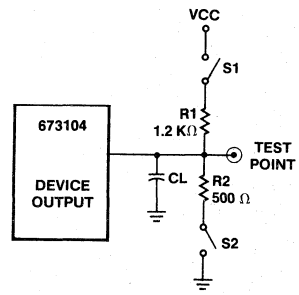
Note 2: This test is provided as a monitor of driver output source and sink current capability. Caution should be exercised in testing this parameter. One output should be tested at a time and test duration should not exceed one second.

Note 3: Output load capacitance is typical for four banks of 32 DRAMs with trace capacitance. The values are: Q0-8 C_L = 800 pF, $\overline{RAS}$0-3 C_L = 250 pF, $\overline{WE}$ C_L = 800 pF, $\overline{CAS}$0-3 C_L = 300 pF.



Change in Propagation Delays vs. Change in Loading Capacitance Relative to the Specified Load

673104 Test Loads (See Note)



Note: Input pulse 0 V to 3.0 V, $t_R = t_F = 2.5$ ns, f = 1.0 MHz, $t_{PW} = 200$ ns.
Input reference point on AC measurements is 1.5 V.
Output reference points are 2.4 V for HIGH and 0.8 V for LOW.

Address Outputs

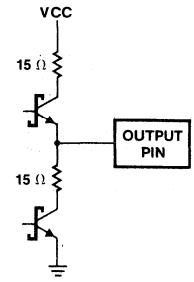
TEST	S1	S2	CL	MEASURED AT
t_{PD}	Open	Closed	800 pF	0.8 V, 2.4 V
t_{PZH}	Closed	Closed	800 pF	2.4 V
t_{PHZ}	Open	Closed	15 pF	V_{OH} -0.5 V
t_{PZL}	Closed	Closed	800 pF	0.8 V
t_{PLZ}	Closed	Open	15 pF	V_{OL} +0.5 V

Control Outputs

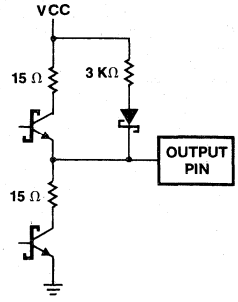
TEST	S1	S2	CL	MEASURED AT
t_{PD}	Open	Closed	CL	0.8 V, 2.4 V
t_{PZH}	Open	Closed	CL	2.4 V
t_{PHZ}	Open	Closed	15 pF	V_{OH} -0.5 V
t_{PZL}	Open	Open	CL	0.8 V
t_{PLZ}	Open	Open	15 pF	V_{OL} +0.5 V

Where C_L = 250 pF for $\overline{RAS}$, 300 pF for $\overline{CAS}$, and 800 pF for $\overline{WE}$.

Address Driver Output Stage



Control Driver Output Stage



Applications

Microprocessor Interface

The 673104 Dynamic RAM Controller provides the address and control signals required to access and refresh dynamic RAMs. When interfaced to a 32-bit microprocessor, some external logic is required to generate a refresh clock as well as to perform access/refresh arbitration and interface handshake functions. For some microprocessors external logic is required also to decode the address and control signal to arrive at four data strobes. A hidden refresh (refresh which is transparent to the system) scheme may be implemented in the interface circuitry taking advantage of "free" system time to refresh the memory, and falling back to "forced" refresh when hidden refresh cannot be performed.

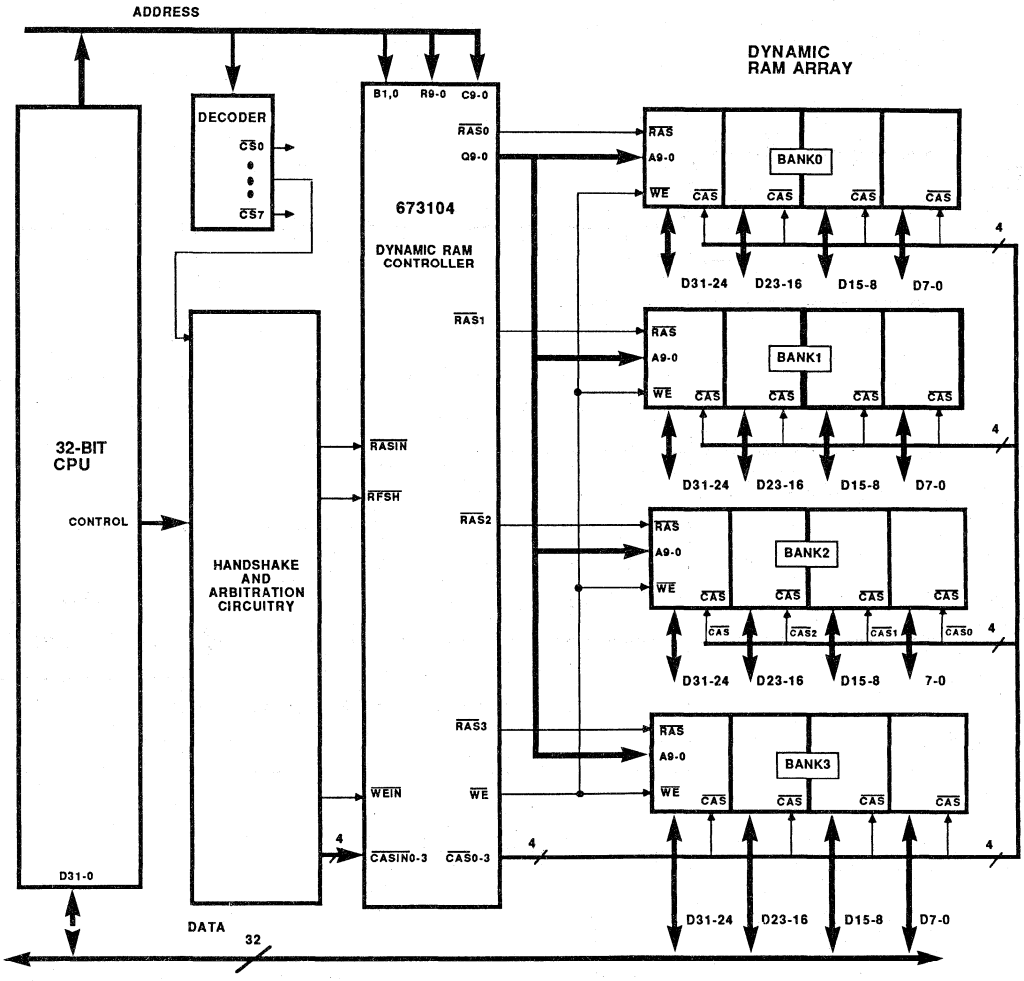


Figure 1. A CPU Interfaced to the 673104 Driving 16 M Bytes of Dynamic Memory

Determining System Performance (Auto-Access)

When determining system performance the dynamic RAM parameters must be considered as well as the controller's propagation delays. For both read and write cycles the access time for the dynamic RAM is t_{RAC} ($\overline{RAS}$ access time) from $\overline{RAS}$ going LOW or t_{CAC} ($\overline{CAS}$ access time) from $\overline{CAS}$ going LOW. Since the $\overline{RAS}$ and $\overline{CAS}$ coming out of the controller are initiated by the $\overline{RASIN}$, the controller-memory performance is measured from the $\overline{RASIN}$ HIGH-to-LOW transition (see Figure 2).

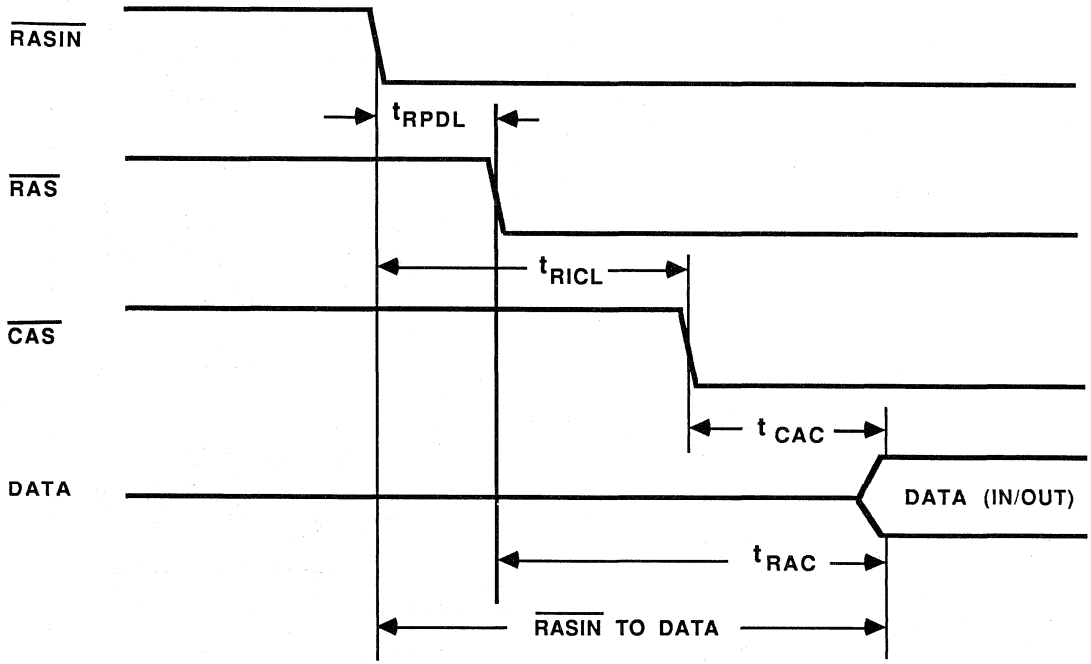


Figure 2. Access Time from $\overline{RASIN}$

The time from $\overline{RASIN}$ to data is calculated to be the longer of:

$t_{RICL} + t_{CAC}$ ($\overline{RASIN}$ to $\overline{CAS}$ + $\overline{CAS}$ to data)

$t_{RPDL} + t_{RAC}$ ($\overline{RASIN}$ to $\overline{RAS}$ + $\overline{RAS}$ to data)

Table 1 illustrates the access times from $\overline{RASIN}$ achieved for various dynamic RAM speeds.

CONTROLLER/MEMORY	PARAMETER				
	t_{RAC}	t_{RPDL}	t_{CAC}	t_{RICL}	ACCESS TIME FROM $\overline{RASIN}$
673104/HM256-12	120	23	60	90	150
673104A/HM256-12	120	23	60	83	143
673104/HM256-15	150	23	75	90	173
673104A/HM256-15	150	23	75	83	173
673104/MB8265A-10	100	23	50	90	140
673104A/MB8265A-10	100	23	50	83	133
673104/MB8265A-12	120	23	60	90	150
673104A/MB8265A-12	120	23	60	83	143
673104/IMS2620-10	100	23	60	90	150
673104A/IMS2620-10	100	23	60	83	143
673104/IMS2620-12	120	23	70	90	160
673104A/IMS2620-12	120	23	70	83	153

Table 1. Access Times from $\overline{RASIN}$ for Various Memory Speeds

673104 Parameters

t_{RICL} — $\overline{RASIN}$ LOW to $\overline{CAS}$ LOW delay

t_{RPDL} — $\overline{RASIN}$ LOW to $\overline{RAS}$ LOW delay

DRAM Parameters

t_{RAC} — Access time from $\overline{RAS}$ LOW

t_{CAC} — Access time from $\overline{CAS}$ LOW

Using the Externally Controlled Access

In the Externally Controlled Access mode $\overline{RASIN}$ controls the selected $\overline{RAS}$ output, $\overline{CASIN}$0-3 control $\overline{CAS}$0-3 outputs respectively and R/$\overline{C}$ controls the address multiplexer. The system designer may create, using the $\overline{RASIN}$, $\overline{CASIN}$ and R/$\overline{C}$ inputs, the required control signal sequence for the specific system being designed. Special dynamic RAM access modes such as Nibble mode and Page mode access cycles may be performed simply by toggling the appropriate control inputs. Special skew timing specifications have been specified to allow tighter timing control as outlined in the following examples. Both following examples relate to the scheme depicted in Figure 3.

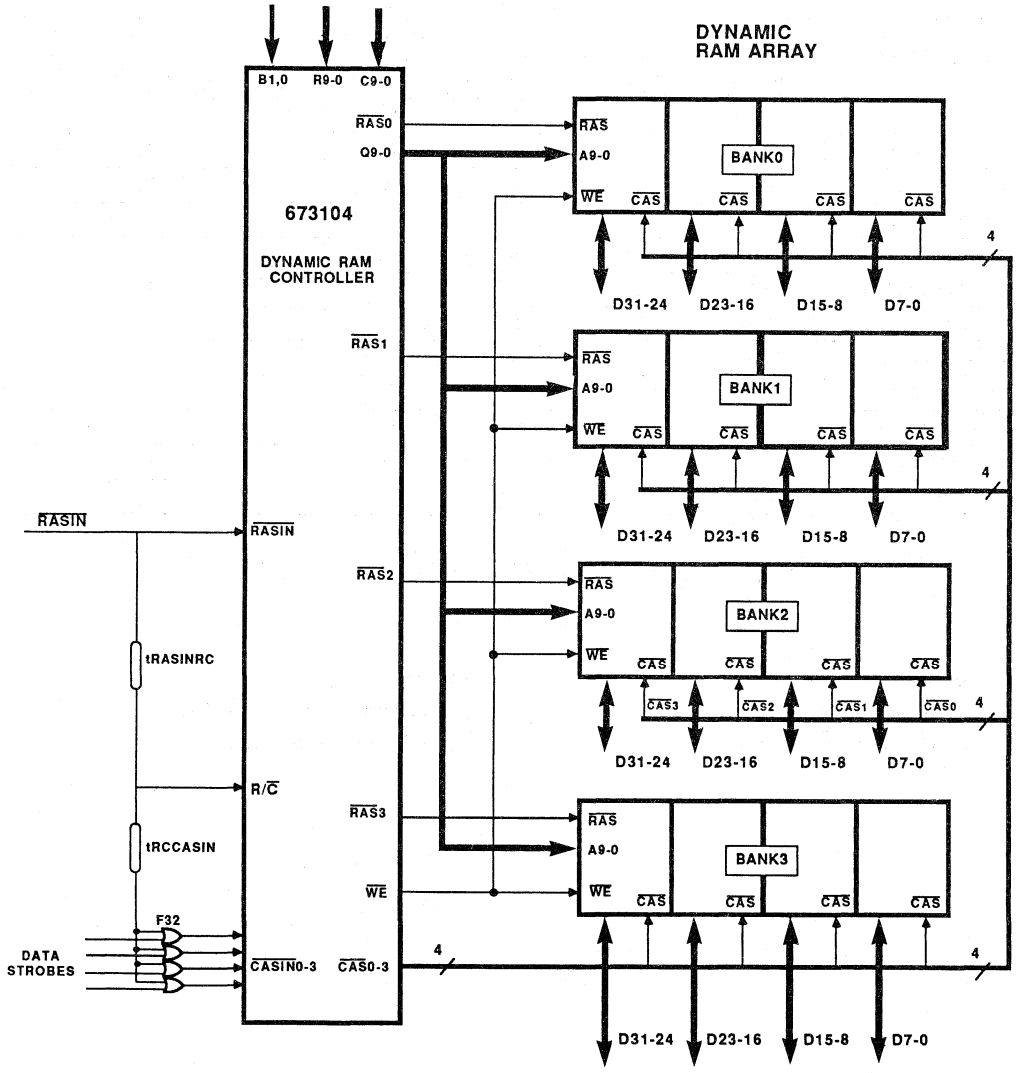


Figure 3. The 673104 in the Externally-Controlled Access Mode

Externally Controlled Access (ECA)
(Continued)

Example 1: Computing $\overline{\text{RASIN}}$ to R/$\overline{\text{C}}$ Delay

The delay between $\overline{\text{RASIN}}$ going LOW to R/C going LOW ($t_{RASINRC}$) which is required in order to satisfy the dynamic RAMs' row address hold time (t_{RAH}) is computed as follows:

$t_{RASINRC} = t_{RAH}(min) + t_{d7}$

Where:

$t_{RAH}(min)$ — Row address hold time (dynamic RAM parameter)

$t_{d7}(max) = t_{RPDL} - t_{RHA}$

t_{RPDL} — $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ LOW delay

t_{RHA} — Row address held valid from R/$\overline{\text{C}}$ LOW

Example 2: Computing R/$\overline{\text{C}}$ to $\overline{\text{CASIN}}$ Delay

The delay between R/$\overline{\text{C}}$ going LOW and $\overline{\text{CASIN}}$ going LOW ($t_{RCCASIN}$) which is required in order to satisfy the dynamic RAMs' column address setup (t_{ASC}) is computed as follows:

$t_{RCCASIN} = t_{ASC}(min) + t_{d8} + t_{PD}F32(max)$

Where:

$t_{ASC}(min)$ — Column address setup (dynamic RAM parameter)

$t_{d8}(max) = t_{RCC} - t_{CPDL}$

t_{RCC} — R/$\overline{\text{C}}$ low to column address valid

t_{CPDL} — $\overline{\text{CASIN}}$ to $\overline{\text{CAS}}$ LOW delay

$t_{PD}F32(max)$ — Propagation delay of the OR gate used to validate $\overline{\text{CASIN}}$

Better system performance may be achieved using the t_{d7}, t_{d8} switching parameters to calculate $t_{RASINRC}$ and $t_{RCCASIN}$ than when using the t_{RPDL}, t_{RCDL}, t_{RCC} and t_{RHA} parameters (see Externally Controlled Access switching parameters).

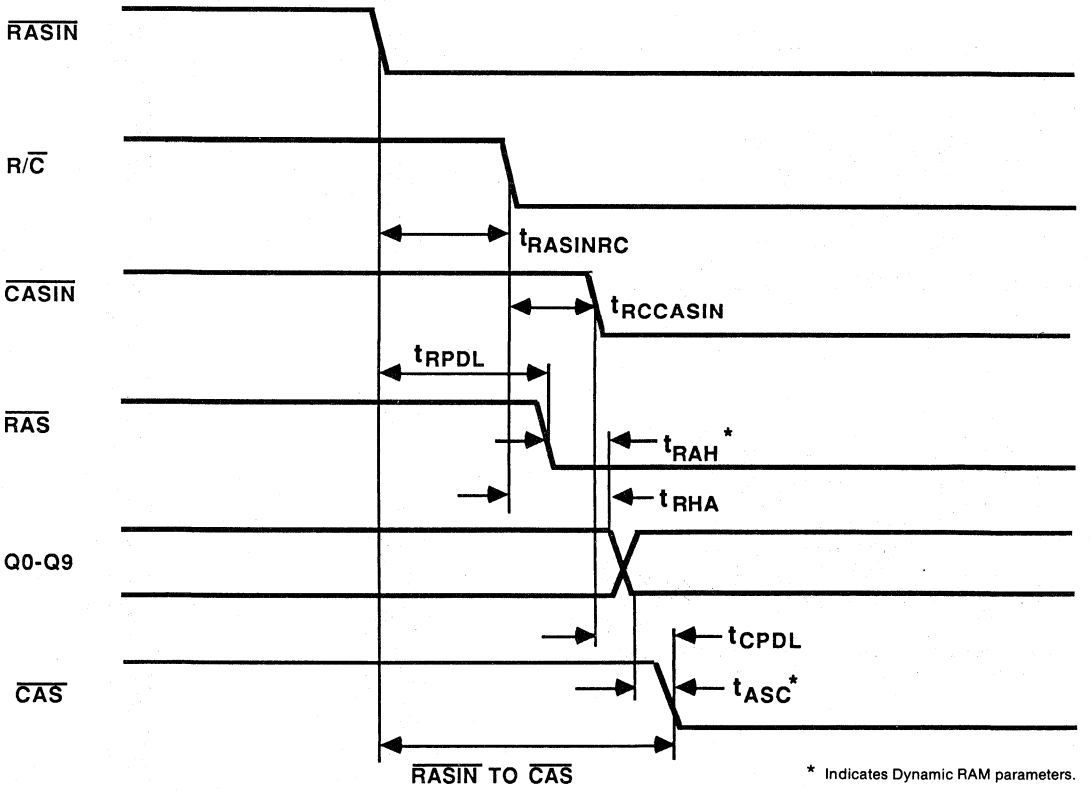


Figure 4. Externally Controlled Access Timing

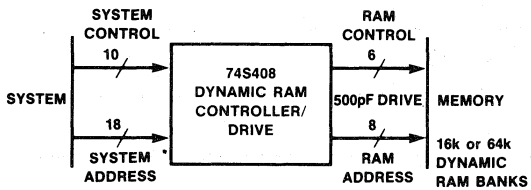
64K Dynamic RAM Controller/Driver

SN74S408/DP8408A
SN74S408-2/DP8408A-2

Features/Benefits

- All DRAM drive functions on one chip have on-chip high-capacitance-load drivers (specified up to 88 DRAMs)
- Drives directly all 16K and 64K DRAMs: Capable of addressing up to 256K words
- Propagation delays of 25 nsec typical at 500-pF load
- Supports READ, WRITE and READ-MODIFY-WRITE cycles
- Six operating modes support externally-controlled access and refresh, automatic access, as well as special memory initialization access
- On-chip 8-bit refresh counter with selectable End-of-Count (127 or 255)
- Direct replacement for National DP8408, DP8408A

MODE	MODE OF OPERATION
0,1,2	Externally-controlled refresh
3	Externally-controlled All-$\overline{RAS}$ write
4	Externally-controlled access
5	Auto access, slow t_{RAH}
6	Auto access, fast t_{RAH}
7	Set end of count

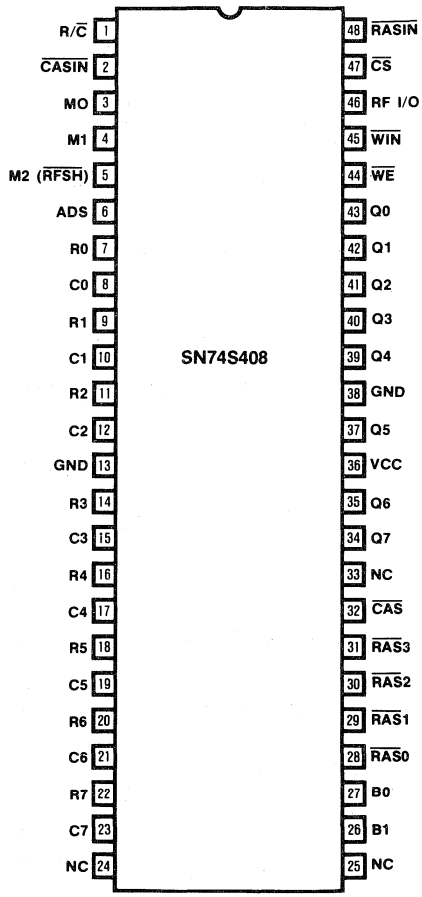


74S408 Interface Between System and DRAM Banks

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN74S408	48 N, D	Com
SN74S408-2	48 N, D	Com, Speed Option

Pin Configuration



NC = NO CONNECTION

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374
Monolithic Memories

Block Diagram

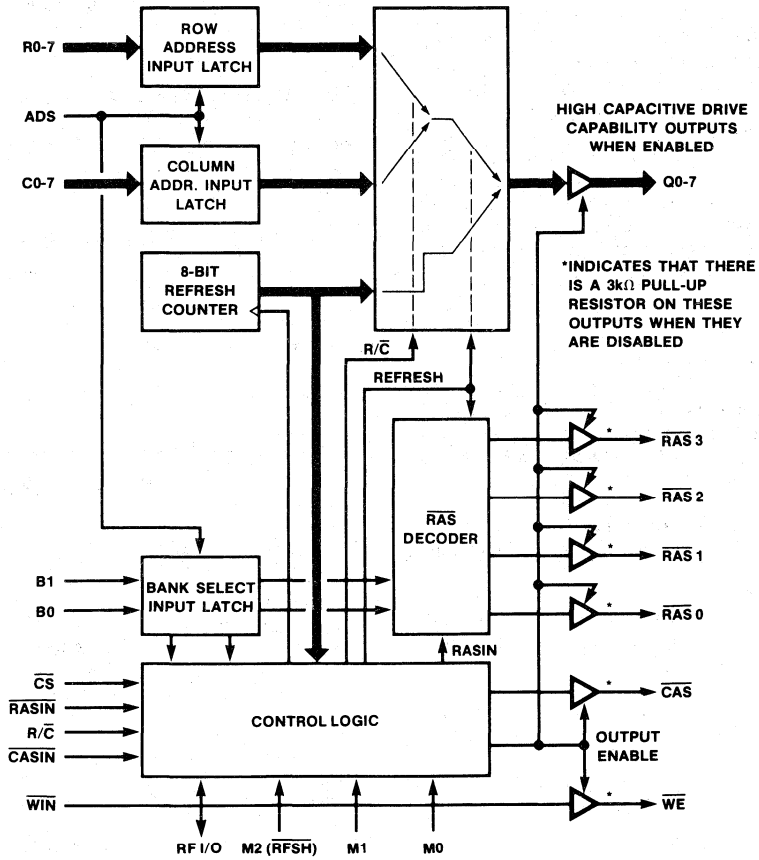


Figure 1. 74S408 Functional Block Diagram

Description

The 74S408 is a Multi-Mode Dynamic RAM Controller/Driver capable of driving directly up to 88 DRAMs. 18 address lines allow the 74S408 to drive all 16K and 64K DRAMs and addresses up to 256K words. Since the 74S408 is a one-chip solution (including capacitive-load drivers), it minimizes propagation delay skews, and saves board space.

The 74S408's 6 operating modes offer externally-controlled or on-chip automatic access and externally-controlled refresh. An on-chip refresh counter makes refreshing less complicated; and automatic memory initialization is both simple and fast.

The 74S408 is a 48-pin DRAM Controller/Driver with 8 multiplexed address outputs and 6 control signals. It consists of two 8-bit address latches, an 8-bit refresh counter, and control logic. All address output drivers are capable of driving 500pf loads with propagation delays of 25nsec. The 74S408 timing parameters are specified driving the typical load capitance of 88 DRAMs, including trace capitance.

The 74S408 can drive up to 4 banks of DRAMs, with each bank comprised of 16Ks, or 64Ks. Control signal outputs $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ are provided with the same driving capability. Each $\overline{RAS}$ output drives one bank of DRAMs so that the four $\overline{RAS}$ outputs are used to select the banks, while $\overline{CAS}$, $\overline{WE}$ and the multiplexed addresses can be connected to all the banks of DRAMs. This leaves the nonselected banks in the standby mode (less than one tenth of the operating power) with the data output in three-state. Only the bank with its associated $\overline{RAS}$ low will be written to or read from, except in mode 3 where all $\overline{RAS}$ signals go low to allow fast memory initialization.

Pin Definitions

V_{CC} GND, GND—$V_{CC} = 5V \pm 5\%$. The three supply pins have been assigned to the center of the package to reduce voltage drops, both DC and AC. There are also two ground pins to reduce the low level noise. The second ground pin is located two pins from V_{CC}, so that decoupling capacitors can be inserted directly next to these pins. It is important to adequately decouple this device, due to the high switching currents that will occur when all 8 address bits change in the same direction simultaneously. Recommended solution would be a 1μF multilayer ceramic capacitor in parallel with a low-voltage tantalum capacitor, both connected close to pins 36 and 38 to reduce lead inductance.

R0-R7: Row Address Inputs.

C0-C7: Column Address Inputs.

B0, B1: Bank Select Inputs—Strobed by ADS. Decoded to enable one of the $\overline{RAS}$ outputs when $\overline{RASIN}$ goes low, in modes 4-6. In mode 7 B0, B1 are used to define End-of-Count (see table 3).

Q0-Q8: Multiplexed Address Outputs—Selected from the Row Address Input Latch, the Column Address Input Latch, or the Refresh Counter.

$\overline{RASIN}$: Row Address Strobe Input—Enables selected $\overline{RAS}_n$ output when M2 ($\overline{RFSH}$) is high (modes 4-6), and all $\overline{RAS}_n$ outputs in modes 0, 1, 2 and 3.

R/$\overline{C}$: Row/Column Select Input—Selects either the row or column address input latch onto the output bus.

$\overline{CASIN}$: Column Address Strobe Input—Inhibits $\overline{CAS}$ output when high in Modes 4 and 3. In Mode 6 it can be used to prolong $\overline{CAS}$ output.

ADS: Address (Latch) Strobe Input—Strobes Input Row Address, Column Address, and Bank Select Inputs into respective latches when high; latches on High-to-Low transition.

$\overline{CS}$: Chip Select Input—Three-state's the Address Outputs and puts the control signal into a high-impedance logic "1" state when high (unless refreshing in mode 0, 1, 2). Enables all outputs when low.

M0, M1, M2 ($\overline{RFSH}$): Mode Control Inputs—These 3 control pins determine the 6 modes of operation of the 74S408 as depicted in Table 1.

RF I/O—The I/O pin functions as a Reset Counter Input when set low from an external open-collector gate, or as a flag output. The flag goes active (low) when M2 = 0 (modes 0, 1, 2 or 3) and the End-of-Count output is at 127 or 255 (see Table 3).

$\overline{WIN}$: Write Enable Input.

$\overline{WE}$: Write Enable Output—Buffered output from $\overline{WIN}$.

$\overline{CAS}$: Column Address Strobe Output—In Modes 5 and 6, $\overline{CAS}$ transitions low following valid column address. In Modes 3 and 4, it goes low after R/$\overline{C}$ goes low, or follows $\overline{CASIN}$ going low if R/$\overline{C}$ is already low. $\overline{CAS}$ is high during refresh.

$\overline{RAS}$ 0-3: Row Address Strobe Outputs—When M2($\overline{RFSH}$) is high (modes 4-7), the selected row address strobe output (decoded from signals B0, B1) follows the $\overline{RASIN}$ input. When M2 ($\overline{RFSH}$) is low (modes 0-3) all $\overline{RAS}_n$ outputs go low together following $\overline{RASIN}$ going low.

BANK SELECT (STROBED BY ADS)		ENABLED $\overline{RAS}_n$
B1	B0	
0	0	$\overline{RAS}_0$
0	1	$\overline{RAS}_1$
1	0	$\overline{RAS}_2$
1	1	$\overline{RAS}_3$

Table 1. Memory Bank Decode

Input Addressing

The address block consists of a row-address latch, a column-address latch, and a resettable refresh counter. The address latches are fall-through when ADS is high and latch when ADS goes low. If the address bus contains valid addresses until after the valid address time, ADS can be permanently high. Otherwise ADS must go low while the addresses are still valid.

In normal memory access operation, $\overline{RASIN}$ and R/$\overline{C}$ are initially high. When the address inputs are enabled into the address latches (modes 4-6) the row addresses appear on the Q outputs. The Address Strobe also inputs the bank-select address, (B0 and B1). If $\overline{CS}$ is low, all outputs are enabled. When $\overline{CS}$ is transitioned high, the address outputs go three-state and the control outputs first go high through a low impedance, and then are held by an on-chip high impedance. This allows output paralleling with other 74S408s for multi-addressing. All outputs go active about 50ns after the chip is selected again. If $\overline{CS}$ is high, and a refresh cycle begins, all the outputs become active until the end of the refresh cycle.

Drive Capability

The 74S408 has timing parameters that are specified with up to 600pF loads for $\overline{CAS}$, 500pF loads for Q_0-Q_7 and $\overline{WE}$, and 150 pF loads for $\overline{RAS}_n$ outputs. In a typical memory system this is equivalent to about 88 5V-only DRAMs, with trace lengths kept to a minimum. Therefore, the chip can drive four banks each of 16 or 22 bits, or two banks of 32 or 39 bits, or one bank of 64 or 72 bits.

Less loading will slightly reduce the timing parameters, and more loading will increase the timing parameters, according to the graph of Figure 6). The AC performance parameters are specified with the typical load capacitance of 88 DRAMs. This graph can be used to extrapolate the variations expected with other loading.

74S408 Driving Any 16K or 64K DRAMs

The 74S408 can drive any 16K or 64K DRAMs. The on-chip 8-bit counter with selectable End-of-Count can support refresh of 128 or 512 rows, while the 8 address and 4 $\overline{RAS}_n$ outputs can address 4 banks of 16K or 64K DRAMs.

Read, Write, and Read-Modify-Write Cycles

The output signal, $\overline{WE}$, determines what type of memory access cycle the memory will perform. If $\overline{WE}$ is kept high while $\overline{CAS}$ goes low, a read cycle occurs. If $\overline{WE}$ goes low before $\overline{CAS}$ goes low, a write cycle occurs and DATA at DI (DRAM input data) is written into the DRAM as $\overline{CAS}$ goes low. If $\overline{WE}$ goes low later than t_{CWD} after $\overline{CAS}$ goes low, first a read occurs and DO (DRAM output data) becomes valid; then data DI is written into the same address in the DRAM when $\overline{WE}$ goes low. In this read-modify-write case, DI and DO cannot be linked together. The type of cycle is therefore controlled by $\overline{WE}$, which follows $\overline{WIN}$.

Power-Up Initialize

When V_{CC} is first applied to the 74S408, an internal pulse clears the refresh counter, the internal control flip-flops, and sets the End-of-Count of the refresh counter to 127 (which may be changed via Mode 7). As V_{CC} increases to about 2.3 volts, it holds the output control signals at a level of one Schottky diode-drop below V_{CC}, and the output address to three-state. As V_{CC} increases above 2.3 volts, control of these outputs is granted to the system.

74S408 Functional Mode Description

The 74S408 operates in 6 different functional modes. The operating mode is selected by signals M_0, M_1, M_2. Selecting M_2, M_1, M_0 = 0,0,0 or 0,0,1 or 0,1,0 will result at the same operating mode designated as mode 0,1,2 (see Table 2).

MODE	($\overline{RFSH}$) M2	M1	M0	MODE OF OPERATION	CONDITIONS
0,1,2	0 0 0	0 0 1	0 1 0	Externally-controlled refresh	RF I/O = EOC
3	0	1	1	Externally-controlled All-$\overline{RAS}$ write	All-$\overline{RAS}$ active
4	1	0	0	Externally-controlled access	Active $\overline{RAS}$ defined by Table 2
5	1	0	1	Auto access, slow t_{RAH}	Active $\overline{RAS}$ defined by Table 2
6	1	1	0	Auto access, fast t_{RAH}	Active $\overline{RAS}$ defined by Table 2
7	1	1	1	Set end of count	See Table 3 for Mode 7

Table 2. 74S408 Mode Select Options

74S408 Functional Mode Descriptions

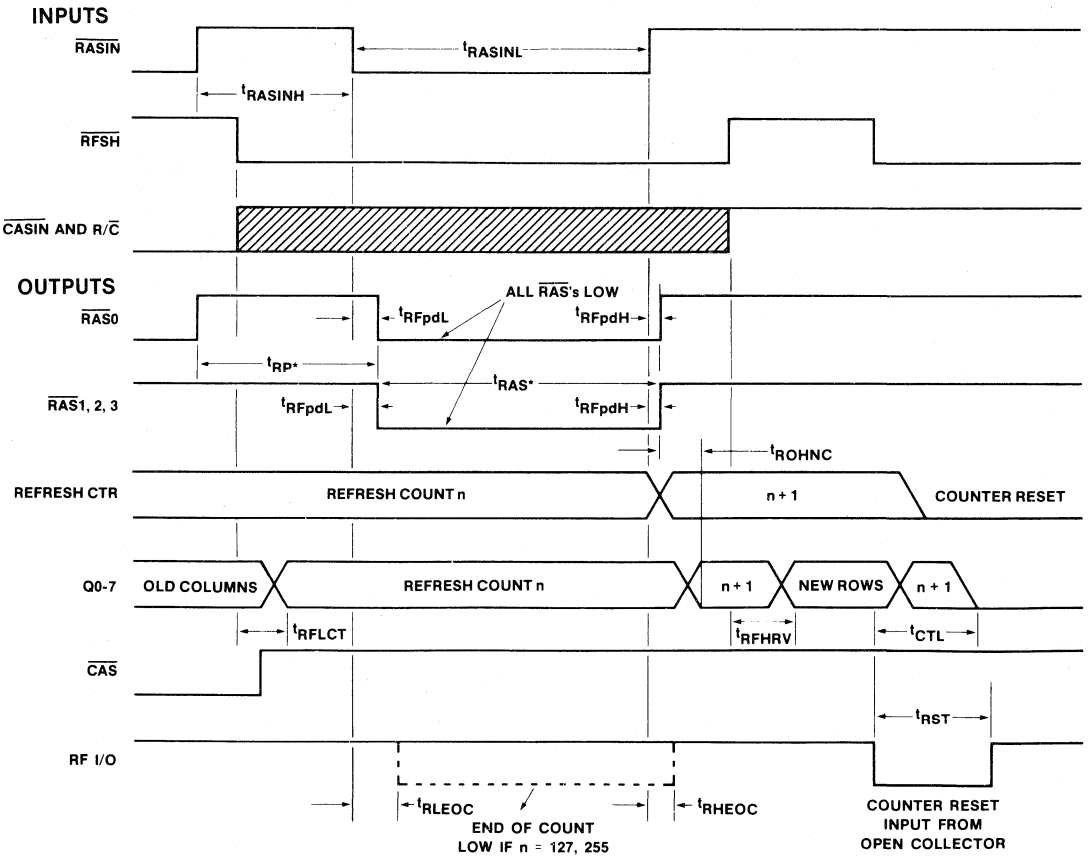
Modes 0, 1, 2—Externally Controlled Refresh

In this mode, the input address latches are disabled from the address outputs and the refresh counter is enabled onto R_0-R_7 outputs, all $\overline{RAS}$ outputs are enabled following $\overline{RASIN}$, and $\overline{CAS}$ is inhibited. This refreshes the same row in all four banks. The refresh counter increments when either $\overline{RASIN}$ or $M_2(\overline{RFSH})$ goes low-to-high while the other is low. RF I/O goes low when the count is 127 or 255 with $\overline{RASIN}$ and $\overline{RFSH}$ as set by End-of-Count (see Table 3), low. To reset the counter to all zeroes, RF I/O is set low through an external open-collector driver.

During refresh, $\overline{RASIN}$ and $M_2(\overline{RFSH})$ can transition low simultaneously because the refresh counter becomes valid on the output but t_{RFLCT}. This means the counter address is valid on the Q outputs before $\overline{RAS}$ occurs on all $\overline{RAS}$ outputs, strobing the counter address into that row of all the DRAMS (see Figure 2). To perform externally controlled burst refresh $M_2(\overline{RFSH})$ initially can again have the same edge as $\overline{RASIN}$, but then can maintain a low state, since $\overline{RASIN}$ going low-to-high increments the counter (performing the burst refresh).

Mode 3—Externally Controlled All-$\overline{RAS}$ Write

This mode is useful at system initialization. The memory address is provided by the processor, which also perform the incrementing. All four $\overline{RAS}$ outputs follow $\overline{RASIN}$ (supplied by the processor), strobing the row address into the DRAMs. R/$\overline{C}$ can now go low, while $\overline{CASIN}$ may be used to control $\overline{CAS}$ (as in the Externally Controlled Access mode), so that $\overline{CAS}$ strobes the column address contents into the DRAMs. At this time $\overline{WE}$ should be low, causing the data to be written into all four banks of DRAMs. At the end of the write cycle, the input address is incremented and latched by the 74S408 for the next write cycle.



*INDICATES DYNAMIC RAM PARAMETERS

Figure 2. External Control Refresh Cycle (Modes 0, 1, 2)

Mode 4—Externally Controlled Access

This mode facilitates externally controlling all access-timing parameters associated with the DRAMs. The application of modes 0 and 4 are shown in Figure 3.

Output Address Selection

Refer to Figure 4a. With M2 ($\overline{RFSH}$) and R/$\overline{C}$ high, the row address latch contents are transferred to the multiplexed address bus output Q0-Q7, provided $\overline{CS}$ is set low. The column address latch contents are output after R/$\overline{C}$ goes low. $\overline{RASIN}$ can go low after the row addresses have been set up on Q0-Q7. This selects one of the $\overline{RAS}$ outputs, strobing the row address on the Q outputs into the desired bank of memory. After the row-address hold-time of the DRAMs, R/$\overline{C}$ can go low so that about 40 ns later column addresses appear on the Q outputs.

Automatic $\overline{CAS}$ Generation

In a normal memory access cycle $\overline{CAS}$ can be derived from inputs $\overline{CASIN}$ or R/C. If $\overline{CASIN}$ is high, then R/$\overline{C}$ going low switches the address output drivers from rows to columns. $\overline{CASIN}$ then going low causes $\overline{CAS}$ to go low approximately 40 ns later, allowing $\overline{CAS}$ to occur at a predictable time (see Figure 4b). For maximum system speed, $\overline{CASIN}$ can be kept low, since $\overline{CAS}$ will automatically occur approximately 20 ns after the column addresses are valid, or about 60 ns after R/$\overline{C}$ goes low (see Figure 4a). Most DRAMs have a column address set-up time before $\overline{CAS}$ (t_{ASC}) of 0 ns or – 10 ns. In other words, a t_{ASC} greater than 0 ns is safe. This feature reduces timing-skew problems, thereby improving access time of the system.

Fast Memory Access

For faster access time, R/$\overline{C}$ can go low a time delay (t_{RPDL} + t_{RAH} – t_{RHA}) after RASIN goes low, where t_{RAH} is the Row-Address hold-time of the DRAM.

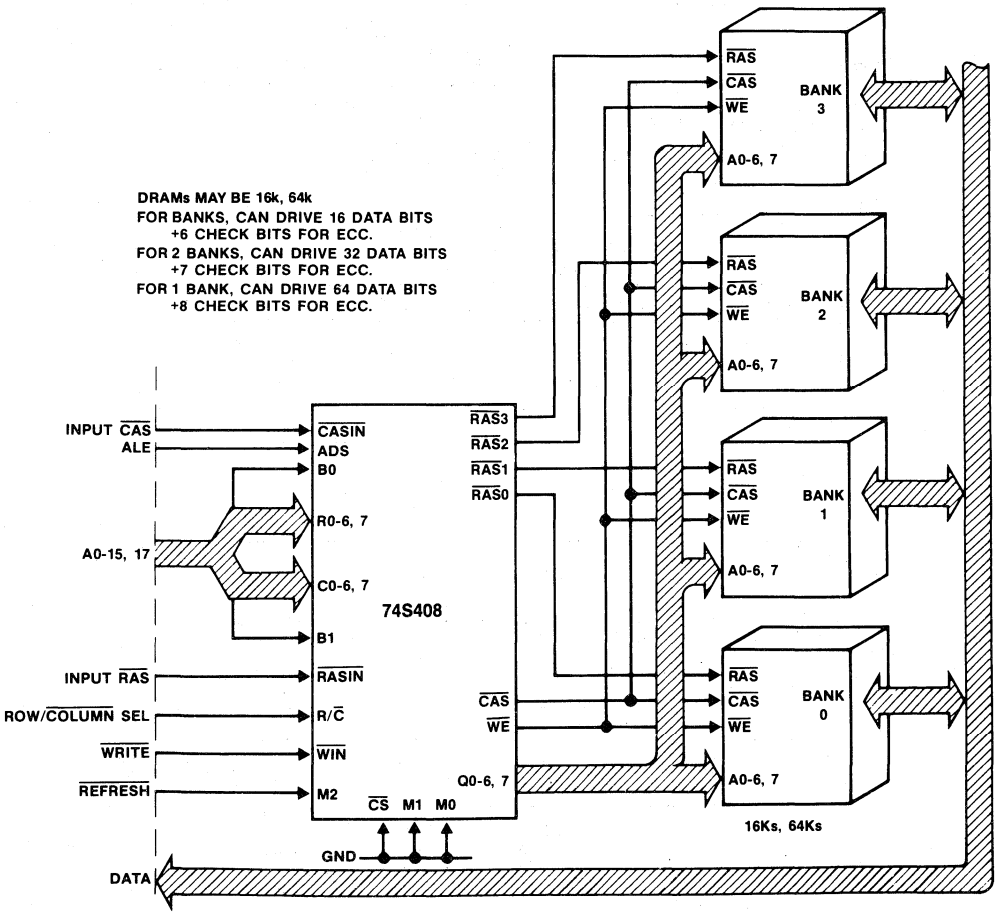
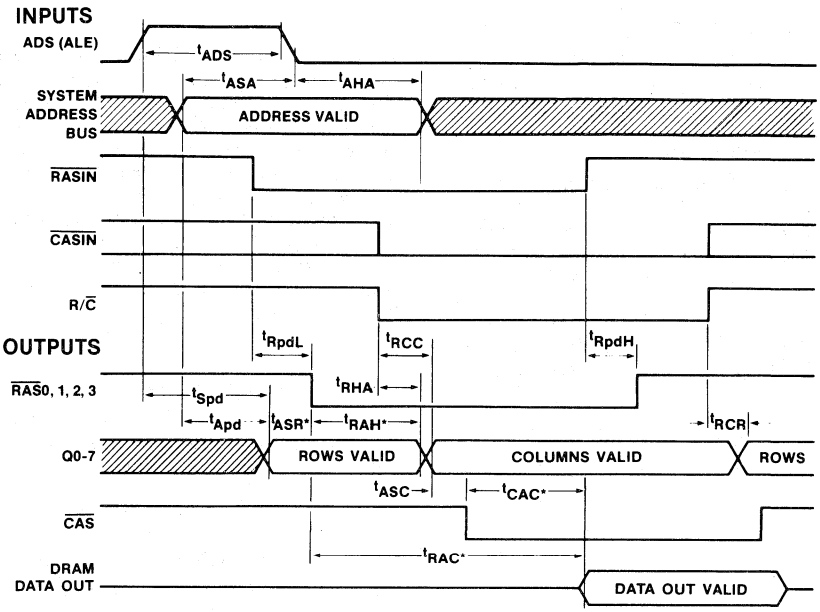
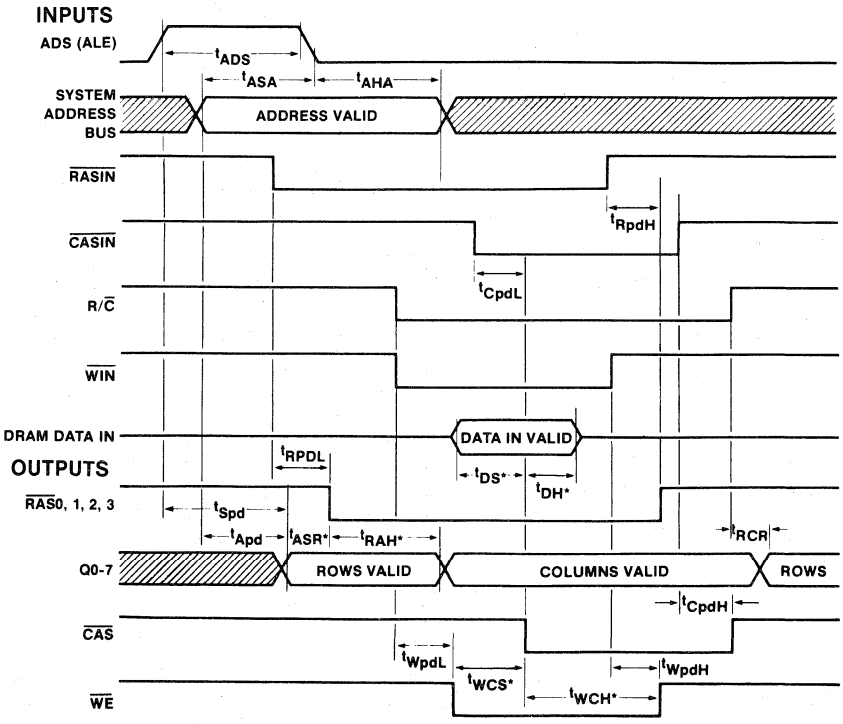


Figure 3. Typical Application of 74S408 Using Externally Controlled Access and Refresh in Modes 0 and 4



*INDICATES DYNAMIC RAM PARAMETERS

Figure 4a. Read Cycle Timing (Mode 4)



*INDICATES DYNAMIC RAM PARAMETERS

Figure 4b. Write Cycle Timing (Mode 4)

Mode 5—Automatic Access

In the Auto Access mode all outputs except $\overline{WE}$ are initiated from $\overline{RASIN}$. Inputs R/$\overline{C}$ and $\overline{CASIN}$ are unnecessary and the output control signals are derived internally from one input signal ($\overline{RASIN}$) minimizing timing-skew problems, thereby reducing memory-access time substantially and allowing the use of slower DRAMs.

Automatic Access Control

The major disadvantage of DRAMs compared to static RAMs is the complex timing involved. First, a $\overline{RAS}$ must occur with the row address previously set up on the multiplexed address bus. After the row address has been held for t_{RAH}, (the Row-Address hold-time of the DRAM), the column address is set up and then $\overline{CAS}$ occurs. This is all performed automatically by the 74S408 in this mode.

Provided the input address is valid as ADS goes low, $\overline{RASIN}$ can go low any time after ADS. This is because the selected $\overline{RAS}$ occurs typically 27 ns later, by which time the row address is already valid on the address output of the 74S408. The Address Set-Up time (t_{ASR}), is 0 ns on most DRAMs. The 74S408 in this mode (with ADS and $\overline{RASIN}$ edges simultaneously applied) produces a minimum t_{ASR} of 0 ns. This is true provided the input address was valid t_{ASA} before ADS went low (see Figure 5a).

Next, the row address is disabled after t_{RAH} (30 ns minimum); in most DRAMs, t_{RAH} minimum is less than 30 ns. The column address is then set up and t_{ASC} later, $\overline{CAS}$ occurs. The only other control input required is $\overline{WIN}$. When a write cycle is required, $\overline{WIN}$ must go low at least 30 ns before $\overline{CAS}$ is output low.

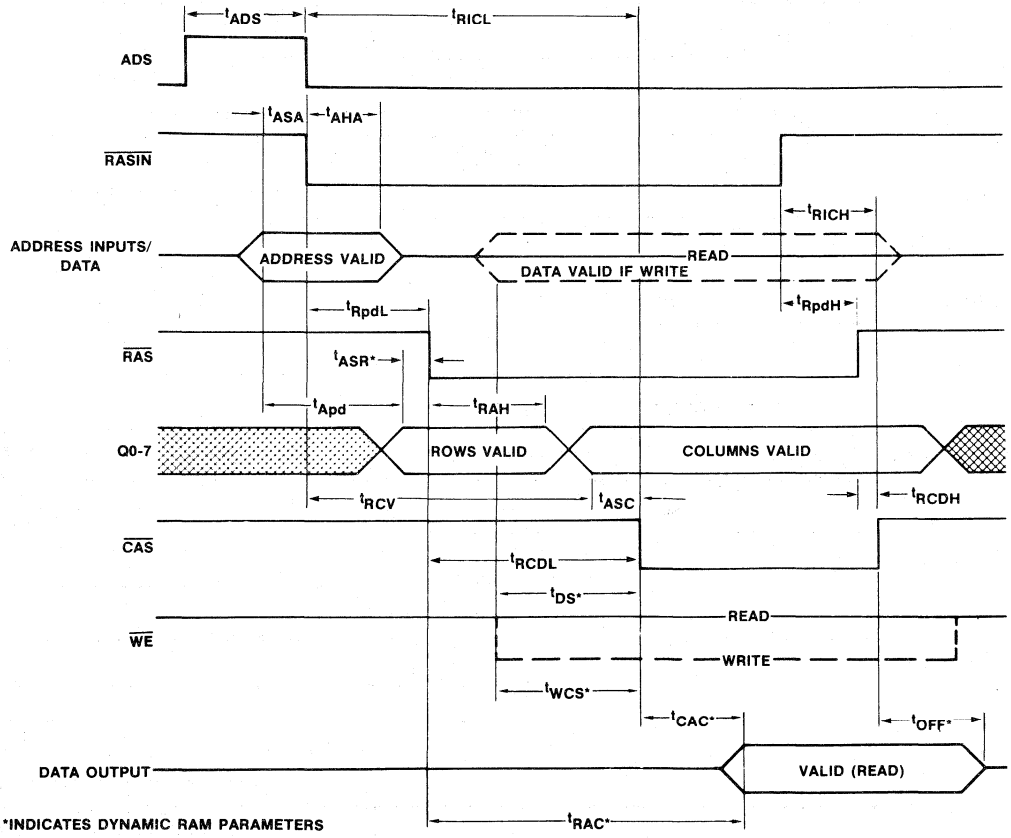


Figure 5a. Modes 5, 6 Timing ($\overline{CASIN}$ High in Mode 6)

This gives a total typical delay from: input address valid to $\overline{RASIN}$ (15 ns); to $\overline{RAS}$ (27 ns); to rows held (50 ns); to columns valid (25 ns); to $\overline{CAS}$ (23 ns) = 140 ns (that is, 125 ns from $\overline{RASIN}$). All of these typical figures are for heavy capacitive loading, of approximately 88 DRAMs. This mode is therefore extremely fast. The external timing is greatly simplified for the memory system designer: the only system signal required is $\overline{RASIN}$.

Mode 6—Fast Automatic Access

The Fast Access mode is similar to Mode 5, but has a faster t_{RAH} of 20 ns, minimum. It therefore can only be used with fast 16k or 64k DRAMs (which have a t_{RAH} of 10 ns to 15 ns) in applications requiring fast access times; $\overline{RASIN}$ to $\overline{CAS}$ is typically 105 ns.

In this mode, the R/$\overline{C}$ pin is not used, but $\overline{CASIN}$ is used to allow an extended $\overline{CAS}$ after $\overline{RAS}$ has already terminated. Refer to Figure 5b. This is desirable with fast cycle-times where $\overline{RAS}$ has to be terminated as soon as possible before the next $\overline{RAS}$ begins (to meet the precharge time, or t_{RP}, requirements of the DRAM). $\overline{CAS}$ may then be held low by $\overline{CASIN}$ to extend the data output valid time from the DRAM to allow the system to read the data. $\overline{CASIN}$ subsequently going high ends $\overline{CAS}$. If this extended $\overline{CAS}$ is not required, $\overline{CASIN}$ should be set high in Mode 6.

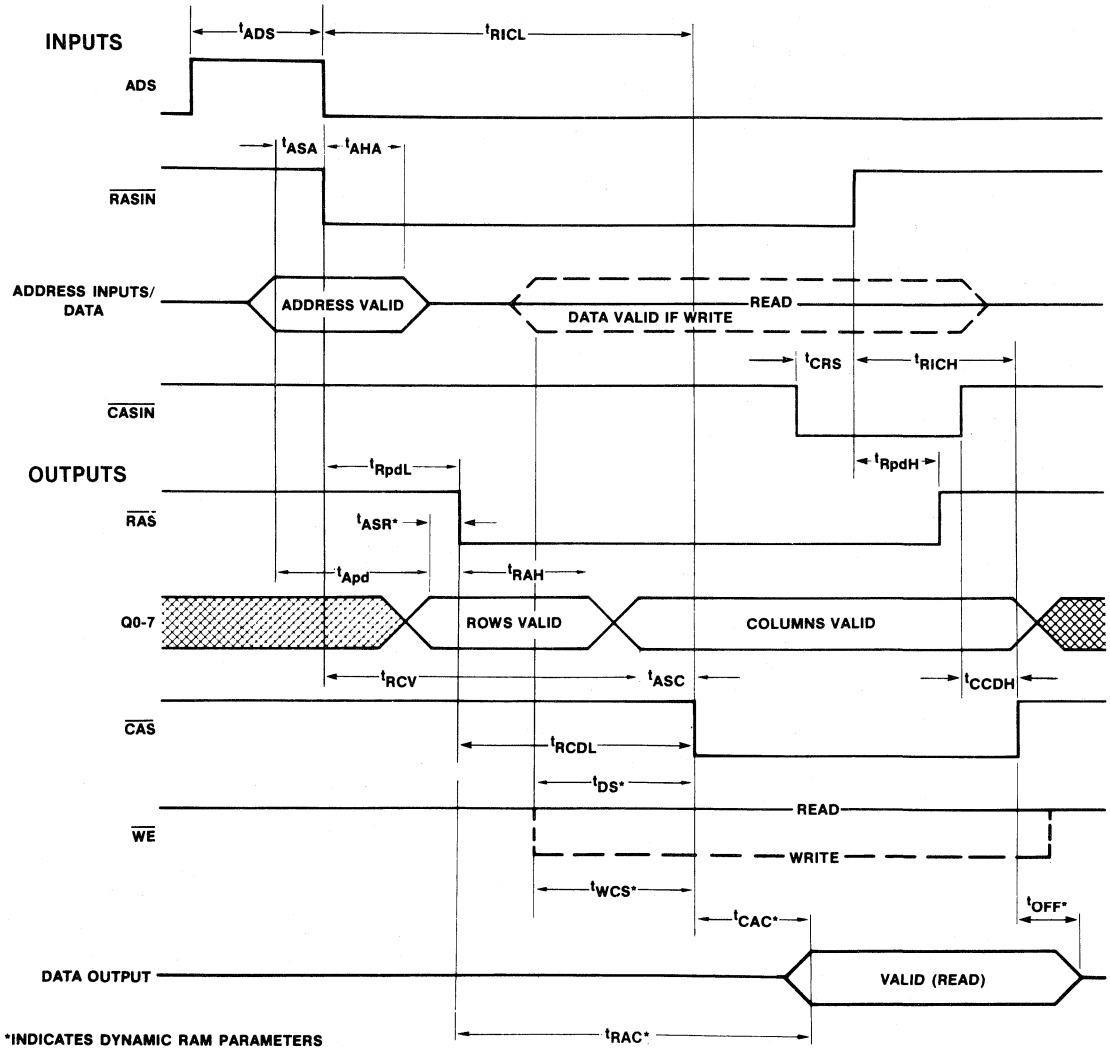


Figure 5b. Mode 6 Timing, Extended CAS

Mode 7—Set End-of-Count

The End-of-Count can be externally selected in Mode 7, using ADS to strobe in the respective value of B1 and B0 (see Table 3). With B1 and B0 the same EOC is 127; with B1 = 0 and B0 = 1, EOC is 255; and with B1 = 1 and B0 = 0, EOC is 127. This selected value of EOC will be used until the next Mode 7 selection. At power-up the EOC is automatically set to 127 (B1 and B0 set to 11).

BANK SELECT (STROBED BY ADS)		END OF COUNT SELECTED
B1	B0	
0	0	127
0	1	255
1	0	127
1	1	127

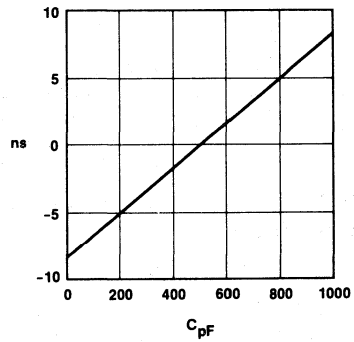


Figure 6. Change in Propagation Delay vs Loading Capacitance Relative to a 500pF Load

SN74S408/-2 Specifications:

Absolute Maximum Ratings (Note 1)

Supply voltage V_{CC} ..... -0.5 V to 7.0 V
Storage temperature range ..... -65° to +150° C
Input voltage ..... -1.5 V to 5.5 V
Output current ..... 150 mA
Lead temperature (soldering, 10 seconds) ..... 300° C

NOTE 1: "Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of operating conditions provides conditions for actual device operation.

Operating Conditions

SYMBOL	PARAMETER	FIGURE	'S408 MIN	'S408 TYP	'S408 MAX	'S408-2 MIN	'S408-2 TYP	'S408-2 MAX	UNIT
V_{CC}	Supply voltage		4.75		5.25	4.25		5.25	V
T_A	Operating free-air temperature		0		+75	0		+75	°C
t_{ASA}	Address setup time to ADS	Figures 4a,4b,5a,5b	15			15			ns
t_{AHA}	Address hold time from ADS	Figures 4a,4b,5a,5b	15			15			ns
t_{ADS}	Address strobe pulse width	Figures 4a,4b,5a,5b	30			30			ns
t_{RHA}	Row address held from column select	Figure 4a	10			10			ns
$t_{RASINL,H}$	Pulse width of $\overline{RASIN}$ during refresh	Figure 2	50			50			ns
t_{RST}	counter reset pulse width	Figure 2	70			70			ns

Electrical Characteristics: $V_{CC} = 5.0V \pm 5.0\%$, $0°C \leq T_A \leq 75°C$ Typicals are for $V_{CC} = 5V$, $T_A = 25°C$

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_C	Input clamp voltage	V_{CC} = MIN, I_C = −12mA		−0.8	−1.2	V
I_{IH1}	Input high current for ADS. R/$\overline{C}$ only.	V_{IN} = 2.5V		2.0	100	μA
I_{IH2}	Input high current for other inputs, except RF I/O	V_{IN} = 2.5V		1.0	50	μA
I_{IRSI}	Output load current for RF I/O	V_{IN} = 0.5V, output high		−1.5	−2.5	mA
I_{ICTL}	Output load current for $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	V_{IN} = 0.5V, chip deselect		−1.5	−2.5	mA
I_{IL1}	Input low current for ADS. R/$\overline{C}$ only	V_{IN} = 0.5V		−0.1	−1.0	mA
I_{IL2}	Input low current for other inputs, except RF I/O	V_{IN} = 0.5V		−0.05	−0.5	mA
V_{IL}**	Input low threshold				0.8	V
V_{IH}**	Input high threshold		2.0	V		
V_{OL1}	Output low voltage, except RF I/O	I_{OL} = 20mA		0.3	0.5	V
V_{OL2}	Output low voltage for RF I/O	I_{OL} = 10mA		0.3	0.5	V
V_{OH1}	Output high voltage, except RF I/O	V_{OH} = −1mA	2.4	3.5		V
V_{OH2}	Output high voltage for RF I/O	I_{OH} = −100μA	2.4	3.5		V
I_{1D}	Output high drive current except RF I/O	V_{OUT} = 0.8V (Note 3)		−200		mA
I_{0D}	Output low drive current, except RF I/O	V_{OUT} = 2.7V (Note 3)		200		mA
I_{OZ}	Three-state output current (address outputs)	$0.4V \leq V_{OUT} \leq 2.7V$, CS = 2.0V, Mode 4	−50	1.0	50	μA
I_{CC}	Supply current	V_{CC} = MAX		210	285	mA
C_{IN}	Input capacitance ADS, R/$\overline{C}$	T_A = 25°C		8		pF
C_{IN}	Input capacitance all other inputs	T_A = 25°C		5		pF

Switching Characteristics: V_{CC} = 5.0V ± 5.0%, 0°C T_A 75°C See Figure 7 for test load (switches S1 and S2 are closed unless otherwise specified) typicals are for V_{CC} = 5V, T_A = 25°C.

SYMBOL	ACCESS PARAMETER	TEST CONDITIONS	'S408			'S408-2			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 5)	Figure 5a	95	125	160	75	100	130	ns
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 5a,5b	80	105	140	65	90	115	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 5)	Figure 5a	50	63	80	50	63	80	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 5a,5b	40	48	60	40	48	60	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 5)	Figure 5a		98	125		75	100	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 5a,5b		78	105		65	85	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 5)	Figure 5a		27	40		27	40	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 6)	Figure 5a		40	65		40	65	ns
t_{CCDH}	$\overline{CASIN}$ to $\overline{CAS}$ output delay (Mode 6)	Figure 5b	40	54	70	40	54	70	ns
t_{RCV}	$\overline{RASIN}$ to column address valid (Mode 5)	Figure 5a		90	120		30	105	ns
t_{RCV}	$\overline{RASIN}$ to column address valid (Mode 6)	Figure 5a		75	105		70	90	ns
t_{RPDL}	$\overline{RASIN}$ to $\overline{RAS}$ delay	Figures 4a,4b,5a,5b	20	27	35	20	27	35	ns
t_{RPDH}	$\overline{RASIN}$ to $\overline{RAS}$ delay	Figures 4a,4b,5a,5b	15	23	32	15	23	32	ns
t_{APDL}	Address input to output low delay	Figures 4a,4b,5a,5b		25	40		25	40	ns
t_{APDH}	Address input to output high delay	Figures 4a,4b,5a,5b		25	40		25	40	ns
t_{SPDL}	Address strobe to address output low	Figure 4b,4a		40	60		40	60	ns
t_{SPDH}	Address strobe to address output high	Fibure 4b,4a		40	60		40	60	ns
t_{WPDL}	$\overline{WIN}$ to $\overline{WE}$ output delay	Figure 4b	15	25	30	15	25	30	ns
t_{WPDH}	$\overline{WIN}$ to $\overline{WE}$ output delay	Figure 4b	15	30	60	15	30	60	ns
t_{CPDL}	$\overline{CASIN}$ to $\overline{CAS}$ delay (RiC) low in Mode 4)	Figure 4b	32	41	58	32	41	58	ns
t_{CPDH}	$\overline{CASIN}$ to $\overline{CAS}$ delay	Figure 4b	25	39	50	25	39	50	ns
t_{RCC}	Column select to column address valid	Figure 4a		40	58		40	58	ns
t_{RCR}	Row select to row address valid	Figure 4a,4b		40	58		40	58	ns
t_{CTL}	RF I/O low to counter outputs all low	Figure 2			100			100	ns
t_{RFPDL}	$\overline{RASIN}$ to $\overline{RAS}$ delay during refresh	Figure 2	35	50	70	35	50	70	ns
t_{RFPDH}	$\overline{RASIN}$ to $\overline{RAS}$ delay during refresh	Figure 2	30	40	55	30	40	55	ns
t_{RFLCT}	$\overline{RFSH}$ low to counter address valid	CS = X, Figure 2		47	60		47	60	ns
t_{RFHRV}	$\overline{RFSH}$ high to row address valid	Figure 2		45	60		45	60	ns
t_{ROHNC}	$\overline{RAS}$ high to new count valid	Figure 2		30	55		30	55	ns
t_{RLEOC}	$\overline{RASIN}$ low to end-of-count low	C_L = 50pF, Figure 2			80			80	ns
t_{RHEOC}	$\overline{RASIN}$ high to end-of-count high	C_L = 50pF, Figure 2			80			80	ns
t_{RAHI}	Row address hold time (Mode 5)	Figure 5a	30			20			ns
t_{RAH}	Row address hold time (Mode 6)	Figures 5a,5b	20			12			ns
t_{ASC}	Column address setup time (Mode 5)	Figure 5a	8			3			ns
t_{ASC}	Column address setup time (Mode 6)	Figures 5a,5b	6			3			ns
t_{RHA}	Row address held from column select	Figure 4a	10			10			ns
t_{CRS}	$\overline{Casin}$ setup time to $\overline{Rasin}$ high (Mode 6)	Figure 5b	35			35			ns

9

Switching Characteristics: (Cont.)

SYMBOL	ACCESS PARAMETER	TEST CONDITIONS	'S408			'S408-2			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
	THREE-STATE PARAMETER								
t_{ZH}	$\overline{CS}$ low to address output high from HI—Z	Figure 7 R1 = 3.5k R2 = 1.5K		35	60		35	60	ns
t_{HZ}	$\overline{CS}$ high to address output Hi-Z from high	C_L = 15p, Figure 7 R2 = 1k, S1 open		20	40		20	40	ns
T_{ZL}	$\overline{CS}$ low to address output low from Hi-Z	Figure 7 R1 = 3.5k R2 = 1.5k		35	60		35	60	ns
t_{LZ}	$\overline{CS}$ high to address output Hi-Z from low	C_L = 15pF, Figure 7 R1 = 1k, S2 open		25	50		25	50	ns
T_{HZH}	$\overline{CS}$ low to control output high from Hi-Z high	Figure 7 R2 = 750 Ω S1 open		50	80		50	80	ns
t_{HHZ}	$\overline{CS}$ high to control output Hi-Z high from high	C_L = 15pF Figure 7 R2 = 750Ω, S1 open		40	75		45	75	ns
t_{HZL}	$\overline{CS}$ low to control output low from Hi-Z high*	Figure 7, S1, S2 open		45	75		45	75	ns
t_{LHZ}	$\overline{CS}$ high to control output Hi-Z high from low*	C_L = 15pF Figure 7 R2 = 750Ω S1 open		50	80		50	80	ms

*Internally the device contains a 3K resistor in series with a Schottky Diode to V_{CC}.

Note 1: Output load capacitance is typical for 4 banks of 22 DRAMs or 88 DRAMs including trace capacitance. These values are: Q0-Q8, $\overline{WE}$ C_L = 500 pF; $\overline{RAS}$ C_L = 150 pF; $\overline{CAS}$ C_L = 600pF unless otherwise noted.

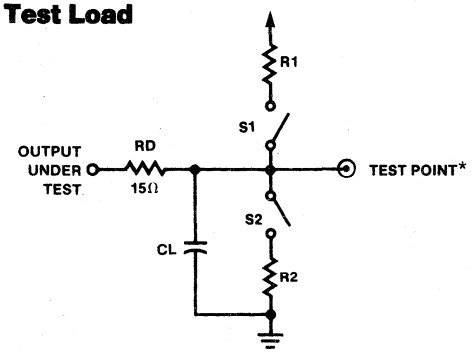
Note 2: All typical values are for T_A = 25° and V_C = 5.0V.

Note 3: This test is provided as a monitor of driver output source and sink current capability. Caution should be exercised in testing this parameter. In testing these parameters a 15Ω resistor should be placed in series with each output under test. One output should be tested at a time and test time should not exceed 1 second.

Note 4: Input pulse 0V to 3.0V, t_R = t_F = 2.5 ns, f = 2.5 MHz, t_{PW} = 200 ns. Input reference point on AC measurements is 1.5V. Output reference points are 2.7V for High and 0.8V for Low.

Note 5: The load capacitance on RF I/O should not exceed 50 pF.

Test Load



R_1, R_2 = 4.7K Except as specified

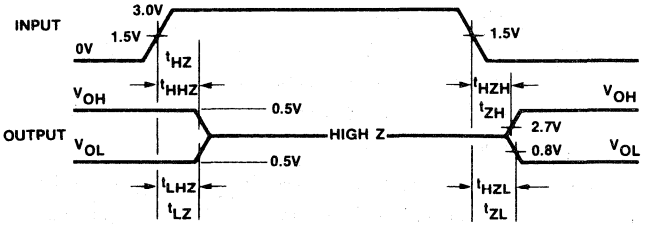


Figure 7. Waveform

* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

256K Dynamic RAM Controller/Driver

SN74S409-2/DP8409A-2
SN74S409/DP8409A

Features/Benefits

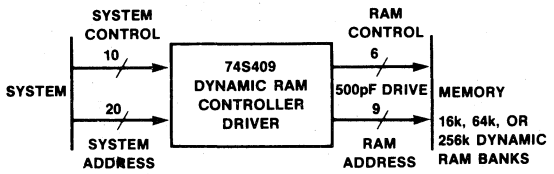
- All DRAM drive functions on one chip have on-chip high-capacitance load drivers (specified up to 88 DRAMs)
- Drives directly all 16K, 64K and 256K DRAMs; capable of addressing up to 1M words
- Propagation delays of 25 nsec typical at 500 pF load
- Supports READ, WRITE and READ-MODIFY-WRITE cycles
- Eight modes of operation support externally-controlled and automatic access and refresh, as well as special memory initialization access
- On-chip 9-bit refresh counter with selectable End-of-Count (127, 255 or 511)
- Direct replacement for National DP8409, DP8409A

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN74S409	48 N, D	Com
SN74S409-2	48 N, D	Com, Speed Option

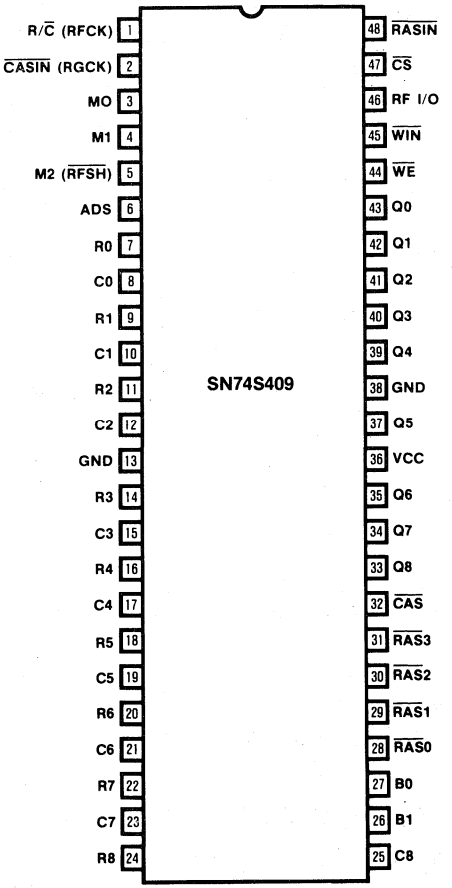
Operating Modes

0	Externally-controlled fresh
1	Auto refresh—forced
2	Automatic burst refresh
3a	All-$\overline{RAS}$ auto write
3b	Externally-controlled All-$\overline{RAS}$ write
4	Externally-controlled access
5	Auto access, slow t_{RAH}, hidden refresh
6	Auto access, fast t_{RAH}
7	Set end of count



Interface Between System and DRAM Banks

Pin Configuration



9

Portions of this Data Sheet are reprinted courtesy of National Semiconductor Corporation.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories MMI

Block Diagram

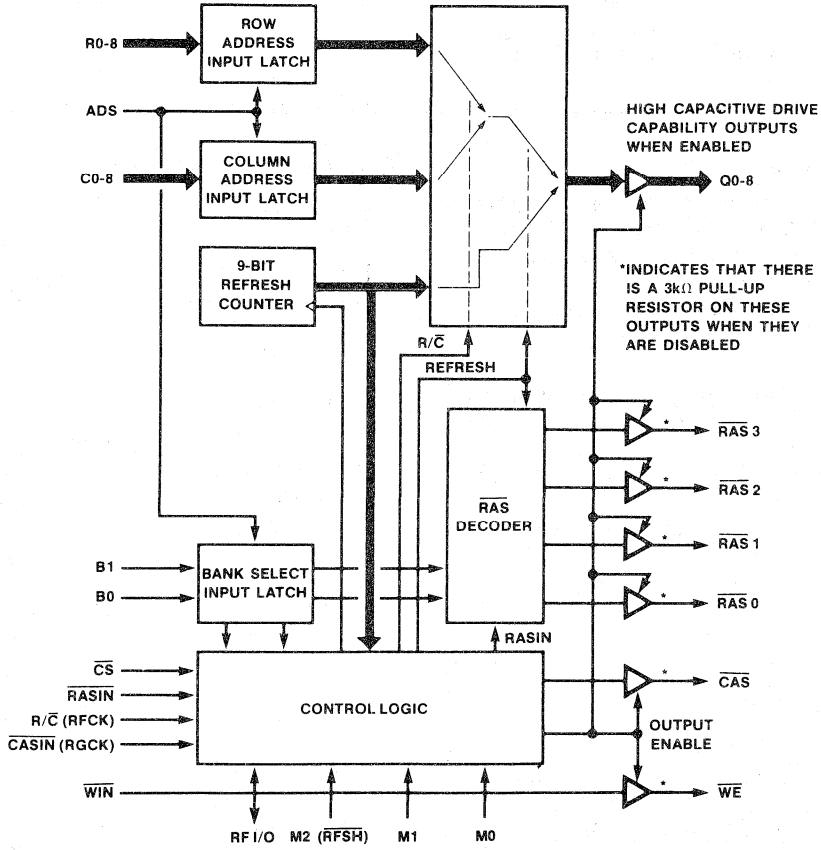


Figure 1. 74S409 Functional Block Diagram

Description

The 74S409 is a Multi-Mode Dynamic RAM Controller/Driver capable of directly driving up to 88 DRAMs. 20 address lines to the 74S409 allow it to address up to 1M words and it can drive 16K, 64K and 256K DRAMs. Since the 74S409 is a one-chip solution (including capacitive-load drivers), it minimizes propagation delay skews, and saves board space.

The 74S409's 8 operating modes offer externally-controlled or on-chip automatic access and refresh. An on-chip refresh counter makes refreshing (either externally or automatically controlled) less complicated; and automatic memory initialization is both simple and fast.

The 74S409 is a 48-pin DRAM Controller/Driver with 9 multiplexed address outputs and 6 control signals. It consists of two 9-bit address latches, a 9-bit refresh counter, and control logic. The 74S409 timing parameters are specified when driving the typical load capitance of 88 DRAMs, including trace capacitance.

The 74S409 can drive up to 4 banks of DRAMs, with each bank comprised of 16Ks, 64Ks or 256Ks. Control signal outputs $\overline{CAS}$ and $\overline{WE}$ are provided with the same driving capability. Each $\overline{RAS}$ output drives one bank of DRAMs so that the four $\overline{RAS}$ outputs are used to select the banks, while $\overline{CAS}$, $\overline{WE}$ and the multiplexed addresses can be connected to all the banks of DRAMs. This leaves the non-selected banks in the standby mode (less than one tenth of the operating power) with the respective data outputs in three-state. Only the bank with its associated $\overline{RAS}$ low will be written to or read from, except in mode 3 where all $\overline{RAS}$ signals go low to allow fast memory initialization.

Pin Definitions

V_{CC} GND, GND—V_{CC} = 5V ± 5%. The three supply pins have been assigned to the center of the package to reduce voltage drops, both DC and AC. There are also two ground pins to reduce the low level noise. The second ground pin is located two pins from V_{CC}, so that decoupling capacitors can be inserted directly next to these pins. It is important to adequately decouple this device, due to the high switching currents that will occur when all 9 address bits change in the same direction simultaneously. A recommended solution is a 1-μF multilayer ceramic capacitor in parallel with a low-voltage tantalum capacitor, both connected close to pins 36 and 38 to reduce lead inductance.

R0-R8: Row Address Inputs.

C0-C8: Column Address Inputs.

B0, B1: Bank Select Inputs—Strobed by ADS. Decoded to enable one of the $\overline{RAS}$ outputs when $\overline{RASIN}$ goes low, in modes 4-6. In mode 7 B0, B1 are used to define End-of-Count (see table 3), and select mode 3a or 3b.

Q0-Q8: Multiplexed Address Outputs—Selected from the Row Address Input Latch, the Column Address Input Latch, or the Refresh Counter.

$\overline{RASIN}$: Row Address Strobe Input—Enables selected $\overline{RAS}_n$ output when M2 ($\overline{RFSH}$) is high (modes 4-6), and all $\overline{RAS}_n$ outputs in modes 0 and 3. $\overline{RASIN}$ input is disabled in modes 1 and 2.

R/$\overline{C}$ (RFCK)—In Auto-Refresh Mode this pin is the external Refresh Clock Input: one refresh cycle has to be performed each clock period. In all other modes it is Row/$\overline{Column}$ Select Input, selecting either the row or column address input latch onto the output bus.

$\overline{CASIN}$ (RGCK)—In modes 1, 2 and 3a, this pin is the $\overline{RAS}$ Generator Clock input. In all other modes it is $\overline{CASIN}$ (Column Address Strobe Input), which inhibits $\overline{CAS}$ output when high in Modes 3b and 4. In Mode 6 it can be used to prolong $\overline{CAS}$ output.

ADS: Address (Latch) Strobe Input—Strobes Input Row Address, Column Address, and Bank Select Inputs into respective latches when high; latches on High-to-Low transition.

$\overline{CS}$: Chip Select Input—three-state's the Address Outputs and puts the control signal into a high-impedance logic "1" state when high (unless refreshing in one of the Refresh Modes). Enables all outputs when low.

M0, M1, M2 ($\overline{RFSH}$): Mode Control Inputs—These 3 control pins determine the 8 major modes of operation of the 74S409 as depicted in Table 2.

RF I/O $\overline{RFRQ}$ — This I/O pin functions as a Reset Counter Input when set low from an external open-collector gate, or as a flag output. The flag goes active-low in Modes 0, 2 and 3a when the End-of-Count output is at 127, 255, or 511 (see Table 3). In Auto-Refresh Mode (mode 5) it is the $\overline{Refresh}$ $\overline{Request}$ ($\overline{RFRQ}$) output.

BANK SELECT (STROBED BY ADS)		ENABLED $\overline{RAS}_n$
B1	B0	
0	0	$\overline{RAS}_0$
0	1	$\overline{RAS}_1$
1	0	$\overline{RAS}_2$
1	1	$\overline{RAS}_3$

Table 1. Memory Bank Decode

$\overline{WIN}$: Write Enable Input.

$\overline{WE}$: Write Enable Output—Buffered output from $\overline{WIN}$.

$\overline{CAS}$: Column Address Strobe Output—In Modes 3a, 5, and 6, $\overline{CAS}$ transitions low following valid column address. In Modes 3b and 4, it goes low after R/$\overline{C}$ goes low, or follows $\overline{CASIN}$ going low if R/$\overline{C}$ is already low. $\overline{CAS}$ is high during refresh.

$\overline{RAS}$ 0-3: Row Address Strobe Outputs—When M2($\overline{RFSH}$) is high (modes 4-6), the selected row address strobe output (decoded from signals B0, B1) follows the $\overline{RASIN}$ input. When M2 ($\overline{RFSH}$) is low (modes 0-3) all $\overline{RAS}_n$ outputs go low together following $\overline{RASIN}$ going low in modes 0 and 3 and automatically in modes 1 and 2.

Input Addressing

The address block consists of a row-address latch, a column-address latch, and a resettable refresh counter.

The address latches are fall-through when ADS is high and latch when ADS goes low. If the address bus contains valid address until after the valid address time, ADS can be permanently high. Otherwise ADS must go low while the address is still valid.

In normal memory-access operation, $\overline{RASIN}$ and R/$\overline{C}$ are initially high. When the address inputs are enabled into the address latches (modes 3-6) the row addresses appear on the Q outputs. The Address Strobe also inputs the bank-select address, (B0 and B1). If $\overline{CS}$ is low, all outputs are enabled. When $\overline{CS}$ goes high, the address outputs go three-state and the control outputs first go high through a low impedance, and then are held by an on-chip high impedance. This allows output paralleling with other 74S409s for multi-addressing. All outputs go active about 50ns after the chip is selected again. If $\overline{CS}$ is high, and a refresh cycle begins, all the outputs become active until the end of the refresh cycle.

Drive Capability

The 74S409 has timing parameters that are specified with up to 600pF loads for $\overline{CAS}$ and $\overline{WE}$, 500pF loads for Q_0-Q_8, and 150pF loads for $\overline{RAS}_n$ outputs. In a typical memory system this is equivalent to about 88 5V-only DRAMs, with trace lengths kept to a minimum. Therefore, the chip can drive four banks each of 16 or 22 bits, or two banks of 32 or 39 bits, or one bank of 64 or 72 bits.

Less loading will slightly reduce the timing parameters, and more loading will increase the timing parameters, according to the graph of Figure 14. The AC performance parameters are specified with the typical load capacitance of 88 DRAMs. This graph can be used to extrapolate the variations expected with other loading.

74S409 Driving Any 16K, 64K or 256K DRAMs

The 74S409 can drive any 16K, 64K, or 256K DRAMs. The on-chip 9-bit counter with selectable End-of-Count can support refresh of 128, 256 and 512 rows, while the 9 address and 4 $\overline{RAS}_n$ outputs can address 4 banks of 16K, 64K or 256K DRAMs.

Read, Write, and Read-Modify-Write Cycles

The output signal, $\overline{WE}$, determines what type of memory access cycle the memory will perform. If $\overline{WE}$ is kept high while $\overline{CAS}$ goes low, a read cycle occurs. If $\overline{WE}$ goes low before $\overline{CAS}$ goes low, a write cycle occurs and data at DI (DRAM input data) is written into the DRAM as $\overline{CAS}$ goes low. If $\overline{WE}$ goes low later than t_{CWD} after $\overline{CAS}$ goes low, first a read occurs and DO (DRAM output data) becomes valid; then data DI is written into the same address in the DRAM when $\overline{WE}$ goes low. In this read-modify-write case, DI and DO cannot be linked together. The type of cycle is therefore controlled by $\overline{WE}$, which follows $\overline{WIN}$.

Power-Up Initialize

When V_{CC} is first applied to the 74S409, an internal pulse clears the refresh counter, the internal control flip-flops, and sets the End-of-Count of the refresh counter to 127 (which may be changed via Mode 7). As V_{CC} increases to about 2.3 volts, it holds the output control signals at a level of one Schottky diode-drop below V_{CC}, and the output address to three-state. As V_{CC} increases above 2.3 volts, control of these outputs is granted to the system.

74S409 Functional Modes Description

The 74S409 operates in 8 different functional modes selected by signals M_0,M_1,M_2. Mode 3 splits further to modes 3a and 3b determined by signals B_0,B_1 in mode 7.

Mode 0 and mode 1 are generally used as Refresh modes for mode 4 and mode 5 respectively, and therefore will be described as mode-pairs 0,4 and 1,5.

Mode 6 is a fast access made for very fast DRAMs and mode 7 is used only to determine choice of mode 3a or 3b and for setting End-of-Count for the refresh modes.

MODE	($\overline{RFSH}$) M2	M1	M0	MODE OF OPERATION	CONDITIONS
0	0	0	0	Externally-controlled refresh	RF I/O = $\overline{EOC}$
1	0	0	1	Auto refresh—forced	RF I/O = Refresh request ($\overline{RFRQ}$)
2	0	1	0	Automatic burst refresh	RF I/O = $\overline{EOC}$
3a*	0	1	1	All-$\overline{RAS}$ auto write	RF I/O = $\overline{EOC}$; all $\overline{RAS}$ active
3b*	0	1	1	Externally-controlled All-$\overline{RAS}$ write	All-$\overline{RAS}$ active
4	1	0	0	Externally-controlled access	Active $\overline{RAS}$ defined by Table 2
5	1	0	1	Auto access, slow t_{RAH}, hidden refresh	Active $\overline{RAS}$ defined by Table 2
6	1	1	0	Auto access, fast t_{RAH}	Active $\overline{RAS}$ defined by Table 2
7	1	1	1	Set end of count; determines mode 3a or 3b	See Table 3 for Mode 7

*Mode 3a is selected by setting B_0,B_1 to 01, 00, or 10 in mode 7.
*Mode 3b is selected by setting B_1,B_0 to 11 in mode 7.

Table 2. 74S409 Mode Select Options

Mode 0 — Externally-Controlled Refresh
Mode 4 — Externally-Controlled Access

Modes 0 and 4 facilitate external control of all timing parameters associated with the DRAMs. These modes are independent modes of operation though generally used together in the same application as shown in Figure 2.

Mode 0—Externally-Controlled Refresh

In this mode the input address latches are disabled from the address outputs and the refresh counter is enabled. All $\overline{RAS}$ outputs go low following $\overline{RASIN}$ and refresh the enabled row in all four banks. $\overline{CASIN}$ and R/$\overline{C}$ inputs are not used and $\overline{CAS}$ is inhibited. The refresh counter increments when either $\overline{RASIN}$ or M2 ($\overline{RFSH}$) switch high while the other is still low.

RF I/O goes low when the count equals End-of-Count (as set in mode 7), and $\overline{RASIN}$ is low. The 9-bit counter will always roll-over to zero at 512, regardless of End-of-Count. However, the counter can be reset at any time by driving RF I/O low through an external open-collector.

During refresh, $\overline{RASIN}$ and M2 ($\overline{RFSH}$) can transition low simultaneously because the refresh counter becomes valid on the output bus t_{RFLCT} after $\overline{RFSH}$ goes low, which is a shorter time than t_{RFPDL}. This means the counter address is valid on the Q outputs before $\overline{RAS}$ occurs on all $\overline{RAS}$ outputs, strobing the counter address into that row of all the DRAMs (see Figure 2.). To perform externally-controlled burst refresh, $\overline{RFSH}$ initially can again have the same edge as $\overline{RASIN}$, but then maintains a low state, since $\overline{RASIN}$ going low-to-high increments the counter (performing the burst refresh).

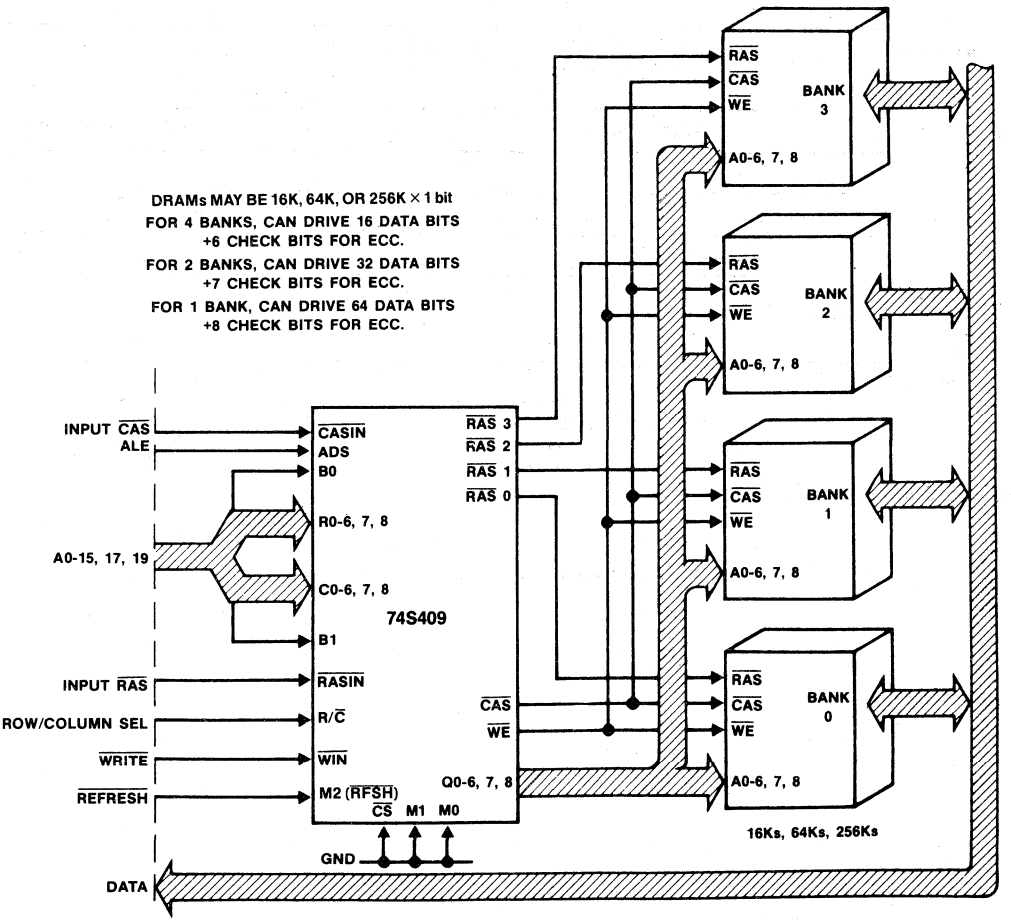


Figure 2. Typical Application of 74S409 Using Externally-Controlled Access and Refresh in Modes 0 and 4

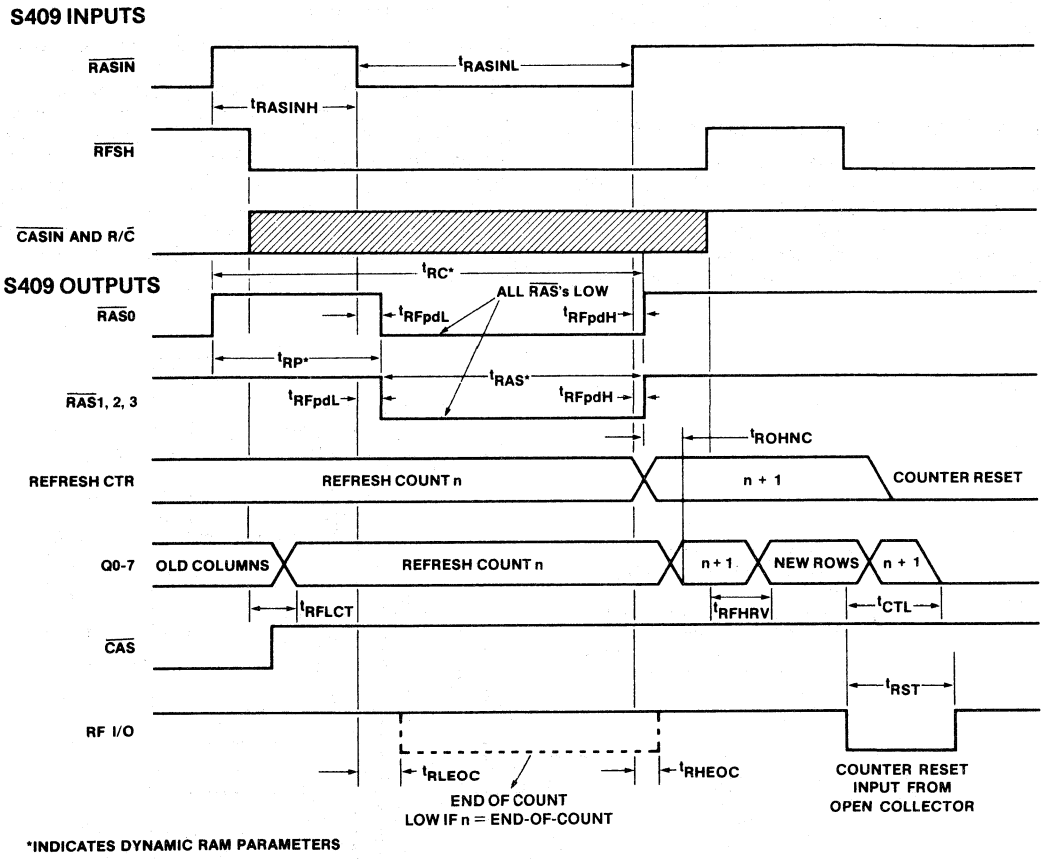


Figure 3. External Control Refresh Cycle (Mode 0)

Mode 4 — Externally-Controlled Access

This mode facilitates externally controlling all access-timing parameters associated with the DRAMs. Figures 4 and 5 show the timing for read and write cycles.

Output Address Selection

In this mode $\overline{CS}$ has to be low at least 50 nsec before the outputs will be valid. With R/$\overline{C}$ high, the row address latch contents are transfered to the multiplexed address bus output Q0-Q8. $\overline{RASIN}$ can go low after the row addresses have been set up on Q0-Q8, and enables one $\overline{RAS}$ output selected by signals B0, B1 to strobe the Q outputs into the desired bank of memory. After the row-address hold-time of the DRAMs, R/$\overline{C}$ can go low so that about 40 nsec later, the column address appears on the Q output.

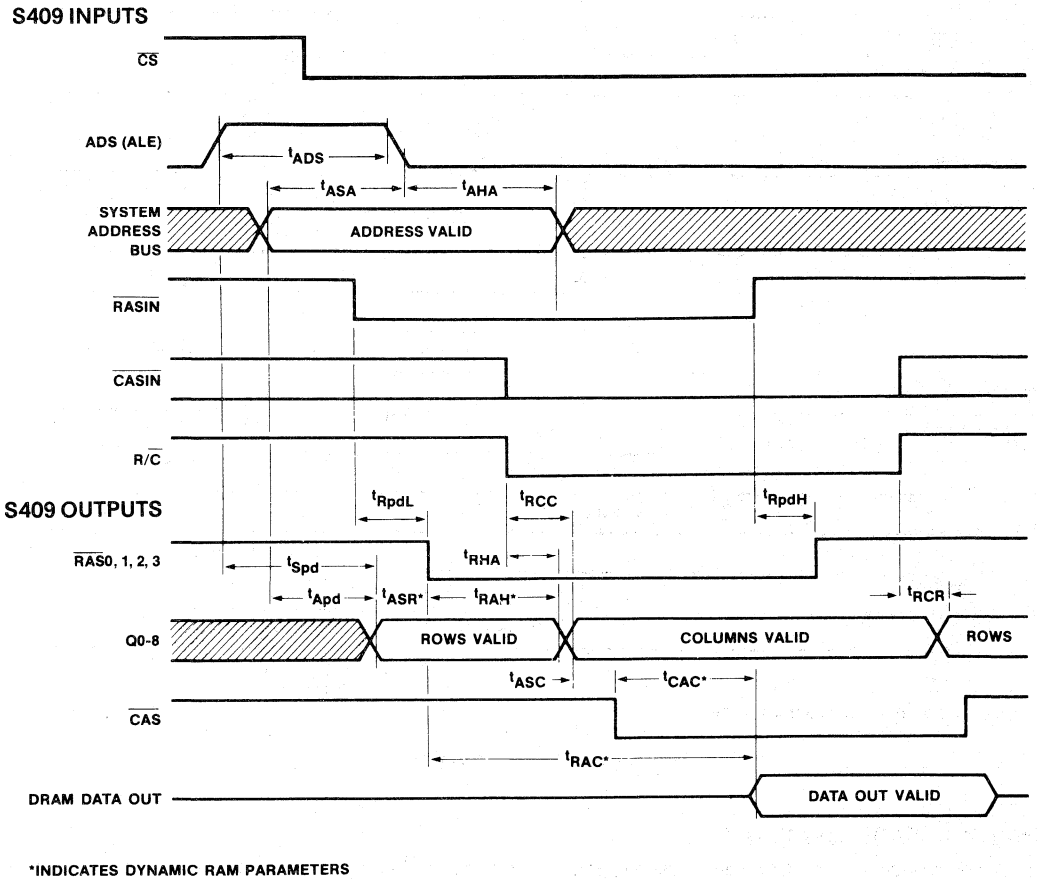


Figure 4. Read Cycle Timing (Mode 4)

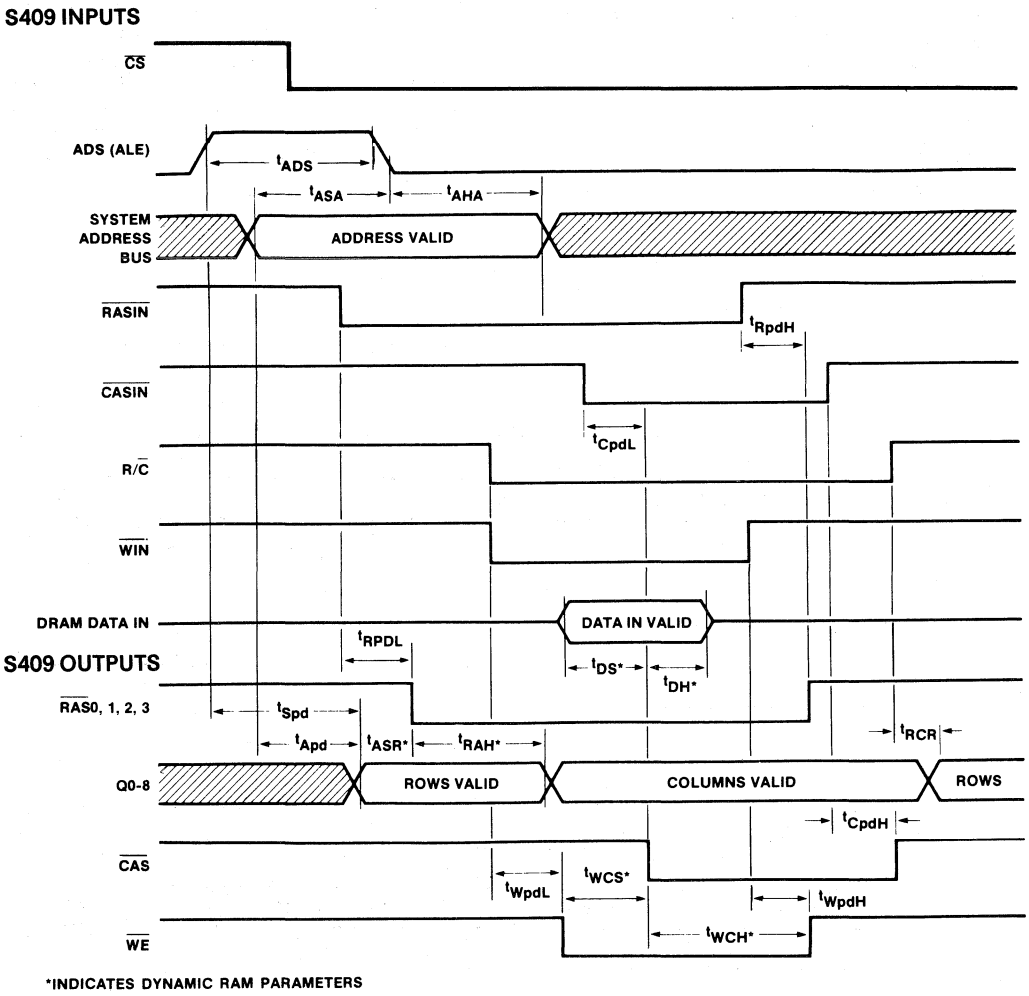


Figure 5. Write Cycle Timing (Mode 4)

Automatic $\overline{CAS}$ Generation

In a normal memory access cycle $\overline{CAS}$ can be derived from inputs $\overline{CASIN}$ or R/$\overline{C}$. If $\overline{CASIN}$ is high, then R/$\overline{C}$ going low switches the address output drivers from rows to columns. $\overline{CASIN}$ then going low causes $\overline{CAS}$ to go low approximately 40 ns later, allowing $\overline{CAS}$ to occur at a predictable time (see Figure 5). For maximum system speed, $\overline{CASIN}$ can be kept low, since $\overline{CAS}$ will automatically occur approximately 60 ns after R/$\overline{C}$ goes low (see Figure 4). Most DRAMs have a column address set-up time before $\overline{CAS}$ (t_{ASC}) of 0 ns or −10 ns. In other words, a t_{ASC} greater than 0 ns is safe. This feature reduces timing-skew problems, thereby improving access time of the system.

Fast Memory Access

For faster access time, R/$\overline{C}$ can go low a time delay ($t_{RPDL} + t_{RAH} - t_{RHA}$) after $\overline{RASIN}$ goes low, where t_{RAH} is the Row-Address hold-time of the DRAM, and $\overline{CASIN}$ can go low $t_{RCC} - t_{CPOL} + t_{ASC}$ (min.) after R/$\overline{C}$ goes low (see t_{DiF1}, t_{DiF2} switching characteristics).

Mode 1 – Automatic Forced Refresh Mode 5 – Automatic Access with Hidden Refresh

Mode 1 and Mode 5 are generally used together incorporating the advantages of the "hidden refresh" performed in mode 5 with the possibiity to force a refresh by changing to mode 1. An advantage of the Automatic Access over the Externally-Controlled Access is the reduced memory access time, due to the fact that the output control signals are derived internally from one input signal ($\overline{RASIN}$).

Hidden and Forced Refresh

Hidden Refresh is a term describing memory refresh performed when the system does not access the portion of memory controlled by the 74S409 ($\overline{CS}$ = 1). A hidden refresh will occur once per Refresh Clock (RFCK) cycle provided $\overline{CS}$ went high and $\overline{RASIN}$ went low. If no hidden refresh occurred while RFCK was high, the RF I/O ($\overline{RFRQ}$) goes low immediately after RFCK goes low, indicating to the system when a forced refresh is required. The system must allow a forced refresh to take place while RFCK is low by driving M2 ($\overline{RFSH}$) low, thereby changing mode of operation to Mode 1.

The Refresh Request on RF I/O ($\overline{RFRQ}$) is terminated as soon as $\overline{RAS}$ goes low, indicating to the system that the foced refresh has been done. The system should then drive M2 ($\overline{RFSH}$) high, changing the mode of operation back to Mode 5 (see Figure 6).

Mode 1 – Automatic Forced Refresh

In Mode 1, the R/$\overline{C}$ (RFCK) pin functions as RFCK (refresh cycle clock) instead of R/$\overline{C}$, and $\overline{CAS}$ remains high. If RFCK is kept permanently high then whenever M2 ($\overline{RFSH}$) goes low, an externally-controlled refresh will occur and all $\overline{RAS}$ outputs will follow $\overline{RASIN}$, strobing the refresh counter contents to the DRAMs. The RF I/O pin will always output high, but can be set low externally through an open-collector driver, to reset the refresh counter.

If RFCK is an input clock, one and only one refresh cycle must take place every RFCK cycle. If a hidden refresh does not occur while RFCK is high, in Mode 5, then RF I/O (Refresh Request) goes low immediately after RFCK goes low, indicating to the system that a forced refresh is required. The system must allow a forced refresh to take place while RFCK is low The Refresh Request signal on RF I/O may be connected to a Hold or Bus Request input to the system. The system acknowledges the Hold or Bus Request when ready, and outputs Hold Acknowledge or Bus Request Acknowledge. If this is connected to the M2 ($\overline{RFSH}$) pin, a forced-refresh cycle will be initiated by the S409, and $\overline{RAS}$ will be internally generated on all four $\overline{RAS}$ outputs, strobing the refresh counter contents on the address ouputs into all the DRAMs. An external $\overline{RAS}$ Generator Clock (RGCK) is requred for this function. It is fed to the $\overline{CASIN}$ (RGCK) pin, and may be up to 10 MHz. Whenever M2 goes low (inducing a forced refresh), $\overline{RAS}$ remains high for one to two periods of RGCK, depending on when M2 goes low relative to the high-to-low triggering edge of RGCK; $\overline{RAS}$ then goes low for two periods, performing a refresh on all banks. In order to obtain the minimum delay from M2 going low to $\overline{RAS}$ going low, M2 should go low t_{RFSRG} before the next falling edge of RGCK. The Refresh Request on RF I/O is terminated as $\overline{RAS}$ begins, so that by the time the system has acknowledged the removal of the request and disabled its Acknowledge, (i.e., M2 goes high), Refresh $\overline{RAS}$ will have ended, and normal operations can begin again in the Automatic Access mode (Mode 5). If it is desired that Refresh $\overline{RAS}$ end in less than 2 periods of RGCK from the time $\overline{RAS}$ went low, then M2 may go high earlier than t_{FRQH} after RF I/O goes high and $\overline{RAS}$ will go high t_{RFRH} after M2.

Mode 5 – Automatic Access with Hidden Refresh

In this mode all address outputs, $\overline{RAS}$ and $\overline{CAS}$ are initiated from $\overline{RASIN}$ making the DRAM access appear similar to static RAM access. The hidden refresh feature enables DRAM refresh accomplished with no time-loss to the system.

Provided the input address is valid as ADS goes low, $\overline{RASIN}$ can go low any time after ADS. This is because the selected $\overline{RAS}$ occurs typically 27 ns later, by which time the row address is already valid on the address output of the 74S409. The Address Set-Up time (t_{ASR}), is 0 ns on most DRAMs. The 74S409 in this mode (with ADS and $\overline{RASIN}$ edges simultaneously applied) produces a minimum t_{ASR} of 0 ns. This is true provided the input address was valid t_{ASR} before ADS went low (see Figure 7).

Next, the row address is disabled t_{RAH} after $\overline{RAS}$ goes low (30 ns minimum); in most DRAMs, t_{RAH} minimum is less than 30 ns. The column address is then set up and (t_{ASC} later,) $\overline{CAS}$ occurs. The only other control input required is $\overline{WIN}$. When a write cycle is required, $\overline{WIN}$ must go low at least 30 ns before $\overline{CAS}$ is output low.

This gives a total typical delay from: input address valid to $\overline{RASIN}$ (15 ns); to $\overline{RAS}$ (27 ns); to rows held (50 ns); to columns valid (25 ns); to $\overline{CAS}$ (23 ns) = 140 ns (that is, 125 ns from $\overline{RASIN}$). All of these typical figures are for heavy capacitive loading, of approximately 88 DRAMs.

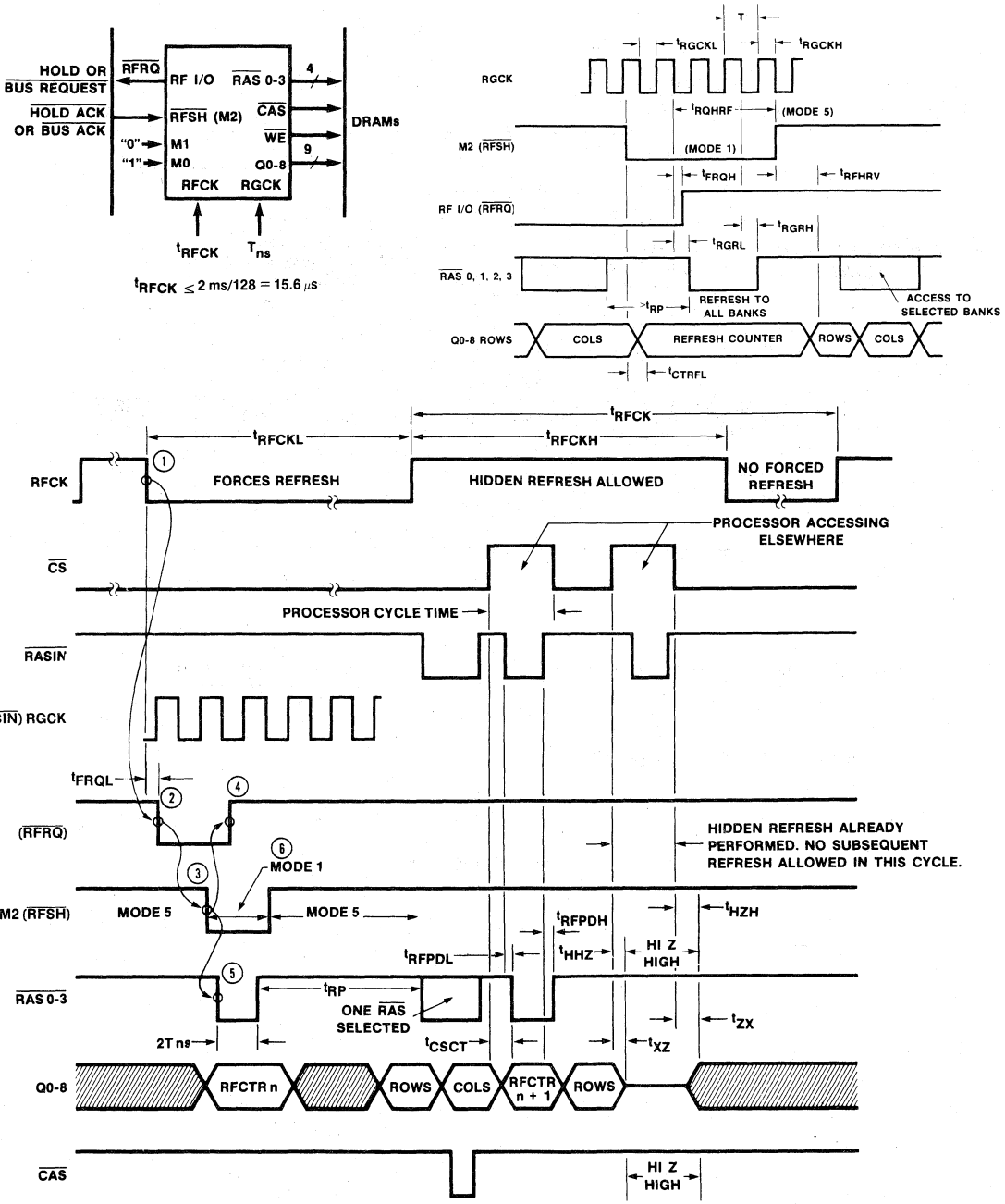
Refreshing

In this mode R/$\overline{C}$ (RFCK) functions as Refresh Clock and $\overline{CASIN}$ (RGCK) functions as $\overline{RAS}$ Generator Clock.

One refresh cycle must occur during each refresh clock period, and then the refresh address must be incremented before the next refresh cycle. As long as 128 rows are refreshed every 2 ms (one row every 16 μs), all 16K and 64K DRAMs will be correctly refreshed. The cycle time of RFCK must, therefore, be less than 16 μs. RFCK going high sets an internal refresh-request flipflop. First the 74S409 will attempt to perform a hidden refresh so that the system thruput will not be affected. If, during the time RFCK is high, $\overline{CS}$ on the 74S409 goes high and $\overline{RASIN}$ occurs, a hidden refresh will occur. In this case, $\overline{RASIN}$ should be considered a common read/write strobe. In other words, if the processor is accessing elsewhere (other than the DRAMs) while RFCK is high, the 74S409 will perform a refresh. The refresh counter is enabled to the address outputs whenever $\overline{CS}$ goes high with RFCK high, and all $\overline{RAS}$ outputs follow $\overline{RASIN}$. If a hidden refresh is taking place as RFCK goes low, the refresh continues. At the start of the hidden refresh, the refresh-request flipflop is reset so on further refresh can occur until the next RFCK period starts with the positive-going edge of RFCK (see Figure 6). $\overline{RASIN}$ should go low at least 20 ns before RFCK goes low, to ensure occurrence of the hidden refresh.

To determine the probability of a hidden refresh occurring, goes low, (and the internal-request flipflop has not been for 8μs, then the system has 20 chances to not select the 74S409. If during this time a hidden refresh did not occur, then the 74S409 forces a refresh while RFCK is low, but the system chooses when the refresh takes place. After RFCK goes low, (and the internal-request flip-flop has not been reset), RF I/O goes low indicating that a refresh is requested to the system. Only when the system acknowledges this request by setting M2 ($\overline{RFSH}$) low does the 74S409 initiate a forced refresh (which is performed automatically). Refer to Mode 1, and Figure 6. The internal refresh request flipflop is then reset.

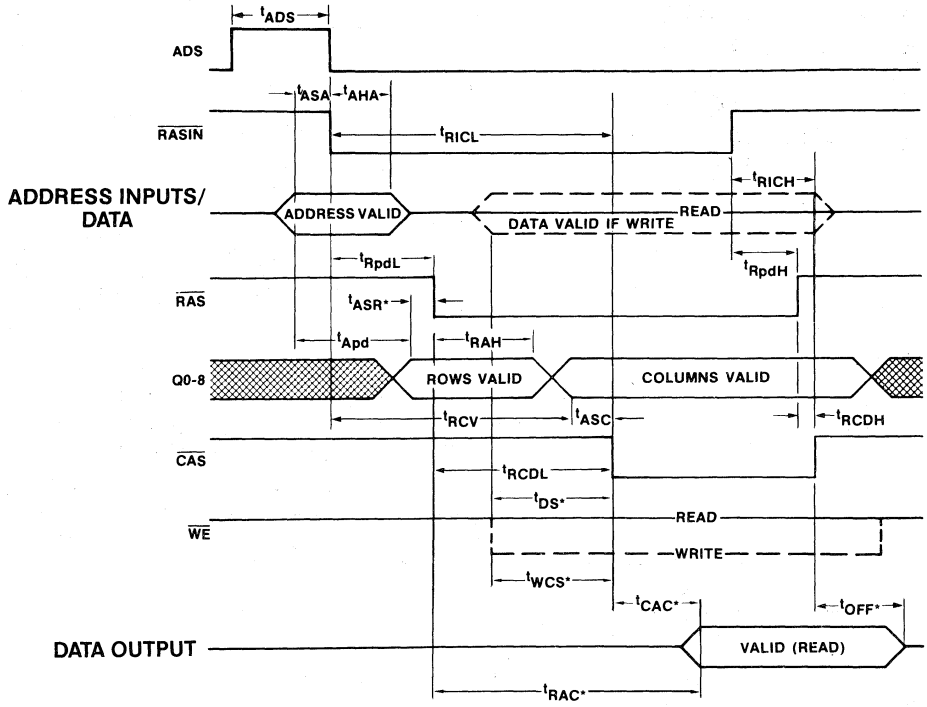
Figure 6 illustrates the refresh alternatives in Mode 5. If a hidden refresh has occurred and $\overline{CS}$ again goes high before RFCK goes low, the chip is deselected. All the control signals go high-impedance high (logic "1") and the address outputs go three-state until $\overline{CS}$ again goes low. This mode (combined with Mode 1) allows very fast access, and automatic refreshing (possibly not even slowing down the system), with no extra ICs. Careful system design can, and should, provide a higher probability of hidden refresh occurring. The duty cycle of RFCK need not be 50 percent; in fact, the low-time should be designed to be a minimum. This is determined by the worst-case time (required by the system) to respond to the 74S409's forced-refresh request.



*INDICATES DYNAMIC RAM PARAMETERS

1. RFCK GOES LOW
2. RFRQ GOES LOW IN NO HIDDEN REFRESH OCCURRED WHILE RFCK WAS HIGH
3. M2 (RFSH) DRIVEN LOW EXTERNALLY
4. REFRESH REQUEST RELEASED
5. RAS 0-3 GO LOW TO PERFORM REFRESH
6. M2 (RFSH) RELEASED

Figure 6. Hidden Refreshing (Mode 5) and Forced Refreshing (Mode 1) Timing



*INDICATES DYNAMIC RAM PARAMETERS

Figure 7. Mode 5 Timing

Mode 2 – Automatic Burst Refresh

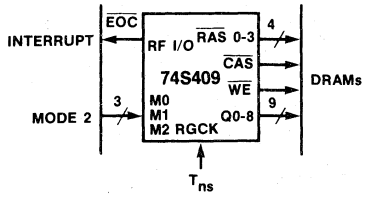
This mode is normally used before and/or after a DMA operation to ensure that all rows remain refreshed, provided the DMA transfer takes less than 2 ms (see Figure 8). When the 74S409 enters this mode, $\overline{CASIN}$ (RGCK) becomes the $\overline{RAS}$ Generator Clock (RGCK), and $\overline{RASIN}$ is disabled. $\overline{CAS}$ remains high, and RF I/O goes low when the refresh counter has reached the selected End-of-Count and the last $\overline{RAS}$ has ended. RF I/O then remains low until the Auto-Burst Refresh mode is terminated. RF I/O can therefore be used as an interrupt to indicate the End-of-Burst condition.

The signal on all four $\overline{RAS}$ outputs is just a divide-by-four of RGCK; in other words, if RGCK has a 100 ns period, $\overline{RAS}$ is high and low for 200 ns each cycle. The refresh counter increments at the end of each $\overline{RAS}$, starting from the count it contained when the mode was entered. If this was zero then for a RGCK with a 100 ns period with End-of Count set to 127, RF I/O will go low after 128 x 0.4μs, or 51.2μs. During this time, the system may be performing operations that do not involve DRAM. If all rows need to be burst refreshed, the refresh counter may be cleared by setting RF I/O low externally before the burst begins.

Burst-mode refreshing is also useful when powering down systems for long periods of time, but with data retention still required while the DRAMs are in standby. To maintain valid refreshing, power can be applied to the 74S409 (set to Mode 2), causing it to perform a complete burst refresh. When end-of-bust occurs (after 26 μs), power can then be removed from the 74S409 for 2 ms, consuming an average power of 1.3% of normal operating power. No control signal glitches occur when switching power to the 74S409.

Mode 3a – All-$\overline{RAS}$ Automatic Write

Mode 3a is useful at system initialization, when the memory is being cleared (i.e., with all-zeroes in the data field and the corresponding check bits for error detection and correction). This requires writing the same data to each location of memory (every row of each column of each bank). All $\overline{RAS}$ outputs are activated, as in refresh, and so are $\overline{CAS}$ and $\overline{WE}$. To write to all four banks simultaneously, every row is strobed in each column, in sequence, until data has been written to all locations. The refresh counter is used to address the rows, and $\overline{RAS}$ is low for two RGCK cycles and high for two cycles.



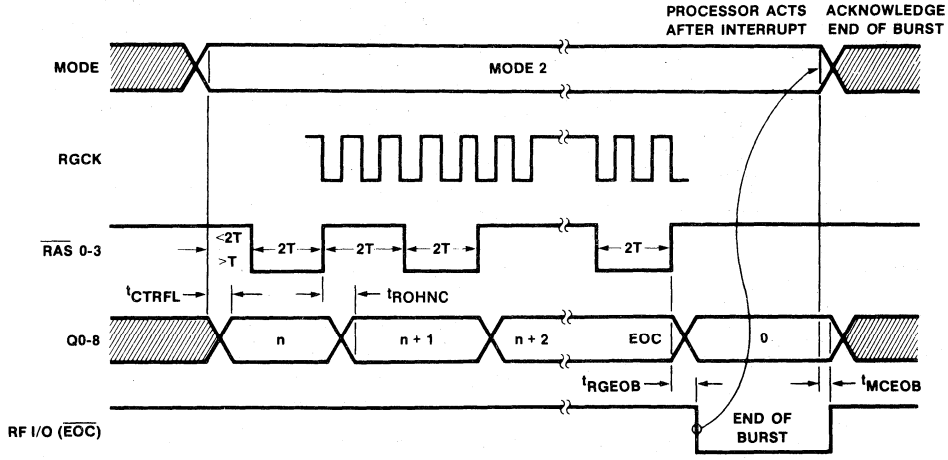
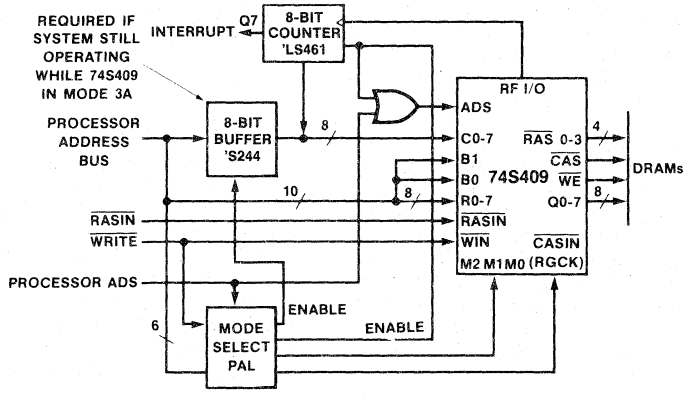


Figure 8. Auto-Burst Mode, Mode 2

To select this mode, B1 and B0 must have previously been set to 00, 01, or 10 in Mode 7, depending on the DRAM size. For example, for 16K DRAMs, B1 and B0 are 00. For 64K DRAMs, B1 and B0 are 01.

In this mode, R/$\overline{C}$ is disabled, $\overline{WE}$ is permanently enabled low, and $\overline{CASIN}$ (RGCK) becomes RGCK. RF I/O goes low whenever the refresh counter is 127, 255, or 511 (as set by End-of-Count in Mode 7), and the $\overline{RAS}$ outputs are active.



74S409 Extra Circuitry Required for All-$\overline{RAS}$ Auto Write Mode, Mode 3a

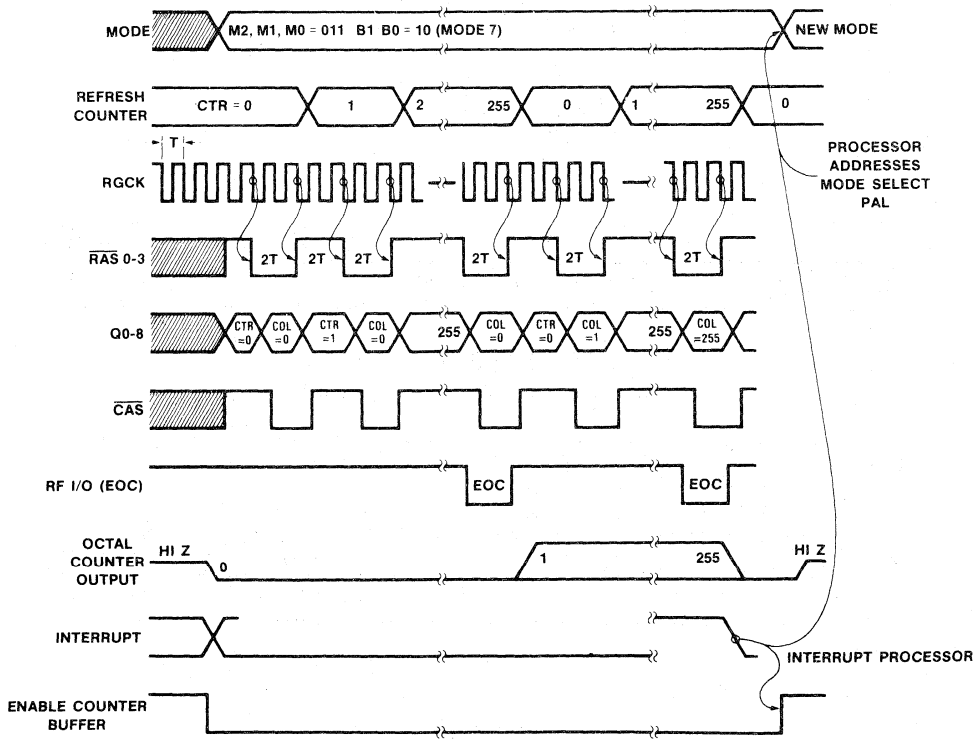


Figure 9. 74S409 All-$\overline{RAS}$ Auto Write Mode, Mode 3a, Timing Waveform

Mode 3b — Externally-Controlled All-$\overline{RAS}$ Write

To select this mode, B1 and B0 must first have been set to 11 in Mode 7. This mode is useful at system initialization, but under processor control. The memory address is provided by the processor, which also performs the incrementing. All four $\overline{RAS}$ outputs follow $\overline{RASIN}$ (supplied by the processor), strobing the row address into the DRAMs. R/$\overline{C}$ can now go low, while $\overline{CASIN}$ may be used to control $\overline{CAS}$ (as in the Externally-Controlled Access mode), so that $\overline{CAS}$ strobes the column address contents into the DRAMs. At this time $\overline{WE}$ should be low, causing the data to be written into all four banks of DRAMs. At the end of the write cycle, the input address is incremented and latched by the 74S409 for the next write cycle. This method is slower than Mode 3a, since the processor must perform the incrementing and accessing. Thus the processor is occupied during RAM initialization, and is not free for other initialization operations. However, initialization sequence timing is under system control, which may provide some system advantage.

Mode 4 — Externally-Controlled Access

Mode 4 is described in with mode 0 in section "Mode 0 and Mode 4."

Mode 5 — Automatic Access with Hidden Refresh

See description of mode 0 and mode 5.

Mode 6 — Fast Automatic Access

The Fast Automatic Access mode can only be used with fast DRAMs which have t_{RAH} of 10 nsec-15nsec. The typical $\overline{RASIN}$ to $\overline{CAS}$ delay is 105nsec. In this mode $\overline{CAS}$ can be extended after $\overline{RAS}$ goes high to extend the data output valid time. This feature is useful in applications with short cycles where $\overline{RAS}$ has to be terminated as soon as possible to meet the precharge (t_{RP}) requirements of the DRAM.

Mode 6 timing is illustrated in Figures 10 and 11. Provided that the input address is valid as ADS goes low, $\overline{RASIN}$ can go low any time after ADS. This is because the selected $\overline{RAS}$ occurs typically 27 ns later, by which time the row address is already valid on the address output of the 74S409. The Address Set-Up time (t_{ASR}), is 0 ns on most DRAMs. The 74S409 in this mode (with ADS and $\overline{RASIN}$ edges simultaneously applied) produces a minimum t_{ASR} of 0 ns. This is true provided the input address was valid t_{ASA} before ADS went low (see Figure 10).

Next, the row address is disabled t_{RAH} after $\overline{RAS}$ goes low (20 ns minimum); the column address is then set up and t_{ASC} later, $\overline{CAS}$ occurs. The only other control input required is $\overline{WIN}$. When a write cycle is required, $\overline{WIN}$ must go low at least 30 ns before $\overline{CAS}$ is output low.

This gives a total typical delay from: input address valid to $\overline{RASIN}$ (15 ns); to $\overline{RAS}$ (27 ns): to rows valid (50 ns); to columns valid (25 ns); to $\overline{CAS}$ (23 ns) = 140 ns (that is, 125 ns from $\overline{RASIN}$). All of these typical figures are for heavy capacitive loading, of approximately 88 DRAMs.

This mode is therefore extremely fast. The external timing is greatly simplified for the memory system designer: the only system signal required is $\overline{RASIN}$.

In this mode, the R/$\overline{C}$ (RFCK) pin is not used, but $\overline{CASIN}$ (RGCK) is used as $\overline{CASIN}$ to allow an extended $\overline{CAS}$ after $\overline{RAS}$ has already terminated. Refer to Figure 11.

Mode 7 — Set End-of-Count (3a, 3b select)

The End-of-Count can be externally selected in Mode 7, using ADS to strobe in the respective value of B1 and B0 (see Table 3). With B1 and B0 the same $\overline{EOC}$ is 127; with B1 = 0 and B0 = 1, $\overline{EOC}$ is 255; and with B1 = 1 and B0 = 0, $\overline{EOC}$ is 511. This selected value of $\overline{EOC}$ will be used until the next Mode 7 selection. At power-up the $\overline{EOC}$ is automatically set to 127 (B1 and B0 set to 11).

When B_1,B_2 are set to 11 in mode 7, mode 3b will be selected if mode 3 is selected (M_2, M_1, M_0 = 0, 1, 1). If B_1,B_2 is set to 00, 01 or 10 then mode 3a will be selected.

BANK SELECT (STROBED BY ADS)		END OF COUNT SELECTED
B1	B0	
0	0	127
0	1	255
1	0	511
1	1	127

Table 3. Mode 7

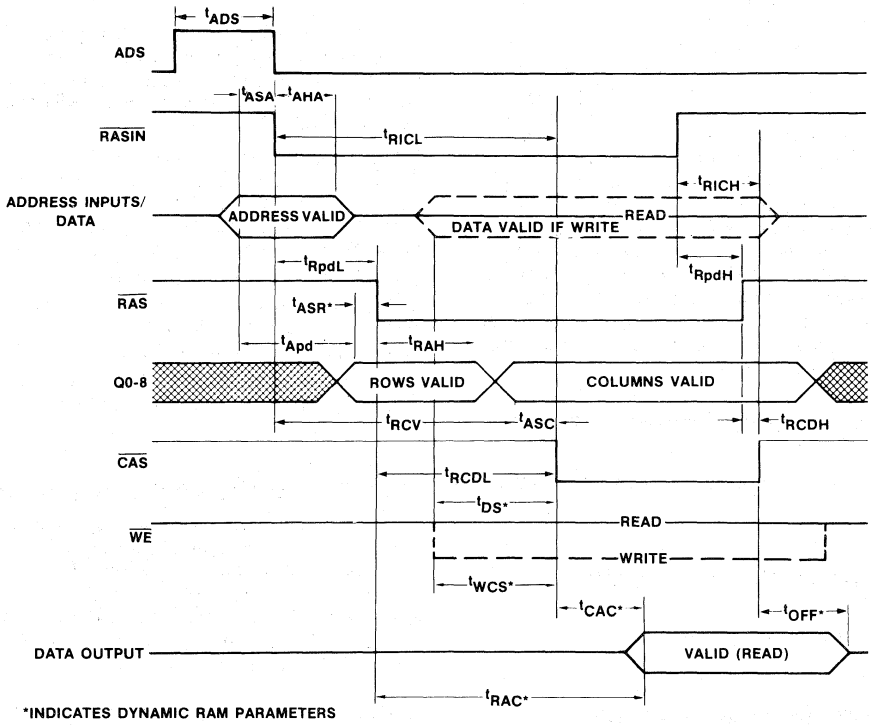


Figure 10. Mode 6 Timing ($\overline{\text{CASIN}}$ High)

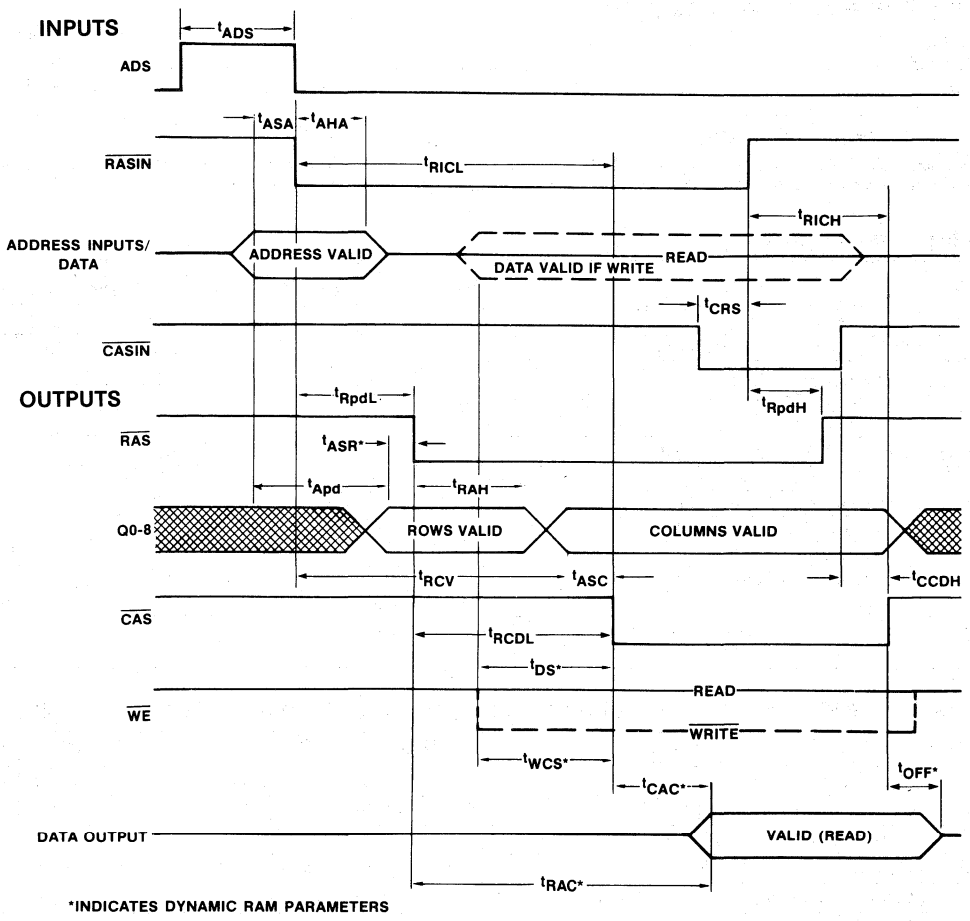


Figure 11. Mode 6 Timing, Extended $\overline{CAS}$

SN74S409/-2 Specifications:

Absolute Maximum Ratings (Note 1)

Supply voltage V_{CC} ..... -0.5 V to 7.0 V
Storage temperature range ..... -65° to +150°C
Input voltage ..... -1.5 V to 5.5 V
Output current ..... 150 mA
Lead temperature (soldering, 10 seconds) ..... 300°C

NOTE 1: "Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of operating conditions provides conditions for actual device operation.

Operating Conditions

SYMBOL	PARAMETER	FIGURE	'S409 MIN	'S409 TYP	'S409 MAX	'S409-2 MIN	'S409-2 TYP	'S409-2 MAX	UNIT
V_{CC}	Supply voltage		4.75		5.25	4.75		5.25	V
T_A	Operating free-air temperature		0		75	0		75	°C
t_{ASA}	Address setup time to ADS	Figures 4, 5, 7, 10, 11	15			15			ns
t_{AHA}	Address hold time from ADS	Figures 4, 5, 7, 10, 11	15			15			ns
t_{ADS}	Address strobe pulse width	Figures 4, 5, 7, 10, 11	30			30			ns
$t_{RASINL,H}$	Pulse width of $\overline{RASIN}$ during refresh	Figure 3	50			50			ns
t_{RST}	Counter reset pulse width	Figure 3	70			70			ns
$t_{RFCKL,H}$	Minimum pulse width of RFCK	Figure 6	100			100			ns
T	Period of $\overline{RAS}$ generator clock	Figure 6	100			100			ns
t_{RGCKL}	Minimum pulse width low of RGCK	Figure 6	35			35			ns
t_{RGCKH}	Minimum pulse width high of RGCK	Figure 6	35			35			ns
t_{CSRL}	$\overline{CS}$ low to access $\overline{RASIN}$ low	See Mode 5 description	10			10			ns
t_{RFSRG}	$\overline{RFSH}$ low set-up to RGCK low (Mode 1)	See Mode 1 description	35			35			ns
t_{RQHRF}	$\overline{RFSH}$ hold time from $\overline{RFRQ}$ (RF I/O)	Figure 6	2T			2T			ns

Electrical Characteristics: $V_{CC} = 5.0V \pm 5.0\%$, $0°C \leq T_A \leq 75°C$ Typicals are for $V_{CC} = 5V$, $T_A = 25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_C	Input clamp voltage	V_{CC} = MIN, I_C = −12mA		−0.8	−1.2	V
I_{IH1}	Input high current for ADS, R/C only	V_{IN} = 2.5V		2.0	100	μA
I_{IH2}	Input high current for other inputs, except RF I/O	V_{IN} = 2.5V		1.0	50	μA
I_IRSI	Output load current for RF I/O	V_{IN} = 0.5V, output high		−1.5	−2.5	mAV
I_ICTL	Output load current for $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	V_{IN} = 0.5V, chip deselct		−1.5	−2.5	mA
I_{IL1}	Input low current for ADS, R/$\overline{C}$ only	V_{IN} = 0.5V		−0.1	−1.0	mA
I_{IL2}	Input low current for other inputs, except RF I/O	V_{IN} = 0.5V		−0.05	−0.5	mA
V_{IL}**	Input low threshold				0.8	V
V_{IH}**	Input high threshold		2.0			V
V_{OL1}	Output low voltage, except RF I/O	I_{OL} = 20mA		0.3	0.5	V
V_{OL2}	Output low voltage for RF I/O	I_{OL} = 10mA		0.3	0.5	V
V_{OH1}	Output high voltage, except RF I/O	I_{OH} = −1mA	2.4	3.5		V
V_{OH2}	Output high voltage for RF I/O	I_{OH} = −100μA	2.4	3.5		V
I_{1D}	Output high drive current, except RF I/O	V_{OUT} = 0.8V (Note 3)		−200		mA
I_{0D}	Output low drive current, except RF I/O	V_{OUT} = 2.7V (Note 3)		200		mA
I_{OZ}	Three-state output current (address outputs)	$0.4V \leq V_{OUT} \leq 2.7V$, CS = 2.0V, Mode 4	−50	1.0	50	μA
I_{CC}	Supply current	V_{CC} = MAX		250	325	mA
C_{IN}	Input capacitance ADS, R/$\overline{C}$	T_A = 25°C		8		pF
C_{IN}	Input capacitance all other inputs	T_A = 25°C		5		pF

** These are absolute voltages with respect to pins 13 or 38 on the device and include all overshoots due to system or tester noise. Do not attempt to test these values without suitable equipment.

Switching Characteristics: $V_{CC} = 5.0V \pm 5.0\%$, $0°C \leq T_A \leq 75°C$ See Figure 12 for test load (switches S1 and S2 are closed unless otherwise specified) typicals are for $V_{CC} = 5V$, $T_A = 25°C$.

SYMBOL	ACCESS PARAMETER	FIGURE	'S409 MIN	'S409 TYP	'S409 MAX	'S409-2 MIN	'S409-2 TYP	'S409-2 MAX	UNIT
t_{RHA}	Row address held from column select	Figure 4	10			10			ns
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 5)	Figures 7, 10	95	125	160	75	100	130	ns
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 7, 10, 11	80	105	140	65	90	115	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 5)	Figures 7, 10	50	63	80	50	63	80	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 7, 10, 11	40	48	60	40	48	60	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 5)	Figures 7, 10		98	125		75	100	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 7, 10, 11		78	105		65	85	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 5)	Figures 7, 10		27	40		27	40	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 7, 10		40	65		40	65	ns
t_{CCDH}	$\overline{CASIN}$ to $\overline{CAS}$ output delay Mode 6)	Figure 11	40	54	70	40	54	70	ns
t_{RCV}	$\overline{RASIN}$ to column address valid (Mode 5)	Figures 7, 10		90	120		80	105	ns
t_{RCV}	$\overline{RASIN}$ to column address valid (Mode 6)	Figures 7, 10, 11		75	105		70	90	ns
t_{RPDL}	$\overline{RASIN}$ to $\overline{RAS}$ delay	Figures 4, 5, 7, 10, 11	20	27	35	20	27	35	ns
t_{RPDH}	$\overline{RASIN}$ to $\overline{RAS}$ delay	Figures 4, 5, 7, 10, 11	15	23	32	15	23	32	ns
t_{APDL}	Address input to output low delay	Figures 4, 5, 7, 10, 11		25	40		25	40	ns
t_{APDH}	Address input to output high delay	Figures 4, 5, 7, 10, 11		25	40		25	40	ns
t_{SPDL}	Address strobe to address output low	Figures 4, 5		40	60		40	60	ns
t_{SPDH}	Address strobe to address output high	Figures 4, 5		40	60		40	60	ns
t_{WPDL}	$\overline{WIN}$ to $\overline{WE}$ output delay	Figure 5	15	25	30	15	25	30	ns
t_{WPDH}	$\overline{WIN}$ to $\overline{WE}$ output delay	Figure 5	15	30	60	15	30	60	ns
t_{CRS}	$\overline{CASIN}$ setup time to $\overline{RASIN}$ high (Mode 6)	Figure 11	35			35			ns
t_{CPDL}	$\overline{CASIN}$ to $\overline{CAS}$ delay (R/C low in Mode 4)	Figure 5	32	41	58	32	41	58	ns
t_{CPDH}	$\overline{CASIN}$ to $\overline{CAS}$ delay	Figure 5	25	39	50	25	39	50	ns
t_{RCC}	Column select to column address valid	Figure 4		40	58		40	58	ns
t_{RCR}	Row select to row address valid	Figures 4, 5		40	58		40	58	ns
t_{RAH}	Row address hold time (Mode 5)	Figures 7, 10	30			20			ns
t_{RAH}	Row address hold time (Mode 6)	Figures 7, 10, 11	20			12			ns
t_{ASC}	Column address setup time (Mode 5)	Figures 7, 10	8			3			ns
t_{ASC}	Column address setup time (Mode 6)	Figures 7, 10, 11	6			3			ns
t_{DIF1}	Maximum ($t_{RPDL} - t_{RHA}$) (Mode 4)				15			15	ns
t_{DIF2}	Maximum ($t_{RCC} - t_{CPDL}$) (Mode 4)				15			15	ns

SYMBOL	REFRESH PARAMETER	TEST CONDITIONS	'S409 MIN	'S409 TYP	'S409 MAX	'S409-2 MIN	'S409-2 TYP	'S409-2 MAX	UNIT
t_{FRQL}	RFCK low to forced $\overline{RFRQ}$ low	C_L = 50 pF, Figure 6		20	30		20	30	ns
t_{FRQH}	RGCK low to force $\overline{RFRQ}$ high	C_L = 50pF, Figure 6		50	75		50	75	ns
t_{RGRL}	RGCK low to $\overline{RAS}$ low	Figure 6	50	65	95	50	65	95	ns
t_{RGRH}	RGCK low to $\overline{RAS}$ high	Figure 6	40	60	85	40	60	85	ns
t_{RFRH}	$\overline{RFSH}$ high to $\overline{RAS}$ high (encoding forced RFSH)	See Mode 1 description	55	80	110	55	80	110	ns
t_{CSCT}	$\overline{CS}$ high to $\overline{RFSH}$ counter valid	Figure 6		55	70		55	70	ns
t_{CTL}	RF I/O low to counter outputs all low	Figure 3			100			100	ns
t_{RFPDL}	$\overline{RASIN}$ to $\overline{RAS}$ delay during refresh	Figures 3, 6	35	50	70	35	50	70	ns
t_{RFPDH}	$\overline{RASIN}$ to $\overline{RAS}$ delay during refresh	Figures 3, 6	30	40	55	30	40	55	ns
t_{RFLCT}	$\overline{RFSH}$ low to counter address valid	$\overline{CS}$ = X, Figures 3, 6, 8		47	60		47	60	ns
t_{RFHRV}	$\overline{RFSH}$ high to row address valid	Figures 3, 6		45	60		45	60	ns
t_{ROHNC}	$\overline{RAS}$ high to new count valid	Figures 3, 8		30	55		30	55	ns
t_{RLEOC}	$\overline{RASIN}$ low to end-of-count low	C_L = 50pF, Figure 3			80			80	ns
t_{RHEOC}	$\overline{RASIN}$ high to end-of-count high	C_L = 50pF, Figure 3			80			80	ns
t_{RGEOB}	RGCK low to end-of-burst low	C_L = 50pF, Figure 8			95			95	ns
t_{MCEOB}	Mode change to end-of-burst high	C_L = 50pF, Figure 8			75			75	ns

9

Switching Characteristics: (Cont'd)

SYMBOL	ACCESS PARAMETER	TEST CONDITIONS	'S409 MIN	'S409 TYP	'S409 MAX	'S409-2 MIN	'S409-2 TYP	'S409-2 MAX	UNIT
	THREE-STATE PARAMETER								
t_{ZH}	$\overline{CS}$ low to address output high from Hi	Figures 6, 12 R1 = 3.5k, R2 = 1.5k		35	60		35	60	ns
t_{HZ}	$\overline{CS}$ high to address output Hi-Z from high	C_L = 15pF, Figures 6,12 R2 = 1k, S1 Open		20	40		20	40	ns
t_{ZL}	$\overline{CS}$ low to address output low from Hi-Z	Figures 6, 12 R1 = 3.5k, R2 = 1.5k		35	60		35	60	ns
t_{LZ}	$\overline{CS}$ high to address output Hi-Z from low	C_L = 15pF, Figures 6,13 R1 = 1k, S2 Open		25	50		25	50	ns
t_{HZH}	$\overline{CS}$ low to control output ($\overline{WE}$, $\overline{CAS}$, ($\overline{RAS0}$-3) high from Hi-Z high	Figures 6,12 R2 = 750Ω, S1 open		50	80		50	80	ns
t_{HHZ}	$\overline{CS}$ high to control output ($\overline{WE}$, $\overline{CAS}$, ($\overline{RAS0}$-3) Hi-Z high from high	C_L = 15pF R2 = 750Ω, S1 open		40	75		40	75	ns
t_{HZL}	$\overline{CS}$ low to control output ($\overline{WE}$, $\overline{CAS}$, ($\overline{RAS0}$-3) low from Hi-Z high	Figure 12 S1, S2 Open		45	75		45	75	ns
t_{LHZ}	$\overline{CS}$ high to control output ($\overline{WE}$, $\overline{CAS}$, ($\overline{RAS0}$-3) Hi-Z high from low	C_L = 15pF, Figure 12 R2 = 750Ω, S1 open		50	80		50	80	ns

*Internally the device contains a 3K resistor in series with a Schottky Diode to V_{CC}.

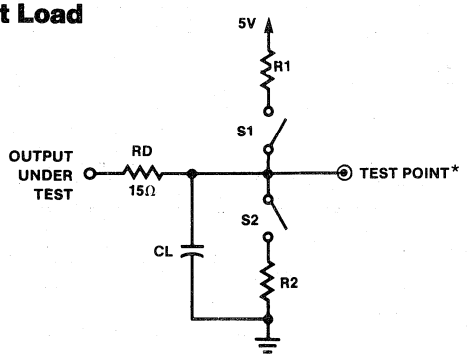
Note 1: Output load capacitance is typical for 4 banks of 22 DRAMs or 88 DRAMs including trace capacitance. These values are: Q0-Q8. C_L = 500pF; RAS0-RAS3, C_L = 150pF; CAS C_L = 600pF unless otherwise noted.

Note 2: All typical values are for T_A = 25°C and V_{CC} = 5.0V.

Note 3: This test is provided as a monitor of Driver output source and sink current capability. Caution should be exercised in testing this parameter. In testing these parameters, a 15Ω resistor should be placed in series with each output under test. One output should be tested at a time and test time should not exceed 1 second.

Note 4: Input pulse 0V to 3.0V, $t_R = t_F$ = 2.5 ns, f = 2.5 MHz. t_{PW} = 200 ns. Input reference point on AC measurements is 1.5V. Output reference points are 2.7V for High and 0.8V for Low.

Test Load



R1, R2 = 4.7K EXCEPT AS SPECIFIED.

* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

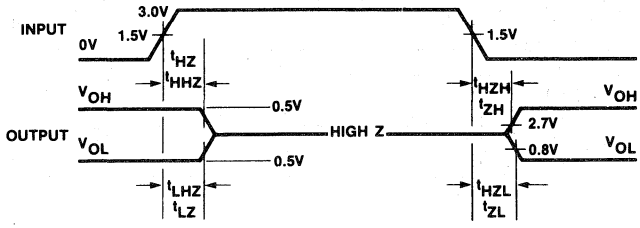


Figure 12. Waveform

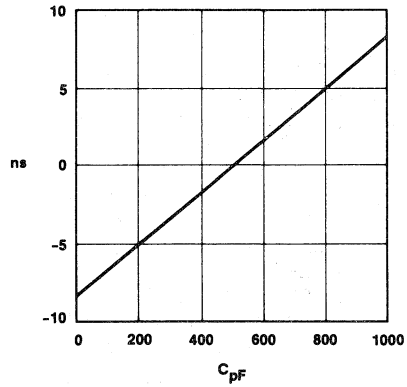


Figure 13. Change in Propagation Delay vs Loading Capacitance Relative to a 500 pF Load

Applications

The 74S409 Dynamic RAM Controller provides all the address and control signals necessary to access and refresh dynamic RAMs. Since the 74S409 is not compatible with a specific bus or microprocessor, an interface is often necessary between the 74S409 and the system. A general application using PAL to implement the interface and two additional chips to provide refresh clock and chip select is shown in Figure 14.

The 74S409 operating modes may vary from application to application. For efficient refresh it is recommended to use mode 1 and mode 5 to take advantage of the hidden (transparent) refresh with forced refresh backup.

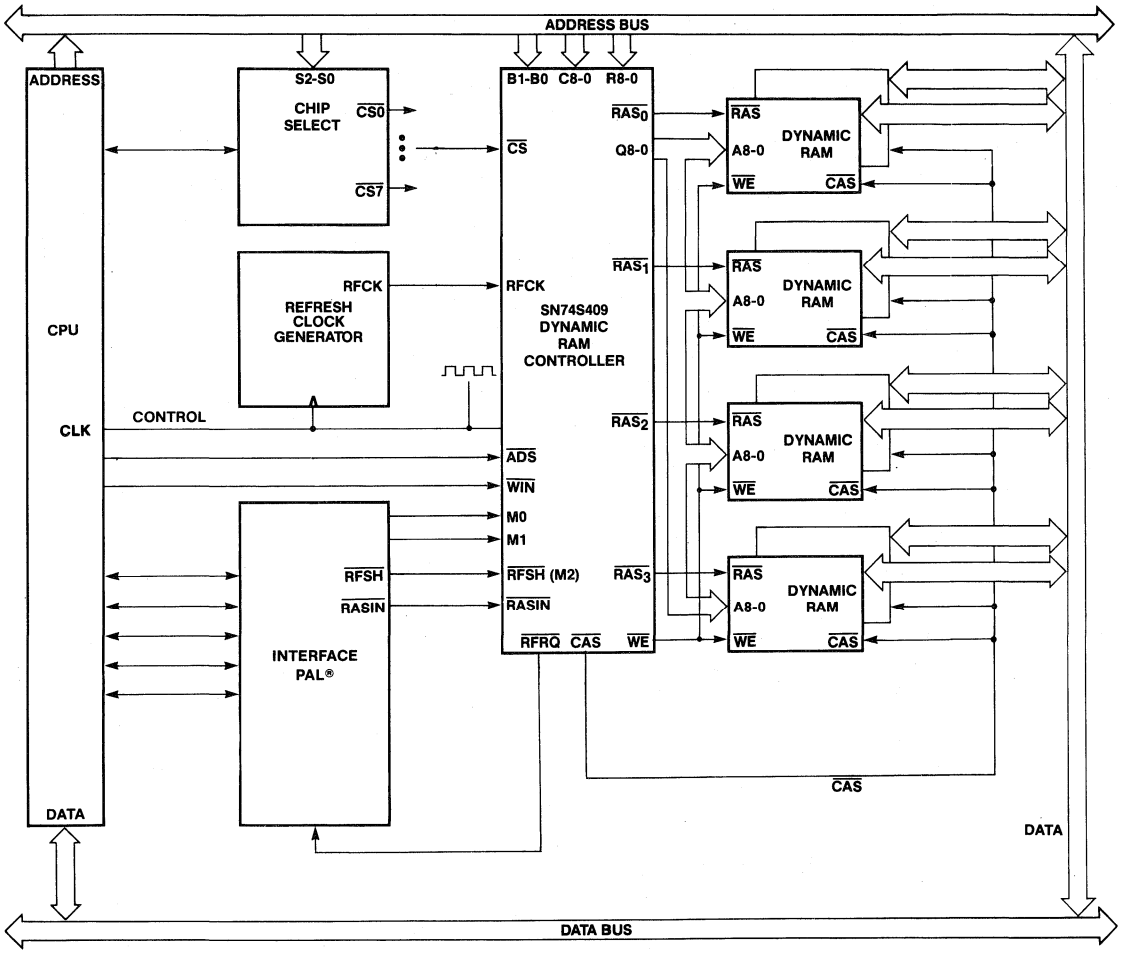
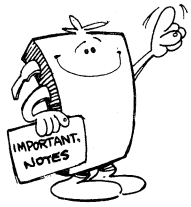
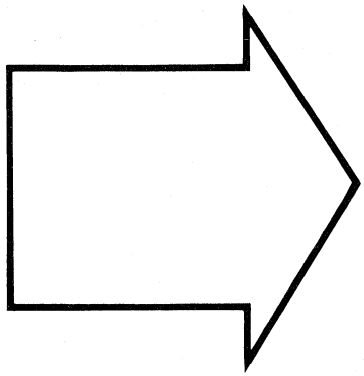


Figure 14. 74S409 in General Application


IMPORTANT
NOTES



ARITHMETIC ELEMENTS AND LOGIC

Arithmetic Logic Unit/ Function Generator

SN74S381

Features/Benefits

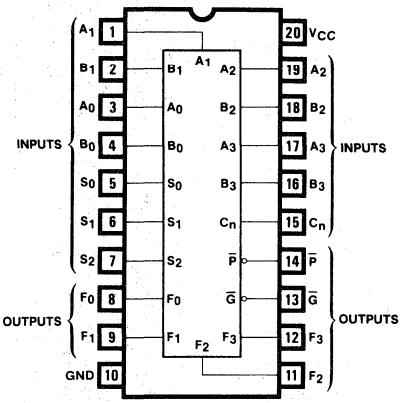
- A fully parallel 4-bit ALU
- Ideally suited for high-speed processors
- Generate and propagate outputs for full carry lookahead
- Three arithmetic functions
- Three logic functions
- Preset and clear functions

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN74S381	N, J	Commercial

Pin Configuration

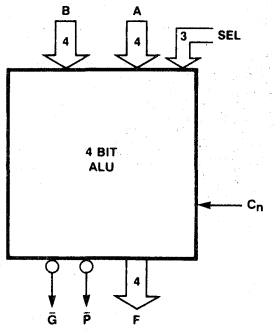
SN74S381



Description

The 'S381 is a Schottky TTL arithmetic logic unit (ALU)/function generator that performs eight binary arithmetic/logic operations on two 4-bit words as shown in the function table. These operations are selected by the three function-select lines (S0, S1, S2). A full lookahead carry circuit is provided for fast, simultaneous carry generation by means of two cascaded outputs (P and G) for the four bits in the package.

Logic Symbol



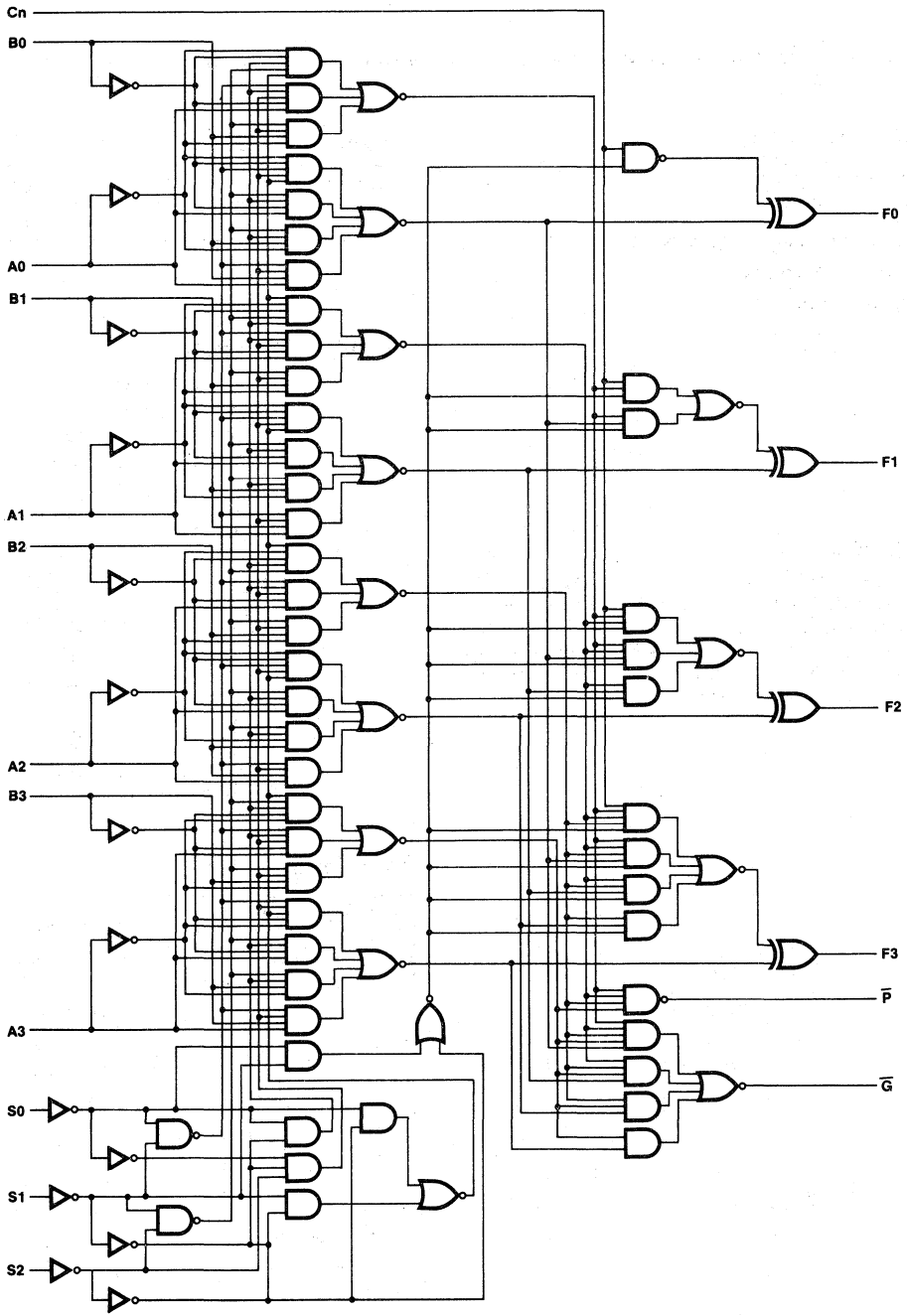
Function Table

SELECTION			ARITHMETIC/LOGIC OPERATION
S2	S1	S0	
L	L	L	Clear †
L	L	H	B minus A
L	H	L	A minus B
L	H	H	A plus B
H	L	L	A ⊕ B
H	L	H	A + B
H	H	L	AB
H	H	H	Preset ††

† Force all F outputs to be Lows.
†† Force all F outputs to be Highs.

10

Logic Diagram



Function Table

	INPUTS											OUTPUTS					
FUNCTION	S2	S1	S0	Cn	A3	A2	A1	A0	B3	B2	B1	B0	F3	F2	F1	F0	$\overline{G}$	$\overline{P}$
Clear	0	0	0	X	X	X	X	X	X	X	X	X	0	0	0	0	0	0
B minus A (Inverse Subtraction)	0	0	1	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
				0	0	0	0	0	1	1	1	1	1	1	1	0	0	0
				0	1	1	1	1	0	0	0	0	0	0	0	0	1	1
				0	1	1	1	1	1	1	1	1	1	1	1	1	1	0
				1	0	0	0	0	0	0	0	0	0	0	0	0	1	0
				1	0	0	0	0	1	1	1	1	1	1	1	1	0	0
				1	1	1	1	1	0	0	0	0	0	0	0	1	1	1
				1	1	1	1	1	1	1	1	1	0	0	0	0	1	0
A minus B (Subtract)	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
				0	0	0	0	0	1	1	1	1	0	0	0	0	1	1
				0	1	1	1	1	0	0	0	0	1	1	1	0	0	0
				0	1	1	1	1	1	1	1	1	1	1	1	1	1	0
				1	0	0	0	0	0	0	0	0	0	0	0	0	1	0
				1	0	0	0	0	1	1	1	1	0	0	0	1	1	1
				1	1	1	1	1	0	0	0	0	1	1	1	1	0	0
				1	1	1	1	1	1	1	1	1	0	0	0	0	1	0
A plus B (Add)	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
				0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
				0	1	1	1	1	0	0	0	0	1	1	1	1	1	0
				0	1	1	1	1	1	1	1	1	1	1	1	0	0	0
				1	0	0	0	0	0	0	0	0	0	0	0	1	1	1
				1	0	0	0	0	1	1	1	1	0	0	0	0	1	0
				1	1	1	1	1	0	0	0	0	0	0	0	0	1	0
				1	1	1	1	1	1	1	1	1	1	1	1	1	0	0

10

Function Table

	INPUTS											OUTPUTS			
FUNCTION	S2	S1	S0	Cn	A3	A2	A1	A0	B3	B2	B1	B0	F3	F2	F1	F0
A⊕B (OR)	1	0	0	X	0	0	0	0	0	0	0	0	0	0	0	0
				X	0	0	0	0	1	1	1	1	1	1	1	1
				X	1	1	1	1	0	0	0	0	1	1	1	1
				X	1	1	1	1	1	1	1	1	0	0	0	0
A⊕B (XOR)	1	0	1	X	0	0	0	0	0	0	0	0	0	0	0	0
				X	0	0	0	0	1	1	1	1	1	1	1	1
				X	1	1	1	1	0	0	0	0	1	1	1	1
				X	1	1	1	1	1	1	1	1	1	1	1	1
A • B (AND)	1	1	0	X	0	0	0	0	0	0	0	0	0	0	0	0
				X	0	0	0	0	1	1	1	1	0	0	0	0
				X	1	1	1	1	0	0	0	0	0	0	0	0
				X	1	1	1	1	1	1	1	1	1	1	1	1
Preset	1	1	1	X	0	0	0	0	0	0	0	0	1	1	1	1
				X	0	0	0	0	1	1	1	1	1	1	1	1
				X	1	1	1	1	0	0	0	0	1	1	1	1
				X	1	1	1	1	1	1	1	1	1	1	1	1

1 = HIGH voltage level
0 = LOW voltage level
X = Don't care

Absolute Maximum Ratings

Supply voltage V_{CC} ..... 7 V
Input voltage ..... 5.5 V
Storage temperature range ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
T_A	Operating free-air temperature	0		75	°C

Electrical Characteristics Over Operating Conditions

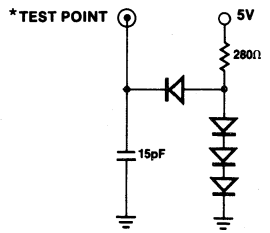
SYMBOL	PARAMETER	TEST CONDITIONS			COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA				−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.5 V	Any S input			−2	mA
				Cn			−8	
				All others			−6	
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7 V	Any S input			50	μA
				Cn			250	
				All others			200	
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V				1	mA
V_{OL}	Low-Level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V	V_{IH} = 2 V, I_{OL} = 20 mA				0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V	V_{IH} = 2 V, I_{OH} = −1 mA		2.7	3.4		V
I_{OS}	Output short-circuit current*	V_{CC} = MAX			−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX			105		160	mA

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	FROM (INPUT)	TO (OUTPUT)	74S381 TYP	74S381 MAX	UNIT
t_P	Propagation delay time	C_L = 15 pF R_L = 280Ω	C	Any F	10	17	ns
t_P	Propagation delay time		Any A or B	$\overline{G}$	12	20	ns
t_P	Propagation delay time		Any A or B	$\overline{P}$	11	18	ns
t_{PLH}	Propagation delay, low-to-high		Any A or B	Any F	18	27	ns
t_{PHL}	Propagation delay, high-to-low				16	25	ns
t_P	Propagation delay time		Any S	Any F, $\overline{G}$, $\overline{P}$	18	30	ns

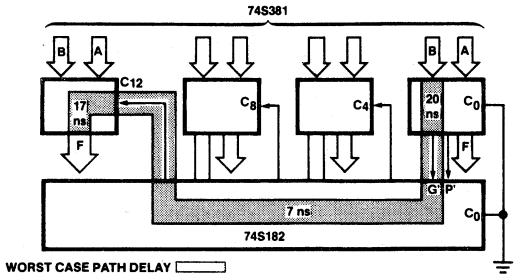
Test Load



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

10

16-BIT ALU (USING 74S381)



MAXIMUM DELAY OF ADDITION/SUBTRACTION.

	74S381 + 74S182
1-4 bits	27ns
5-16 bits	44ns
17-64 bits	64ns


IMPORTANT.
NOTES

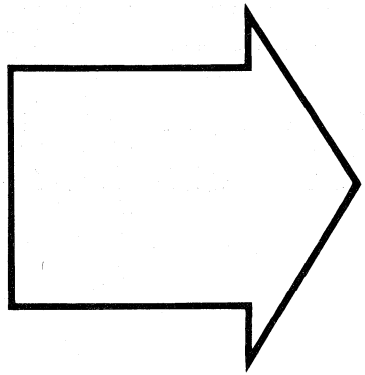


Table of Contents

Cray Multipliers

DESCRIPTION	PART NUMBER	MAX DELAY	PINS
8x8 Multiplier (latched)	SN74S557	60 ns (X_i, Y_i, to S_{15})	40
8x8 Multiplier	SN74S558	60 ns	40
8x8 Multiplier	SN54S558	60 ns	40
16x16 Multiplier	SN74S556	76 ns (X_i, Y_i to S_{15-0}) 90 ns (X_i, Y_i to S_{31-16})	84 84

Five New Ways to Go Forth and Multiply

Chuck Hastings

Our Multiplier Population Explosion

Recently it has seemed as if every time you turned around Monolithic Memories was announcing *another* new multiplier. Want to catch your breath, and find out where each of these fits into the overall scheme of things? Read on.

Actually, there have been five new multipliers in all within the last three years, plus two which had previously been available for several years. In time order of introduction, these are:

Parts No.	Description[A]
57/67558	150-nsec 8x8 Flow-Through Cray Multiplier[B]
57/67558-1	125-nsec 8x8 Flow-Through Cray Multiplier[B]
54/74S508	8-Bit Bus-Oriented Sequential Multiplier/Divider
54/74S558	60-nsec 8x8 Flow-Through Cray Multiplier
54/74S557	60-nsec 8x8 Flow-Through Cray Multiplier with Transparent Output Latches
54/74S516	16-Bit Bus-Oriented Sequential Multiplier/Divider
54/74S556	90-nsec 16x16 Flow-Through Cray Multiplier with Transparent Input and Output Latches for full 32-bit output

NOTES: A. Times are worst-case times for commercial-temperature-range parts.

B. Obsolete. 54/74S558 replaces these in both new and existing designs.

You will notice that the above parts fall into two categories: flow-through Cray multipliers, and bus-oriented sequential multiplier/dividers. Although all of these parts get referred to rather casually as "multipliers," there are major differences between the two general types; see Table 1 below.

The Cray Multipliers

The essential idea of a Cray multiplier, as originally put together by Seymour Cray in the late 1950s with discrete logic at Control Data Corporation, is to wire up an array of full adders in the form of a binary-arithmetic-multiplication pencil-and-paper example.[3] That is, everywhere that there is a "1" or a "0" in a longhand binary-multiplication example, the Cray type of multiplication uses a full adder. One may visualize a Cray multiplier functionally as a "diamond," as follows:

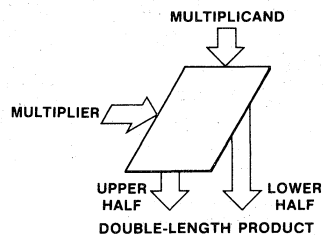


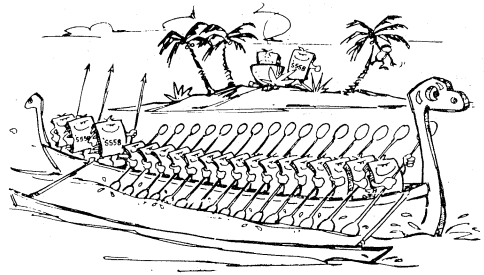
Figure 1. Pencil-and-Paper Analogy to Cray-Multiplier Operation

	Flow-Through Cray Multiplier	Bus-Oriented Sequential Multiplier/Divider
Role in System	*Building-block role* — as many as 34 parts used in one super-minicomputer (NORD-500 from Norsk Data[1]).	*Co-processor role* — one, or occasionally two, parts used in one microcomputer[2].
Internal Operation	Static arithmetic-logic network; multiplies without being clocked[3] using eight bits of the multiplier at a time.	State machine; requires clocking to operate; contains edge-triggered registers; sequenced by a state counter; multiplies using two bits of the multiplier at a time[4].
External Control	Controlled by several mode-control input signals.	Controlled by sequences of micro-opcodes which come from a microprocessor, a registered PAL, or some other sequential-control device.
Package	40-pin DIP ('S557/8); 84-pin LCC or 88-pin PGA ('S556)	24-pin DIP.
Operations Performed	Can only perform multiplication.	Can perform multiplication, division, and multiplication-with-accumulation.
Storage Capabilities	Either no storage capabilities ('558 types), or optional storage for the double-length product only ('557 type), or full product and input storage ('556 type).	Four full-length registers; capable of storing both input operands and the double-length product.
Second Sources	8x8, Multiple-sourced (AMD, Fairchild, Monolithic Memories).	Sole-sourced; only bipolar *dividers* on the market.
Where Used	Initial usage has been in high-end minicomputers, array processors, and signal processors.	Initial usage has been in industrial-control microcomputers, digital modems, military avionics, CRT graphic systems, video games, and cartographic analysis systems.
Future Prospects	Potential large market today since these parts are now low-cost and multiple-sourced, and should be used in *all* new minicomputer designs!	Potential huge world-wide market for enhancement of microprocessor, bit-slice processor, and microcomputer capabilities, and for small-scale signal processing!

Table 1. A comparison of the two types of Monolithic Memories Multipliers

Our 57/67558, introduced in the mid-1970s, was the original *single-chip* Cray multiplier. To achieve what was for that time very high performance for a Schottky-TTL-technology part, the internal design of the 57/67558 also exploited other speed-freak multiplication techniques such as Booth multiplication[4] and Wallace-Tree addition[5]. All of these techniques achieve increased speed through extensive parallelism, and can be used at the system level as well as within LSI components. Subsequently, process improvements made it possible to offer a faster final-test option, the 57/67550-1, which attained a sales-volume level essentially equal to that of the original part.

About five years ago, AMD paid us the sincere compliment of second-sourcing these parts with the 75-nsec 25S558. Three years ago, we returned the compliment with the 60-nsec 54/74S558. All of these '558 parts, and the 70-nsec 54/74F558 announced by Fairchild, are fully compatible drop-in equivalents except for the variations in logic delay.



"ALL OF THESE TECHNIQUES ACHIEVE INCREASED SPEED THROUGH EXTENSIVE PARELLELISM."

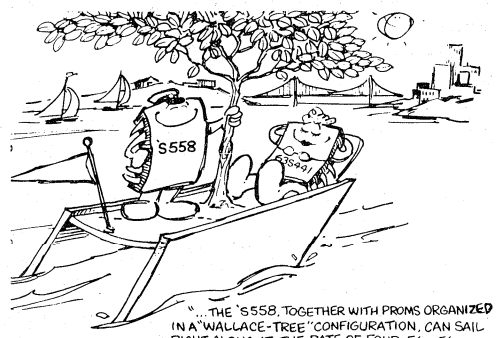
When AMD introduced the 25S558, they introduced along with it the 80-nsec 25S557, a "metal option" of the same basic design with "transparent" output latches to hold the double-length product. "Transparent" means that the latches go away when you don't want them there; a latch-control line like that of the 54/74S373 controls whether these output latches store information, or simply behave as output buffers. Anyway, when we introduced our 54/74S558, we followed it within a few weeks with the 60-nsec 54/74S557, which is a much faster drop-in replacement for AMD's part. And subsequently, Fairchild has announced a 70-nsec 54/74F557.

Because AMD's 'S557 has the output latches implemented in TTL technology *after* the ECL-to-TTL converters, whereas our 'S557 has them implemented in ECL technology *before* the conversion, the latches operate much faster in ours. Our 'S557 is typically only about a nanosecond slower than our 'S558, whereas the logic-delay difference between AMD's two parts is considerably greater. Consequently, our margin of superiority over AMD for the 'S557 is even greater than for the 'S558.

More recently, we introduced the 90-nsec 'S556, which is a 16x16 direct size-upgrade of the 'S557/8 architecture, with the addition of input latches. In a "pipelined" mode, an 'S556 can produce a new 32-bit product every 75 nsec.

'S557/8 Cray multipliers come in a 40-pin dual-inline package, either ceramic or plastic. Worst-case power-supply current is 280 mA. The 'S556 comes in your choice of an 84-pin LCC (*L*eadless *C*hip *C*arrier) or an 88-pin PGA (*P*in-*G*rid *A*rray) package. Worst-case power-supply current is 800 mA (900 mA over military temperature range). The data-bus outputs can sink up to 8 mA I_{OL}, for all of these multipliers.

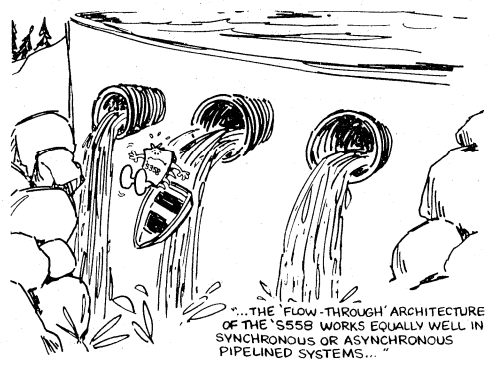
References 5 and 6 discuss technical approaches to using Cray multipliers in high-performance minicomputers. The 'S558, together with PROMs organized in a "Wallace-tree" configuration, can sail right along at the rate of four 56x56 multiplications every microsecond, on the basis of fixed-point arithmetic with no renormalization. (See table 7 on page 16 of reference 5; the multiplication time is 238 nsec for a "division step," which is a fixed-point multiplication, and 319 nsec for a floating-point multiplication where extra time is required for renormalization and correction of the exponent of the product.) 34 'S558s or 'S557s are required to perform this multiplication if the computer system architecture does not call for the computation of the least-significant half of the double-length product; 49 are required if it does.



"...THE 'S558, TOGETHER WITH PROMS ORGANIZED IN A "WALLACE-TREE" CONFIGURATION, CAN SAIL RIGHT ALONG AT THE RATE OF FOUR 56 x 56 MULTIPLICATIONS EVERY MICROSECOND..."

The "local" architecture of the multiplier section of a digital system can take two rather different forms. A minicomputer[5], which executes an unpredictable mixture of arithmetic and logical instructions one after the other, typically needs to be able to get the complete multiplication over and done with before going on to the next program step—which is probably not another multiplication. An array processor or digital correlator, however, tends to do very regular iterative computations; and the performance of such a system can often be greatly increased by a technique called "pipelining," in which the arithmetic unit consists of stages with registers or latches in between each stage, and partial computational results move from one stage to the next on each clock.

The "flow-through" architecture of the 'S558 works equally well in synchronous or asynchronous pipelined systems, but registers or latches must be provided externally. The 'S557, however, is actually a *superset* of the 'S558, and the added internal-output-latch feature adapts it particularly well to pipelined systems. The 'S556 provides latches at *both* ends.



"...THE 'FLOW-THROUGH' ARCHITECTURE OF THE 'S558 WORKS EQUALLY WELL IN SYNCHRONOUS OR ASYNCHRONOUS PIPELINED SYSTEMS..."

Even a smaller-scale system can make effective use of these parts. To return to the case of 56x56 multiplication, which corresponds to the word-length needed for multiplying mantissas in several popular floating-point-number formats, an iterative clocked scheme using just seven 8x8 multipliers, some adders, and an accumulator register can form the entire 112-bit double-length product in just seven multiply/add cycles. A number of mid-range minicomputers today multiply in this manner. The multipliers are configured as suggested by the following block diagram:

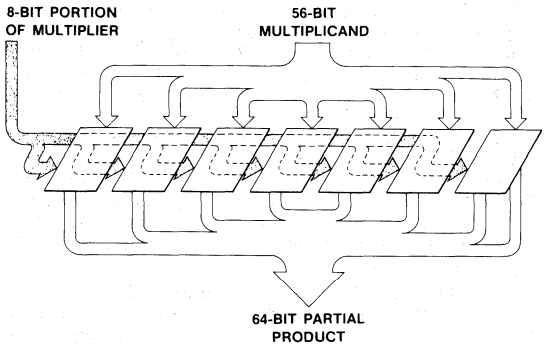


Figure 2. 8x56 Cray Multiplier In Diamond Representation

There is even an occasional 8-bit or 16-bit microprocessor-based system with a need for *very* fast multiplication, where 'S557/8s or 'S556s may get used as microprocessor peripherals[7,8]. Digital-video systems, in particular electronic games, with "vector graphic" capabilities are one example.

The world of 'S556/7/8 applications has turned out to include *all* sizes of minicomputers, digital video systems, and signal processors — FFT (Fast Fourier Transform) processors, voice recognition equipment, radar systems, digital correlators and filters, electronic seismographs, brain and body scanners, and so forth. And there are many unexpected off-beat applications, such as real-time data-rescaling circuits in instruments, altogether too numerous to list here. After all, an'S556 can multiply two 16-bit numbers together and output their entire 32-bit product in 90 nsec *worst case*... less time than it would take a speeding bullet to move the distance equal to the thickness of this piece of paper. How's that for Supermultiplier?

The Multiplier/Dividers

The Monolithic Memories 'S516 and 'S508 are state-of-the-art TTL-compatible intelligent peripherals for microprocessors, somewhere between arithmetic sequential circuits and specialized bipolar microprocessors. The 'S516 and 'S508 each can perform any of 28 different multiply and multiply-and-accumulate instructions, plus any of 13 different divide instructions, at bipolar speeds under the control of an internal state counter. (See Figure 2 of the 'S516 data sheet.) The state counter's sequence is in turn guided by 3-bit instruction codes which are external inputs to the 'S516/508. The 'S516 computes with 16-bit binary numbers, and the 'S508 computes with 8-bit binary numbers, as the part numbers none-too-subtly imply.

A 16-bit bi-directional data bus connects the 'S516 with the outside world for bringing in multipliers, multiplicands, dividends, and divisors; and returning products, quotients and remainders. It also has clock (CK) and run/wait ($\overline{GO}$) inputs, and an overflow indication (OVR) output.

The 'S508 has all of the above inputs and outputs also, except that it has only an 8-bit bidirectional data bus. Since it comes in the same 24-pin package as the 'S516, it obviously has eight more pins available for other purposes. Four of these are used to bring out the internal-state-counter value; one each is used for a completion ($\overline{DONE}$) status output, an output-enable control (OE) input, and a master-reset ($\overline{MR}$) control input; and one is not used at all.

A simple, general interfacing scheme can be used to team a 'S516 with any of the currently popular 16-bit microprocessors,or an 'S508 with any 8-bit microprocessor. (See Figure 7 of the'S516 data sheet.) With a couple extra interface circuits, an'S516 can also be interfaced to an 8-bit microprocessor.Particularly if the system software is written in a highly-structured language such as PASCAL or FORTH, an'S516/508 can be retrofitted into an existing system with a large gain in performance and very little impact on either hardware or software — calls to the previous software-implemented one-step-at-a-time multiply and divide subroutines are simply rerouted to substitute a command from the microprocessor to the 'S516/508 to accept an operand and start its operation sequence.

The 'S516 and 'S508 are in fact two different "metal options" of one basic design; the 'S516 has twice as many data bits in each internal register. The 'S516 and 'S508 both have a worst-case clock rate of 6 MHz (commercial) or 5 MHz (military); the typical rate is 8 MHz. The simplest complete twos-complement 16x16 multiplication instruction can be performed in nine clock cycles by an 'S516, or in five by an 'S508, since 2-bits-at-a-time Booth multiplication is used;[4] thus, the worst-case time required by the 'S516 to multiply in this mode is 1.5 μsec for a commercial part, and for an 'S508 it is 833 nsec. On the same basis, 32/16 division can be done in 21 clock cycles, or 3.5 μsec worst-case, by an 'S516; and 16/8 division can be done in 13 clock cycles, or 2.2 μsec worst-case, by an 'S508.

An 'S516/508 can perform either positive or negative multiplication or multiply-accumulation, and many of the instructions provide for "chaining" of successive computations to eliminate extra operand transfers on the bus; these features further enhance the computational speed of the 'S516/508 in particular applications. Arithmetic can be either integer or fractional with respect to positioning of the results.

An 'S516 can powerfully enhance the capabilities of *any* present-day 16-bit or 8-bit microprocessor in a compute-bound application. In fact, it can be used in any digital system where there is a need to multiply and divide on a bus. An 'S508 can likewise enhance the capabilities of any 8-bit microprocessor.

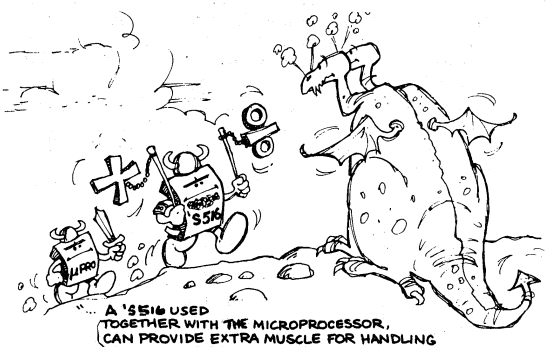
11

The 'S516 comes in an industry-standard 600-mil 24-pin dual-inline package, modified to include an integral aluminum heatsink which does not add appreciably to the package height. It requires only +5V and ground power connections, and draws a worst-case power-supply current of 450mA (commercial) or 500mA (military). Power consumption is greatest at cold temperatures, and decreases substantially as operating temperature increases. The 16 databus inputs require at most 0.25mA input current; the other inputs require at most 1mA. The 16 databus outputs can sink up to 8mA I_{OL}. The 'S508 also fits the above description, except that its worst-case power-supply current is 380mA (commercial) or 400mA (military), and it has only 8 databus inputs and outputs.

In describing applications of these parts, it is difficult to know where to start — they can be used in almost any design where a microprocessor can be used, and you know how many places that is today. So, perhaps a good starting point is to see what uses customers have thought up all by themselves. One customer even used *two* 'S516s in "pingpong" mode on a single 16-bit bus! So, rather than merely speculating as to what these parts *might* be good for, here's a list of what Monolithic Memories's customers have already *proven* they are good for:

- Real-time control of heavy machinery[9]
- Low-cost, high-performance digital modems
- CRT graphics, including video games
- Military avionics
- Cartographic analysis

As it happens, the above are 'S516 applications, except that digital modem designs have been done with both the 'S516 and the 'S508. Several of the 'S516 designs are already in production. In each of these applications, the microprocessor could have coped all right with the computational complexity, albeit at its own less-than-tremendous speed, but a 'S516 used together with the microprocessor can provide extra muscle for handling formidable problems.



Competition? Well, since there are no second sources for the 'S516, and no competitor at present has a similar fast part capable of performing division as well as multiplication, right now the 'S516 has no *direct* competition. Indirectly, there are some competing parts which perform *only* multiplication, and would have to perform division by Newton-Raphson iteration to be usable for any application where division is required. However, the 'S516 is (as far as we know) by far the lowest-priced *bipolar* 16-bit multiplier, and the other microprocessor peripheral chips which can perform division as well as multiplication are relatively-slow MOS devices. In one case, an 8-bit cascadable CMOS part requires a 50% reduction in clock rate to do 16-bit arithmetic. And considerable numerical-analysis and programming sophistication are required to implement Newton-Raphson division with *fixed-point* operands. (It's easier with floating-point operands.) In contrast, the 'S516/508 can be easily interfaced to almost any microprocessor using one or two PALs,* and can perform *either* multiplication or division on command[2]

The 'S516 is so much faster than the competing MOS chips that it can even take them on for *floating-point* computations (which some of them are designed to do) and *win* . A conference paper[10] describes the design of an 'S516-based S-100-bus card capable of beating an Intel 8087 2:1 on floating-point arithmetic.

Some competing parts, in particular the AMI 2811 and Nippon Electric μPD7720, include an on-board ROM which must be mask-programmed at the factory, which makes life difficult for small companies (or even larger ones) which are trying to get a microprocessor-based product to market quickly. Also, some competing parts require sequencing by external TTL jellybeans.

And, as for using AMD/TRW 64-pin 16x16 Cray multiplier chips as microprocessor peripherals, these cost much more than the 'S516, occupy about three times the circuit-board space, multiply faster, don't divide at all except by Newton-Raphson iteration, and also require one or two "overhead" microprocessor instructions to interface for a given arithmetic operation. From a *system* viewpoint, when this overhead time is reckoned with, these chips provide little actual gain in multiply performance over the 'S516 at lots of extra cost, and an actual loss in divide performance: the 'S516 is *much more cost-effective overall.*

'S516s potentially fit into many, many places in commercial, industrial, and military electronics, particularly into small-scale real-time systems. The part is fast enough to enhance the performance of a 16-bit Motorola 68000, Zilog Z8000, or Intel 8086, as well as that of *any* 8-bit microprocessor. It is also fast enough to considerably improve the multiplication and division performance of 16-bit 2901-based "bit-slice" bipolar microcomputers, which are often used as processors in desktop graphics CRT terminals.

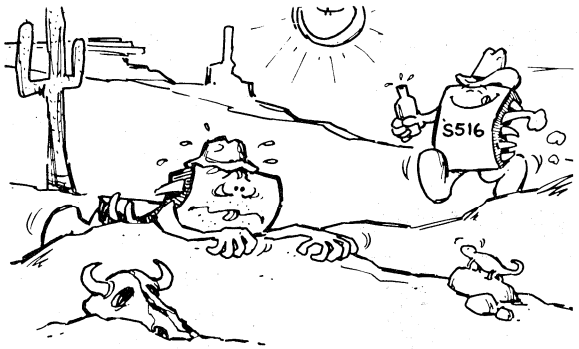
It is worth bringing the 'S516 to the attention of *any* designer who is developing:

- A personal computer or small business computer.
- A word processor, or a more grandiose "office automation system."
- A cruise missile, or any other "smart weapon."
- A digital modem.
- A small-scale speech-processing system. (These are *very* multiplication-intensive. We have one magazine article on the 'S516 in such an application![11])
- A smart instrument, which does data conversion.
- An industrial control system, particularly one which must do many coordinate transformations.
- An all-digital studio-quality high-fidelity system.
- A cost-reduced computerized medical scanning system.
- A multiprocessor system for scientific computations![12])

If an 'S516/508 is introduced into a system configured around an older microprocessor as a "co-processor" or

helpmate for the microprocessor, and the application is arithmetic-intensive, the end effect can be a major upgrading of performance at the system level.[2-7] Consequently, a major reason for designing these parts in is *microprocessor life-cycle enhancement*. In particular, many MOS microprocessors have single-length and double-length add and subtract instructions: but either they have no multiply or divide instructions at all, or else they perform their multiply and divide instructions so slowly as to jeopardize the ability of the entire system to handle its computing load in real time.

So picture, if you will, the entrepreneur or chief engineer of a firm making a successful microprocessor-based widget which has been on the market for a few months, which uses an older 8-bit microprocessor such as a 6800 or 8085 or Z80. Just when his/her sales are really taking off, here comes a new start-up competitor with a similar system, using a Motorola 68000, with added features and faster performance made possible by the 68000's 16-bit word length and multiply/divide capabilities. The 'S516 can, in this instance, serve as a "great equalizer"—it can be retrofitted into the older system as previously described, and provides even higher-speed multiplication and division than the 68000. (Enough so, actually, that there are designers using the 'S516 *with* the 68000.) Thus, the 'S516 can dramatically extend the life cycle of existing microcomputer systems based on microprocessors which either don't have multiplication and division instructions, or perform these operations relatively slowly.



"... THE 'S516 CAN DRAMATICALLY EXTEND THE LIFE CYCLE OF EXISTING MICROCOMPUTER SYSTEMS BASED ON MICROPROCESSORS WHICH EITHER DON'T HAVE MULTIPLICATION AND DIVISION INSTRUCTIONS, OR PERFORM THESE OPERATIONS RELATIVELY SLOWLY..."

'S508s are somewhat easier to control from a logic-design viewpoint than 'S516s, purely because they have more control inputs and outputs. However, the shorter 'S508 word length makes the part naturally fit into smaller-scale systems than those which might use an 'S516. Essentially, the 'S508 is optimized for small-scale systems.

Now that you know what these parts are, can't you think of at least half a dozen prime uses for them right in your own back yard?

References (all available from Monolithic Memories)

1. "Combinatorial Floating Point Processor as an Integral Part of the Computer," Tor Undheim, *Electro/80 Professional Program Session Record,* Session 14 reprint, paper 14/1.
2. "SN54/74S516 Co-Processor Supercharges 68000 arithmetic," Richard Wm. Blasco, Vincent Coli, Chuck Hastings and Suneel Rajpal, Monolithic Memories Application Note AN-114.
3. "How to Design Superspeed Cray Multipliers with 558s," Chuck Hastings, included within the SN54/74S557/8 data sheet.
4. "Doing Your Own Thing in High-Speed Digital Arithmetic," Chuck Hastings, Monolithic Memories Conference Proceedings reprint CP-102.
5. "Big, Fast, and Simple — Algorithms, Architecture, and Components for High-End Superminis," Ehud Gordon and Chuck Hastings, Monolithic Memories Application Note AN-111.
6. "Fast 64x64 Multiplication using 16x16 Flow-Through Multipliers and Wallace Trees," Marvin Fox, Chuck Hastings and Suneel Rajpal, Monolithic Memories Conference Proceedings reprint CP-111.
7. "An 8x8 Multiplier and 8-bit μp Perform 16x16 Bit Multiplication," Shai Mor, *EDN,* November 5, 1979. Monolithic Memories Article Reprint AR-109.
8. "Using a 16x16 Cray Multiplier as a 16-Bit Microprocessor Peripheral to Perform 32-Bit Multiplication and Division," Chuck Hastings, Monolithic Memories Conference Proceedings reprint CP-140
9. "The Design and Application of a High-Speed Multiply/Divide Board for the STD Bus," Michael Linse, Gary Oliver, Kirk Bailey, and Michael Alan Baxter, Monolithic Memories Application Note AN-115.
10. "Minimum Chip-Count Number Cruncher Uses Bipolar Co-Processor," C. Hastings, E. Gordon, and R. Blasco. Monolithic Memories Conference Proceedings reprint CP-109.
11. "Medium-speed Multipliers Trim Cost, Shrink Band-width in Speed Transmission," Shlomo Waser and Allen Peterson, *Electronic Design,* February 1, 1979; pages 58-65. Monolithic Memories Article Reprint AR-107.
12. "A Synchronous Multi-Microprocessor System for Implementing Digital Signal Processing Algorithms," T.P. Barnwell, III and C.J.M. Hodges, *Southcon/82 Professional Program Session Record,* Session 21 reprint, paper 21/4.

16x16 Multiplier/Divider
SN74S516

Features/Benefits

- **Co-processor for enhancing the arithmetic speed of all present 16-bit and 8-bit microprocessors**
- **Bus-oriented organization**
- **24-pin package**
- **16/16 or 32/16 division in less than 3.5 μsec**
- **16x16 multiplication in less than 1.5 μsec**
- **28 different multiplication instructions such as "fractional multiply and accumulate"**
- **13 different divide instructions**
- **Self-contained and microprogrammable**

Description

The SN74S516 ('S516) is a bus-organized 16x16 Multiplier/Divider. The device provides both multiplication and division of 2s-complement 16-bit numbers at high speed. There are 28 different multiply options, including: positive and negative multiply, positive and negative accumulation, multiplication by a constant, and both single-length and double-length addition in conjunction with multiplication. 13 different divide options allow single-length or double-length division, division of a previously-generated result, division by a constant, and continued division of a remainder or quotient.

The 'S516 is a time-sequenced device requiring a single clock. It loads operands from, and presents results to, a bidirectional 16-bit bus. Loading of the operands, reading of the results, and sequential control of the device is performed by a 3-bit instruction field.

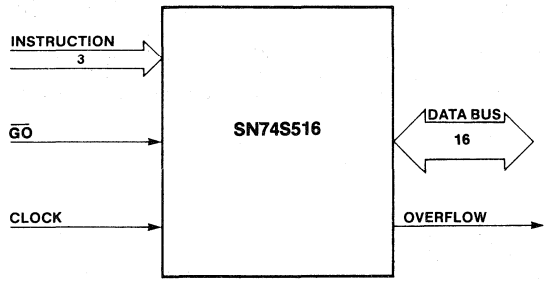
The 'S516 has the additional feature that operands and results can be either integers or fractions; when it deals with fractions, automatic scaling occurs. Results can be rounded if required, and an Overflow output indicates whenever a result is outside the normally-accepted number range.

For a simple multiplication of two operands the device takes nine clock periods — one for initialization, and eight for the actual multiplication. A realistic clock period is 167 ns, which gives a multiplication time of 1333 ns typical for 16x16 multiplication, plus 167 ns additionally for initialization, or 1500 ns in all. More complex multiplications will take additional clock periods for loading the additional operands. A simple division operation requires 16 + 4 = 20 clock periods for a typical time of 3.333 ns (32 bits/16 bits), also plus 167 ns for initialization, or 3500 ns in all.

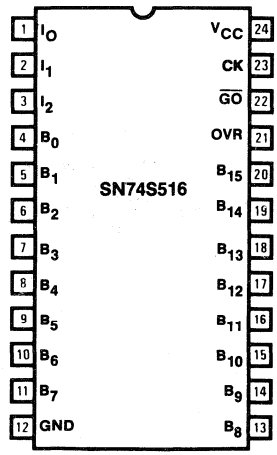
Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN74S516	24T	Commercial

Logic Symbol



Pin Configuration



2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories

INSTRUCTION SEQUENCE				OPERATION	CLOCK CYCLES
ARITHMETIC OPERATIONS					
			0	$X1 \cdot Y$	9
			1	$-X1 \cdot Y$	9
			2	$X1 \cdot Y + K_Z, K_W$	9
			3	$-X1 \cdot Y + K_Z, K_W$	9
			4	$K_Z, K_W/X1$	21
		5/6	0	$X \cdot Y$	10
		5/6	1	$-X \cdot Y$	10
		5/6	2	$X \cdot Y + K_Z, K_W$	10
		5/6	3	$-X \cdot Y + K_Z, K_W$	10
		5/6	4	K_W/X	22
		5/6	5	K_Z/X	22
	5/6	6	0	$X \cdot Y + Z$	11
	5/6	6	1	$-X \cdot Y + Z$	11
	5/6	6	2	$X \cdot Y + K_Z \cdot 2^{-16}$	11
	5/6	6	3	$-X \cdot Y + K_Z \cdot 2^{-16}$	11
	5/6	6	4	Z, W/X	23
	5/6	6	5	Z/X	23
5/6	6	6	0	$X \cdot Y + Z$, W	12
5/6	6	6	1	$-X \cdot Y + Z$, W	12
5/6	6	6	2	$X \cdot Y + W_{sign}$	12
5/6	6	6	3	$-X \cdot Y + W_{sign}$	12
5/6	6	6	4	W/X	24
5/6	6	6	5	W_{sign}/X	24
5/6	6	6	6	(See Note 9 below.)	—
5/6	6	6	7	Load X, Load Z, Load W, Clear Z	4
	5/6	6	7	Load X, Load Z, Read Z	3
READING OPERATIONS					
			7	Read Z	1
		7	7	Read Z, W	2
	7	7	7	Read Z, W, Z	3
7	7	7	7	Read Z, W, Z, W	4
		5	7	Round, then Read Z	2
	5	7	7	Round, then Read Z, W	3

NOTES:
1. X,Y are input multiplier and multiplicand.
2. X1 is the previous contents of the first rank of the X register (either the old X or a new X).
3. Fractional or integer arithmetic is specified by having the next-to-the-last operand loaded using a 5 or 6 instruction respectively. All rows beginning with "5/6" in effect represent *two* instructions. 5 does fractional arithmetic and 6 does integer arithmetic.
4. Z, W is a double-precision number. Z is the most significant half. Z, W represents addend upon input, and product (or accumulated sum) after multiplication.
5. K_Z, K_W represents previous accumulator contents. K_Z is the most-significant half.
6. W_{sign} is a single-length signed number, with sign extension.
7. Maximum clock cycle = 167 ns for an 6-MHz clock.
8. If n instruction codes are shown at the left under "instruction sequences," the number of clock cycles at the right is n+8 for multiplication and n+20 for division.
9. The code "5/6 6 6 6" represents an incomplete operation since it leaves the 'S516 in state 1 rather than in state 0, 8, or 10.

Figure 1. 'S516 Instruction Set (Partial List)

SUMMARY OF SIGNALS/PINS	
B_{15}-B_0	Bidirectional data bus inputs/outputs
I_2-I_0	Instruction (sequential control) input
CK	Clock pulse input
$\overline{GO}$	Chip activation input
OVR	Arithmetic overflow output

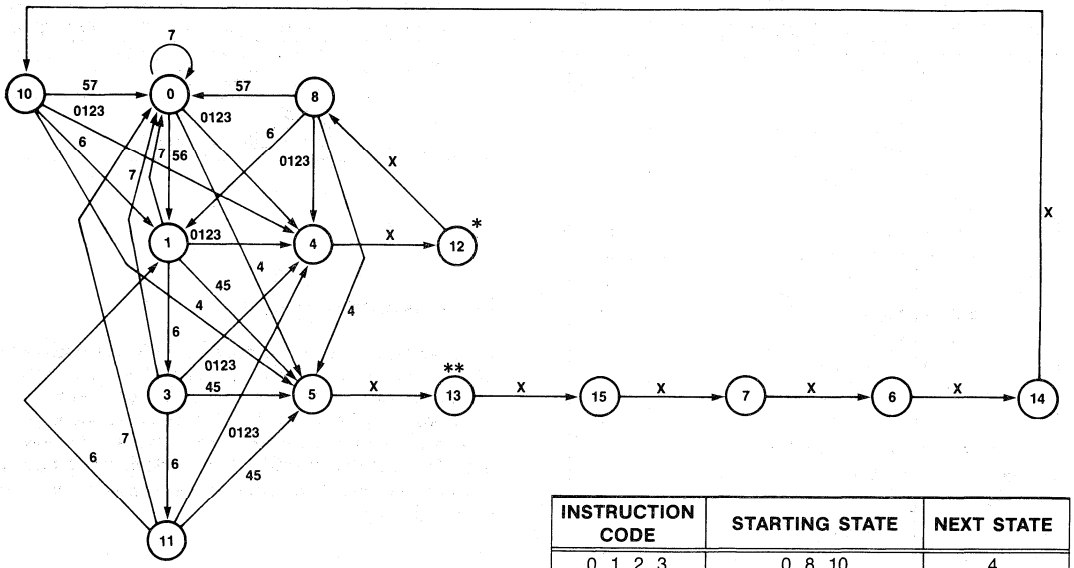
Description (continued)

The 'S516 device uses standard low-power Schottky technology, requires a single +5V power supply, and is fully TTL compatible. Bus inputs require at most 250 μA input current, and control and clock inputs require at most 1 mA input current. Bus outputs are three-state, and are capable of sinking 8 mA at the low logic level. The 'S516 is available in both commercial-temperature and military-temperature ranges, in a 600-mil 24-pin dual-in-line ceramic package.

Device Operation

The 'S516 contains four 16-bit working registers. Y is the multiplier register; X is the multiplicand and divisor register; W is the least-significant half of a double-length accumulator, and holds the least-significant half of the product after a multiplication operation, or the remainder after a division operation; and Z is the most-significant half of this same accumulator. In addition to these registers, there is a high-speed arithmetic unit which performs addition, subtraction, and shifting steps in order to accomplish the various arithmetic operations; a loading sequencer; and a PLA control network.

Operands are loaded into the working registers in time sequence at each clock period, under the control of this sequencer. The chip-activation signal $\overline{GO}$ must be LOW in order to begin the loading process and continue to the next step in the loading operation. If $\overline{GO}$ is continually held HIGH, the 'S516 remains in a wait state with its outputs held in their high-impedance states, so that the other devices attached to the bus may drive it. In this condition, the 'S516 does not respond to any codes on its instruction inputs; in effect, it does not "wake up" until $\overline{GO}$ goes LOW. Also, $\overline{GO}$ may change only when the clock input CK is HIGH. After all of the operands are loaded, the 'S516 jumps to the multiply routine, or to the divide routine, and performs the required operations as indicated in Figure 1. After 9 clock periods for a simple multiply or 21 clock periods for a simple divide, for example, the result is placed on the bus in time sequence.



INSTRUCTION CODE	STARTING STATE	NEXT STATE
0, 1, 2, 3	0, 8, 10	4
4	0, 8, 10	5
5	0	1
5, 7	8, 10	0
6	0, 8, 10	1
7	0, 8, 10	0

*Loop 7 times for multiplication.
**Loop 14 times for fractional division, or 15 times for integer division.

KEY:

The numbers inside the circles indicate the *state* of the 'S516 multiplier/divider. These states are represented by a four-bit state counter, where A is the least-significant bit of this state counter and D is the most-significant bit. (These four bits are not available externally on the 'S516.)

The next state of the 'S516 is a function of the present state and the instruction lines. For example if the 'S516 is at state 0 and the instruction is 0, 1, 2, or 3, then the next state is state 4 (multiply instruction); if the instruction is 4, the next state is state 5 (divide instruction); and so forth. The instructions which take the 'S516 from one state to another are indicated by the numbers written next to the state-transition path lines. "0123," for instance, implies that *any* of instructions 0, 1, 2, or 3 will take the 'S516 along the path marked "0123."

"X" next to a path implies that the path will be followed regardless of the value of the instruction inputs at that time. In other words, for the purpose of state transitions, X means "don't care." There are cases, however, where the particular instruction used may affect when the contents of the registers are available on the bus — see Figures 9 and 10 for contrasting examples of how this effect operates.

Figure 2. Transition Diagram for the 'S516 Multiplier/Divider

Three instruction inputs I_2, I_1, I_0, which may change only when the clock input CK is HIGH, select the required function and drive the sequencer from state to state. Thus, the action of the multiplier/divider at any clock period is a function of the machine state and the state of the control inputs. Figure 2 shows the multiply/divide state table, and all possible operations. After a Read or Round operation, the machine is driven back to state 0, and a new sequence of arithmetic operations is assumed. If a chain operation is being performed, such as accumulation of products, state 0 is bypassed, and loading of an operand or jumping to the next arithmetic operation occurs at the end of the previous arithmetic operation — at state 8 for a multiplication instruction, or at state 10 for a division instruction.

Register X is a dual-rank register, which allows the loading of an operand X during the multiplication or division process. If the machine enters the loading sequence and a new X operand has not been loaded, then the machine proceeds with the previously-loaded X, denoted in this text as "X1." This loading-while-processing capability allows a cycle to be saved during "chained" calculations, and also allows multiplication and division by a constant. (See Figure 13). (continued next page)

Figures 3 and 4 show the codes and durations for the 41 different possible arithmetic operations. These operations can be concatenated in strings to perform complicated 2s-complement arithmetic operations at high-speed. Rounding and reading of results can be performed after any operation. Figure 5 is a block diagram of the 'S516 16x16 Multiplier/Divider.

(continued page after next)

OPERATION		TIME-SLOT 1	2	3	4	5	6	7	8	9	10	11	12
X1 · Y	INS CODE	0	MULTIPLY										
	BUS	Y											
-X1 · Y	INS CODE	1	MULTIPLY										
	BUS	Y											
X1 · Y + K_Z, K_W	INS CODE	2	MULTIPLY										
	BUS	Y											
-X1 · Y + K_Z, K_W	INS CODE	3	MULTIPLY										
	BUS	Y											
X · Y	INS CODE	5/6	0	MULTIPLY									
	BUS	X	Y										
-X · Y	INS CODE	5/6	1	MULTIPLY									
	BUS	X	Y										
X · Y + K_Z, K_W	INS CODE	5/6	2	MULTIPLY									
	BUS	X	Y										
-X · Y + K_Z, K_W	INS CODE	5/6	3	MULTIPLY									
	BUS	X	Y										
X · Y + Z	INS CODE	5/6	6	0	MULTIPLY								
	BUS	X	Z	Y									
-X · Y + Z	INS CODE	5/6	6	1	MULTIPLY								
	BUS	X	Z	Y									
X · Y + $K_Z \cdot 2^{-16}$	INS CODE	5/6	6	2	MULTIPLY								
	BUS	X	—	Y									
-X · Y + $K_Z \cdot 2^{-16}$	INS CODE	5/6	6	3	MULTIPLY								
	BUS	X	—	Y									
X · Y + Z, W	INS CODE	5/6	6	6	0	MULTIPLY							
	BUS	X	Z	W	Y								
-X · Y + Z, W	INS CODE	5/6	6	6	1	MULTIPLY							
	BUS	X	Z	W	Y								
X · Y + W_{sign}	INS CODE	5/6	6	6	2	MULTIPLY							
	BUS	X	—	W	Y								
-X · Y + W_{sign}	INS CODE	5/6	6	6	3	MULTIPLY							
	BUS	X	—	W	Y								

NOTES: 1) X1 is the previous contents of the first rank of the X register (either old X or a new X).
2) $K_Z \cdot 2^{-16}$ is a single-length signed number comprising the most-significant half of the previous double-length product and here gets added in at the least-significant end of the new result.
3) W_{sign} is a single-length signed number, with sign-extension as needed.
4) Fractional or integer arithmetic is specified by having the next-to-the-last operand loaded using a 5 or 6 instruction respectively. All rows beginning with "5/6" in effect represent *two* instructions. 5 does fractional arithmetic and 6 does integer arithmetic.

Figure 3. Multiplication Codes and Times for 16x16 Multiplication in the 'S516

OPERATION		TIME-SLOT 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
$K_Z, K_W/X_1$	INS CODE	4	DIVIDE																			1			
	BUS	—																							
K_W/X	INS CODE	5/6	4	DIVIDE																			1		
	BUS	X	—																						
K_Z/X	INS CODE	5/6	5	DIVIDE																			1		
	BUS	X	—																						
Z, W/X	INS CODE	5/6	6	4	DIVIDE																			1	
	BUS	X	Z	W																					
Z/X	INS CODE	5/6	6	5	DIVIDE																			1	
	BUS	X	Z	—																					
W/X	INS CODE	5/6	6	6	4	DIVIDE																			1
	BUS	X	—	W	—																				
W_{sign}/X	INS CODE	5/6	6	6	5	DIVIDE																			1
	BUS	X	0	W	—																				

NOTES: 1) X1 is the previous contents of the first rank of the X register (either old X or a new X).
2) Fractional division divides a 32-bit 2s-complement number in 1 clock period less than integer division.
3) W_{sign} is a single-length signed number, with sign-extension as needed.
4) Division operation W_{sign}/X requires that the Z register be initialized with all-zero contents at the time Z is loaded.
5) Fractional or integer arithmetic is specified by having the next-to-the-last operand loaded using a 5 or 6 instruction respectively. All rows beginning with "5/6" in effect represent *two* instructions, one of which does fractional arithmetic and one of which does integer arithmetic.

Figure 4. Division Codes and Times for 32/16 Division in 'S516

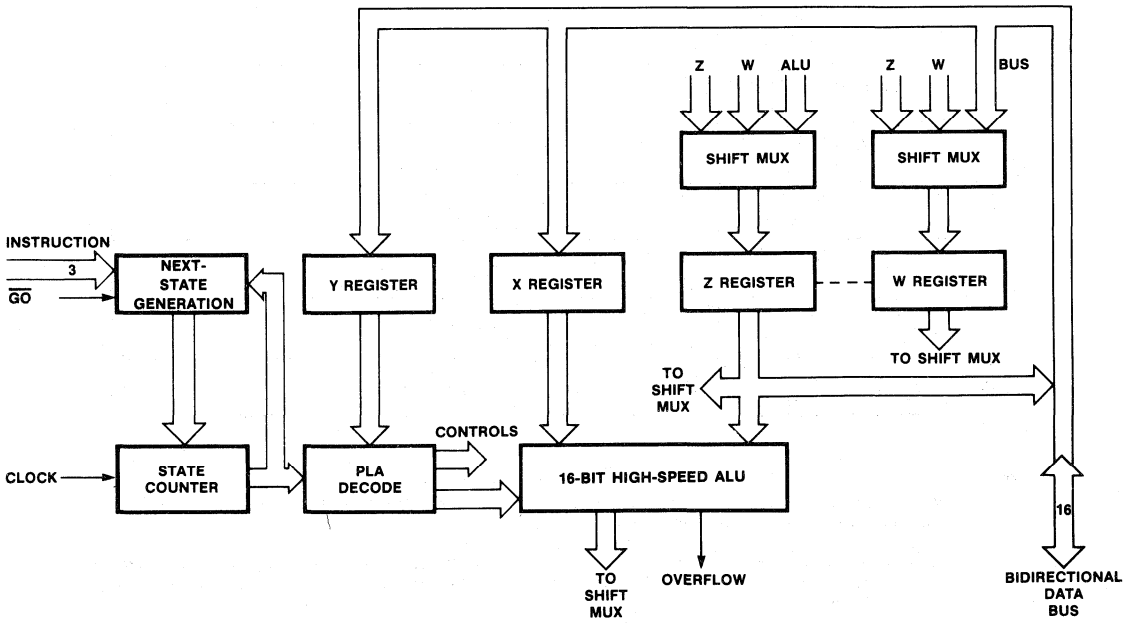


Figure 5. Internal Architecture of the 'S516

Initialization

The 'S516 has no direct master reset input. However, initialization of the 'S516 can easily be performed by continually presenting instruction code 7, which after a maximum of 21 clock periods forces the machine back to state 0.

Multiplication

The 'S516 provides 2s-complement 16-bit multiplication, and can also accumulate previously-generated double-length products. No time penalty is incurred for accumulation, since the machine accumulates while the multiplication operation is proceeding. In addition to accumulation, the device can add into a product either a single-length or a double-length number. It can also use a previously-loaded operand as a constant, so that constant multiplication and accumulation is possible.

One key feature is the ability to perform both positive multiplications and negative multiplications, again without any speed penalty. This feature allows complex-arithmetic multiplications to be programmed with very little overhead. Another important feature is the ability to work with either fractions or integers.

Division

The 'S516 also provides a range of division operations. A double-length number in Z,W is divided by X; the result Q is stored in Z, and the remainder R in W. Again all numbers are in the 2s-complement number representation, with the most significant bit of an operand (whether single-length or double-length) having a negative weight. In order to facilitate repeated division, with the multiple-length quotient always keeping the same sign, the remainder is always the same sign as the dividend. Fractional or integer operation is possible, and division and multiplication operations can be concatenated. For example, the operations (AxB)/C, (A + B)/C can easily be performed. The dividend can be any previously-generated result — product, quotient, or remainder; or it may be a double-length or single-length signed operand.

Reading Results

The result of an arithmetic operation, or of a string of operations, can be read onto the 16-bit bus if the machine is at the end of an operation or at the start of a new sequence. The read operation requires that the $\overline{GO}$ signal be held LOW so that the information is read out onto the bidirectional bus, when code 7 is specified. (See Figure 6.) Since there is a double-length accumulator Z,W, reading can take two cycles. First, register Z is read. After another clock has been received, if code 7 is still present, the least-significant half of the product from the W register is placed on the bus, or likewise the remainder if a division operation had been performed.

If the 'S516 is instructed to perform a read operation during the loading sequence, then the sequence is broken and the machine is forced back to state 0 ready to start the sequence again. Control read operations at state 0 just swap the contents of register Z and W.

Integer and Fractional Arithmetic

The 'S516 can work with either fractional or integer number representations. When working with integers, all numbers are scaled from the least-significant end, and the least-significant bit is assumed to have a weight of 2^0. For integer multiplication, accumulation, and division, all numbers are scaled from this least-significant weight, and results are correct if interpreted in this manner. The double-length register Z,W can therefore hold numbers in the range -2^{31} to $+2^{31}-1$; the operands X and Y, and single-length results, are in the range -2^{15} to $+2^{15}-1$.

When working with fractions, the machine automatically performs scaling so that input operands and results have a consistent format. All numbers in the fractional representation are scaled from the most significant end, which has a weight of -2^0 *(negative)*. The binary point is one place to the right of this most-significant bit, so that the next bit has a weight of 2^{-1}. The double-length register Z,W therefore holds numbers in the range -1 to $+1-2^{-31}$ and the operands X and Y and single-length results are in the range -1 to $+1-2^{15}$. Since automatic scaling occurs, the product of two numbers always has the least-significant bit as a 0, unless an accumulation is performed with the least-significant bit being a 1.

During a chain operation with the partial results not being read onto the bus, the 'S516 will stay in either the fractional or integer mode. At the start of a sequence of operations, fractional or integer operation is designated by loading operands using instruction code 5 or instruction code 6 respectively.

Mixed fractional and integer arithmetic is also possible, by redefining the weight of the least-significant or most-significant bits. However, care must be exercised, due to the automatic scaling feature, when fractional arithmetic is programmed.

Rounding

Rounding can be performed on the result of a multiplication or division. Generally rounding would only be called out during fractional operation, but nothing in the 'S516 precludes forming a rounded result during integer arithmetic.

Rounding for multiplication provides the best single-length most-significant half of the product. Rounding occurs at the end of a multiplication, and is performed instead of a Load or Read operation when a code 5 is specified, instead of a code 7, to get from state 8 or state 10 back to state 0. (See Figure 2; also, note that this mode of operation precludes "stealing" a cycle according to the method illustrated in Figure 9.) The 'S516 looks at the most-significant bit of the least-significant half of the product W_{15}, and adds 1 to the most-significant half of the product at the least-significant end if W_{15} is a 1. After the operation, the 'S516 is in state 0, so that the rounded product can be read, and the W register is cleared.

Rounding for division is performed by forcing the least-significant bit of the quotient in Z to a 1 unless the division is exact (remainder is zero). This method of rounding causes a slightly higher variance in the result than having an additional iterative division operation, but is considerably easier to perform. Again, after rounding the 'S516 goes to state 0, so that a read operation can be performed, and the W register is cleared.

Overflow

The 'S516 has an overflow output OVR which is cleared prior to each operation, and is set during an operation if the product or quotient goes outside the normally-accepted range.

For multiplication, overflow can only occur if the most negative number in the operand range is used: $(-1)x(-1)=+1$, which cannot be held in the 'S516's internal registers. Overflow can more easily occur during either positive or negative accumulation of products. For fractional arithmetic, if the product or accumulation goes outside the range of -1 to $+1-2^{-31}$, then the overflow flipflop will be set.

The overflow flip-flop is enabled in state 8 for the multiply operation or in state 10 for a divide operation. It only gets reset when a transition to state 0 from states 0, 3, 8, 10 and 11, when instruction 7 is being presented to the 'S516.

Overflow may also occur during division if the quotient goes outside the generally-accepted number range of -1 to $+1-2^{-15}$ during fractional operation. This would occur if the divisor is less than the dividend, or equal to the dividend if a positive quotient is being generated. For integer arithmetic the numbers must be scaled by 2^{15}.

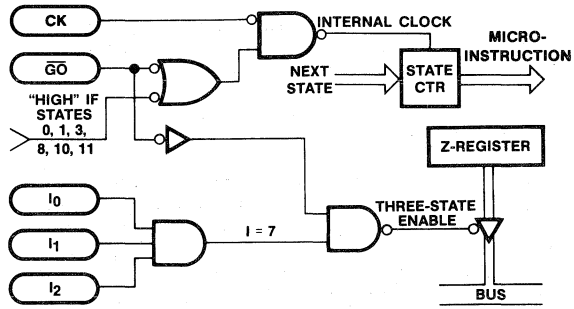


Figure 6. 'S516 Internal Circuitry of "$\overline{GO}$" Line and Three-State-Enable

During the states 0, 1, 3, 8, 10 and 11 if the "GO" line ($\overline{GO}$) is held at logic HIGH then the machine will be in a wait state until $\overline{GO}$ goes to logic LOW.

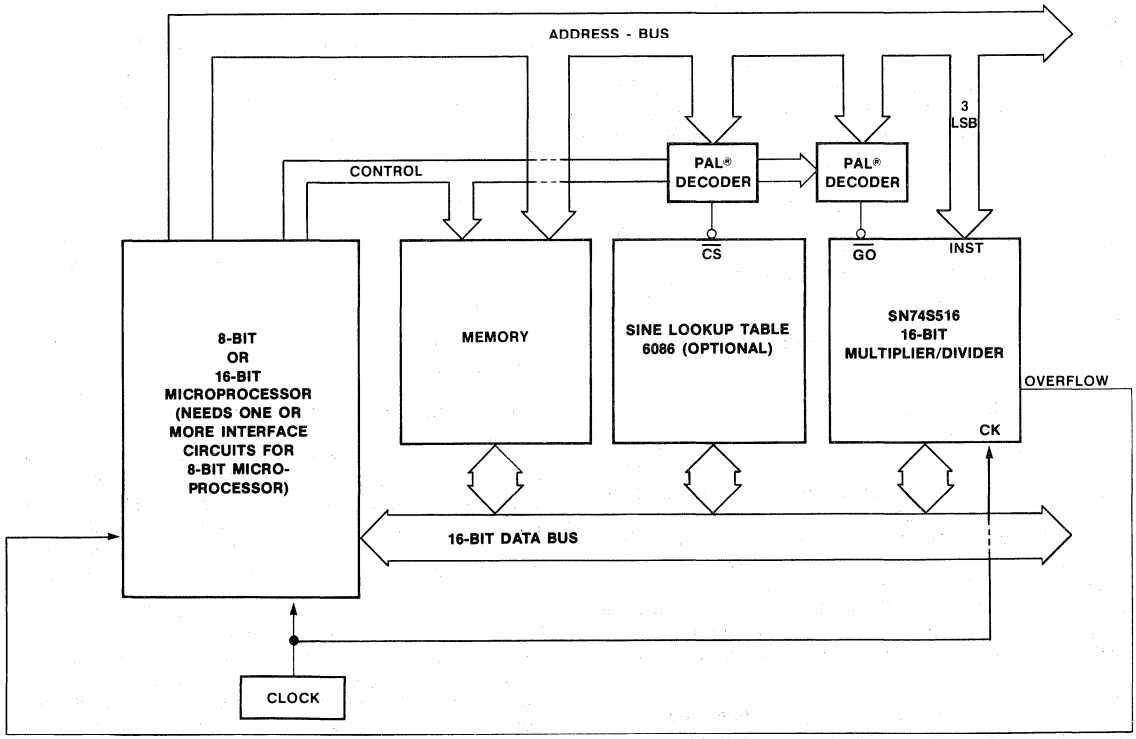


Figure 7. Interfacing the 'S516 to a Microprocessor

Figure 7 shows the block diagram of a microprocessor system with its arithmetic capabilities enhanced by the use of a 'S516 16x16 multiplier/divider. The relatively small number of instruction lines (only 3) of the 'S516 provides a unique way to control the multiplier/divider. As may be seen from Figure 7, these three instruction lines are assigned to the three least-significant bits (LSBs) of the address bus, while the remaining address bits are decoded by a Programmable Array Logic (PAL®) circuit to determine when the multiplier/divider is selected. For example, suppose the 'S516 is assigned address 100; then any address in the range of 100-107 will enable the 'S516 (i.e., the $\overline{GO}$ line is LOW). Thus, if the address is 100 the 'S516 instruction is 0; if the address is 106 the 'S516 instruction is 6; and so forth.

Data Formats

Fractional Multiply

X_i, Y_1 - Input, Multiplicand, Multipler

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

Z_i - MS Half Output Product

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

W_i - LS Half Output Product*

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}	"0"

* The least significant bit of W_i is always a binary 0 due to normalization. Note that -1 x -1 yields an overflow in fractional multiply.

Integer Multiply

X_i, Y_1 - Input, Multiplicand, Multiplier

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Z_i - MS Half Output Product

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}

W_i - LS Half Output Product**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

** The least significant bit of W_i is a valid data bit. Note that $2^{-15} \times 2^{-15}$ yields $+2^{30}$ which can be represented in the output bits without overflowing.

Fractional Divide

Z_i - Input Dividend

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

X - Input Divisor

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

Z_i - Output Quotient

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

W - Output Partial Remainder †

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

† Note that the partial remainder $R = 2^{-15}$ (W)

Integer Divide Example (Z, W)/X

Z_i - MSB Input Dividend

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}

W_i - LSB Input Dividend

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

X - Input Divisor

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Z_i - Output Quotient

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

W_i - Output Partial Remainder

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Absolute Maximum Ratings

Supply voltage V_{CC} ..... 7.0 V
Input voltage ..... 7.0 V
Off-state output voltage ..... 5.5 V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETERS	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		45**	°C
f_{MAX}	Clock frequency	8	6			MHz
t_{CWP}	Positive clock pulse width	8	70			ns
t_{CWN}	Negative clock pulse width	8	50			ns
t_{BS}	Bus setup time for inputting data*	8	50			ns
t_{BH}	Bus hold time for inputting data*	8	35			ns
t_{INSS}	Instruction, GO setup time	8	10			ns
t_{INSH}	Instruction, GO hold time	8	30			ns

* During operations when the bus is being used to input data.
** This device has a limited operating temperature range.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN I_I = −18mA				−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX V_I = 0.5V	B_{15}-B_0			−250	μA
			All other inputs			−1	mA
I_{IH}	High-level input current	V_{CC} = MAX V_I = 2.4V				250	μA
I_I	Maximum input current	V_{CC} = MAX V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN I_{OL} = 8mA			0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN I_{OH} = −2mA		2.4			V
I_{OS}	Output short-circuit current*	V_{CC} = MAX V_O = 0V		−10		−90	mA
I_{CC}	Supply current	V_{CC} = MAX			370	450†	mA

* Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.
† At cold temperatures see the "I_{CC} vs Temperature" curves on the next page for more complete information. The typical values shown here are at 5.0 V.

Switching Characterictics Over Operating Conditions

SYMBOL	PARAMETER		FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{BO}	Bus output delay from CK for outputting data;* C_L = 30 pF		8		70	95	ns
t_{PXZ}	Output disable delay	FROM I_2-I_0 to bus			30	65	ns
		From GO to bus			20	40	
t_{PZX}	Output enable delay; C_L = 30 pF	FROM I_2-I_0 to bus			55	80	ns
		From GO to bus			25	45	
t_{OVR}	Overflow output delay from CK; C_L = 30 pF		8		60	95	ns

* During operations when the bus is being used to output data.

Test Waveforms

TEST	V_X*		OUTPUT WAVEFORM — MEAS. LEVEL
All t_{PD}	5.0V		V_{OH}, V_{OL}, 1.5V
t_{PXZ}	t_{PHZ}	t_{PLZ}	V_{OH}, 0.5V, 0.5V, V_{OL}, 2.8V, 0.0V
	0.0V	5.0V	
t_{PZX}	t_{PZH}	t_{PZL}	2.8V, 0.0V, 1.5V, V_{OH}, V_{OL}
	0.0V	5.0V	

*At diode; see "Test Circuit" figure below.

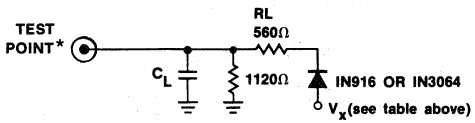
AC Test Conditions

Inputs 0 V_{LOW}, 3 V_{HIGH}. Rise and fall time 1-3 ns from 1 V to 2 V. Measurements are made from 1.5 V_{IN} to 1.5 V_{OUT}, except that t_{PXZ} is measured by a delta in the outputs of 0.5 V from V_{OL} or V_{OH} respectively.

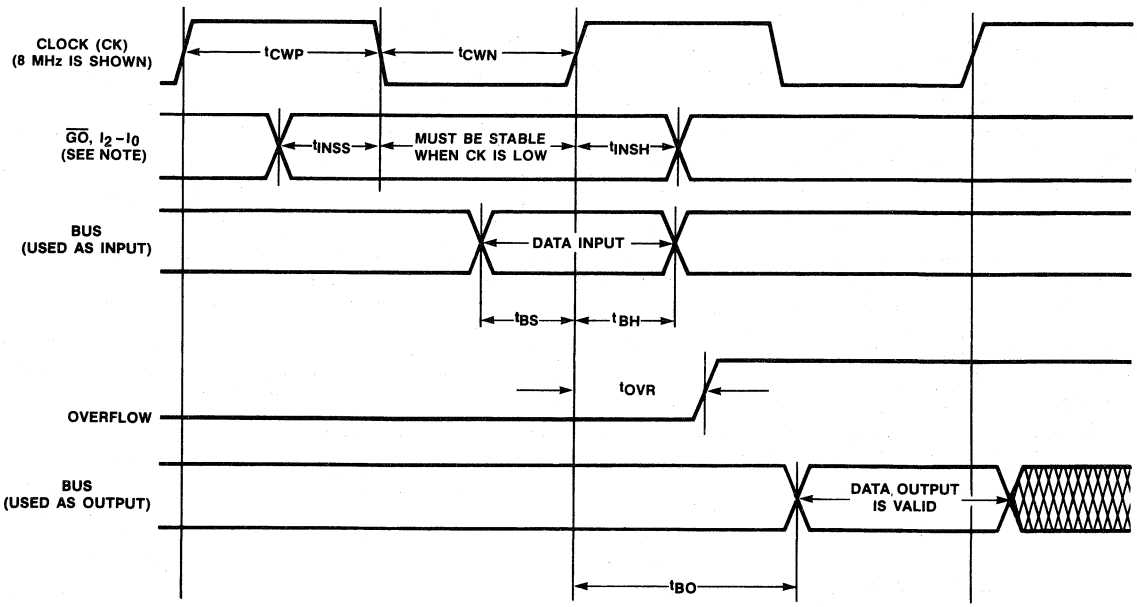
Timing

Timing waveforms are shown in Figure 8. Specific instruction timing examples are shown in Figures 9 through 13.

Test Load

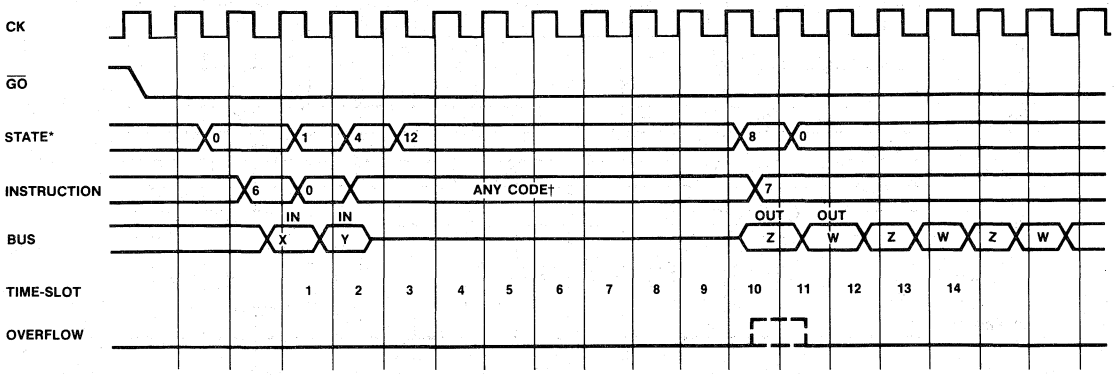


* The "TEST POINT" is driven by the output under test, and observed by instrumentation.



NOTE: $\overline{GO}$ and I_2-I_0 can change only when CK is high.

Figure 8. Timing Diagram of the 'S516



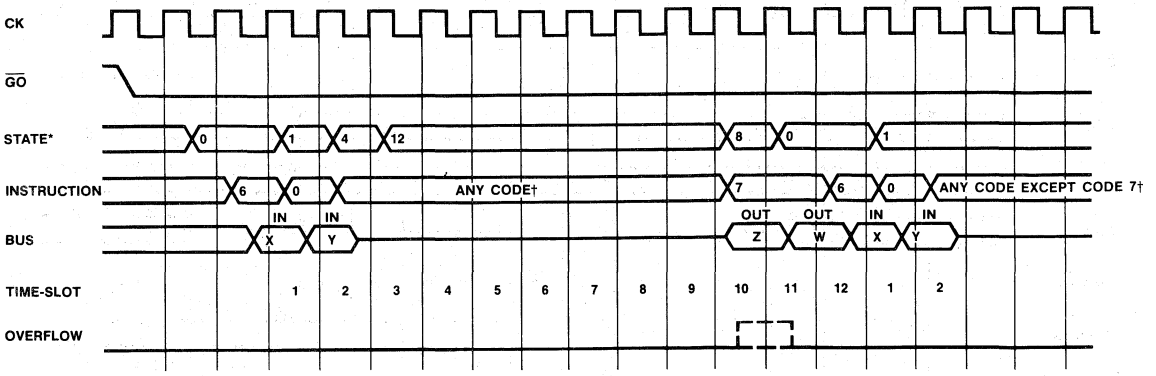
NOTES: Register Z is read at the same time that the overflow signal (if present) is set. If the instruction remains at code 7 after time-slot 11, the contents of registers Z and W are swapped each cycle.

†"Any code" means any of code 0 through code 7. However, code 6 will load a new value of X, and code 7 will cause the 'S516 to attempt to drive the data bus.

*Not available externally on the 'S516.

Figure 9. Instruction Timing Example No. 1: Load X, Load Y, Multiply, Read Z, Read W. By Presenting Code 7 on the Instruction Lines During the Last Multiply Cycle (State 8), the Results May Be Read During Time-Slots 10 and 11

11

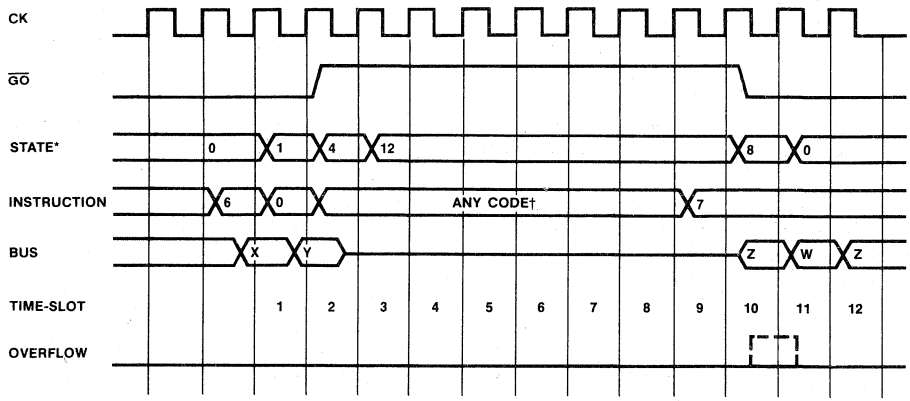


NOTES: The instruction lines may be changed only when CK is high.

†"Any code" means any of code 0 through code 7. Code 6 may be used here since a new X explicitly gets loaded for the next multiply operation. However, code 7 will cause the 'S516 to attempt to drive the data bus.

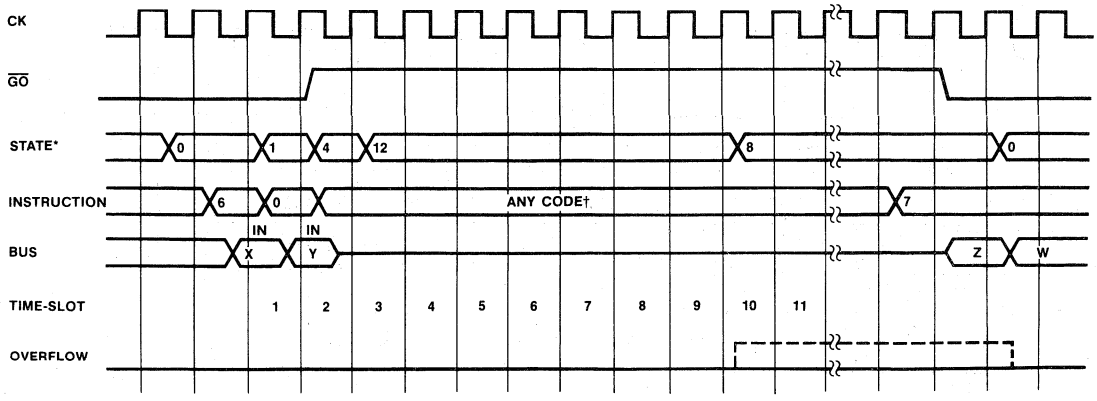
*Not available externally on the 'S516.

Figure 10. Instruction Timing Example No. 2: Repeat: "Load X, Load Y, Multiply, Read Z, Read W"



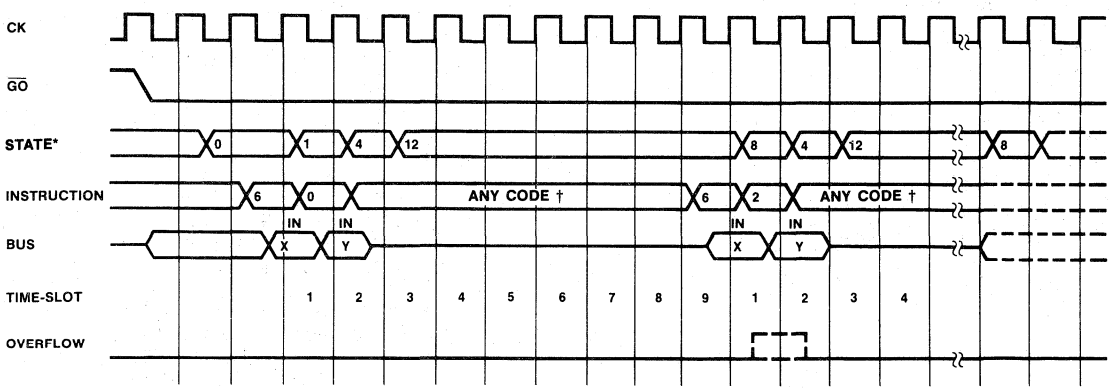
NOTES: Code 7 is given in time-slot 9, but has no effect until time-slot 10 since $\overline{GO}$ is HIGH. After $\overline{GO}$ goes LOW in time-slot 10, Z may be read.
†"Any code" means any of code 0 through code 7.
*Not available externally on the 'S516.

Figure 11. Instruction Timing Example No. 3: Load X, Load Y, Multiply, Read Z, Read W. This Timing Diagram Corresponds to Table 1. Only After Eight Clock Pulses of the Operation Cycle, the Result Is Read — Z During Time-Slot 10 and W During Time-Slot 11



NOTES: †"Any code" means any of code 0 through code 7. Code 6 or code 7 may be used here; since $\overline{GO}$ is HIGH, no new X can be loaded, and the 'S516 cannot attempt to drive the data bus.
*Not available externally on the 'S516.

Figure 12. Instruction Timing Example No. 4: Load X, Load Y, Multiply, Wait, Read Z, Read W



NOTES: This sequence of operations is suitable for use when reading is to be done only at the very end of the operation sequence. The new X value is loaded during the time that the previous multiplication is being performed. See Programming Example #3 for $\sum_{i=1}^{N} X_i \cdot Y_i$

†"Any code" means any of code 0 through code 7. However, code 7 will cause the 'S516 to attempt to drive the data bus.

*Not available externally on the 'S516.

††Code 6 allows loading of a new X in State 12 and it takes the 'S516 State Counter to State 8. In State 8, Y is loaded via instruction 2 and the next multiply-accumulate cycle is initiated.

Figure 13. Instruction Timing Example No. 5: Sum of Products

Programming Examples

In the following examples assume that each line with a separate instruction corresponds to one clock pulse. Instruction codes are 0, 1, 2, 3, 4, 5, 6, 7 and x according to the usage explained in the key to Figure 2.

Programming Example 1

Calculating X · Y (A·B)

INST 6	X ← A
INST 0	Y ← B
INST X	MULT
INST X	MULT
INST X	MULT
INST X	MULT
INST X	MULT
INST X	MULT
INST X	MULT
INST 7	MULT AND READ Z = 16 MSB OF (A·B)
INST 7	READ W = 16 LSB OF (A·B)

Programming Example 2

Calculating X1 · Y (A·C)

X1 is a previous multiplier value. It was previously loaded (in example 1) with A.

INST 0	Y ← C
INST X	MULT
INST X	MULT
INST X	MULT
INST X	MULT
INST X	MULT
INST X	MULT
INST X	MULT
INST 7	MULT and READ Z = 16 MSB OF (A·C)
INST 7	READ W = 16 LSB OF (A·C)

Programming Example 3

Calculating $\sum_{i=1}^{N} X_i \cdot Y_i$ (A·B + C·D + E·F + . . .)

In this case we read only after N multiplications. A new X_{i+1} is loaded during the multiplication process for X_iY_i.

Assume N = 3.

The sequence of instructions and operations for calculating $\sum_{i=1}^{3} X_i \cdot Y_i$ is: (A·B + C·D + E·F)

N = 1	INST 6	X ← A
	INST 0	Y ← B
	INST X	MULT
	INST X	MULT
	INST X	MULT
	INST X	MULT
	INST X	MULT
	INST X	MULT
	INST X	MULT
N = 2	INST 6	MULT and LOAD X ← C Z ← 16 MSB of (A·B) W ← 16 LSB of (A·B)
	INST 2	Y ← D
	INST X	MULT
	INST X	MULT
	INST X	MULT
	INST X	MULT
	INST X	MULT
	INST X	MULT
	INST X	MULT
N = 3	INST 6	MULT and LOAD X ← E Z ← 16 MSB of (C·D + A·B) W ← 16 LSB of (C·D + A·B)
	INST 2	Y ← F
	INST X	MULT
	INST X	MULT
	INST X	MULT
	INST X	MULT
	INST X	MULT
	INST X	MULT
	INST X	MULT
READ Z	INST 7	MULT and READ Z = 16 MSB of (E·F + C·D + A·B
READ W	INST 7	READ W = 16 LSB of (E·F + C·D + A·B

Programming Example 4

Multiplication plus a constant (A·B + Constant)
Assume that the constant is a 32-bit 2s-complement number.

INST 6	X ← A	
INST 6	Z ← C	LOAD 16 MSB of constant
INST 6	W ← D	LOAD 16 LSB of constant
INST 0	Y ← B	
INST X	MULT	} Perform A·B + (Z, W)
INST X	MULT	
INST X	MULT	
INST X	MULT	
INST X	MULT	
INST X	MULT	
INST X	MULT	
INST 7	MULT and READ Z = 16 MSB of (A·B + (C, D))	
INST 7	READ W = 16 LSB of (A·B + (C, D))	

Programming Example 5

Dividing a 32-bit number by a 16-bit number ((B, C)/A)

INST 6	X ← A	
INST 6	Z ← B	
INST 4	W ← C	
INST X		} Perform Division $\frac{(Z, W)}{X}$
INST X		
INST X		
INST X		
INST X		
INST X		
INST X		
INST X		
INST X		
INST X		
INST X		
INST X		
INST X		
INST X		
INST X		
INST X		
INST 7	DIVIDE and READ the quotient Z = $\frac{(B, C)}{A}$	
INST 7	READ the remainder W of $\frac{(B, C)}{A}$	

11

16x16 Flow-Thru™ Multiplier Slice
74S556

Features/Benefits

- **Twos-complement, unsigned, or mixed operands**
- **Full 32-bit product immediately available on each cycle**
- **High-speed 16x16 parallel multiplier**
- **Latched or transparent inputs/outputs**
- **Three-state output controls, independent for each half of the product**
- **Single +5 V supply (via multiple pins)**
- **Available in 84-terminal Leadless-Chip Carrier and 88-Pin-Grid-Array packages**

Description

The 'S556 is a high-speed 16x16 combinatorial multiplier which can multiply two 16-bit unsigned or signed twos-complement numbers on every cycle. Each operand X and Y has an associated mode-control line, XM and YM respectively. When a mode-control line is at a LOW logic level, the operand is treated as an unsigned 16-bit number; when the mode-control line is at a HIGH logic level, the operand is treated as a 16-bit signed twos-complement number. Additional inputs RS and RU allow the addition of a bit into the multiplier array at the appropriate bit positions for rounding. The entire 32-bit double-length product is available at the outputs at one time.

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
74S556	P88, L84*	Commercial

P88 is an 88-Pin-Grid-Array Package.

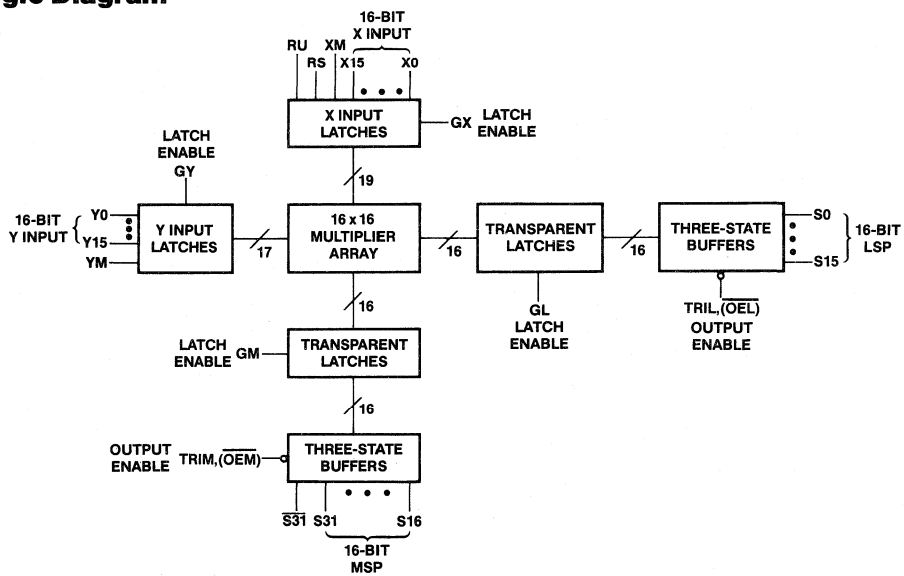
L84 is an 84-terminal Leadless-Chip Carrier Package.

* The 84-terminal leadless chip carrier, L84, and its socket, L84-2, are in development; contact the factory for further details.

The most-significant product bit, S31, is available in both true and complemented form to simplify longer-wordlength multiplications. The product outputs are three-state, controlled by assertive-low enables. The MSP outputs are controlled by the TRIM ($\overline{OEM}$) control input, while the LSP outputs are controlled by the TRIL ($\overline{OEL}$) control input. This allows one or more multipliers to be connected to a parallel bus or to be used in a pipelined system.

All inputs and outputs have transparent latches. The latches become transparent when the input to the corresponding gate control line GX, GY, GM, GL is HIGH. If latches are not required, these control inputs may be tied HIGH, leaving the multiplier fully transparent for combinatorial cascading. The device uses a single +5 V power supply, and is available both in an 84-terminal leadless chip carrier (LCC) package and in an 88-pin-grid-array package.

'S556 Logic Diagram



2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Monolithic Memories MMI

SUMMARY OF SIGNALS/PINS	
X_{15-0}	Multiplicand 16-bit data inputs
Y_{15-0}	Multiplier 16-bit data inputs
XM, YM	Mode-control inputs for each data word; LOW for unsigned data and HIGH for twos-complement data
S_{31-0}	Product 32-bit output
$\overline{S}_{31}$	Inverted MS product bit (for expansion)
RS, RU	Rounding inputs for signed and unsigned data, respectively
GX	Gate control for X_i, RS, RU
GY	Gate control for Y_i
GL	Gate control for least-significant half of product
GM	Gate control for most-significant half of product
TRIL / $\overline{\text{OEL}}$	Three-state control for least-significant half of product
TRIM / $\overline{\text{OEM}}$	Three-state control for most-significant half of products

Rounding Inputs

INPUTS		ADDS		USUALLY USED WITH	
RU	RS	2^{15}	2^{14}	XM	YM
L	L	NO	NO	X	X
L	H	NO	YES	H†	H†
H	L	YES	NO	L	L
H	H	YES	YES	*	*

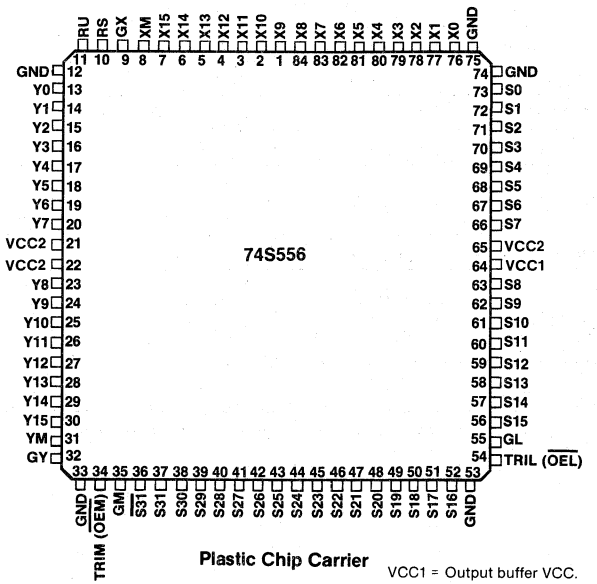
† In mixed mode, one of these could be low but not both.

* Usually a nonsense operation.

Mode-Control Inputs

OPERATING MODE	INPUT DATA		MODE-CONTROL INPUTS	
	X_{15-0}	Y_{15-0}	XM	YM
Unsigned	Unsigned	Unsigned	L	L
Mixed	Unsigned	Twos-Comp.	L	H
	Twos-Comp.	Unsigned	H	L
Signed	Twos-Comp.	Twos-Comp.	H	H

84-Terminal Leadless Chip Carrier Pinout



Plastic Chip Carrier

VCC1 = Output buffer VCC.
VCC2 = Logic VCC.

All V_{CC} and GND pins must be connected to the respective V_{CC} and GND connections on the board and should not be used for daisychaining through the IC.

Operating Conditions

SYMBOL	PARAMETER		FIGURE	COMMERCIAL MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage			4.75	5	5.25	V
T_A	Operating free-air temperature			0		75	°C
t_{S1}	Setup time $(X_i, R_i)/Y_i$ to GX/GY		2a, 2b	10			ns
t_{S2}	Setup time X_i, Y_i, R_i to GM, GL	t_{S2L}	3a, 3b	60			ns
		t_{S2M}		74			
t_{S3}	Setup time GX, GY to GL, GM	t_{S3L}	4a, 4b, 4c, 4d, 4e, 4f	60			ns
		t_{S3M}		75			
t_{H1}	Hold time $(X_i, R_i)/Y_i$ to GX/GY		2a, 2b	8			ns
t_{H2}	Hold time X_i, Y_i, R_i to GM, GL	t_{H2L}, t_{H2M}	3a, 3b	3			ns
t_{H3}	Hold time GX, GY to GM, GL	t_{H3L}, t_{H3M}	4a, 4b, 4c, 4d, 4e, 4f	0			ns
t_w	Latch enable pulse width		6	12			ns

* Indicates case temperature.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage**					0.8	V
V_{IH}	High-level input voltage**			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA			−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			−0.4	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4 V			75	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 8 mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = −2 mA	2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.5 V			−100	μA
I_{OZH}			V_O = 2.4 V			100	μA
I_{OS}	Output short-circuit current*	V_{CC} = MAX	V_O = 0 V	−20		−90	mA
I_{CC}	Supply current	V_{CC} = MAX			600	800	mA
I_{CC}	Supply current at hot temperature limit	V_{CC} = 5.25 V	T_A = 75°C			700	mA

† Typicals at 5.0 V and 25°C T_A.

* Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

** These are absolute voltages with respect to the ground pins and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	74S556 COMMERCIAL			UNIT
				MIN	TYP	MAX	
t_{DTL}	Transparent Multiply GX, GY, GM, GL = H	X_i,Y_i,R_i to S_{15-0} Figs. 1, 2c, 3b, 4c, 4f	CL = 30 pF RL = 560 Ω See figure 7		50	76	ns
t_{DTM}		X_i,Y_i,R_i to $S_{31},\overline{S}_{31-16}$ Figs. 1, 2c, 3b, 4c, 4f			60	90	ns
t_{D1L}	Transparent Output Multiply GM, GL = H	GX, GY to S_{15-0} Figs. 2a, 2b, 4d, 4e				80	ns
t_{D1M}		GX,GY, to $S_{31},\overline{S}_{31-16}$ Figs. 2a, 2b, 4d, 4e				92	ns
t_{D2}	Transparent Input Multiply GX, GY = H	GM, GL to S_i Figs. 3a, 4a, 4b				35	ns
t_{PXZ}	Three-State Disable Timing	TRIL ($\overline{OEL}$), TRIM ($\overline{OEM}$) to S_i Fig. 5				30	ns
t_{PZX}	Three-State Enable Timing	TRIL ($\overline{OEL}$), TRIM ($\overline{OEM}$) to S_i Fig. 5				30	ns

Transparent Multiply — Flowthrough Operation

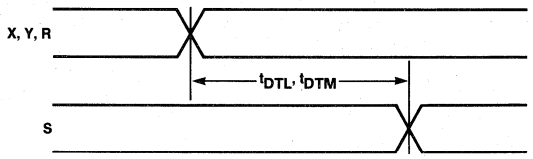
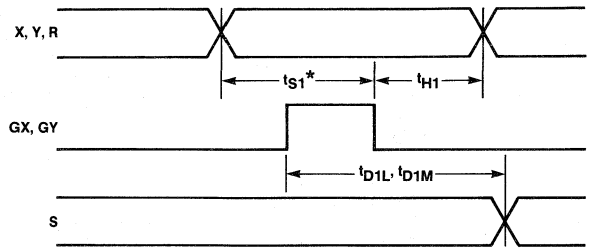


Figure 1

The transparent multiply is a flowthrough operation of the 'S556. Both the input and output latches are made transparent by keeping GX, GY, GM, and GL at a HIGH level. The operands are presented to the X, Y, and R inputs; the results are available t_{DTL} and t_{DTM} later, for the least and most significant halves of the product respectively.

Transparent Output Multiply — Pipelined Input



* With this particular timing, set-up time t_{S1} will automatically be met.

Figure 2a.

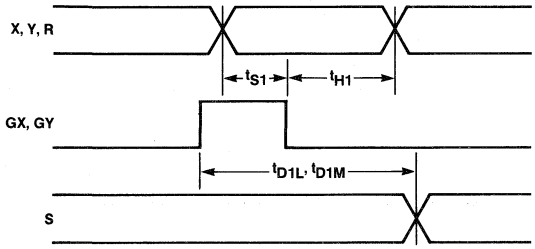


Figure 2b

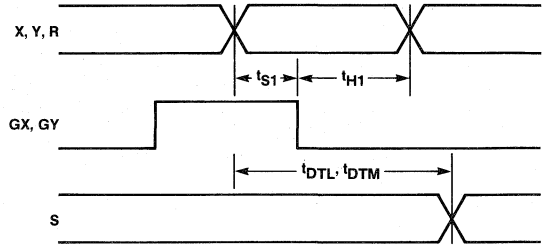


Figure 2c

By tying the GL and GM lines HIGH, the 'S556 can perform transparent output (or pipelined input) multiplies. Data present is latched at the inputs using the GX and GY control signals. The time at which the result S is present at the outputs depends on when the rising edges of GX and GY occur. If the rising edges of GX and GY occur *after* the operand inputs change, then Figure 2a applies; the result will be available at the outputs t_{D1L} and t_{D1M}* after the rising edges of GX and GY. If the rising edges of GX and GY occur *less than* ($t_{W\,min}$ - $t_{S1\,min}$) *before* the operand inputs change, then Figure 2b applies; in this case the result will also be available at the outputs t_{D1L} and t_{D1M}* after the rising edges of GX and GY. However, if the rising edges of GX and GY occur *more than* ($t_{W\,min}$ - $t_{S1\,min}$) *before* the operand inputs change, then Figure 2c applies; the result will appear at the outputs t_{DTL} and t_{DTM}* after the operand inputs change.

* For the least and most significant halves of the product, respectively.

Transparent Input Multiply — Pipelined Output

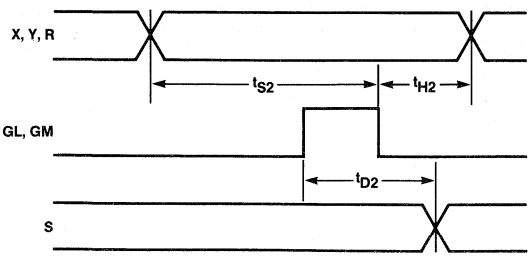


Figure 3a

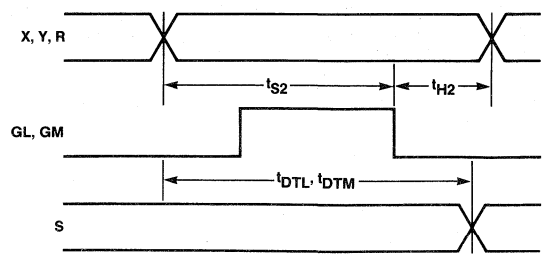


Figure 3b

By tying the GX and GY lines HIGH, the 'S556 can perform transparent input (or pipelined output) multiplies. Data is presented at the inputs, and t_{S2} after X, Y and R change, the results can be latched. The time at which the result S is present at the outputs depends upon when the rising edges of GL and GM occur. If they occur *at or after* ($t_{S2\,min}$ - $t_{W\,min}$) from the inputs changing, then Figure 3a applies; the result appears at the outputs t_{D2} after the rising edges of GL and GM. If the rising edges of GL and GM occur *before* ($t_{S2\,min}$ - $t_{W\,min}$) from the inputs changing, then Figure 3b applies; the result appears at the outputs t_{DTL} and t_{DTM}* after the operand inputs change.

* For the least and most significant halves of the product, respectively.

Gated Multiply — Pipelined Input and Output

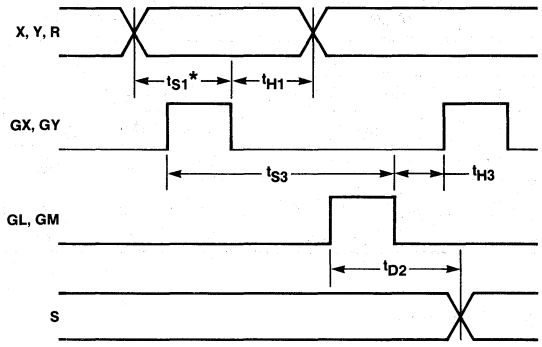


Figure 4a

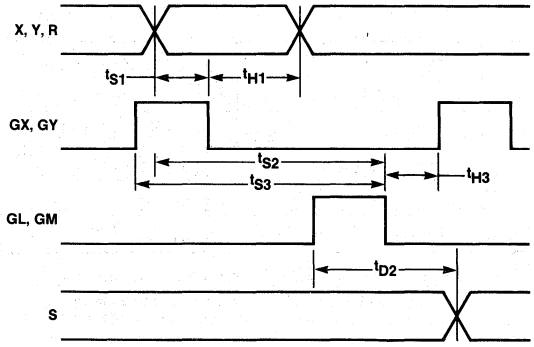


Figure 4b

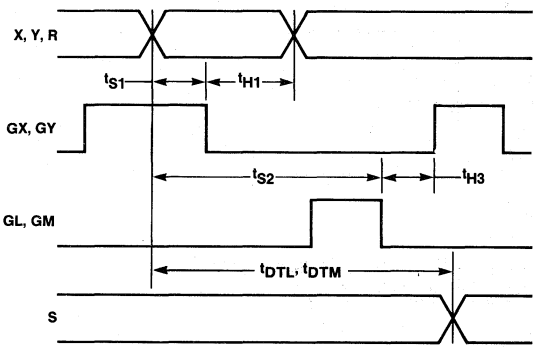


Figure 4c

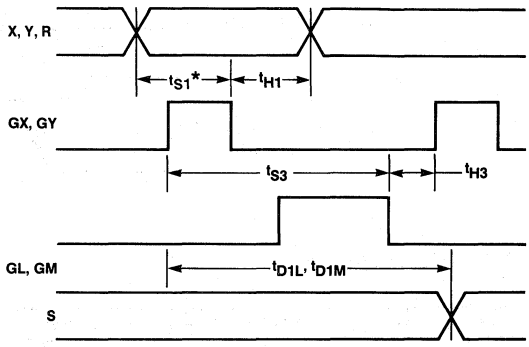


Figure 4d

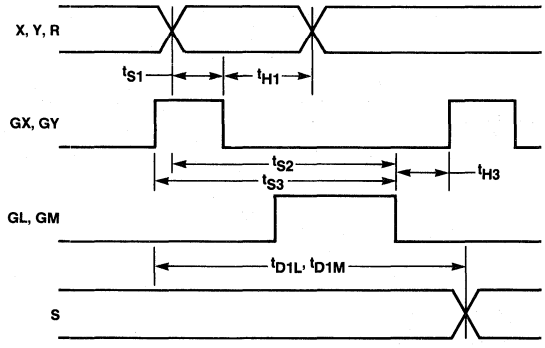


Figure 4e

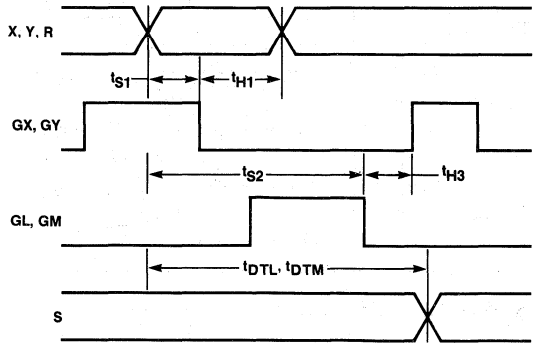


Figure 4f

* With this particular timing setup time t_{S1} will be automatically met.

The gated multiply represents the pipelined input and output operation. The latch enable lines GX, GY, GL, GM are used to store incoming operands and outgoing results. The particular set-up times that must be met and the time the result takes to reach the outputs depends on two timing relationships. The first is when the rising edges of GX and GY occur with respect to the operand inputs changing, and the second is when the rising edges of GL and GM occur with respect to the rising edges of GX and GY. On the above timing diagrams, denote the absolute time that the operand inputs change as T_{XYR}, the absolute time that the rising edges of GX and GY occur as T_{GXY}, and the absolute time that the rising edges of GL and GM occur as T_{GLM}. Thus, the two delays of concern can be explicitly stated as (T_{GXY} - T_{XYR}) and (T_{GLM} - T_{GXY}). Notice that either of these quantities can be positive or negative depending on which event occurs first. Timing for gated multiplies can then be summarized in the following table:

11

$T_{GXY} - T_{XYR}$	$T_{GLM} - T_{GXY}$	FIGURE	WHICH SET-UP TIMES MUST BE MET	WHEN RESULT IS PRESENT AT OUTPUTS
$T_{GXY} - T_{XYR} \geq 0$	$T_{GLM}-T_{GXY} \geq t_{S3min}-t_{Wmin}$	4a	t_{S3}	$T_{GLM} + t_{D2}$
$0<T_{XYR}-T_{GXY} \leq t_{Wmin}-t_{S1min}$	$T_{GLM}-T_{GXY} \geq t_{S3min}-t_{Wmin}$	4b	t_{S1}, t_{S2}, t_{S3}	$T_{GLM} + t_{D2}$
$t_{Wmin} - t_{S1min} < T_{XYR} - T_{GXY}$	$T_{GLM}-T_{GXY} \geq t_{S3min}-t_{Wmin}$	4c	t_{S1}, t_{S2}	$T_{XYR} + (t_{DTL}, t_{DTM})^*$
$T_{GXY} - T_{XYR} \geq 0$	$T_{GLM}-T_{GXY} < t_{S3min}-t_{Wmin}$	4d	t_{S3}	$T_{GXY} + (t_{D1L}, t_{D1M})^*$
$0<T_{XYR}-T_{GXY} \leq t_{Wmin}-t_{S1min}$	$T_{GLM}-T_{GXY} < t_{S3min}-t_{Wmin}$	4e	t_{S1}, t_{S2}, t_{S3}	$T_{GXY} + (t_{D1L}, t_{D1M})^*$
$t_{Wmin} - t_{S1min} < T_{XYR} - T_{GXY}$	$T_{GLM}-T_{GXY} < t_{S3min}-t_{Wmin}$	4f	t_{S1}, t_{S2}	$T_{XYR} + (t_{DTL}, t_{DTM})^*$

* For the least and most significant halves of the product respectively.

NOTE: T_{XYR} represents the absolute time when the operand inputs change.
T_{GXY} and T_{GLM} represent the absolute times when the rising edges of the latch controls occur.

Three-State Timing

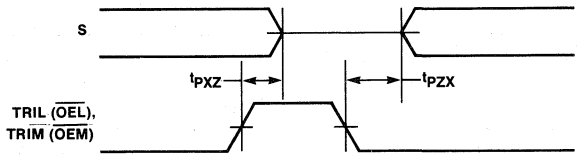


Figure 5

Test Waveforms

TEST	V_X		OUTPUT WAVEFORM — MEAS. LEVEL
All t_{PD}	5.0V		V_{OH}, V_{OL}, 1.5V
t_{PXZ}	t_{PHZ}	0	V_{OH}, 0.5V, 2.8V
	t_{PLZ}	5	V_{OL}, 0.5V, 0.0V
t_{PZX}	t_{PZH}	0	2.8V, V_{OH}, 1.5V
	t_{PZL}	5	0.0V, V_{OL}, 1.5V

Latch Enable Pulse Width (GL, GM, GX, GY)

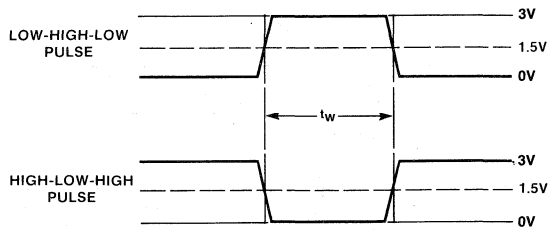


Figure 6

Load Test Circuit

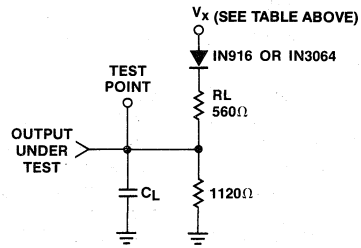


Figure 7

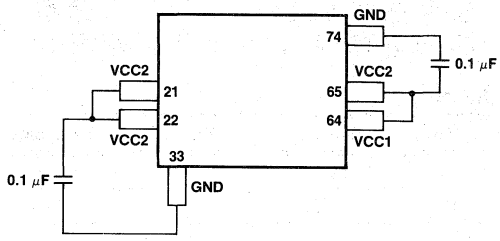
Recommended Bypass Capacitors

The switching currents when the outputs change can be fairly high, and bypass capacitors are recommended to adequately decouple the VCC and GND connections.

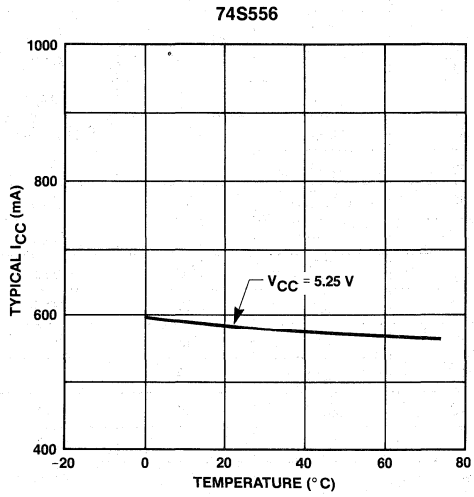
For example, on the 84-terminal LCC package, pins 21 and 22 are VCC2 supplies and should be decoupled with pin 33, a GND input, using a 0.1 μf monolithic ceramic disk capacitor. The capacitor must have good high-frequency characteristics. Also pins 64 and 65, VCC1 and VCC2, should be decoupled with pin 74, a GND input, with a similar capacitor arrangement.

For the 88-pin-grid-array package pins 21 and 22 are VCC2 supplies and should be decoupled with pin 35, the GND pin. Pins 66 and 67, VCC1 and VCC2, should be decoupled with pin 77, the GND pin.

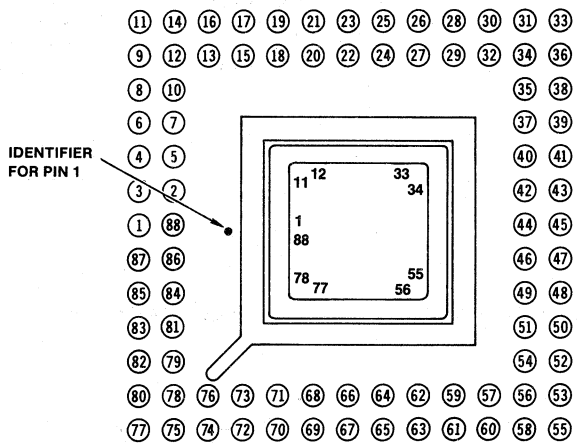
Decoupling Capacitors Shown with the 84-Terminal LCC Package



Typical Supply Current Over Temperature Range



88 Pin-Grid-Array
Pin Locations
Bottom View



Pin-Guide For Pin Grid Array

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	X9	23	N/C*	45	S25	67	VCC2†
2	X10	24	Y8	46	S24	68	N/C*
3	X11	25	Y9	47	S23	69	S7
4	X12	26	Y10	48	S22	70	S6
5	X13	27	Y11	49	S21	71	S5
6	X14	28	Y12	50	S20	72	S4
7	X15	29	Y13	51	S19	73	S3
8	XM	30	Y14	52	S18	74	S2
9	GX	31	Y15	53	S17	75	S1
10	RS	32	YM	54	S16	76	S0
11	RU	33	GY	55	GND	77	GND
12	GND	34	N/C*	56	TRIL ($\overline{\text{OEL}}$)	78	N/C*
13	Y0	35	GND	57	GL	79	GND
14	Y1	36	TRIM ($\overline{\text{OEM}}$)	58	S15	80	X0
15	Y2	37	GM	59	S14	81	X1
16	Y3	38	$\overline{\text{S31}}$	60	S13	82	X2
17	Y4	39	S31	61	S12	83	X3
18	Y5	40	S30	62	S11	84	X4
19	Y6	41	S29	63	S10	85	X5
20	Y7	42	S28	64	S9	86	X6
21	VCC2†	43	S27	65	S8	87	X7
22	VCC2†	44	S26	66	VCC1††	88	X8

* Not connected. † VCC2 = Logic VCC. †† VCC1 = Output buffer VCC.

Rounding

Multiplication of two n-bit operands results in a 2n-bit product†. Therefore, in a pure n-bit system it is necessary to convert the double-length product into a single-length product. This can be accomplished by truncating or rounding. The following examples illustrate the difference between the two conversion techniques in decimal arithmetic:

39.2 → 39
39.6 → 39
Truncating

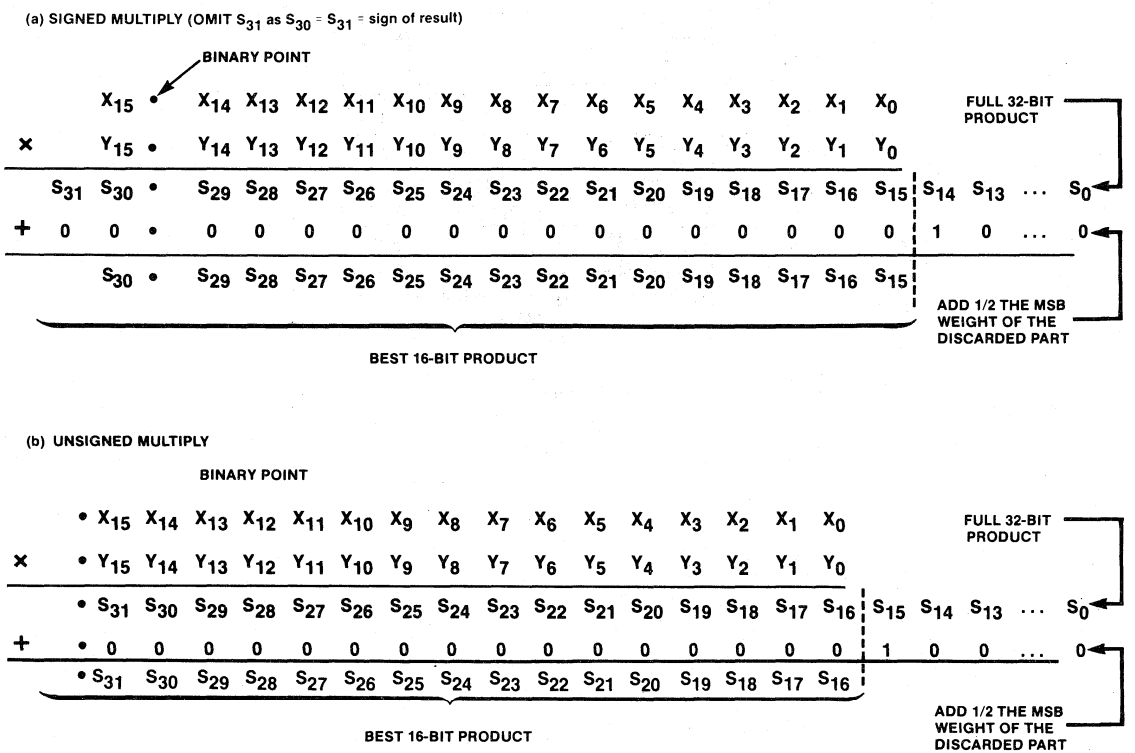
39.2 + 0.5 = 39.7 → 39
39.6 + 0.5 = 40.1 → 40
Rounding

Obviously, rounding maintains more precision than truncating, but it may take one more step to implement. The additional step involves adding one-half of the weight of the single-length LSB to the MSB of the discarded part; e.g., in decimal arithmetic rounding 39.28 to one decimal point is accomplished by adding 0.05 to the number and truncating the LSB:

39.28 + 0.05 = 39.33 → 39.3

The situation in binary arithmetic is quite similar, but two cases need to be considered; signed and unsigned data representation. In signed multiplication, the two MSBs of the result are identical, except when both operands are −1; therefore, the best single-length product is shifted one position to the right with respect to the unsigned multiplications. Figure 8 illustrates these two cases for the 16x16 multiplier. In the signed case, adding one-half of the S_{15} weight is accomplished by adding 1 in bit position 14, and in the unsigned case by adding 1 in bit position 15. Therefore, the 'S556 multiplier has two rounding inputs. RS and RU. Thus, to get a rounded single-length result, the appropriate R input is tied to V_{CC} (logic High) and the other R input is grounded. If a double-length result is desired, both R inputs are grounded.

†In general multiplication of an M-bit operand by an N-bit operand results in an (M + N)-bit product.



NOTES:

(a) In signed (twos-complement) notation, the MSB of each operand is the sign bit, and the binary point is to the right of the MSB. The resulting product has a redundant sign bit and the binary point is to the right of the second MSB of the product. The best 16-bit product is from S_{30} through S_{15}, and rounding is performed by adding "1" to bit position S_{14}.

(b) In unsigned notation the best 16-bit product is the most significant half of the product and is corrected by adding "1" to bit position S_{15}.

Figure 8. Rounding the Result of Binary Fractional Multiplication

Using the 'S556 in a Pipelined Positive-Edge Triggered Clock System

The 'S556 has internal latches which can be used affectively in systems where things happen on positive-going clock edges. This application is an extension of the gated multiply mode shown in Figure 1, in which a 32-bit product can be latched every t_{S3} nsec in the 'S556.

If the signals GX, GY, GM and GL can be derived from the system clock then the latches can almost have the same effect as having a register. The basic philosophy behind the recommended timing is that the input latches are closed when the output latches are open; the outputs are then closed (and have latched results) and new data is presented to the input latches, which are opened. This is shown by the relation between GX, GY and GL, GM in Figure 9. The set-up time t_{S3} is shown as one value but strictly speaking, it is split as t_{S3L} and t_{S3M} for the least significant and most significant half of the product respectively. The value of t_{S3L} is less than t_{S3M}, for applications requiring the least significant bits of the result as fast as possible.

One note of caution is that a design must always meet the set-up and hold times for X_i, R_i with respect to GX and for Y_i with respect to GY.

The result S_i is available t_{D2} after the rising edge of GM and GL.

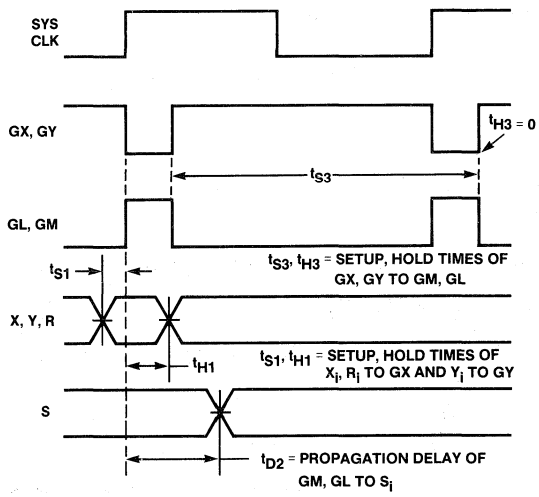


Figure 9

Totally Parallel 32x32 Multiplier

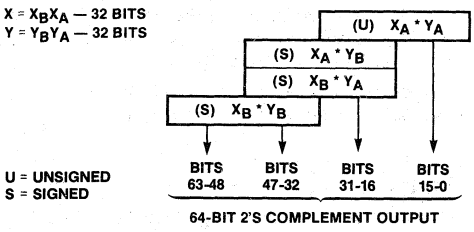
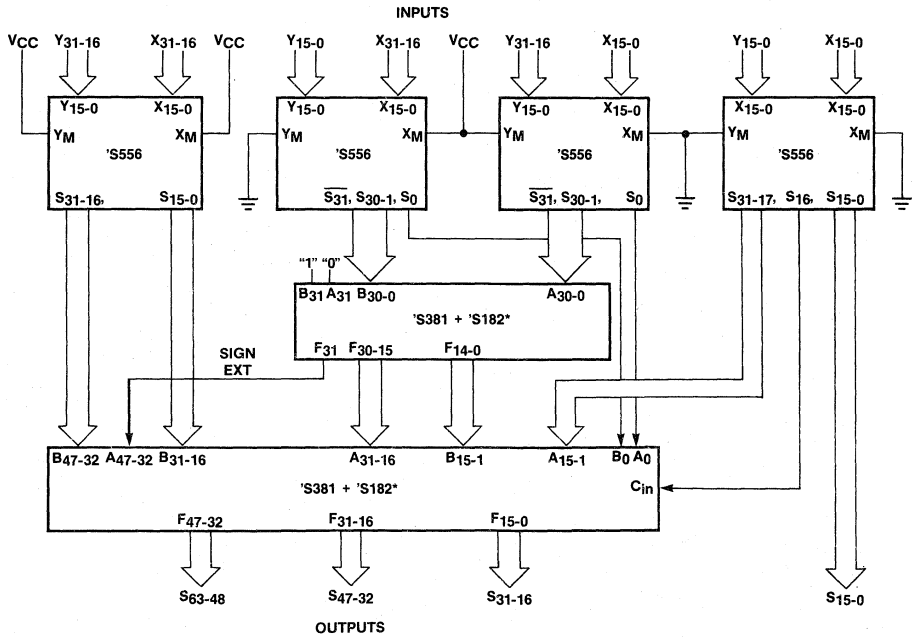


Figure 10. Partial Products for a 32x32 Multiplication

A twos-complement 32x32 multiplication can be performed within 220 nsec using 4 'S556s, 20 'S381s, and 7 'S182s. This 32x32 multiply operation involves adding up four partial products as shown in Figure 10. These four partial products are generated in four multipliers; the outputs are XA*YA, XA*YB, XB*YA, XB*YB, where X31-16 = XB, X15-0 = XA, Y31-16 = YB, Y15-0 = YA.

The implementation of this twos-complement 32x32 multiplier is shown in Figure 11. The outputs of the 16x16 multipliers are connected to two levels of adders to give a 64-bit product. The first level of adders is needed to add the two central partial products of Figure 10, XA*YB and XB*YA. Notice the technique which is used to generate the "sign extension", or the most-significant sum bit of the first level of adders. The 'S556 provides, as a direct output, the complement of the most-significant product bit; having this signal immediately speeds up the sign-extension computation, and reduces the external parts count.



* THESE ARE ADDER BLOCKS USING THE 'S381, A 4-BIT ALU FUNCTION GENERATOR, TO PERFORM A HIGH SPEED ADD OPERATION. THE 'S182 IS A LOOK-AHEAD CARRY GENERATOR WHICH REDUCES THE PROPAGATION DELAY. ALL THE ABOVE PARTS ARE AVAILABLE FROM MONOLITHIC MEMORIES INCORPORATED.

TOTAL MULTIPLY TIME = MULTIPLIER DELAY + ADDER LEVEL 1 DELAY + ADDER LEVEL 2 DELAY = 90 + 65 + 65 = 220 nsec

Figure 11. Implementation of the 32x32 Multiplier

For example, the inputs to the adder in the most significant position are the $\overline{S31}$ outputs from the two central multipliers. The sign extension of the addition of XA*YB and XB*YA is defined as

SIGN EXT = $\overline{\overline{A}.\overline{B}. + \overline{A}.C. + \overline{B}.C.}$, where

A is the most-significant bit of the term XA*YB;
B is the most-significant bit of the term XB*YA; and
C is the carry-in to the most-significant bits of XA*YB and XB*YA, in the adder.

The sign extension can be computed as the negation of the carry-out term of three terms, $\overline{A}$, $\overline{B}$, and C. This term corresponds to the negative of the carry-out of the bit position just one place to the right of the most-significant bit position of the first level of adders. The negative of the carry-out can be generated by presenting a carry-out and a binary "one" to the most significant bit of the adder. The generated sum bit then corresponds to the negation of the carry-out of the previous stage, which is the sign extension required to be added to the 16 most-significant bits of the XB*YB partial product term.

The second level of adders, which performs a 48-bit add function, is fairly straightforward. These adders can be implemented using 'S381 four-bit ALUs and 'S182 carry-bypasses ("carry-lookahead generators") which are available from Monolithic Memories Inc. and from other vendors.

Other configurations such as 48x48 and 64x64 multipliers can be designed using the same methodology, r1.

References

1. "Fast 64x64 Multiplication using 16x16 Flow-through Multiplier and Wallace Trees," Marvin Fox, Chuck Hastings and Suneel Rajpal, *Monolithic Memories System Design Handbook,* pages 8-53 to 8-61.

8x8 High Speed Schottky Multipliers

SN74S557
SN54/74S558

Features/Benefits

- **Industry-standard 8x8 multiplier**
- **Multiplies two 8-bit numbers; gives 16-bit result**
- **Cascadable; 56x56 fully-parallel multiplication uses only 34 multipliers for the most-significant half of the product**
- **Full 8x8 multiply in 60ns worst case**
- **Three-state outputs for bus operation**
- **Transparent 16-bit latch in 'S557**
- **Plug-in compatible with original Monolithic Memories' 67558**

Description

The 'S557/'S558 is a high-speed 8x8 combinatorial multiplier which can multiply two eight-bit unsigned or signed twos-complement numbers and generate the sixteen-bit unsigned or signed product. Each input operand X and Y has an associated Mode control line, X_M and Y_M respectively. When a Mode control line is at a Low logic level, the operand is treated as an unsigned eight-bit number; whereas, if the Mode control is at a High logic level, the operand is treated as an eight-bit signed twos-complement number. Additional inputs, R_S and R_U, (R, in the 'S557) allow the addition of a bit into the multiplier array at the appropriate bit positions for rounding signed or unsigned fractional numbers.

The 'S557 internally develops proper rounding for either signed or unsigned numbers by combining the rounding input R with X_M, Y_M, $\overline{X_M}$, and $\overline{Y_M}$ as follows:

$R_U = \overline{X_M} \cdot \overline{Y_M} \cdot R$ = Unsigned rounding input to 2^7 adder.

$R_S = (X_M + Y_M)\, R$ = Signed rounding input to 2^6 adder.

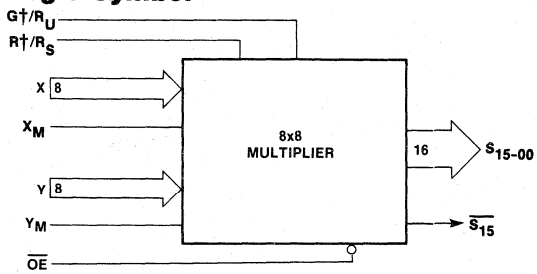
Since the 'S558 has no latches, it does not require the use of pin 11 for the latch enable input G, so R_S and R_U are brought out separately.

The most-significant product bit is available in both true and complemented form to assist in expansion to larger signed multipliers. The product outputs are three-state, controlled by an assertive-low Output Enable which allows several multipliers to be connected to a parallel bus or be used in a pipelined system. The device uses a single +5V power supply and is packaged in a standard 40-pin DIP.

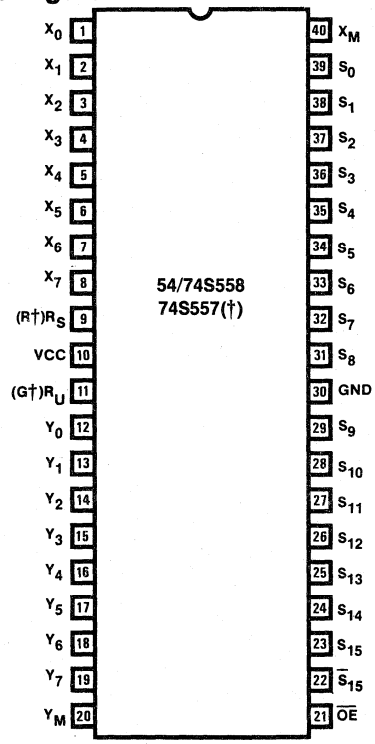
Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
54S558	J, (44), (L)	Military
74S557, 74S558	N,J,	Commercial

Logic Symbol



Pin Configuration



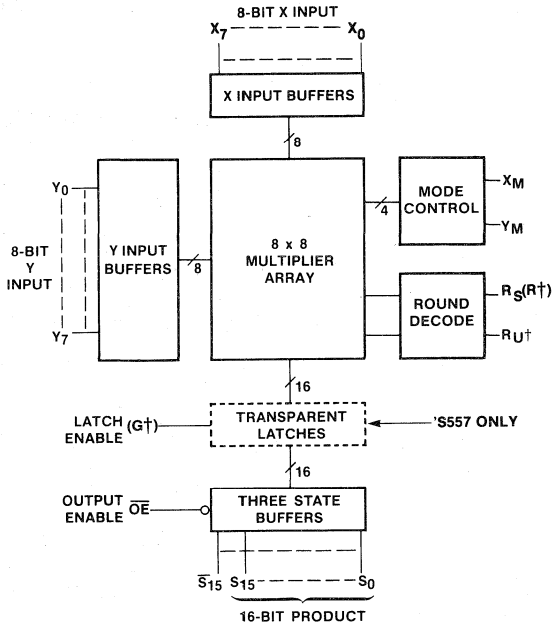
†For 74S557 Pin 9 is R and Pin 11 is G.

11

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Monolithic Memories

Logic Diagram



†For 74S557 Pin 9 is R and Pin 11 is G.

Absolute Maximum Ratings

Supply voltage V_{CC} ..... 7.0 V
Input voltage ..... 7.0 V
Off-state output voltage ..... 5.5 V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	DEVICE	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNITS
V_{CC}	Supply voltage	all	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	all	−55		125*	0		75	°C
t_{su}	X_i, Y_i to G set	'S557				40			ns
t_h	X_i, Y_i to G hold time	'S557				0			ns
t_w	Latch enable pulse width	'S557				15			ns

* Case temperature

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.5V			−1	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4V			100	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = −2mA	2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.5V			−100	μA
I_{OZH}			V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current*	V_{CC} = MAX	V_O = 0V	−20		−90	mA
I_{CC}	Supply current	V_{CC} = MAX			200	280	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typicals at 5.0V V_{CC} and 25°C T_A.

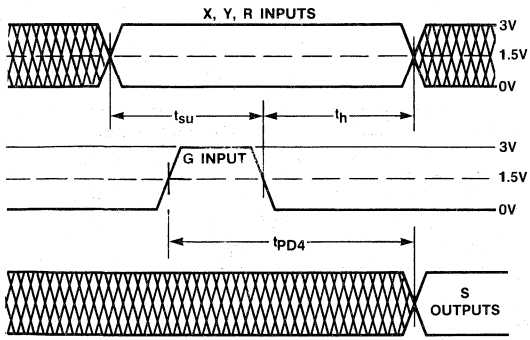
Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	DEVICE	TEST CONDITIONS	MILITARY MIN	MILITARY TYP†	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP†	COMMERCIAL MAX	UNIT
t_{PD1}	X_i, Y_i to S_{7-0}	All	C_L = 30pF, R_L = 560Ω, see test figures		40	60		40	50	ns
t_{PD2}	X_i, Y_i to S_{15-8}	All			45	70		45	60	ns
t_{PD3}	X_i, Y_i to $\overline{S}_{15}$	All			50	75		50	65	ns
t_{PD4}	G to S_i	'S557			20	40		20	35	ns
t_{PXZ}	$\overline{OE}$ to S_i	All			20	40		20	30	ns
t_{PZX}	$\overline{OE}$ to S_i	All			15	40		15	30	ns

11

Timing Waveforms

Setup and Hold Times ('S557)

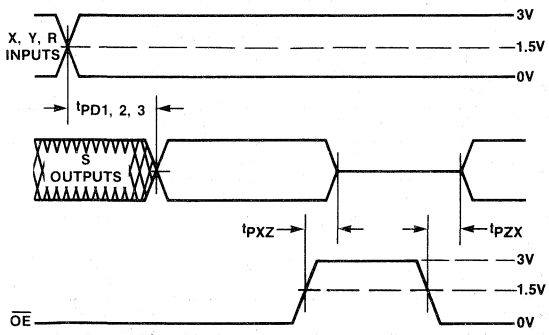


NOTE: If the rising edge of G occurs *before* ($t_{SU_{MIN}}$-$t_{W_{MIN}}$) from the inputs changing, then the applicable propagation delays are t_{PD}, t_{PD2} and t_{PD3}, (and not t_{PD4}). In this case the time at which the results arrive at the outputs depends on when the inputs change instead of when the rising edge of G occurs.

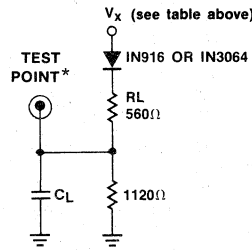
Test Waveforms

TEST	V_X		OUTPUT WAVEFORM — MEAS. LEVEL
All t_{PD}	5.0V		V_{OH}, V_{OL}, 1.5V
t_{PXZ}	for t_{PHZ}	for t_{PLZ}	V_{OH}, 0.5V, 0.5V, V_{OL}, 2.8V, 0.0V
	0.0V	5.0V	
t_{PZX}	for t_{PZH}	for t_{PZL}	2.8V, 0.0V, 1.5V, V_{OH}, V_{OL}
	0.0V	5.0V	

Propagation Delay

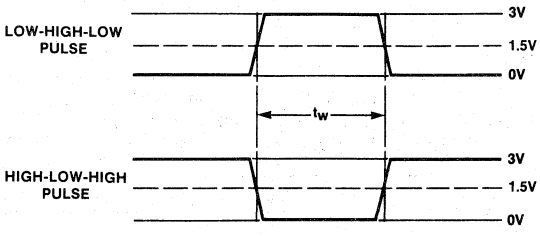


Test Load



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Latch-Enable Pulse Width ('S557)



Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

SUMMARY OF SIGNALS/PINS	
X_7-X_0	Multiplicand 8-bit data inputs
Y_7-Y_0	Multiplier 8-bit data inputs
X_M, Y_M	Mode control inputs for each data word; LOW for unsigned data and HIGH for twos-complement data
S_{15}-S_0	Product 16-bit output
$\overline{S}_{15}$	Inverted MSB for expansion
R_S, R_U	Rounding inputs for signed and unsigned data, respectively ('S558 only)
G	Transparent latch enable ('S557 only)
$\overline{OE}$	Three-state enable for S_{15}-S_0 and $\overline{S}_{15}$ outputs
R	Rounding input for signed or unsigned data; combined internally with X_M, Y_M ('S557 only)

ROUNDING INPUTS
'S557

INPUTS			ADDS	
X_M	Y_M	R	2^7	2^6
L	L	H	YES	NO
L	H	H	NO	YES
H	L	H	NO	YES
H	H	H	NO	YES
X	X	L	NO	NO

'S558

INPUTS		ADDS		USUALLY USED WITH	
R_U	R_S	2^7	2^6	X_M	Y_M
L	L	NO	NO	X	X
L	H	NO	YES	H†	H†
H	L	YES	NO	L	L
H	H	YES	YES	*	*

†In mixed mode, one of these could be Low but not both.
*Usually a nonsense operation. See applications section of data sheet.

74S557 FUNCTION TABLE

INPUTS		PRODUCT RESULT FROM ARRAY	LATCH CONTENTS (INTERNAL TO PART)	OUTPUTS	FUNCTION
$\overline{OE}$	G	T_i	Q_i	S_i	
L	L	X	L	L	Latched
L	L	X	H	H	
L	H	L	(L)*	L	Transparent
L	H	H	(H)*	H	
H	L	X	(L)	Z	Hi-Z; Latched Data not Changed
H	L	X	(H)	Z	
H	H	X	(X)*	Z	Hi-Z

*Identical with product result passing through latch.

MODE CONTROL INPUTS

OPERATING MODE	INPUT DATA		MODE CONTROL INPUTS	
	X_7-X_0	Y_7-Y_0	X_M	Y_M
Unsigned	Unsigned	Unsigned	L	L
Mixed	Unsigned	Twos-Comp.	L	H
	Twos-Comp.	Unsigned	H	L
Signed	Twos-Comp.	Twos-Comp.	H	H

11

Functional Description

The 'S557 and 'S558 multipliers are 8x8 full-adder Cray arrays capable of multiplying numbers in unsigned, signed, twos-complement, or mixed notation. Each 8-bit input operand X and Y has associated with it a mode control which determines whether the array treats this number as signed or unsigned. If the mode control is at High logic level, then the operand is treated as a twos-complement number with the most-significant bit having a negative weight; whereas, if the mode control is at a Low logic level, then the operand is treated as an unsigned number.

The multiplier provides all 16 product bits generated by the multiplication. For expansion during signed or mixed multiplication the most-significant product bit is available in both true and complemented form. This allows an adder to be used as a subtractor in many applications and eliminates the need for certain SSI circuits.

Two additional inputs to the array, R_S and R_U, allow the addition of a bit at the appropriate bit position so as to provide rounding to the best signed or unsigned fractional eight-bit result. These inputs can also be used for rounding in larger multipliers. In the 'S557, these two inputs are generated internally from the mode controls and a single R input.

The product outputs of the multiplier are controlled by an assertive-low Output Enable control. When this control is at a Low logic level the multiplier outputs are active, while if the control is at a High logic level then the outputs are placed in a high-impedance state. This three-state capability allows several multipliers to drive a common bus, and also allows pipelining of multiplication for higher-speed systems.

Rounding

Multiplication of two n-bit operands results in a 2n-bit product†. Therefore, in an n-bit system it is necessary to convert the double-length product into a single-length product. This can be accomplished by truncating or rounding. The following examples illustrate the difference between the two conversion techniques in decimal arithmetic:

$$\left.\begin{array}{l} 39.2 \rightarrow 39 \\ 39.6 \rightarrow 39 \end{array}\right\} \text{ Truncating}$$

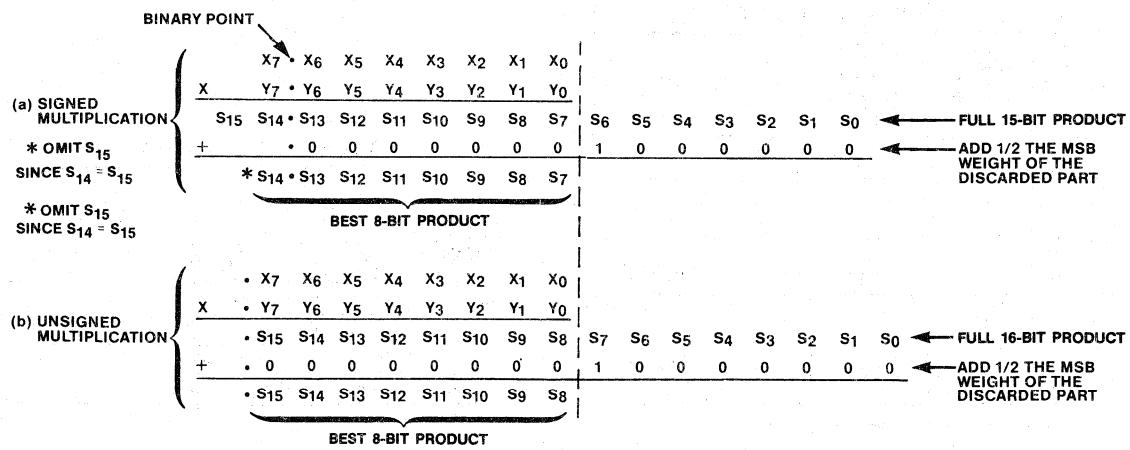
$$\left.\begin{array}{l} 39.2 + 0.5 = 39.7 \rightarrow 39 \\ 39.6 + 0.5 = 40.1 \rightarrow 40 \end{array}\right\} \text{ Rounding}$$

Obviously, rounding maintains more precision than truncating, but it may take one more step to implement. The additional step involves adding one-half of the weight of the single-length LSB to the MSB of the discarded part; e.g., in decimal arithmetic rounding 39.28 to one decimal point is accomplished by adding 0.05 to the number and truncating the LSB:

$$39.28 + 0.05 = 39.33 \rightarrow 39.3$$

The situation in binary arithmetic is quite similar, but two cases need to be considered: signed and unsigned data representation. In signed multiplication, the two MSBs of the result are identical, except when both operands are −1; therefore, the best single-length product is shifted one position to the right with respect to the unsigned multiplications. Figure 1 illustrates these two cases for the 8x8 multiplier. In the signed case, adding one-half of the S_7 weight is accomplished by adding 1 in bit position 6, and in the unsigned case 1 is added to bit position 7. Therefore, the 'S558 multiplier has two rounding inputs, R_S and R_U. Thus, to get a rounded single-length result, the appropriate R input is tied to V_{CC} (logic High) and the other R input is grounded. If a double-length result is desired, both R inputs are grounded for the 'S558, and the single R input is grounded for the 'S557.

†In general: multiplication of an M-bit operand by an N-bit operand results in an (M + N)-bit product.



NOTES:

(a) In signed (twos-complement) notation, the MSB of each operand is the sign bit, and the binary point is to the right of the MSB. The resulting product has a redundant sign bit and the binary point is to the right of the second MSB of the product. The best eight-bit product is from S_{14} through S_7, and rounding is performed by adding "1" to bit position S_6.

(b) In unsigned notation the best 8-bit product is the most significant half of the product and is corrected by adding "1" to bit position S_7.

Figure 1. Rounding the Result of Binary Fractional Multiplication

Signed Expansion

The most-significant product bit has both true and complement outputs available. When building larger signed multipliers, the partial products (except at the lower stages) are signed numbers. These unsigned and signed partial products must be added together to give the correct signed product. Having both the true and complemented form of the most-significant product bit available assists in this addition. For example, say that two signed partial products must be added and MSI adders are used; we then have the situation of adding together the carry from the previous adder stage plus the addition of the two negative most-significant partial-product bits. The result of adding these variables must be a positive sum and a negative carry (borrow). The equations for this are:

$S = A \oplus B \oplus C$

$C_{OUT} = AB + BC + CA$

where C is the carry-in and A and B are the sign bits of the two partial products.

Now an adder produces the equations:

$S = A \oplus B \oplus C$

$C_{OUT} = AB + BC + CA$

Examining these equations, it can be seen that, if the inversions of A and B are used, then the most significant sum bit of the adder is the sign extension bit.

Sign ext $= AB + B\overline{C} + \overline{C}A = \overline{\overline{A}\overline{B} + \overline{B}\overline{C} + \overline{C}\overline{A}}$,

and the sum remains the same.

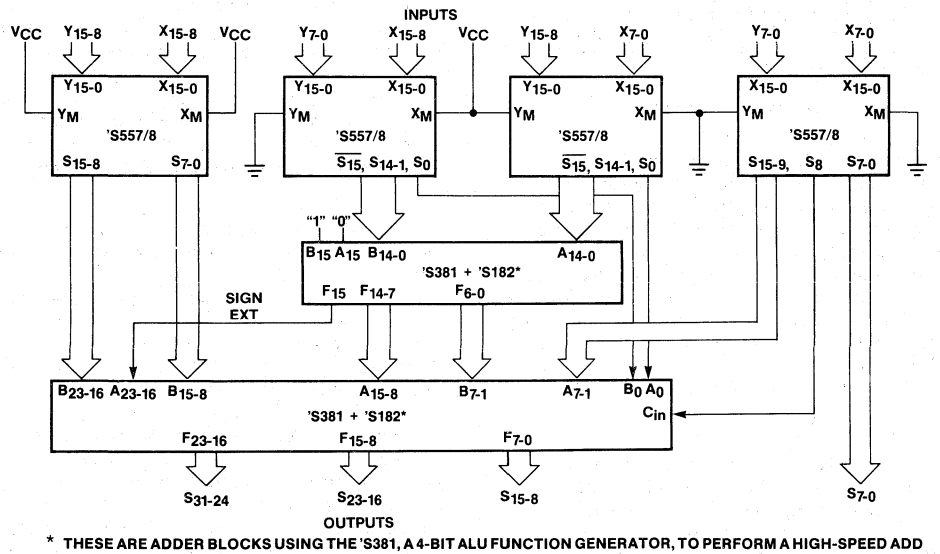
16x16 Twos-Complement Multiplication

The 16-bit X operand is broken into two 8-bit operands (X_7-X_0 and X_{15}-X_8), as is the Y operand. Since the situation is that of a cross-product, four partial products are generated as follows:

$$A = X_L * Y_L$$
$$B = X_L * Y_H$$
$$C = X_H * Y_L$$
$$D = X_H * Y_H$$

where the subscript L stands for bits 7-0, ("low or least-significant half), and the subscript H stands for bits 15-8.

Expanded twos-complement multiplication requires a sign extension of the B and C partial products. Thus, B_{15} and C_{15} need to be extended eight positions to the left (to align with D_{15}). In this approach two more adders are required. But the complement of the MSB ($\overline{S}_{15}$) on the 'S557/8 can be used to save these two adders. Figure 2 shows the implementation of 16x16 signed twos-complement multiplication in this manner.



* THESE ARE ADDER BLOCKS USING THE 'S381, A 4-BIT ALU FUNCTION GENERATOR, TO PERFORM A HIGH-SPEED ADD OPERATION. THE 'S182 IS A LOOKAHEAD CARRY GENERATOR AND REDUCES THE PROPAGATION DELAY. ALL OF THE ABOVE PARTS ARE AVAILABLE FROM MONOLITHIC MEMORIES INCORPORATED.

TOTAL MULTIPLY TIME = MULTIPLIER DELAY + ADDER LEVEL 1 DELAY + ADDER LEVEL 2 DELAY = 60+44+64 = 168 nsec

Figure 2. 16x16 Twos-Complement Signed Multiplication

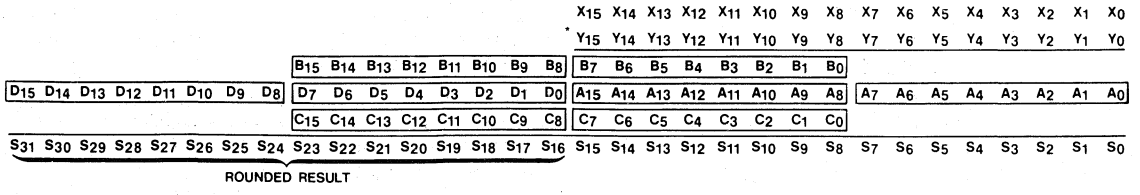


Figure 3. Unsigned Expansions of the 8x8 Multiplier to 16x16 Multiplication

Applications:
How to Design Superspeed Cray Multipliers with '558s

by Chuck Hastings

Multiplication, as most of us think of it, is performed by repeated addition and shifting. When we multiply using pencil and paper, according to the familiar elementary-school method, we first write down the multiplicand, and then write down the multiplier immediately under it and underline the multiplier. Then we take the least-significant digit of the multiplier, multiply that digit by the entire multiplicand, and record the answer in the top row of our workspace, underneath the line. Then we repeat, using now the second-least-significant multiplier digit, and record that answer below the first one, pushed one digit position (that is, "shifted") to the left. This process continues until we run out of multiplier digits (or out of patience), at which point we add up the constants of the whole diamond-shaped workspace and record at the bottom an answer which consists of either m + n - 1 digits or m + n digits, where there are m digits in the multiplier and n digits in the multiplicand. An example, voila':

```
  125  (multiplicand)
 x107  (multiplier)
-------------------------------------------
  875  (7 x 125)
  000  (0 x 125, shifted left one digit position)
  125  (1 x 125, shifted left two digit positions)
-------------------------------------------
13375  (sum of the above)
```

Figure 4. Decimal Multiplication

The decimal number system has no monopoly on truth — our ancestors simply happened to have ten fingers at the time when someone came up with the idea of counting. Binary numbers, as you know, are more copacetic than are decimal numbers with digital-logic elements, which like to settle comfortably into one voltage state ("High) or another ("Low"), rather than into one of ten different states. So we can repeat the above example using binary numbers, right? First, we convert our multiplicand and multiplier to binary:

$$125_{10} = 01111101_2$$
$$107_{10} = 01101011_2$$

The subscripts 10 and 2 refer to the "base" or "radix" of the number system, 10 for decimal and 2 for binary. (Remember your New Math?) For sneaky reasons to be revealed soon, I've used 8-bit binary numbers, which is one bit more than necessary for my example, and added a leading zero. So, we multiply:

```
  01111101₂ = 125₁₀
x 01101011₂ = 107₁₀
----------
  01111101
 01111101
00000000
 01111101
00000000
 01111101
 01111101
00000000
----------------
0011010000111111 = 13375₁₀
```

Figure 5. Binary Multiplication

I've left off the remarks this time, but they're just like the remarks in the decimal example, at least in principle. Just in case you doubt this answer, I'll convert it back:

```
1     1
1     2
1     4
1     8
1    16
1    32
0     0      (   64)
0     0      (  128)
0     0      (  256)
0     0      (  512)
1  1024
0     0      ( 2048)
1  4096
1  8192
0     0      (16384)
0     0      (32768)
---------
   13375
```

Figure 6. Binary-to-Decimal Conversion

Now look carefully at the diamond-shaped array of numbers in the workspace in Figure 5. Each row is either the multiplicand 01111101, or else all zeroes. The 01111101 rows correspond to "1" digits in the multiplier, and the all-zero rows to "0" digits in the multiplier. Life does get simpler in some ways when we switch to binary numbers: "multiplying a multiplier digit by the multiplicand" now means just gating a copy of the multiplicand into that position if the digit is "1," and not doing so if the digit is "0."

Seymour Cray, the master computer designer from Chippewa Falls, Wisconsin, whose career has spanned three companies (Univac, Control Data, and now Cray Research) and many inventions, first observed some time in the late 1950s that *computers* also could actually multiply this way, if one merely provided enough components. This last qualifying remark; in those days when even transistors, let alone integrated circuits, in computers were still a novelty was by no means a trivial one! To prove his point (and satisfy a government contract), Cray designed, and Control Data built, a 48x48 multiplier which operated in one microsecond, about 1960. This multiplier was part of a special-purpose array processor for a classified application, and was so big that a CDC 1604 (then considered a large-scale processor) served as its input/output controller. In principle, such a multiplier at that time would have had to consist of 48 48-bit full adders or "mills," each of which received one input 48-bit number from the outputs of the mill immediately above it in the array, and the other 48-bit number from a gate which either allowed the multiplicand to pass through, or else supplied an all-zero 48-bit number. Actually, these mills have to be somewhat *longer* than 48 bits. Anyway, that is at least 2304 full adders, and in 1960 a full-adder circuit normally occupied one small plug-in circuit card.

A later version of this multiplier, in the CDC 7600 super-computer, could produce one 48x48 product out every 275 nanoseconds on a pipelined basis. The pipelining was asynchronous, and the entire humungous array of adders and gating logic could have up to three different products rippling down it at a given instant!

Back to the 1980s. Monolithic Memories has for several years produced an 8x8 Cray multiplier, the 67588, as a single 600-mil 40-pin DIP. After we invented this part, AMD second-sourced it, and by now it has become an industry standard. We now also have faster pin-compatible parts, the 54/74S558 and 74S557. Like other West Coast companies 2,000 miles from Wisconsin and Minnesota where Seymour Cray does his inventing, Monolithic Memories previously used the term "combinatorial multiplier" instead of "Cray multiplier" for this type of part. However, "combinatorial multiplier" has nine extra letters and five extra syllables, and also inadvertently implies that the technique involves combinatorial logic rather than arithmetic circuits. Some West Coast designs, including our 67588, use a modified internal array with only half as many full-adder circuits and slightly different interconnections, based on the two-bit "Booth-multiplication" algorithm (see reference 1), plus the two-bit "Wallace-tree" or "carry-save adder" technique (see references 2 and 3). Conceptually, however, the entire chip or system continues to operate as a Cray multiplier.

The '558, in particular can be thought of as a static logic network which fits exactly the binary multiplication example of Figure 5. (See now why I insisted on using 8-bit binary numbers?) There are no flipflops or latches whatever in the '558 — it is a "flow-through" device. Its 40 pins are used up as follows:

Use of Pins	Input, Output, or Voltage	Number of Pins
Multiplier	I	8
Multiplicand	I	8
Double-Length Product	O	16
Complement of Most-Significant Bit of Double-Length Product	O	1
3-State Output Enable	I	1
Number-Interpretation-Mode Control	I	2
Rounding Control for Product	I	2
Power and Ground	V	2
		40

Table 1. Use of Pins in the '558

The two number-interpretation-mode control pins, one for the multiplier and one for the multiplicand, allow the format for each of these two 8-bit input numbers to be chosen independently, as follows:

Control Input	Interpretation of 8-bit Input Number
L	8-bit unsigned
H	7-bit plus a sign bit

Table 2. Mode Control Input Encoding

The two rounding control pins allow either integer (right-justified) or fractional (left-justified) interpretation of the 14-bits-plus-sign double-length product of two 7-bits-plus-sign numbers for internal rounding of the double-length result to the most accurate 8-bit number. The control encoding is:

R_S Input	R_U Input	Effect
L	L	Disable Rounding
L	H	Round Unsigned
H	L	Round Signed
H	H	Nonsense (see below)

Table 3. Rounding Control Input Encoding

Rounding is normally disabled if the entire 16-bit double-length product output is to be used. If only an 8-bit subset of this product is to be used, this subset can be either bits 15-8 for unsigned rounding as shown in Figure 7, or bits 14-7 for signed rounding as shown in Figure 8. In either case, a "1" is forced into the '558's internal adder network at the bit position indicated by the arrow; adding a "1" into the bit position *below* the least-significant bit of the final answer has the effect of rounding, as you can see after a little thought. Obviously, forcing a "1" into *both* of these adder positions at the same time is a nonsense operation for most applications — it adds a "3" into the middle of the double-length result.

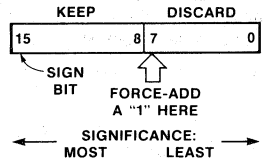


Figure 7. Unsigned Rounding

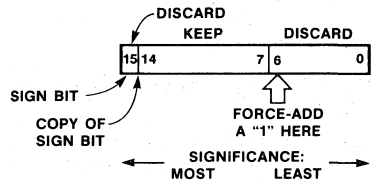


Figure 8. Signed Rounding

By now you probably have a fairly good idea of what a '558 is, and would like a few hints as to how to use it, right? First of all, there is an occasional application in things like video games for *very* fast multiplication, either 8x8 or 16x16, controlled by an 8-bit microprocessor, where there would be one '558 per system (see reference 4). More typically, however, the '558 is a building block, and several of them are used within one system; in fact, maybe more than several — "many." In the usual Silicon-Valley jargon, we can *cascade* a number of '558 (8x8) Cray-multiplier chips to create larger Cray multipliers at the systems level.

For the sake of concreteness, I'll discuss the case of 56x56 multipliers, which are appropriate in floating-point units which deal with "IBM-long-format" numbers which have a 56-bit mantissa. Any computer which emulates, or uses the same floating-point format as, any of the following computers can use such a multiplier:

IBM 360/370
Amdahl 470
Data General Eclipse
Gould/System Engineering SEL 32
Norsk Data 500 (different format)

There are two basic approaches: serial-parallel, and fully parallel. The serial-parallel approach uses seven '558s, and requires seven full multiply-and-add cycles. On the first cycle, the least-significant eight bits of the multiplier are multiplied by the entire multiplicand, and this partial product is saved. On the second cycle, the next-least significant eight bits of the multiplier are multiplied by the multiplicand, and that product (shifted eight bit positions to the left) is added into the first partial product to form the new partial product. And so forth, for five more cycles. It's almost like our decimal-multiplication example of Figure 1, except that instead of base-10 decimal digits we now have base-256 superdigits.

The fully-parallel approach totally applies Cray's usual design philosophy (sometimes characterized as "big, fast, and simple") at the systems level. It uses 49 '558s, in seven ranks; the 'i'th rank performs an operation corresponding to that done during the 'i'th cycle in the serial-parallel implementation. In principle, a complete mill is used to add the outputs of one rank of '558s to those of the rank above it. Or, alternatively, these mills can be laid out in a "tree" arrangement, such as:

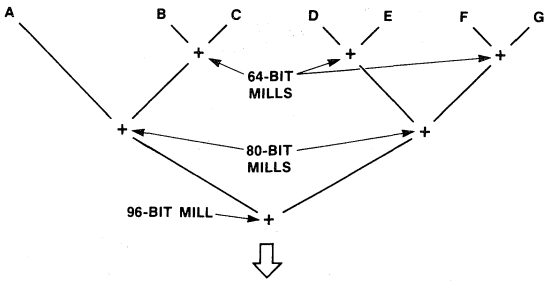


Figure 9. "Tree" Summing Arrangement of Mills for a 56x56 Cray Multiplier

Each letter stands for one rank of '558s, and each "+" stands for a mill of the indicated length. More involved "Wallace-tree" techniques are usually preferable. (See reference 3). If the least-significant half of the double-length product is *never* needed, only 34 'S558s are required. There is one subtlety which needs to be mentioned. If, conceptually, a '558 looks like a diamond —

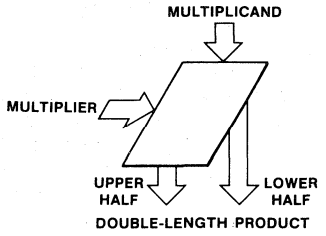


Figure 10. A Single '558 in "Diamond" Notation

then, the 8x56 multiplier for the serial-parallel configuration (which is also one rank of the fully-parallel configuration, which has seven such ranks) looks like this:

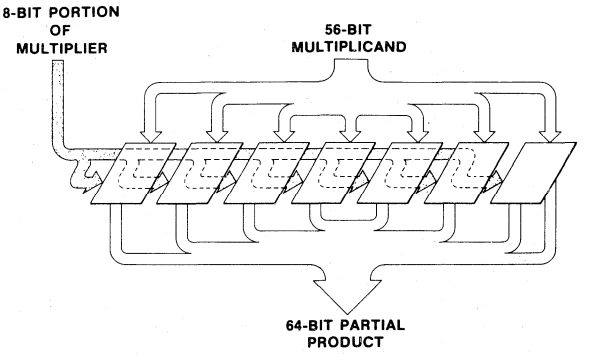


Figure 11. 8x56 Cray Multiplier in "Diamond" Notation

As you may discover after a moment's thought, *each* slanted double line in Figure 8 calls for addition of the outputs of *two* '558s — the eight most significant bits of one, and the eight least-significant bits of the next one to the left. There must also be an extra adder (or at least a "half adder") to propagate the carries from this addition all the way over to the left end of the result. The upshot is that an extra 56-bit mill is needed, in addition to the '558s. The eight least-significant bits of the least-significant '558 do not have to go through this mill, since they do not get added to anything else.

One final note: building up a large Cray-multiplier configuration out of '558s requires a *lot* of full adders, or else a lot of something else equivalent to them. Monolithic Memories also makes 74S381 (a 4-bit "ALU" or "*A*rithmetic *L*ogic *U*nit") and the 74S182 (a carry-bypass circuit which works well with the '381); and two faster ALUs, the 54/74F381 and the 54/74F382 are in design. These ALUs and bypasses are excellent building blocks from which to assemble the mills used for summation within a rank of '558s, and also the mills used for tree-summation of the outputs of all ranks. For how to put together one of these mills using '381s, '382s, and '182s, see reference 1. For how to use PROMs as Wallace trees, see reference 3.

Now you can go ahead, design your Cray multiplier out of '558s, and start multiplying full-length numbers together in a fraction of a microsecond. Sound like fun?

References

1. "Doing Your Own Thing in High-Speed Digital Arithmetic," Chuck Hastings, Monolithic Memories Conference Proceedings Reprint CP-102

2. "Real-Time Processing Gains Ground with Fast Digital Multiplier," Shlomo Waser and Allen Peterson, *Electronics,* September 29, 1977.

3. "Big, Fast and Simple — Algorithms, Architecture, and Components for High-End Superminis," Ehud "Udi" Gordon and Chuck Hastings, 1982 *Southcon Professional Program*, Orlando, Florida, March 23-25, 1982, paper no. 21/3.

4. "An 8x8 Multiplier and 8-bit μP Perform 16x16-bit Multiplication," Shai Mor, EDN, November 5, 1979, Monolithic Memories Article Reprint AR-109.

NOTE: All of these references are available as application notes from Monolithic Memories Inc.

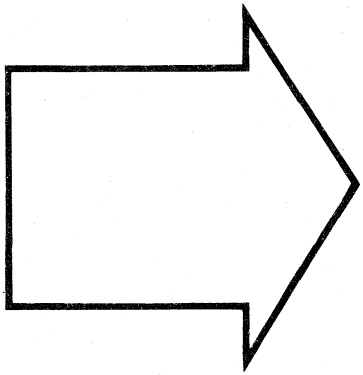


Table of Contents

INTERFACE

12

8-Bit Interface

MILITARY PART NUMBER	FUNCTION	POWER	POLARITY	FEATURE
SN54LS240	Buffer	LS	Invert	—
SN54LS241	Buffer	LS	Noninvert	—
SN54LS244	Buffer	LS	Noninvert	—
SN54S240	Buffer	S	Invert	—
SN54S241	Buffer	S	Noninvert	—
SN54S244	Buffer	S	Noninvert	—
SN54LS245	Buffer Transceiver	LS	Noninvert	—
SN54LS273	Register	LS	Noninvert	Master Reset
SN54LS373	Latch	LS	Noninvert	—
SN54S373	Latch	S	Noninvert	—
SN54LS374	Register	LS	Noninvert	—
SN54S374	Register	S	Noninvert	—

Pick the Right 8-Bit – or 16-Bit – Interface Part for the Job

Chuck Hastings and Bernard Brafman

Introduction

A few years ago, 20-pin 8-bit buffers, registers, latches, and transceivers came into existence as a rather haphazard upwards evolution from the MSI devices available in the mid-1970s. As time went on, usage of these parts increased until they became one of the fundamental computer-system building-block "primitives"—the "glue" which holds the entire system together. System designers demanded, and semiconductor manufacturers provided, many refinements such as inverting outputs to reduce parts count in assertive-low-bus systems, high-drive outputs to rescue designs with overloaded buses, Schmitt-trigger inputs to likewise rescue designs troubled with severe bus noise, high-voltage outputs specifically suited for driving MOS inputs, series-resistor outputs for driving highly-capacitive loads such as dynamic-MOS address buses, and so forth.

Today the demands are to reduce component costs and system board area. Reducing parts count achieves both of these objectives at one stroke. With the development of the 300-mil 24-pin SKINNYDIP™ package, it is now possible to effectively incorporate the equivalent of two 20-pin 8-bit interface parts into one 24-pin "16-bit interface" part. The approach is to look for common configurations of pairs of 8-bit parts, and implement the pair as a single chip. Common configurations include back-to-back "registered (or latched) transceivers," with the same options already available in the 20-pin 8-bit parts read back registers or latches, and pipelined registers or latches.

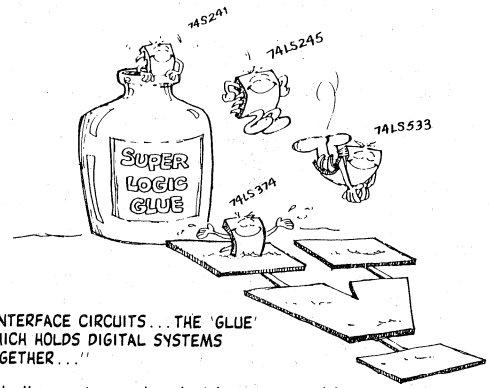
Interface Basics

Where Do Interface Circuits Fit In?

Interface circuits appear as unglamorous bread-and-butter commodity items, as compared to many of the other more complex integrated circuits of today: their sales volume is very high, their average selling price is comparatively low, and essentially interchangeable parts are offered by several suppliers. They have the humble role of being the "glue" which holds digital systems together; they are *means* rather than ends in themselves.

When preliminary system block diagrams turn into detailed schematics, the *blocks* turn into complex circuits—microprocessors, multipliers/dividers, automatic dynamic-MOSRAM refresh controllers, high-speed FIFOs, programmable-logic circuits, arithmetic-logic units, and so forth. But then, however, the *lines* between those blocks turn into interface circuits, which must be there in the final design but never explicitly get noticed during the conceptual-design stage!

The term "interface" is actually a bit of a misnomer, since it implies that these parts always occur at a boundary between two somewhat different types of logic. That may have been true once, and it is still true that many of the circuits commonly called "interface" have inputs and/or outputs which are different electrically from those of, say, triple three-input NAND gates produced using the identical solid-state-circuit technologies. But a general working definition of "interface circuits" also has to cover some other parts which get used



"INTERFACE CIRCUITS... THE 'GLUE' WHICH HOLDS DIGITAL SYSTEMS TOGETHER..."

in similar system roles, but have normal inputs and normal totem-pole or three-state outputs. One such definition, current today at Monolithic Memories, is

"... ultra-high performance integrated circuits which do not lend themselves to higher levels of integration, due either to their parallel data structure or to the electrical properties of their inputs and/or outputs."

Interface circuits get used wherever data must be held, transmitted on demand, power-amplified, level-shifted, read from a noisy bus, inverted, or otherwise operated upon in some simple electrical way. If more complex transformations of the data are called for, of a predominantly mathematical rather than electrical nature, the designer will typically try to perform the required operations with readymade LSI or MSI circuits. Even here, of course, interface circuits often have the inconspicuous but crucial role of performing format conversion so that several LSI circuits can communicate with each other. Still, they are viewed as "overhead," which system designers try to minimize and semiconductor producers often rank well below their top level of corporate priorities.

But interface circuits are here to stay, at least for several more years. And the realization is growing among both users and producers of semiconductors that, since interface parts are not about to vanish soon, they need to be treated as something more than afterthoughts to the design process. Users who select interface circuits shrewdly are achieving real gains in system performance and reliability, and significant reductions in system size, weight, and power consumption. Producers who do a conscientious and professional job of developing and marketing these humble parts are finding increased demand for their wares, even during recessions.

Two major trends currently evident in the world of interface circuits are:

- **The emergence of an orderly, matrix-like approach to interface products, so that taken all together they form an *array* rather than simply a splendid jumble of assorted types.**
- **A strong emphasis on increasing the number of data bits which can be handled or accomodated by a single interface-circuit package.**

12

This paper will discuss each of these trends in some detail, and will then go on to present some realistic interface applications based on several actual designs.

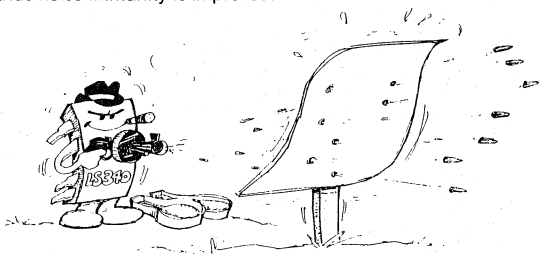
What Kinds of Interface Circuits Are There?

Commonly, the label "interface circuit" is applied to any of a diverse collection of miscellaneous devices which don't seem to fit into any other classification. As the term is used here, however, it means either one of three basic 8-bit types—buffers, latches, and registers—which are *simple* interface circuits, or else one of several 16-bit *compound* interface circuit types such as transceivers and pipelines.

Buffers merely "pass" or transmit information at increased power levels.Most contemporary buffer circuits, including 20-pin 8-bit buffers, also have an electronically-selectable electrical-isolation capability. Such a *three-state* buffer has a type of output which can be switched into a "hi-Z" (high-impedance) state in which it does not drive, nor appreciably load, the circuit node to which it is attached.

True or *noninverting* buffers pass the input information along with the same polarity (i.e., conventions in the representation of ones and zeroes by high and low voltages) that it had when it was received. *Inverting* buffers reverse the polarity of the input information from what was received, complementing all ones to zeroes and all zeroes to ones.

Most buffers feature standard PNP inputs. However, the 'S/'LS340/341/344/310 buffers feature Schmitt-trigger inputs, with a guaranteed 300/400-millivolt deadband (typically twice that) centered about the switching threshold voltage. (This notation is shorthand for "54/74S340, 54/74S341, 54/74S344, 54/74S310, 54/74LS340, 54/74LS341, 54/74LS344 and 54/74LS310," and will be used frequently hereafter.) These Schmitt-trigger buffers won't respond to input noise pulses which would make buffers with normal inputs start to switch, as long as the noise pulses do not completely cross the deadband; thus noise immunity is improved.



"...THE 'LS340/341/344/310 BUFFERS FEATURE SCHMITT-TRIGGER INPUTS, WITH A GUARANTEED... DEADBAND..."

Latches and *registers* have the same basic capability as buffers, but also have the additional capability that they retain stored information as long as power is supplied to them. Each of these circuit types requires an additional control signal in order to perform its system function.

More specifically, *latches* use an *enable* signal. When this signal is on, they store information, and their outputs do not change even if the information presented to their inputs changes. When their enable signal is off, latches act just like buffers. Turning on the enable signal in effect "freezes" in place whatever information was passing through the latch, so that the latch stores it.

Registers use a *clock* signal instead of an enable signal. When the clock signal goes through a transition from off to on, this "rising edge" causes the information present at the inputs to be stored in the register, and then to remain present at the register outputs until another rising edge occurs. When the clock is in a steady-state condition (a "level"), either on or off, or even when the clock goes through a transition from on to off (a "falling edge"), the outputs of the register do not change. Thus, unlike latches, registers lack a mode in which they act exactly like buffers and pass information directly from their inputs to their outputs. This lack is a consequence of the control signal being "edge-sensitive" rather than "level-sensitive."

Transceivers are bidirectional interface circuits capable of interconnecting two buses so that information can pass in either direction. Most of the transceiver parts in production today are *buffer transceivers*—they are like two cross-coupled buffer circuits within a single 20-pin package. A 16-bit buffer transceiver has eight A-bus data pins and eight B-bus data pins. Either the A-to-B buffers may be enabled, or the B-to-A buffers, or neither; if both sets of buffers were to be enabled, obviously there would be a race condition on each of the data lines, and so the control structure of some buffer transceivers specifically disallows that mode of operation. (Some other types do allow it.) Buffers which are not enabled are, of course, in the hi-Z state. Thus each buffer transceiver interface circuit consists of eight logical elements, and each of these logical elements consists of two simple-buffer elements cross-coupled back-to-back so that the input line for one is the output line for the other and conversely.

Latch transceivers and *register transceivers* are now positioned to become major factors in the marketplace; several semiconductor houses now offer such devices. In particular, Monolithic Memories now supplies several different families of these devices in the 24-pin 300-mil SKINNYDIP® package; some of these families are also supplied by Texas Instruments. A variety of speeds and architectures are available; see section 12 of this Databook for details.

Pipelines are unidirectional interface circuits having more than one full-width internal latch/register or "stage," but typically having just one set of parallel data inputs and one set of parallel data outputs. Two-stage latch pipelines, and both two-stage and four-stage register pipelines, are available. The four-stage devices can store twice as much information per package, but the two-stage devices can be reconfigured more flexibly and have a greater degree of separate control for each stage.

Understanding and Using Interface

How Designers Choose Interface Circuits

In the real world, a digital-logic designer doesn't set out deliberately to use some particular interface circuit whose properties he has carefully learned, in the same way that he might for instance set out to use a bit-slice registered ALU or a multiplier/divider. Rather, as we have said, it is much more likely that it all starts with some innocent-looking little line between two blocks on his preliminary system block diagram which, it turns out, can't really be just a simple little line after all.

Maybe the data which travels on that little line goes away at the source unless the little line is actually also capable of seizing it at the proper time and remembering it. Or maybe the end of the little line is an assertive-low system bus, with enough loads hanging off it to call for almost 30 milliamps of drive capability in whatever contemplates driving the bus, which doesn't quite jibe with the 2-milliamp drive capabilities and assertive-high outputs of the MOS LSI device from which the data is coming.

At this point the designer needs an interface circuit, and—wittingly or unwittingly—he must go through a several-stage decision process to determine what interface circuit he needs to actually implement that little line, before his block diagram can turn into a system. He must also fervently hope that, by the time he gets to the final twig on his decision tree, the interface part he needs will turn out to actually exist. Figure 1 is an example.

A top-down design approach, as illustrated in Figure 1, isn't always wise with integrated circuits, simply because the chances are fairly good that the desperately needed circuit actually *won't* exist[1]. And there was a time, not all that long ago, when only a quasi-random subset of all of the obviously possible variations of the basic interface parts had reached full production status, so that they could be bought and plugged in. The hapless designer just had to memorize what that subset was, and do his design bottom-up from there.

Today, chaos is giving way to order, and enough of the possible interface parts which a designer might want do by now exist (or will exist shortly) that the kind of top-down thought process portrayed in Figure 1 really *will* work out all right when designing with interface. For instance, the line of interface parts now in production at Monolithic Memories is sufficiently orderly to be organizable into the matrix of the Interface Selection Guide on page 11-3 of this databook. Although this Guide is still somewhat irregular, it is at least recognizable as first-cousin to a logic-design Karnaugh map, and you can actually get your hands on any of the interface parts in the matrix.

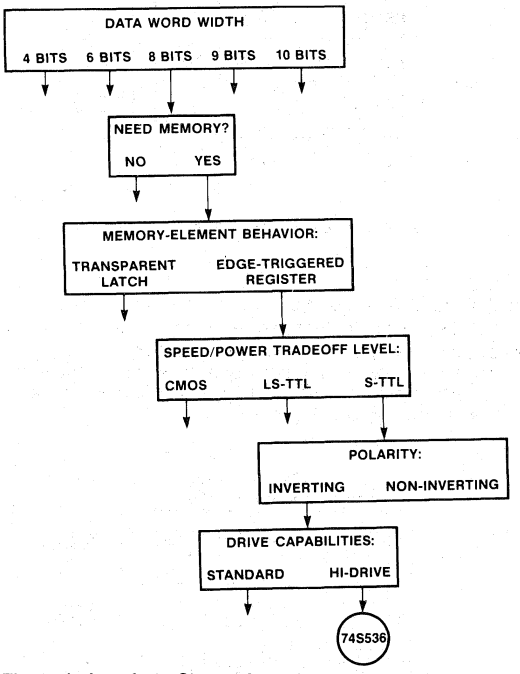


Figure 1. Interface-Circuit-Selection Decision Tree

The dimensions of variation for interface parts in any such Karnaugh map are, of course, two-valued "Boolean" variables. It is realistic from both logical and historical viewpoints to consider that all of the interface parts of the Interface Selection Guide have been derived from a very few basic types, by implementing those combinations which make sense of several two-valued properties of interface parts. These are:

- Commercial versus military temperature-range operation.
- High-speed Schottky (S-TTL) or low-power Schottky (LS-TTL) speed/power range.
- Noninverting or inverting outputs.
- No memory capabilities in the logical elements, so that they operate as buffers; or memory capabilities therein, further subdivided according to whether the logical elements operate as latches or registers.
- Compound 16-bit interface circuits or simple 8-bit interface circuits.
- Hi-drive or standard levels of current-sinking capability (I_{OL}) at the outputs.
- Schmitt-trigger or standard inputs.
- For non-three-state parts, master-reset or clock-enable control inputs.
- Series-resistor or standard outputs.

Obviously, not all imaginable combinations of the above properties actually exist as parts, or would even be useful if they did; and semiconductor houses cannot afford for long to offer 2^n interface-circuit part types for rapidly increasing n. Moreover, certain of the properties which in the past have had just two possible major choices (e.g., S-TTL and LS-TTL) today have more than two; for instance, Section 12 of this Databook includes some CMOS parts.

Nevertheless, by now the matrix approach has been fully-enough implemented to offer a very helpful perspective to the working designer.

Part numbers today allow some of the properties of interface circuits to be directly inferred, at least if the part number follows the conventions of the industry-standard "54/74" numbering series. 54/74 part numbers have a well-defined format VVE4TxxxP, with the following interpretation:

- VV — a prefix which varies somewhat from vendor to vendor.
- E4 — a temperature-range environmental specification. "54" implies the military temperature range (−55°C to +125°C), and "74" the commercial temperature range (0°C to +70°C for several vendors, and 0°C to +75°C for Monolithic Memories). In any case, interface circuits must run properly over a very wide temperature range.
- T — a solid-state-circuit technology. Upwards of a dozen of these have been promoted, with widely varying success, during the last decade. The earliest one, plain old gold-doped TTL, omitted using any special letter in part numbers. Today, the two dominant technologies are "S" (high-speed Schottky) and "LS" (Low-power Schottky). Others becoming quite important include "F" (for "FAST," a lower-power form of high-speed Schottky); "ALS" (advanced low-power Schottky); and "SC," "HCT" and "ACT" (isoplanar CMOS processed to be fully TTL-voltage-level compatible).
- xxx — a two-digit, three-digit, and today sometimes even four-digit number which uniquely specifies the *pin-out* of the part and its "functional behavior" (see the explanation which follows), independent of speed/power range.

12

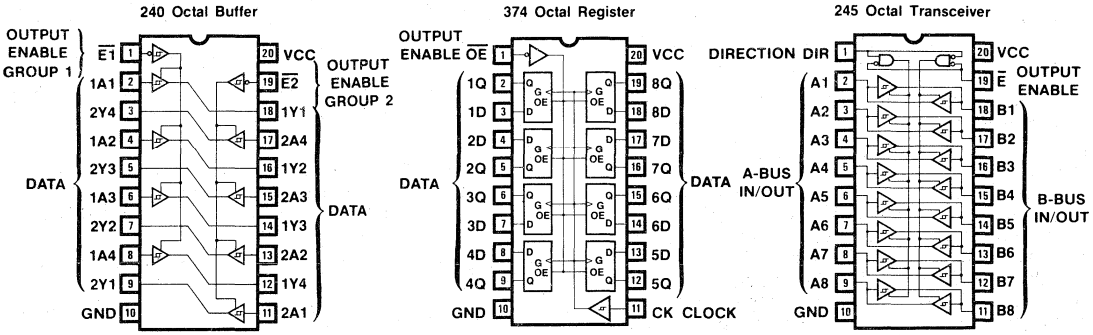
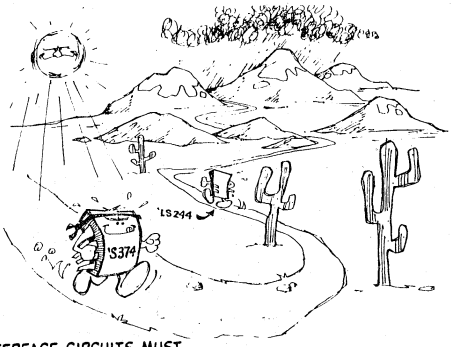


Figure 2. Pinouts for the Three Basic 20-Pin Interface Parts

- P — a package type: plastic, cerdip, flatpack, leadless chip carrier, sidebrazed ceramic, small-outline surface-mount, or whatever.

The functional behavior of a circuit can be defined somewhat circularly as **"what a designer needs to know about the circuit in order to construct designs which operate properly using parts from any supplier interchangeably."** This definition is akin to one classic definition of computer architecture as **"...the structure of the computer a programmer needs to know in order to be able to write any program that will correctly run on the computer."**[2]



"...INTERFACE CIRCUITS MUST RUN PROPERLY OVER A VERY WIDE TEMPERATURE RANGE..."

Two parts produced using different solid-state-circuit technologies may exhibit essentially the same functional behavior. If that is the case, and if either part will also satisfy system timing constraints (which is an issue quite separate from that of "functional behavior") and input/output voltage compatibility constraints, the designer does not need to care what kind of internal gates are used within the part—Schottky TTL, ECL, CMOS, NMOS, or water wheels. On the other hand, two parts produced using the same technology may have subtle, or even drastic, differences in their functional behavior; for example, one may have inverting outputs, or hi-drive outputs, or Schmitt-trigger inputs whereas the other does not.

The Matrix of Interface Part Types

The interface parts of the Interface Selection Guide mostly have one of just three different pinouts, shown in Figure 2, in their usual 20-pin plastic or cerdip SKINNYDIP form.

All of the buffers have the same pinout as the 'S240. They differ in speed/power range, in the polarity of the outputs, in the noise-rejection capabilities of the inputs (Schmitt-trigger or standard), and in enable structure (complementary or assertive-low) as shown in Figure 3, which really *is* unequivocally a Karnaugh map.

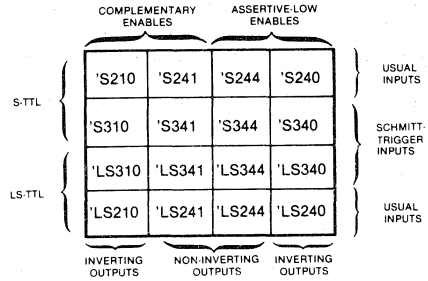


Figure 3. 8-Bit Three-State Buffers

Most of the latches and registers have the same pinout as the 'S374. They differ in whether the memory control line is level-sensitive (latch) or edge-sensitive (register), in speed/power range, in the polarity of the outputs, and in the I_{OL} (current-sinking drive) capability of the outputs as shown in the Karnaugh map of Figure 4.

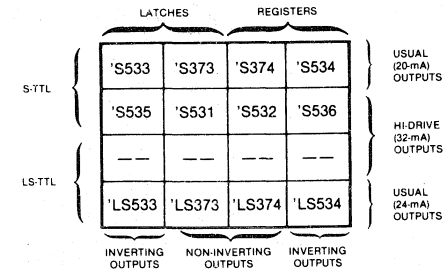
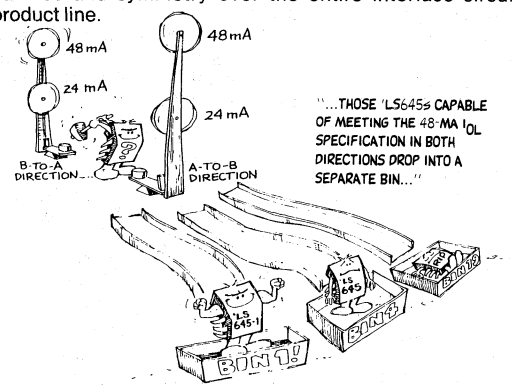


Figure 4. 8-Bit Three-State Latches and Registers

The three transceivers of the Interface Selection Guide are more specifically *buffer transceivers*—compound 16-bit interface circuits like two 8-bit buffer circuits cross-coupled "back-to-back" within a single device. They differ in input-current and output-leakage-current specifications, which here are indistinguishable for test purposes since every data pin is both an input and an output; the 'LS245 specification is tighter. (The 'LS245-1 is *also* specified as faster, but that is *not* a difference in "functional behavior.") There is also a difference in I_{OL} capability; the 'LS645-1 is specified as higher. Actually, all three devices undergo identical fabrication, and are separated only at final testing; for instance, those 'LS645s capable of meeting the 48-mA I_{OL} specification in both directions drop into a separate bin.

Upcoming developments in interface parts will tend in many cases to follow the matrix approach, at least partially. Even where the new parts do not fit perfectly into the matrix of existing parts, some attention is likely to be paid to issues of balance and symmetry over the entire interface-circuit product line.

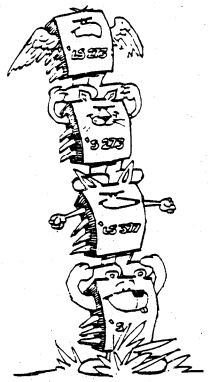


In some cases, new interface parts directly "fill in the holes" in the matrix. For instance, some recent additions to Monolithic Memories' line of interface parts are:

Function	Speed/ Power	Polarity	Feature	Part Number
Register	S	Noninv.	Master Reset	SN54/74S273
Register	S	Noninv.	Clock Enable	SN54/74S377 SN54/74S383@
Buffer	S	Noninv.	Series Output Resistor	SN54/74S734*
Buffer	S	Noninv.	Series Output Resistor	SN54/74S731
Buffer	S	Inv.	Series Output Resistor	SN54/74S730#
Buffer	S	Inv.	Series Output Resistor	SN54/74S700

NOTES: @—The 'S383 differs from the 'S377 only in having open-collector outputs rather than totem-pole outputs.
*—The 'S734 is a direct replacement for AMD's Am2966.
#—The 'S730 is a direct replacement for AMD's Am2965.

Table 1. Recent Additions to the Monolithic Memories Interface-Part-Type Matrix



"...THE 'S273 AND 'S377, LIKE THEIR LS-TTL COUNTERPARTS, ARE DESIGNED WITH STANDARD TTL 'TOTEM-POLE' OUTPUTS..."

The 'S273 and 'S377 bring to higher-performance TTL systems the same functional behavior which has long been available for medium-performance TTL systems, with the popular 'LS273 and 'LS377 parts. The 'S273 and 'S377, like their LS-TTL counterparts, are designed with standard TTL "totem-pole" outputs. Somehow, in the somewhat more chaotic early days of 8-bit interface, the need for high-speed Schottky versions of these parts got overlooked by most interface producers.

Since the 'S273 and 'S377 are totem-pole-output parts, the control pin which gets used on the 'S374 (whose pinout they otherwise follow) for "Output Enable" for the three-state outputs is available for something else. The 'S273 uses it as a "Master Reset" ($\overline{MR}$) input, capable of forcing all of the eight D-type flipflops on the chip into the off (low) state simultaneously, regardless of their previous state—*or* of the state of the clock line and/or the data-input lines. The 'S377, on the other hand, uses that same pin as a "Clock Enable" ($\overline{CK\ EN}$) input, which in effect either allows the clock signal to reach the eight D-type flipflops on the chip, or else cuts it off from reaching the flipflops so that they are not clocked and just sit there holding whatever information they contained previously. The 'S383 is a slight modification of the 'S377 to provide open-collector rather than totem-pole outputs.

The major applications for these parts are in situations where 'S374s would be difficult to control appropriately. Because of the 'S273's $\overline{MR}$ input, its forte is *control* applications—instruction registers, microinstruction registers, timing-pulse registers, and sequential circuits in general, and sometimes as eight *individual* separate D-type control flipflops in one package. In all of these applications, there *has* to be a way to force the system into some proper initial state, so that it "starts off on the right foot" and does not get into some unplanned-for, untestable, unpredictable machine-psycho condition on power-up. The 'S377, on the other hand, because of its $\overline{CK\ EN}$ input, is the optimum choice for the highest-performance TTL pipeline paths for data, instructions, microinstructions, and address parameters in "overlapped-architecture" machines such as array processors and high-performance minicomputers. Its open-collector counterpart, the 'S383, can be used to drive open-collector buses or to provide wired-OR or wired-AND logic functions.

The 'S700, 'S730, 'S731, and 'S734 feature a new type of output stage incorporating a series resistor, designed to efficiently drive highly-capacitative loads such as arrays of dynamic-MOSRAM inputs. Rise and fall times are more

12

symmetric than with 'S240-type buffers, and the latter need an *external* series limiting resistor for their own protection when driving highly capacitative loads.

Consequently, although 'S240-type buffers may exhibit greater speed when tested under light loading conditions, 'S730-type buffers are likely to perform better under realistic system conditions when driving large distributed capacitative loads is a major factor in the application.

Of these four new buffers, two—the 'S730 and 'S734—are second-source versions of the Am2965 and Am2966 respectively, originally introduced by AMD. The other two—the 'S700 and 'S731—are complementary-enable versions of the 'S730 and 'S734 respectively, just as the 'S210 and 'S241 are complementary-enable versions of the 'S240 and 'S244 respectively. Complementary-enable buffers excel in driving buses with two multiplexed sources for the information, such as instruction addresses and data addresses in a bit-slice bipolar microcomputer system.

The four 'S730-type parts may be grouped with Monolithic Memories' line of conventional and Schmitt-trigger-input buffers in a 2x2 matrix chart or Karnaugh map, with the dimensions of this map chosen to be the polarity of the second-buffer-group enable input E_2 (here across the top) and the polarity of the data-buffer logical elements themselves (here down the side), thus:

		Polarity of E_2*	
		$\overline{E}_2$	E_2
Polarity of Data Buffers	Inverting	'LS240 'LS340 'S240 'S340 'S730	'LS210 'LS310 'S210 'S310 'S700
	Noninverting	'LS244 'LS344 'S244 'S344 'S734	'LS241 'LS341 'S241 'S341 'S731

* Since $\overline{E}_1$ is assertive-low for *all* of these parts, the parts with an assertive-low $\overline{E}_2$ are "assertive-low-enable" parts, whereas the parts with an assertive-high E_2 are "complementary-enable" parts.

Table 2. 8-Bit Buffers Grouped by Polarity and Enable Structure

By this time, many presently-unused SN54/74xxx part numbers have already been reserved for other potential new parts, even though not all of these parts are yet in production. Nevertheless, it was at least possible to part-number these four series-output-resistor buffers in such a way that the relationship among the four types remains the same as for 'S240-type buffers. To state this another way, one can add 490 to the last three digits of the usual buffer part number to get the part number for the corresponding series-output-resistor part, e.g., 'S241 + 490 = 'S731, etc.

Directions In The Evolution of Interface Parts

More Bits per Package

Historically, the first interface parts were 16-pin TTL devices offered during the early 1970s, usually with four or six "logical elements" per package. One "logical element" handles one data bit; in simple interface parts, a logical element may be a buffer, a latch, or a register (with "register" here implying an edge-triggered flipflop).

As the digital-electronics industry shifted from MSI to LSI integrated circuits, and from the quaint and irregular old-time computer word lengths to word lengths which are multiples of eight bits (most often 8, 16, or 32), 8-bit interface devices became the only way to go for simple electrical data transformations—chip counts got intolerably high with 4-bit devices, and 6-bit devices were awkward misfits in most of the newer designs![3] And, to have eight input data lines, eight output data lines, power and ground, and two control signals, an integrated-circuit package has to have 20 pins.

To conserve board space, the width of this 20-pin package was chosen to be 300 mils (.300") like that of the overwhelming majority of the then-existing bipolar MSI and SSI devices. Hence, during the 1970s, the present 20-pin 300-mil SKINNYDIP package became the standard for interface circuits. One 20-pin SKINNYDIP takes up only about half as much board space as one of the older 600-mil 24-pin packages, which were then being used for a few early 8-bit interface parts such as the Intel 8212.

"...ONE 20-PIN SKINNYDIP™ TAKES UP ONLY ABOUT HALF AS MUCH BOARD SPACE AS ONE OF THE OLDER 600-MIL 24-PIN PACKAGES..."

24-pin interface parts were obviously the next major development to come. In the early 1980s, mechanical packaging problems which previously had inhibited the introduction of a 24-pin 300-mil SKINNYDIP were solved, and this package is now also in widespread use for PROMs, PAL programmable-logic circuits, and so forth. So what might one do with four additonal pins in an interface part?

One answer is to spend all four of them for additional *control* signals in order to achieve more flexible parts, such as the Monolithic Memories SN54/74LS380 "multifunction" 8-bit register. (See page 6-16 of this databook.) This part is actually implemented with "hard-array logic" technology, and has an internal structure like one form of PAL.

Another answer is to spend all four of them for additional *data* signals, equally for inputs and outputs. The result is 10-bit interface parts with functionality similar to that of existing 20-pin 8-bit parts.

A middle-of-the-road answer is to divide them equally between control signals and data signals. This approach leads to 9-bit interface parts with improved functionality.

16-bit "double-density" interface-circuits — dual 8-bit circuits in a single 24-pin SKINNYDIP — are a more far-reaching answer than the preceding ones. These circuits use the four extra pins to provide separate control inputs for *both* 8-bit internal groups, and also to provide improved functionality. The number of data pins is held at 16 by *multiplexing* the use of two 8-bit groups of input and/or output pins.

The motivation for 16-bit interface parts is, first of all, to cut component counts by replacing two parts with one in as many situations as possible, in order to save board space and assembly costs. Particularly in high-performance computers and array processors, the packaging itself is expensive when it must be designed to provide a proper signal-transmission environment for ultra-fast logic. An almost-50% cut in the board area required for the interface parts—here, as always, the "glue" which holds the whole system together—may result in major indirect savings.

But there are other incentives besides sheer cost reduction which favor cramming as much logic as possible into a given board area. There usually is only one board size in a chassis (or even in a system), and any logic subsystem which cannot fit onto one such board immediately incurs a *speed* penalty attributable to board-to-board communications—extra buffers for noise-free signal transmission, extra signal-path length on each board over to the edge where the connectors are, more extra length in the backplane wiring, and lots of additional inductance and capacitance permeating all of the above.

So, saving board area is very likely to improve *both* system cost *and* system performance, by increasing the probability that a given logic subsystem will fit onto just one board.

Interface-part internal element density has for many years been increasing at a rate which is, to say the least, unspectacular. Going from four to six to eight to sixteen logical elements in an interface-circuit package doesn't seem like a whole lot, compared for instance to going from 1K to 4K to 16K to 64K to 256K bits in a single dynamic-MOSRAM package in roughly the same number of years.

But, consider what a *true* LSI interface circuit would have to look like—one with the same magnitude of "equivalent gate count" being bandied about for today's microprocessors, dynamic MOSRAMs, and so forth. First of all, it would need to have *several hundred data inputs* and *several hundred data outputs,* so that the most immediately-plausible mechanical design for a package would resemble a sea urchin! And, if it were implemented using any present-day TTL technology, the part would dissipate enough *watts* to need cooling fins like a Porsche cylinder head!

And so it has turned out that progress over time in increasing the logical-element density for interface parts has been more or less linear, while progress in increasing the level of integration for microprocessors and dynamic MOSRAMs has been more or less exponential. It is no accident that a basic phrase of the definition for "interface circuits" quoted earlier in this paper is **". . . which do not lend themsives to higher levels of integration . . ."** If these same density trends continue, digital electronic systems of the future may actually have a *higher* proportion of packages allocated to interface circuits than is typical today, which if it happens is likely to surprise quite a few people.

Structure of 16-Bit Interface Circuits

Common configurations of two 8-bit interface parts used together furnish a natural starting point for the definition of useful 16-bit interface parts. When the same configuration tends to occur over and over again, it is natural to "draw a boundary around it and put it all on one chip," unless of course the resulting compound chip turns out to need too many pins.

Figure 5 illustrates three such two-part configurations which are observably very common, and intuitively very plausible:

- "Back-to-back" or "cross-coupled." (Figure 5A).
- "Nose-to-tail" or "pipelined." (Figure 5B.)
- "Side-by-side" or "parallel." (Figure 5C.)

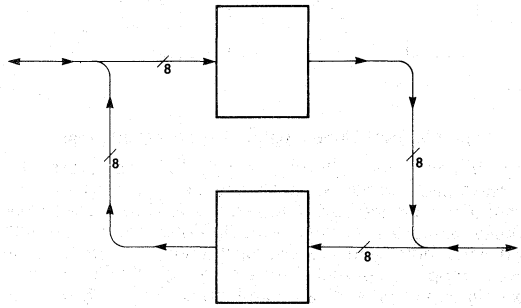


Figure 5A. Back-to-Back Configuration

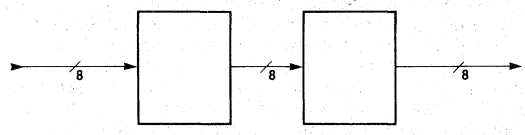


Figure 5B. Nose-to-Tail Configuration

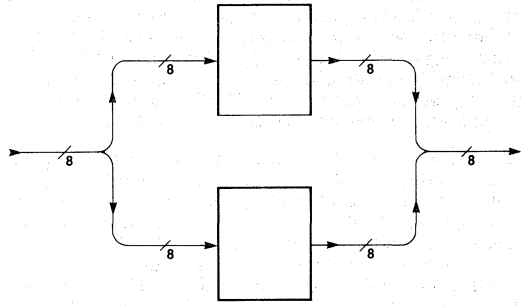


Figure 5C. Side-by-Side Configuration

Figure 5. Common Configurations of Two 8-Bit Interface Parts

The back-to-back configuration, when applied to simple 8-bit buffers, leads to buffer transceivers such as the 'LS245. The 'LS245 is, of course, still a 20-pin part; the choice was made to change its enable structure from that which would be strictly implied by placing two 'LS244s back-to-back, in order to hold the package size to 20 pins and to disallow having both directions simultaneously enabled. These same statements continue to hold for the 'LS645 and 'LS645-1. The 'LS640 and 'LS640-1 are inverting buffer transceivers, and the 'LS643 and 'LS643-1 incorporate an 8-bit inverting buffer back-to-back with an 8-bit noninverting buffer; there are also open-collector equivalents to these parts and the 'LS645 and 'LS645-1. The entire series features the same

12

enable structure, with a master enable line $\overline{E}$ controlling *both* sets of buffers and a direction line DIR to allow just one direction to be enabled at a time.

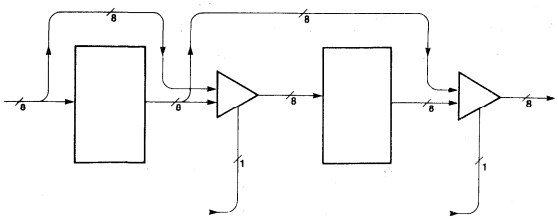


Figure 6. Two-Stage Pipeline Register Configuration

Applied to 'LS373 latches and 'LS374 registers, the back-to-back configuration leads to the 24-pin 'LS547 latch transceiver and the 'LS546 register transceiver respectively. These parts are just what one would expect them to be, with individual output-enable and clock control inputs for each 8-bit group, except that there are enough pins to also give each group clock-enable control inputs like the 'S377. The 'LS567 and 'LS566 are the corresponding inverting parts.

The nose-to-tail and side-by-side configurations do not lead to anything very interesting with buffers, at least as long as there are only enough pins for one 8-bit input data path and one 8-bit output data path. Latches and registers, however, are entirely another matter. It turns out to be attractive to *combine* these two configurations, even though at first glance they look quite dissimilar, into a single "two-stage pipeline" configuration as shown in Figure 6. Such a two-stage pipeline can operate in either a nose-to-tail mode or a side-by-side mode, according to the setting of the two internal multiplexers shown in Figure 6. Applied to 'LS373 latches and 'LS374 registers, this more powerful configuration leads to the 24-pin 'LS549 latch pipeline and the 'LS548 register pipeline. For these parts, the control inputs are a final-stage output enable, selects for each mux, a common clock (or latch-enable for the 'LS549) input for both stages, and individual clock-enable inputs for each stage.

To clarify the timing control of these parts, the 16-bit register parts ('LS546, 'LS566, and 'LS548) have individual clock-enable signals for each 8-bit group, and either individual clock signals ('LS546 and 'LS566) or a common clock signal ('LS548). The 16-bit latch parts ('LS547, 'LS567, and 'LS549), since the "clock" signal turns into a level-sensitive latch-enable signal, have two independent ways of enabling storage in each of the two stages. Thus, the 'LS547 and 'LS567 parts feature two separate and equivalent latch-enable control inputs for each 8-bit group, either one of which can cause the group to "latch up" and store information. The 'LS549 part has the same operating mode, except that each 8-bit group has one *separate* latch-enable control input and there is one more latch-enable input *common* to both groups. *Read-back latches and registers* ('LS793 and 'LS794) also have a back-to-back structure; but their "return" element is a buffer (resembling, say, a '244), rather than another latch or register.

As with other TTL 8-bit latches and registers, the part-numbering scheme for all of the parts just mentioned assigns odd numbers to latches and even numbers to registers.

Front-loading latches are one other type of 16-bit interface part. The 'LS646 (noninverting) is to a first approximation an 'LS645 superimposed upon an 'LS546. (The numbering scheme wasn't *planned* to be that cute—it just happened.) The 'LS648 is a similar inverting part. To clarify what is meant, each of the eight logical elements of an 'LS646 consists of two back-to-back buffers and two back-to-back flipflops, with a parallelled buffer and flipflop pointing in the A-to-B direction and a similar buffer-flipflop pair pointing in the B-to-A direction. The 'LS646 and 'LS648 are three-state parts: the 'LS647 and 'LS649 are respectively the equivalent open-collector parts. The 'LS651 (inverting) and the 'LS652 (noninverting) are equivalent to the 'LS648 and 'LS646 respectively, but have a different control structure which allows independent enabling of either direction; the 'LS653 and 'LS654 are versions of the 'LS651 and 'LS652 respectively in which the A-direction output buffers are open-collector, and the B-direction buffers are still three-state.

32-bit interface parts are also visible on the horizon. Two four-stage pipelines, the Am29520 and Am29521, are offered by AMD as members of a series of signal-processing parts, and Monolithic Memories is introducing them also as the 'S720 and 'S721. As compared to the 'LS548 and 'LS549, they offer twice as many stored bits per square inch of board, but considerably less flexibility in accessing and controlling register contents.

The matrix approach to classifying various interface parts can be extended to encompass transceivers and pipelines, as is done in Table 3. The correspondence between the various 8-bit simple-interface parts and the 16-bit compound interface parts which are in a sense derived from them, is summarized in Table 4.

Configuration	Buffers	Latches	Registers	Front-Loading Latches
Simple	'210 '310 '240 '340 '241 '341 '244 '344	'373 '531 '533 '535	'374 '532 '534 '536	---
Back-to-Back	'245 '640 '640-1 '643 '643-1 '645 '645-1	'547 '567	'546 '566	'646 '647 '648 '649 '651 '652 '653 '654
Two-Stage Pipeline	---	'549	'548	---

Table 3. Matrix Classification Scheme for 8-Bit and 16-Bit Interface Parts

Simple Interface Type	Compound Interface Type	Number Of Pins	Buffer	Latch	Register
	Transceivers:				
'244	'245 '645 '645-1	20	X		
'240	'640 '640-1	20	X		
'240/'244	'643 '643-1	20	X		
'373	'547	24		X	
'374	'546	24			X
'533	'567	24		X	
'534	'566	24			X
	Pipelines:				
'373	'549	24		X	
'374	'548	24			X

Table 4. Equivalences Between Simple and Compound Interface Types

Various Applications of Interface Parts

Some Logic-Design Examples

Several illustrative designs using various interface parts may suggest some design insights and some creative ways to use interface. The designs presented have generally been excerpted from actual digital systems.

Reading a switch setting to establish an externally-defined system parameter, such as a device address, is a mundane but essential task in many microprocessor-based systems. Figure 7 illustrates how a group of eight switches may conveniently be read using a byte-wide buffer such as the 'LS244. Since the switches must be electrically isolated from the bus, the 'LS244's three-state outputs are disabled by control signals originated by the microprocessor until the time comes to read in the switch settings. Because the 'LS244 can supply up to 24 milliamps of I_{OL} to drive the bus, this simple scheme can be utilized even on heavily-loaded system data buses.

If still more drive capability is needed, an 'S244 in the same configuration can sink up to 64 milliamps. And, if the system is to be operated in an industrial environment and the switch signals entering the buffer inputs are subject to severe noise, the Schmitt-trigger 'LS344 type of buffer can also be substituted for the 'LS224 with no other change to the circuit.

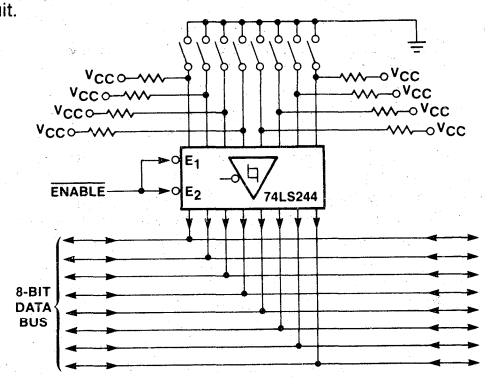


Figure 7. Switch-Setting Readin Circuit

Interfacing two separate buses is a very standard application for transceivers. Figure 8 shows an 'LS245, which has a control structure such that one control signal selects the *direction* of data transfer and the other one independently allows data transfer to be *enabled or disabled.* Thus, the two buses can be operated totally isolated from each other, or else either one may be made to follow the other. Depending on the drive-capability and polarity requirements of the application, any of the other buffer transceivers might be used here instead. Or, if memory as well as cross-coupling is required, a latch transceiver or register transceiver might also be used in a similar manner.

Driving a dynamic-MOSRAM address bus with a multiplexed row/column address can conveniently be done with an 'S700 as shown in Figure 9. This part is an inverting complementary-enable buffer with a series-resistor output structure, which is an ideal combination of characteristics here.

First of all, a TTL inverting buffer normally has one less transistor — and hence one less delay — in its internal data path than does an equivalent noninverting buffer, and hence is faster. And dynamic MOSRAMs really don't care if their addresses come in "true" or "complemented" form as long as that form *never* changes.

Second, a complementary-enable buffer can easily multiplex two different address sources to the same set of outputs without introducing extra switching delay, or allowing a momentary "bus fight" condition, if the same control signal (here $\overline{CAS}$ or "Column Address Strobe") is tied directly to both $\overline{E_1}$ and E_2 and the two 4-bit groups of outputs are tied together.

Finally, because of the internal series resistor in the'S700's output structure, this part (like the 'S730/1/4) can drive highly capacitative loads, of say up to 70 dynamic-MOSRAM inputs, without the need for external limiting resistors to control undershoot, resulting in a net system speed gain since signal rising and falling transition times remain symmetric. Otherwise, the effective logic delay of the buffer (which is simply the

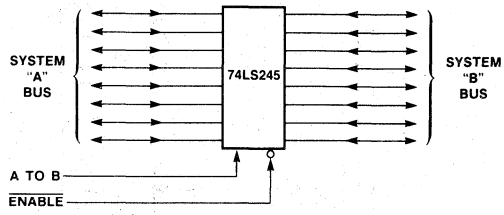


Figure 8. Interfacing Two Separate Buses

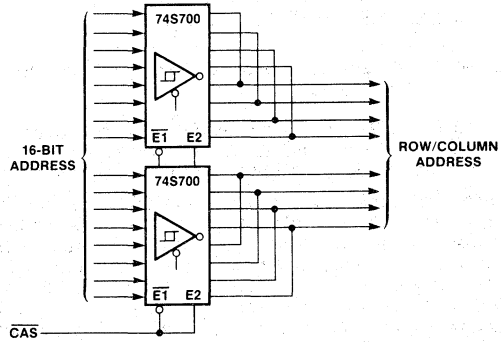


Figure 9. Multiplexed Row/Column Address Drivers

worse of the two transition times) would get degraded, since the use of an external series resistor would have greatly lengthened the low-to-high transition time.

Demultiplexing and holding address and data words for single-bus microprocessors is an application which takes advantage of the strong points of the 'S531 as shown in Figure 10. Since the 'S531 is a "transparent latch" and can operate as a buffer when necessary, the memory system designer can take advantage of the *full* time slots when the address and data signals are present on the microprocessor outputs. Because the address and data signals are then present for a longer period of time at the 'S531 outputs, it may be possible to use slower (and therefore less expensive!) memory devices than if edge-triggered registers had been used here instead. The three-state outputs of the 'S531 allow the designer to implement bidirectional data buses and DMA address schemes. Variations on this approach can use 'S373s if less drive capability is needed, or 'LS373s if less speed is needed as well; or 'S535s, 'S533s, or 'LS533s under the same respective circumstances if the address and data buses to be driven are assertive-low

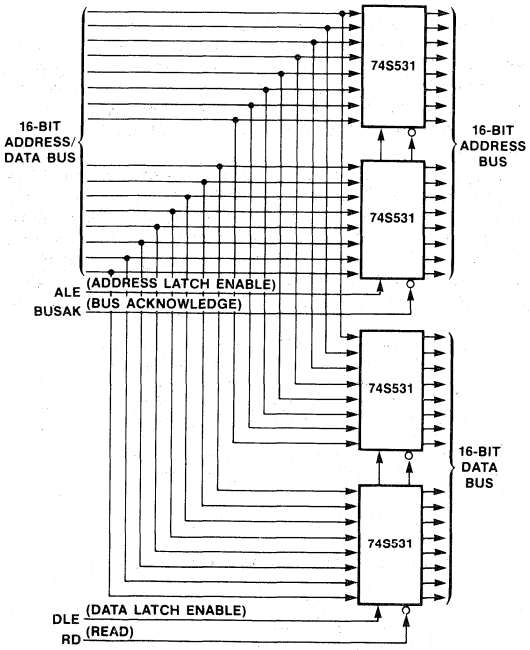


Figure 10. Address/Data Demultiplexer for Single-Bus Microprocessors

according to the system definition. If the data-bus interface needs to have latching capability also for data returning to the microprocessor, then 'LS547s are an excellent choice.

Synchronizing the state changes of a PROM-based control sequencer is easily performed using a register with a clock-enable feature, like the 'LS377 shown in Figure 11. In this simple sequencer, a 4-bit counter steps through the PROM addresses. The counter may be reset to address 0000, or loaded with any 4-bit address. The 32 × 8 PROM, with five address lines, allows for one external input as well as the four bits from the counter. The PROM outputs are pipelined using the 'LS377, which eliminates PROM output glitches, synchronizes the state changes of the sequencer with the system clock, and speeds up the effective cycle time. The availability of enable control inputs on both the counter and the 'LS377 allows forcing "wait" states, where both the counter and the register hold their current state for extended periods of time. If a higher-speed implementation of this design is needed, a 74S161 or 93S16 counter can replace the 74LS161, one of Monolithic Memories' new 63S081A ultra-speed 32x8 PROMs (15 nsec worst-case and 9 nsec typical for t_{AA}, instead of 50 and 37 nsec respectively) can replace the 6331-1, and an 'S377 can replace the 'LS377.

Saving Designs at the Last Minute, or Planning Ahead

Designs hanging out over the edge of unworkability can sometimes be salvaged without any redesign effort, by replacing standard interface parts with hi-drive, Schmitt-trigger-input, or even just inverting pin-compatible parts. Hi-drive parts such as the 'S532 or 'LS645-1 get dropped into 'S374 or 'LS645 sockets respectively late in the design cycle, when the designer suddenly discovers that he has hung several too many inputs on his main system bus. Schmitt-trigger-input parts such as the 'LS341 likewise get dropped into 'LS241 sockets shortly after the designer has recovered from his first observation of his actual bus waveforms on a good laboratory oscilloscope—it's that or back to the old drawing board. And, when he suddenly remembers after laying out a tightly packed board that "Oh, xxxx, that particular bus is assertive-*low*," it's nice to be able to simply substitute an 'S534 for an 'S374 in a few places rather than having to find room for several inverter packages. So a designer who has learned to think of interface parts in terms of the matrix approach will now and then find a particularly quick route to saving his skin.

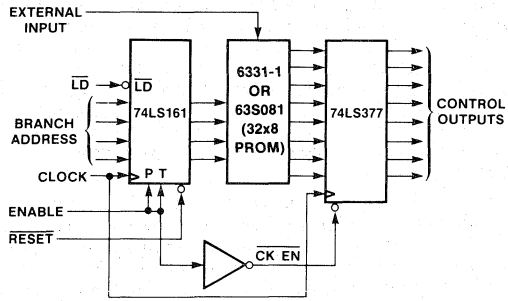


Figure 11. Synchronous PROM-Based Control Sequencer

However, an astute designer may use hi-drive, Schmitt-trigger-input, and inverting parts quite deliberately in order to gain speed, economy, drive capability, or noise immunity. A number of the industry-standard buses in the microcomputer world are assertive-low; and inverting buffers, latches, and registers are much more appropriate for connecting these to a microprocessor, or to a bit-slice arithmetic unit, than non-inverting parts with extra inverters in series just to make the polarity come out right. Similarly, Schmitt-trigger hex inverters whose only function in the data path is to provide noise immunity can be eliminated by using 'LS340-type buffers, which also provide significant drive capability and three-state outputs. The need to parallel three-state drivers and registers and split drive lines, just for extra drive capability, can be reduced or eliminated by using hi-drive parts. And, in an obvious but not trivial switch, substituting a high-speed Schottky part for a low-power Schottky equivalent part can beef up drive capability considerably.

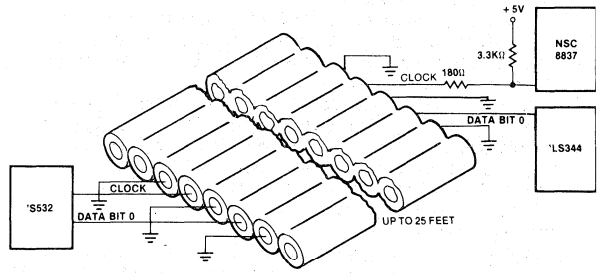
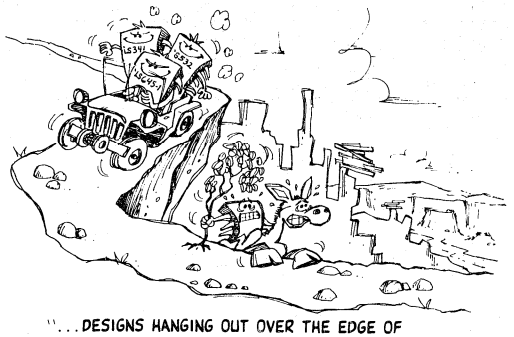


Figure 12. Flat-Cable Transmission Scheme Using Hi-Drive and Schmitt-Trigger-Input Interface Parts

Board-to-board signal transmission via flat cable is a particularly nice application for both hi-drive and Schmitt-trigger-input interface parts. The 32-milliamp outputs of, say, an 'S532 are better matched to the characteristic impedance of flat cable (usually 100 to 120 ohms) than 20-milliamp outputs would be. An adequate scheme, in many cases, for the

transmission of *data* from board to board uses 3M or similar flat cable. Every second cable wire is grounded at both ends for shielding, so that signal wires alternate with ground wires ("signal-ground-signal-ground"), and there is at least one ground wire at each edge of the cable. Signal wires are driven by 32-mA hi-drive latches or registers, and the receivers are Schmitt-trigger-input buffers, and that's all there is to it—no resistors, capacitors, or black magic. For a strobe, clock, or control signal, a linear receiver such as a National Semiconductor 8837 is used together with a 180-ohm series resistor and a 3300-ohm shunt resistor to V_{CC}, as shown in Figure 12. This overall scheme is compatible with some Digital Equipment Corporation buses, and is good for transmission distances of up to 25 feet.



"...DESIGNS HANGING OUT OVER THE EDGE OF UNWORKABILITY CAN SOMETIMES BE SALVAGED..."

Conclusion

Interface parts seem primitive alongside of LSI microprocessors and dynamic MOSRAMs, but they are inescapable and smart designers today have learned how to use them astutely. A powerful aid in doing so is to think of the set of interface parts as an array, which fits into a matrix whose dimensions are various circuit properties. Even though the rate of progress seems slow, the bit-density and functionality of interface parts is steadily increasing, and the time is approaching for designers to learn to take the next logical step and use 16-bit interface parts extensively in their systems, in order both to save cost and to improve overall system performance.

References

r1. "Bottom-Up Design with LSI and MSI Components," Chuck Hastings, *Conference Proceedings of the Fourth West Coast Computer Faire.* 11-13 May 1979, pages 359-365. Available from the Computer Faire, Suite 110, 611 Veterans Boulevard, Redwood City, CA 94063.

r2. "Architecture of the IBM System/360," G. M. Amdahl, G. A. Blaauw, and F. P. Brooks, *IBM Journal of Research and Development,* Volume 8 (1964), pages 87-101.

r3. "The 20-Pin Octal Interface Family—Today's Computer-System Building Blocks," Chuck Hastings, applications note available from Monolithic Memories, Inc. A longer paper written when buffer transceivers were the only visible 16-bit parts, but with more detail on the 8-bit parts.

8-Bit Buffers

SN54LS240 SN54S240
SN54LS241 SN54S241
SN54LS244 SN54S244

Features/Benefits

- **Three-state outputs drive bus lines**
- **Low current PNP inputs reduce loading**
- **8-bit data path matches byte boundaries**
- **Ideal for microprocessor interface**
- **Complementary-enable '241 combines multiplexer and driver functions**

Ordering Information

PART NUMBER	PKG	TEMP	ENABLE	POLARITY	POWER
SN54LS240	J,L,W	Mil	Low	Invert	LS
SN54LS241	J,L,W	Mil	High-Low	Non-Invert	LS
SN54LS244	J,L,W	Mil	Low	Non-Invert	LS
SN54S240	J,L,W	Mil	Low	Invert	S
SN54S241	J,L,W	Mil	High-Low	Non-Invert	S
SN54L244	J,L,W	Mil	Low	Non-Invert	S

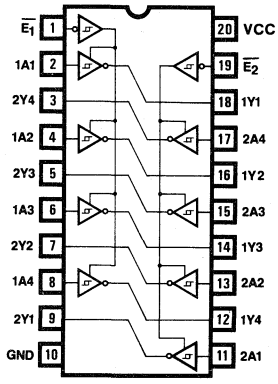
Description

These 8-bit buffers provide high speed and high current interface capability for bus organized digital systems. The three-state drivers will source a termination to ground (up to 133 Ω) or sink a pull-up to V_{CC} as in the popular 220 Ω/330 Ω computer peripheral termination. The PNP inputs provide improved fan-in with 0.2 mA I_{IL} on the low-power Schottky buffers and 0.4 mA I_{IL} on the Schottky buffers.

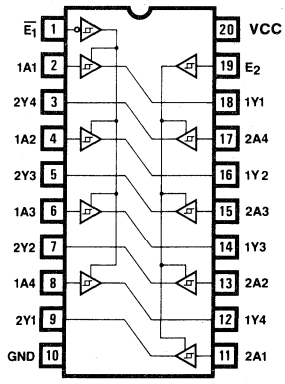
The '240 and '244 provide inverting and noninverting outputs respectively, with assertive low enables. The '241 also provides inverting and noninverting outputs, but with complementary (both assertive-low and assertive-high) enables, to allow transceive or multiplexer operation.

Logic Symbols

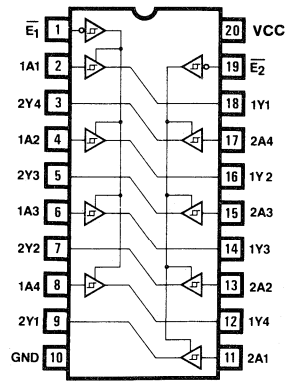
'240 8-Bit Buffer



'241 8-Bit Buffer



'244 8-Bit Buffer



TWX: 910-338-2376
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
Monolithic Memories

Function Tables

'240

$\overline{E1}$	$\overline{E2}$	1A	2A	1Y	2Y
L	L	L	L	H	H
L	L	L	H	H	L
L	L	H	L	L	H
L	L	H	H	L	L
L	H	L	X	H	Z
L	H	H	X	L	Z
H	L	X	L	Z	H
H	L	X	H	Z	L
H	H	X	X	Z	Z

'241

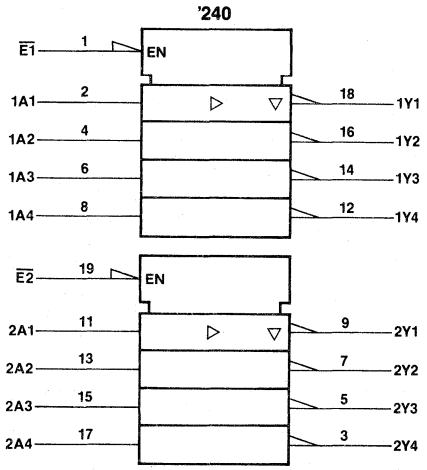
$\overline{E1}$	E2	1A	2A	1Y	2Y
L	L	L	X	L	Z
L	L	H	X	H	Z
L	H	L	L	L	L
L	H	L	H	L	H
L	H	H	L	H	L
L	H	H	H	H	H
H	H	X	L	Z	L
H	H	X	H	Z	H
H	L	X	X	Z	Z

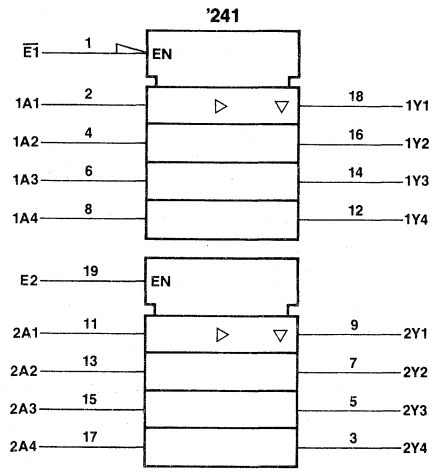
'244

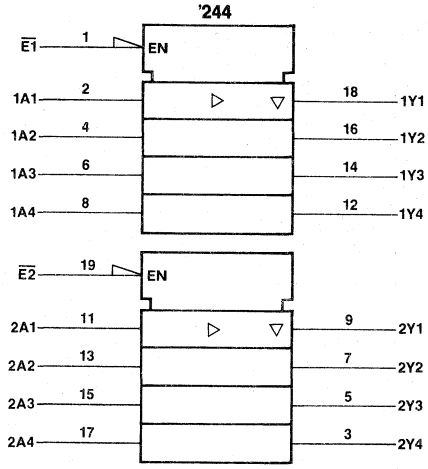
$\overline{E1}$	$\overline{E2}$	1A	2A	1Y	2Y
L	L	L	L	L	L
L	L	L	H	L	H
L	L	H	L	H	L
L	L	H	H	H	H
L	H	L	X	L	Z
L	H	H	X	H	Z
H	L	X	L	Z	L
H	L	X	H	Z	H
H	H	X	X	Z	Z

12

IEEE Symbols







Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
T_A	Operating free-air temperature	-55		125	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	UNIT
V_{IL}	Low-level input voltage						0.7	V
V_{IH}	High-level input voltage				2.0			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = -18 mA			-1.5	V
ΔV_T	Hysteresis (V_{T+}-V_{T-})		V_{CC} = MIN		0.2	0.4		V
I_{IL}	Low-level input current		V_{CC} = MAX	V_I = 0.4 V			-0.2	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7 V			20	μA
I_I	Maximum input current		V_{CC} = MAX	V_I = 7 V			0.1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OL} = 12 mA			0.4	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.5 V, V_{IH} = 2 V	I_{OH} = -3 mA	2.4	3.4		V
				I_{OH} = -12 mA	2.0			
I_{OZL}	Off-state output current		V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2 V	V_O = 0.4 V			-20	μA
I_{OZH}				V_O = 2.7 V			20	μA
I_{OS}	Output short-circuit current*		V_{CC} = MAX		-40		-225	mA
I_{CC}	Supply Current	Outputs High	V_{CC} = MAX, Outputs open	'LS240		17	27	mA
				'LS241, 'LS244		17	27	
		Outputs Low		'LS240		26	44	
				'LS241, 'LS244		27	46	
		Outputs Disabled		'LS240		29	50	
				'LS241, 'LS244		32	54	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	'LS240 MIN	'LS240 TYP	'LS240 MAX	'LS241, 'LS244 MIN	'LS241, 'LS244 TYP	'LS241, 'LS244 MAX	UNIT
t_{PLH}	Data to output delay	C_L = 45 pF R_L = 667 Ω		9	14		12	18	ns
t_{PHL}				12	18		12	18	ns
t_{PZL}	Output enable delay			20	30		20	30	ns
t_{PZH}				15	23		15	23	ns
t_{PZL}	Output disable delay	C_L = 5 pF R_L = 667 Ω		15	25		15	25	ns
t_{PHZ}				10	18		10	18	ns

12

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
T_A	Operating free-air temperature	-55		125	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2.0			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = -18 mA			-1.2	V
ΔV_T	Hysteresis (V_{T+}-V_{T-})		V_{CC} = MIN		0.2	0.4		V
I_{IL}	Low-level input current	Any A	V_{CC} = MAX	V_I = 0.5 V			-0.4	mA
		Any E					-2	
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7 V			50	μA
I_I	Maximum input current		V_{CC} = MAX	V_I = 5.5 V			1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V, V_{IH} = 2 V	I_{OL} = 48 mA			0.55	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V, V_{IH} = 2 V	I_{OH} = -3 mA	2.4	3.4		V
				I_{OH} = -12 mA	2.0			
I_{OZL}	Off-state output current		V_{CC} = MAX, V_{IL} = 0.8 V, V_{IH} = 2 V	V_O = 0.5 V			-50	μA
I_{OZH}				V_O = 2.4 V			50	μA
I_{OS}	Output short-circuit current†		V_{CC} = MAX		-50		-225	mA
I_{CC}	Supply Current	Outputs High	V_{CC} = MAX, Outputs open	'S240		80	123	mA
				'S241, 'S244		95	147	
		Outputs Low		'S240		100	145	
				'S241, 'S244		120	170	
		Outputs Disabled		'S240		100	145	
				'S241, 'S244		120	170	

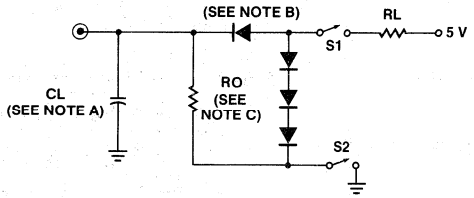
† Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	'S240 MIN	'S240 TYP	'S240 MAX	'S241, 'S244 MIN	'S241, 'S244 TYP	'S241, 'S244 MAX	UNIT
t_{PLH}	Data to output delay	C_L = 50 pF R_L = 90 Ω		4.5	7		6	9	ns
t_{PHL}				4.5	7		6	9	ns
t_{PZL}	Output enable delay			10	15		10	15	ns
t_{PZH}				6.5	10*		8	12	ns
t_{PZL}	Output disable delay	C_L = 5 pF R_L = 90 Ω		10	15		10	15	ns
t_{PHZ}				6	9		6	9	ns

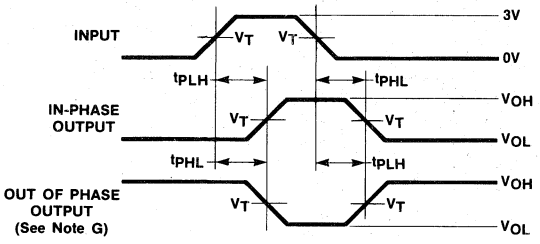
* For the S210 add 2 ns for the E_2 (Pin 19) enable.

Test Load

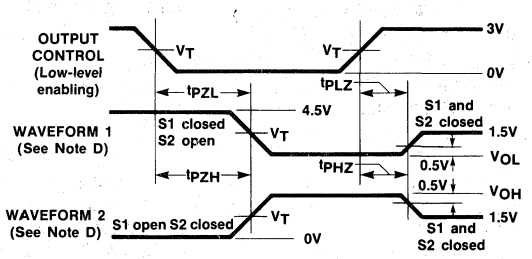


* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Test Waveforms



Propagation Delay



Enable and Disable

Notes: A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. For Series 54S, R_O = 1 K, V_T = 1.5 V.
For Series 54LS, R_O = 5 K, V_T = 1.3 V.
D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz. Z_{OUT} = 50 Ω and:
For series 54S, $t_R \leq 2.5$ ns, $t_F \leq 2.5$ ns.
For Series 54LS and PAL devices, $t_R \leq 15$ ns, $t_F \leq 6$ ns.
G. When measuring propagation delay times of three-state outputs, switches S1 and S2 are closed.

12

8-Bit Buffers with Schmitt Trigger Inputs

SN54/74LS310 SN54/74S310 SN54/74LS340 SN54/74S340 SN54/74LS341 SN54/74S341 SN54/74LS344 SN54/74S344

Features

- Schmitt-trigger inputs guarantee high noise margin
- Three-state outputs drive bus lines
- Typical input and output capacitance ≤10 pf
- Low-current PNP inputs reduce loading
- 20-pin SKINNYDIP® saves space
- 8-bit data path matches byte boundaries
- Ideal for microprocessor interface
- Complementary-enable '310 and '341 types combine multiplexer and driver functions
- Pin-compatible with SN54/74S210/240/1/4 and SN54/74LS210/240/1/4; can be direct replacement in systems with noise problems

Description

In addition to the standard Schottky and low-power Schottky 8-bit buffers, Monolithic Memories provides full hysteresis with a "true" Schmitt-trigger circuit. The improved performance characteristics are designed (1) for the low-power Schottky buffers, to be consistent with the SN54/74LS14 hex Schmitt-trigger inverter, and to guarantee a full 400 mV noise immunity; (2) for the Schottky buffers, to have low propagation delays, and to guarantee a full 500 mV noise immunity. The Schmitt-trigger operation makes these LS/S buffers ideal for bus receivers in a noisy environment.

These 8-bit buffers provide high-speed and high-current interface capability for bus-organized digital systems. The three-state drivers will source a termination to ground (up to 133Ω) or sink a pull-up to V_{CC} as in the popular 220Ω/330Ω computer peripheral termination. The PNP inputs provide improved fan-in with 0.2 mA I_{IL} for the low-power Schottky buffers and 0.25 mA I_{IL} for the Schottky buffers.

The '340 and '344 provide inverting and non-inverting outputs respectively, with assertive-low enables. The '310 and '341 also provide inverting and non-inverting outputs respectively, but with complementary (both assertive-low and assertive-high) enables, to allow transceiver or multiplexer operation.

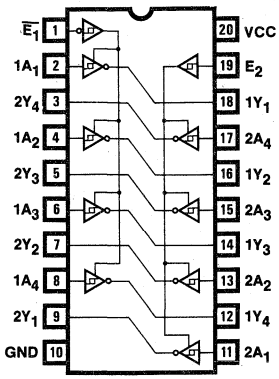
All of the 8-bit devices are packaged in the popular 20-pin SKINNYDIP®.

Ordering Information

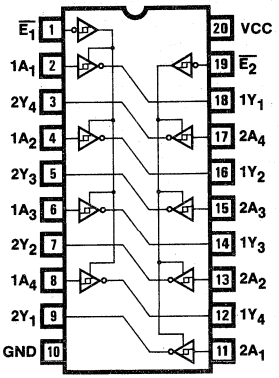
PART NUMBER	PKG*	TEMP	ENABLE	POLARITY	POWER
SN54LS310	J,F	mil	High-Low	Invert	LS
SN74LS310	N,J	com			
SN54LS340	J,F	mil	Low		
SN74LS340	N,J	com			
SN54LS341	J,F	mil	High-Low	Non-Invert	
SN74LS341	N,J	com			
SN54LS344	J,F	mil	Low		
SN74LS344	N,J	com			
SN54S310	J,F	mil	High-Low	Invert	S
SN74S310	N,J	com			
SN54S340	J,F	mil	Low		
SN74S340	N,J	com			
SN54S341	J,F	mil	High-Low	Non-Invert	
SN74S341	N,J	com			
SN54S344	J,F	mil	Low		
SN74S344	N,J	com			

Logic Symbols

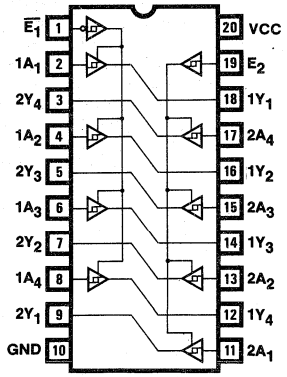
'310 8-Bit Buffer



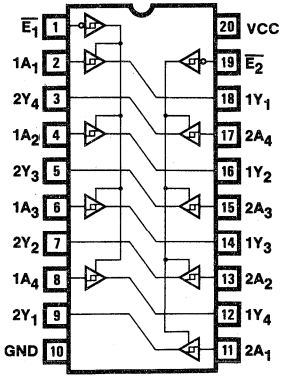
'340 8-Bit Buffer



'341 8-Bit Buffer



'344 8-Bit Buffer



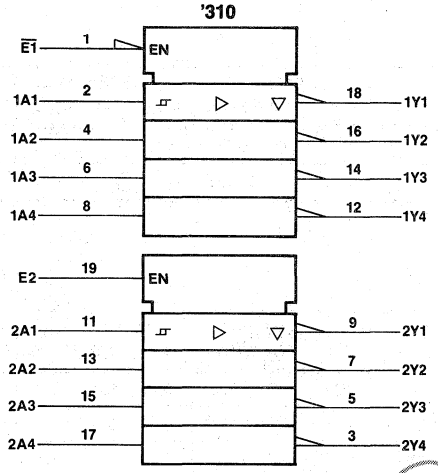
*For other package types, please contact your local sales representative.

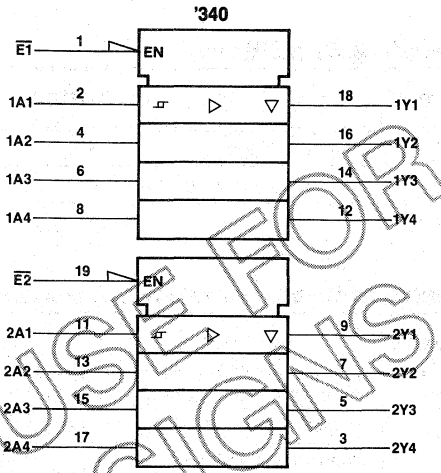
SKINNYDIP® is a registered trademark of Monolithic Memories.

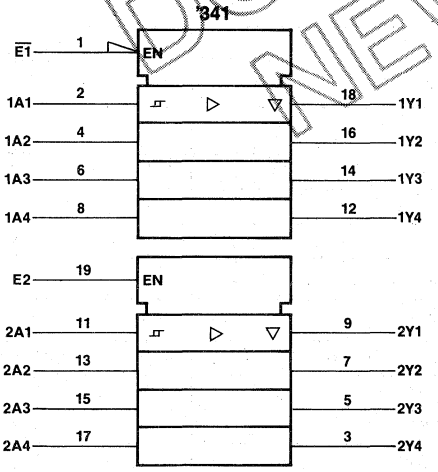
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

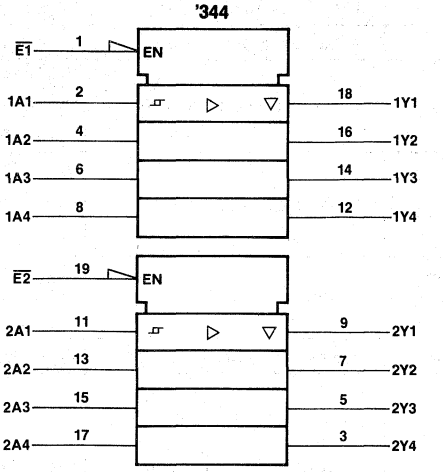
Monolithic Memories MMI

IEEE Symbols









12

Absolute Maximum Ratings

Supply voltage V_{CC} ..... 7 V
Input voltage ..... 7 V
Off-state output voltage ..... 5.5 V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{T+}	Positive threshold voltage		Any A*		1.5	1.7	2.0	1.5	1.7	2.0	V
V_{T-}	Negative threshold voltage		Any A*		0.6	0.9	1.1	0.6	0.9	1.1	V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18 mA			−1.5			−1.5	V
ΔV_T	Hysteresis (V_{T+}−V_{T-})		Any A*		0.4	0.8		0.4	0.8		V
ΔV_{DB}	Dead band voltage		Any A*		0.4			0.4			V
V_{IL}	Input low voltage		Any E*				0.8			0.8	V
V_{IH}	Input high voltage		Any E*		2.0			2.0			V
I_{IL}	Low-level input current		V_{CC} = MAX	V_I = 0.4 V			−0.2			−0.2	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7 V			20				μA
I_I	Maximum input current		V_{CC} = MAX	V_I = 7 V			0.1			0.1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{T+} = 2 V, V_{T-} = 0.6 V	I_{OL} = 12 mA			0.4			0.4	V
				I_{OL} = 24 mA						0.5	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{T+} = 2 V, V_{T-} = 0.6 V	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
				I_{OH} = −12 mA	2						
				I_{OH} = −15 mA				2			
I_{OZL}	Off-state output current		V_{CC} = MAX, V_{T+} = 2 V, V_{T-} = 0.6 V	V_O = 0.4 V			−20			−20	μA
I_{OZH}				V_O = 2.7 V			20			20	μA
I_{OS}	Output short-circuit current**		V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply Current	Outputs High	V_{CC} = MAX, Outputs open	'LS310,'LS340		17	27		17	27	mA
				'LS341, 'LS344		18	35		18	35	
		Outputs Low		'LS310, 'LS340		26	44		26	44	
				'LS341, 'LS344		32	46		32	46	
		Outputs Disabled		'LS310, 'LS340		29	50		29	50	
				'LS341, 'LS344		34	54		34	54	

** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

* "A" indicates data input, "E" indicates enable input.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	'LS310, 'LS340 MIN	TYP	MAX	'LS341, 'LS344 MIN	TYP	MAX	UNIT
t_{PLH}	Data to Output delay	C_L = 45 pF R_L = 667 Ω		19	25		19	25	ns
t_{PHL}				19	25		19	25	ns
t_{PZL}	Output Enable delay			32	40		25	40	ns
t_{PZH}				23	35		24	35	ns
t_{PLZ}	Output Disable delay	C_L = 5 pF R_L = 667 Ω		18	30		21	30	ns
t_{PHZ}				15	25		18	25	ns

Absolute Maximum Ratings

Supply voltage V_{CC} ..... 7.0 V
Input voltage ..... 5.5 V
Off-state output voltage ..... 5.5 V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{T+}	Positive threshold voltage		Any A*		1.5	1.8	2.05	1.6	1.8	2.0	V
V_{T-}	Negative threshold voltage		Any A*		0.8	1.1	1.35	0.8	1.1	1.3	V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18 mA			−1.2			−1.2	V
ΔV_T	Hysteresis (V_{T+}−V_{T-})		Any A*		0.5	0.7		0.5	0.7		V
ΔV_{DB}	Dead band voltage		Any A*		0.15			0.3			V
V_{IL}	Input low voltage		Any E*				0.8			0.8	V
V_{IH}	Input high voltage		Any E*		2.0			2.0			V
I_{IL}	Low-level input current		V_{CC} = MAX	V_I = 0.5 V			−0.25			−0.25	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7 V			50			50	μA
I_I	Maximum input current		V_{CC} = MAX	V_I = 5.5 V			1			1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{T+} = 2 V, V_{T-} = 0.8 V	I_{OL} = 48 mA			0.55				V
				I_{OL} = 64 mA						0.55	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{T+} = 2 V, V_{T-} = 0.8 V	I_{OH} = −1 mA				2.7			V
				I_{OH} = −3 mA	2.4	3.4		2.4	3.4		
				I_{OH} = −12 mA	2						
				I_{OH} = −15 mA				2			
I_{OZL}	Off-state output current		V_{CC} = MAX, V_{IH} = 2.0 V, V_{IL} = 0.8 V	V_O = 0.5 V			−50			−50	μA
I_{OZH}				V_O = 2.7 V			50			50	μA
I_{OS}	Output short-circuit current**		V_{CC} = MAX		−50		−225	−50		−225	mA
I_{CC}	Supply Current	Outputs High	V_{CC} = MAX, Outputs open	'S310,'S340		50	80		50	80	mA
				'S341, 'S344		80	130		80	130	
		Outputs Low		'S310, 'S340		110	155		100	155	
				'S341, 'S344		130	180		130	185	
		Outputs Disabled		'S310, 'S340		135	180		135	180	
				'S341, 'S344		155	180		150	200	

** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

* "A" indicates data input, "E" indicates enable input.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	'S310, 'S340 MIN	TYP	MAX	'S341, 'S344 MIN	TYP	MAX	UNIT
t_{PLH}	Data to Output delay	C_L = 50 pF R_L = 90Ω		11	15		16	22	ns
t_{PHL}				16	22		10	15	ns
t_{PZL}	Output Enable delay			8	15		10	15	ns
t_{PZH}				6	12		7	12	ns
t_{PLZ}	Output Disable delay	C_L = 5 pF R_L = 90Ω		10	15		10	15	ns
t_{PHZ}				7	12		7	12	ns

Function Tables

'310

$\overline{E_1}$	E_2	1Y OUTPUTS	2Y OUTPUTS
H	H	Z	Enabled (Inverting)
H	L	Z	Z
L	H	Enabled (Inverting)	Enabled (Inverting)
L	L	Enabled (Inverting)	Z

'340

$\overline{E_1}$	$\overline{E_2}$	1Y OUTPUTS	2Y OUTPUTS
H	H	Z	Z
H	L	Z	Enabled (Inverting)
L	H	Enabled (Inverting)	Z
L	L	Enabled (Inverting)	Enabled (Inverting)

'341

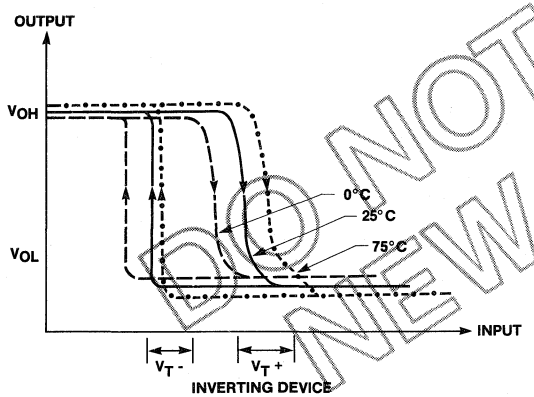
$\overline{E_1}$	E_2	1Y OUTPUTS	2Y OUTPUTS
H	H	Z	Enabled
H	L	Z	Z
L	H	Enabled	Enabled
L	L	Enabled	Z

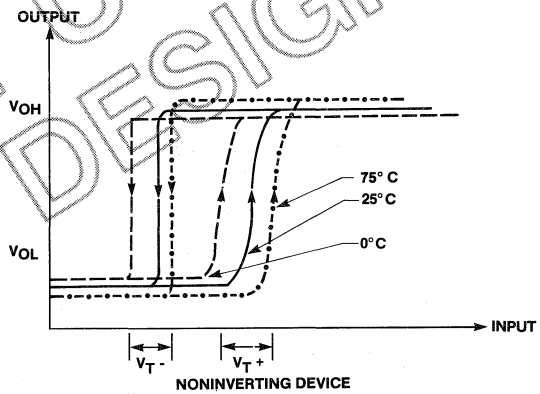
'344

$\overline{E_1}$	$\overline{E_2}$	1Y OUTPUTS	2Y OUTPUTS
H	H	Z	Z
H	L	Z	Enabled
L	H	Enabled	Z
L	L	Enabled	Enabled

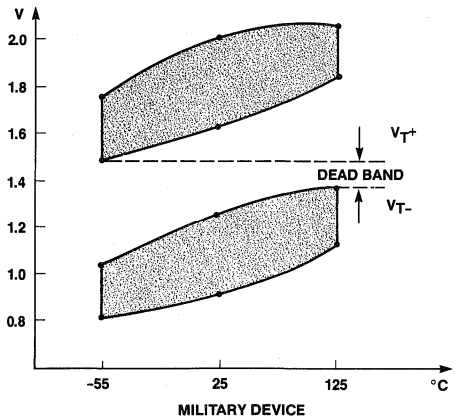
Z ≡ High impedance (output off).

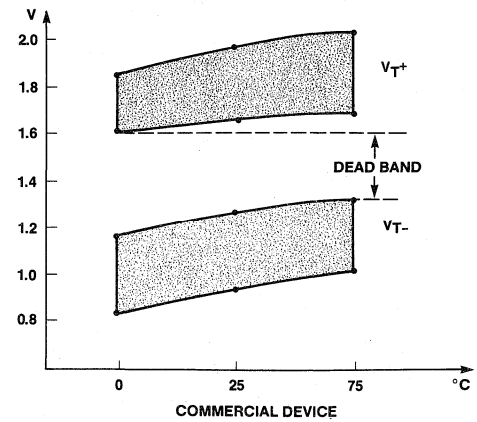
INPUT VS OUTPUT VOLTAGE TRANSFER CHARACTERISTIC





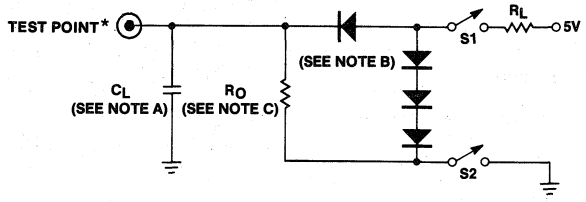
THRESHOLD VOLTAGE VS OPERATING TEMPERATURE





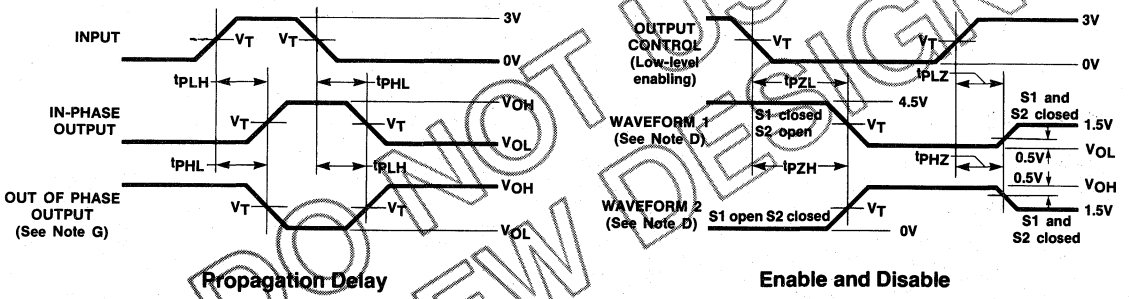
* Dead Band: The hysteresis is guaranteed at any operating temperature and voltage.

Test Load



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Test Waveforms



Propagation Delay

Enable and Disable

NOTES: A. C_L includes probe and jig capacitance.

B. All diodes are 1N916 or 1N3064.

C. For Series 54/74S310/340/341/344 R_O = 5K, $V_T = V_{T+}$ = 1.8 V for low-to-high input transition.
For Series 54/74S310/340/341/344 R_O = 5K, $V_T = V_{T-}$ = 1.1 V for high-to-low input transition.
For Series 54/74LS310/340/341/344 R_O = 5K, $V_T = V_{T+}$ = 1.7 V for low-to-high input transition.
For Series 54/74L310/340/341/344 R_O = 5K, $V_T = V_{T-}$ = 0.9 V for high-to-low input transition.

D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{OUT} = 50Ω and:
For Series 54/74S, $t_R \leq 2.5$ ns, $t_F \leq 2.5$ ns.
For Series 54/74LS and PALs, $t_R \leq 15$ ns. $t_F \leq 6$ ns.

G. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed. (Propagation delays are measured from the inputs crossing V_{T+}, V_{T-} to the outputs crossing V_T)

12

8-Bit Buffer Transceiver

SN54/74LS245

FOR MORE DETAIL SEE SECTION 13

Features/Benefits

- Three-state outputs drive bus lines
- Low current PNP inputs reduce loading
- Symmetric -- equal driving capability in each direction
- 20-pin SKINNYDIP® saves space
- 8-bit data path matches byte boundaries
- Ideal for microprocessor interface
- Pin-compatible with SN54/74LS645 -- improved speed, I_{IL} and I_{OZL} specifications

Ordering Information

PART NUMBER	TYPE	TEMP	POLARITY	POWER
SN54LS245	J,L,W	Mil	Non-invert	LS
SN74LS245	N,J	Com		

Description

These 8-bit bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

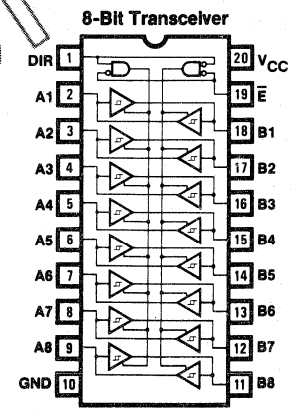
The device allows data transmission from the A bus to the B bus, or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{E}$) can be used to disable the device, so that the buses are affectively isolated.

All of the 8-bit devices are packaged in the popular 20-pin SKINNYDIP.

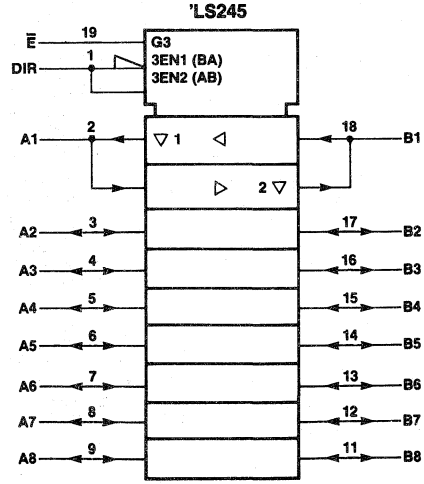
Function Table

ENABLE $\overline{E}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolated

Logic Symbol



IEEE Symbol



SKINNYDIP® is a registered trademark of Monolithic Memories.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374
Monolithic Memories

8-Bit Buffer Transceiver

SN54/74LS645 SN74LS645-1

FOR MORE DETAIL SEE SECTION 13

Features/Benefits

- Three-state outputs drive bus lines
- Low current PNP inputs reduce loading
- Symmetric — equal driving capability in each direction
- 20-pin SKINNYDIP® saves space
- 8-bit data path matches byte boundaries
- Ideal for microprocessor interface
- SN74LS645-1 rated at I_{OL} = 48 mA

Ordering Information

PART NUMBER	TYPE	TEMP	POLARITY	POWER
SN54LS645	J,L,W	Mil	Non-invert	LS
SN74LS645	N,J	Com		
SN74LS645-1	J	Com		

Description

These 8-bit bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{E}$) can be used to disable the device so that the buses are effectively isolated.

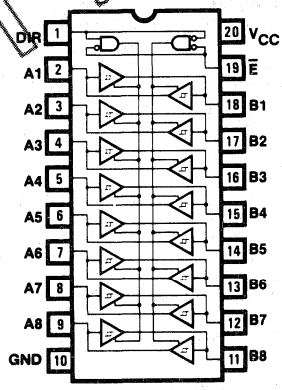
All of the 8-bit devices are packaged in the popular 20-pin SKINNYDIP.

Function Table

ENABLE $\overline{E}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolated

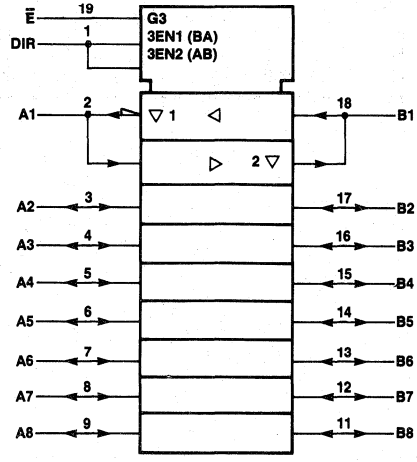
Logic Symbol

8-Bit Transceiver



IEEE Symbol

'LS645/645-1



12

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374
Monolithic Memories

8-Bit Registers with Master Reset or Clock Enable

SN54LS273

Features/Benefits

- 8-bit data path matches byte boundaries
- Ideal for microprogram instruction registers
- Ideal for microprogram interface
- Suitable for pipeline data registers
- Useful in timing, sequencing, and control circuits
- Three '273s may replace four '174s

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	CONTROL OPTION	POWER
SN54LS273	J,L,W	Mil	Non-Invert	Master Reset	LS

Description

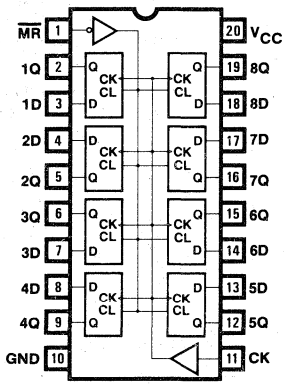
These 8-bit registers contain eight D-type flip-flops, they feature very low I_{CC} (17 mA typical) on the low-power Schottky devices and very-high-speed operation on the Schottky devices. The '273 register is loaded on the rising edge of the clock (CK) and asynchronously cleared whenever the master reset line, $\overline{MR}$, is low.

Function Table

INPUTS			OUTPUT
$\overline{MR}$	CLOCK	DATA	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L or H or ↓	X	Q_0

Logic Symbols

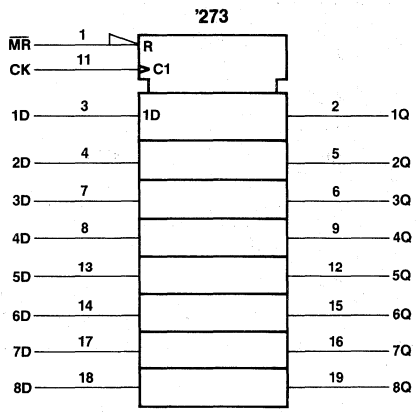
8-Bit Register with Master Reset '273



Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 5.5 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature range ..... -65°C to +150°C

IEEE Symbols



12

Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface, Test Load/Waveforms)	FIGURE	MILITARY MIN	MILITARY TYP	MILITARY MAX	UNIT
V_{CC}	Supply voltage			4.5	5	5.5	V
T_A	Operating free-air temperature			-55		125	°C
t_W	Width of clock	High-t_{WH}	1	20			ns
		Low-t_{WL}					
t_{WMR}	Width of Master Reset	Low-t_{WMRL}	2	20			ns
t_{rec}		$\overline{MR}$ to CK	2	25 ↑			ns
t_{su}	Setup time	Data input to CK	3	20 ↑			ns
			4	25 ↑			
				10 ↑			
t_h	Hold time	Data input	3	5 ↑			ns
			4	5 ↑			
				5 ↑			

↑↓ The arrow indicates the transition of the clock/enable input used for reference. ↑ for the low-to-high transition. ↓ for the high-to-low transition.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	UNIT
V_{IL}	Low-level input voltage					0.7	V
V_{IH}	High-level input voltage			2.0			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA			−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			−0.4	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7 V			20	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 7 V			0.1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OL} = 4 mA		0.25	0.4	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OH} = −400μA	2.5	3.4		V
I_{OS}	Output short-circuit current*	V_{CC} = MAX		−20		−100	mA
I_{CC}	Supply current †	V_{CC} = MAX, Outputs open	'LS273		17	27	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† I_{CC} is measured after first a momentary ground, and then 4.5 V is applied to clock, while the following other input conditions are held: For the 'LS273—4.5 V on all data and master-reset inputs.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	'LS273 MIN	'LS273 TYP	'LS273 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 15 pF R_L = 2 KΩ	30	40		MHz
t_{PLH}	Clock to Output delay				27	ns
t_{PHL}					27	ns
t_{PHL}	Master Reset to output delay				27	ns

CLOCK PULSE WIDTH AND CLOCK TO OUTPUT DELAYS

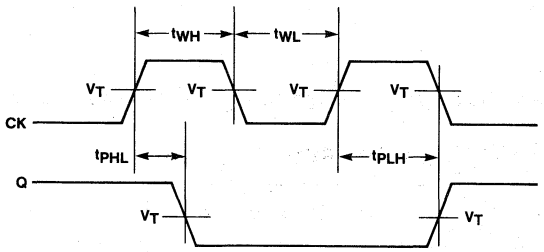


Figure 1

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME FOR 'S273

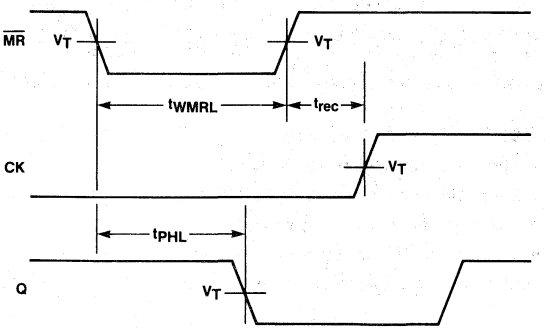


Figure 2

DATA SET-UP AND HOLD TIMES

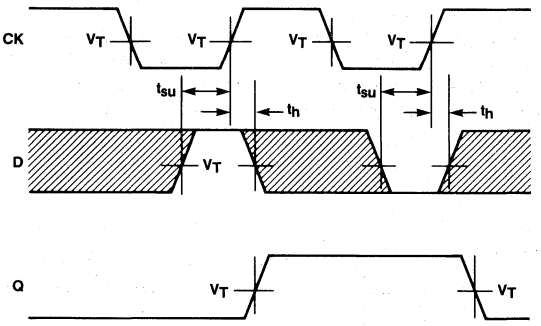
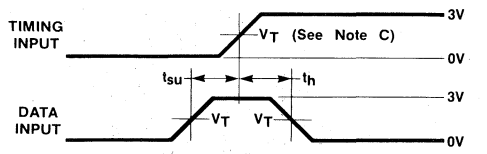


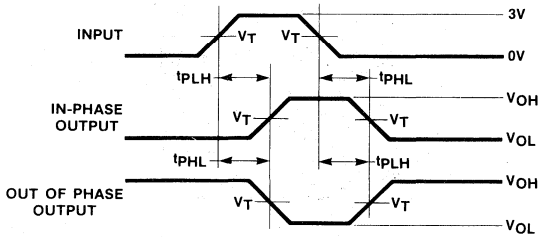
Figure 3

12

Test Waveforms

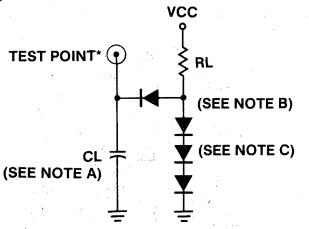


SETUP AND HOLD



PROPAGATION DELAY

Test Load



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS

Notes: A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. For Series 54LS, V_T = 1.3 V.
D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz. Z_{OUT} = 50 Ω.

8- Bit Latches, 8-Bit Registers

SN54LS373 SN54S373
SN54LS374 SN54S374

Features/Benefits

- Three-state outputs drive bus lines
- 8-bit data path matches byte boundaries
- Hysteresis improves noise margin
- Low current PNP inputs reduce loading
- Ideal for microprocessor interface

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	POWER
SN54LS373	J,L,W	Mil	Non-invert	Latch	LS
SN54LS374				Register	
SN54S373				Latch	S
SN54S374				Register	

Description

The latch passes eight bits of data from the inputs (D) to the outputs (Q) when the gate (G) is high. The data is "latched" when the gate (G) goes low. The register loads eight bits of input data and passes it to output on the "rising edge" of the clock.

The three-state outputs are active when $\overline{OE}$ is low, and high-impedance when $\overline{OE}$ is high. Schmitt-trigger buffers at the gate/clock inputs improve system noise margin by providing typically 400 mV of hysteresis.

Function Tables

'373 8-Bit Latch

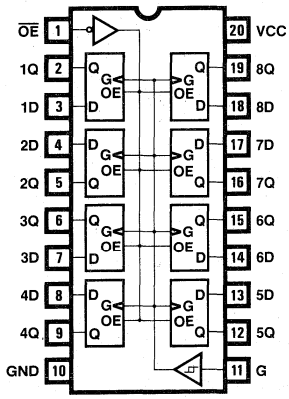
$\overline{OE}$	G	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

'374 8-Bit Register

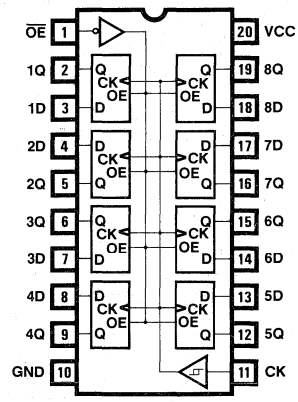
$\overline{OE}$	CK	D	Q
L	↑	H	H
L	↑	L	L
L	L or H or ↓	X	Q_0
H	X	X	Z

Logic Symbols

'373 8-Bit Latch



'374 8-Bit Register



Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
T_A	Operating free-air temperature		-55		125	°C
t_w	Width of Clock/Gate	High	15			ns
		Low	15			
t_{su}	Setup time	'LS373	5↓			ns
		'LS374	20↑			
t_h	Hold time	'LS373	20↓			ns
		'LS374	0↑			

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	UNIT
V_{IL}	Low-level input voltage					0.7	V
V_{IH}	High-level input voltage			2.0			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA			-1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			-0.4	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7 V			20	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 7 V			0.1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OL} = 12 mA		0.25	0.4	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OH} = -1 mA	2.4	3.4		V
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2 V	V_O = 0.4 V			-20	μA
I_{OZH}			V_O = 2.7 V			20	μA
I_{OS}	Output short-circuit current*	V_{CC} = MAX		-30		-130	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	'LS373		24	40	mA
			'LS374		27	40	

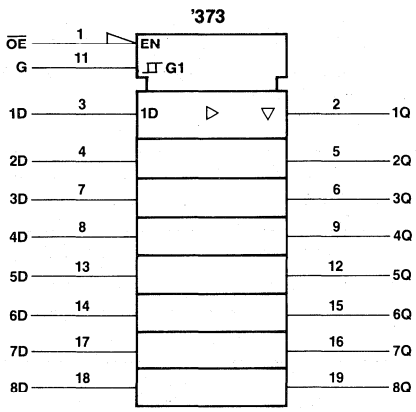
* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

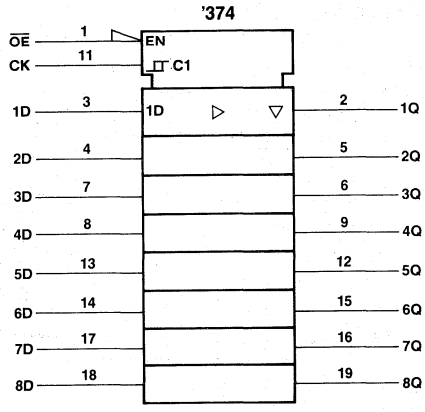
Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	'LS373 MIN	'LS373 TYP	'LS373 MAX	'LS374 MIN	'LS374 TYP	'LS374 MAX	UNIT
f_{MAX}	Maximum clock frequency	C_L = 45 pF R_L = 667 Ω				35	50		MHz
t_{PLH}	Data to output delay			12	18				ns
t_{PHL}				12	18				ns
t_{PLH}	Clock/Gate to output delay			20	30		15	28	ns
t_{PHL}				18	30		19	28	ns
t_{PZL}	Output enable delay			25	36		21	28	ns
t_{PZH}				15	28		20	28	ns
t_{PLZ}	Output disable delay	C_L = 5 pF R_L = 667 Ω		15	25		14	25	ns
t_{PHZ}				12	20		12	20	ns

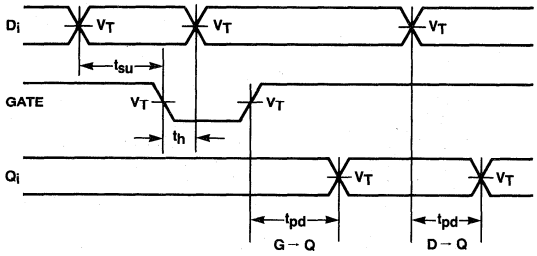
12

IEEE Symbols

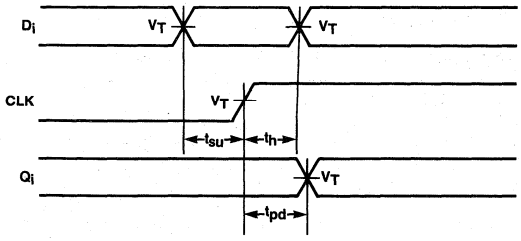




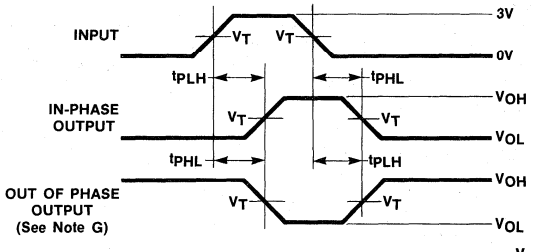
'373 Timing Diagrams



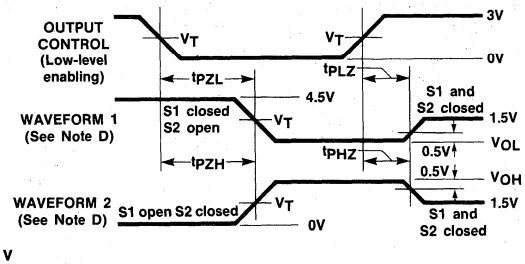
'374 Timing Diagrams



Test Waveforms



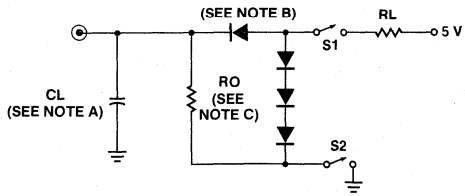
Propagation Delay



Enable and Disable

Notes: A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. For Series 54S, R_O = 1 K, V_T = 1.5 V.
For Series 54LS, R_O = 5 K, V_T = 1.3 V.
D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz. Z_{OUT} = 50 Ω and:
For series 54S, $t_R \leq 2.5$ ns, $t_F \leq 2.5$ ns.
For Series 54LS and PAL devices, $t_R \leq 15$ ns, $t_F \leq 6$ ns.
G. When measuring propagation delay times of three-state outputs, switches S1 and S2 are closed.

Standard Test Load



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
T_A	Operating free-air temperature		-55		125	°C
t_w	Width of Clock/Gate	High	6			ns
		Low	7.3			
t_{su}	Setup time	'S373	0↓			ns
		'S374	5↑			
t_h	Hold time	'S373	10↓			ns
		'S374	2↑			

↑↓ The arrow indicates the transition of the clock input used for reference. ↑ for the low-to-high transition, ↓ for the high-to-low transition.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2.0			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA			-1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.5 V			-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7 V			50	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, V_{IH} = 2 V	I_{OL} = 20 mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, V_{IH} = 2 V	I_{OH} = -2 mA	2.4	3.4		V
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8 V, V_{IH} = 2 V	V_O = 0.5 V			-50	μA
I_{OZH}			V_O = 2.4 V			50	μA
I_{OS}	Output short-circuit current*	V_{CC} = MAX		-40		-100	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	'S373		105	160	mA
			'S374		90	140	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	'S373 MIN	'S373 TYP	'S373 MAX	'S374 MIN	'S374 TYP	'S374 MAX	UNIT
f_{MAX}	Maximum clock frequency	C_L = 15 pF R_L = 280 Ω				75	100		MHz
t_{PLH}	Data to output delay			7	12				ns
t_{PHL}				7	12				ns
t_{PLH}	Clock/Gate to output delay			7	14		8	15	ns
t_{PHL}				12	18		11	17	ns
t_{PZL}	Output enable delay			11	18		11	18	ns
t_{PZH}				8	15		8	15	ns
t_{PLZ}	Output disable delay	C_L = 5 pF R_L = 280 Ω		8	12		7	12	ns
t_{PHZ}				6	9		5	9	ns

8-Bit Register With Clock Enable and Open-Collector Outputs
SN54/74S383

Features

- 20-Pin SKINNYDIP® Saves Space
- 8-bit data path matches byte boundaries
- Only available TTL open-collector-output register
- Ideal for certain microprocessor system buses
- Suitable for pipeline data registers
- Excellent for multiple, physically-separated connections to buses in microprocessor-based systems
- Wired-OR or wired-AND logic with outputs

Description

This 8-bit register contains 8 D-type flip-flops and features very fast switching. The 'S383 register is loaded on the rising edge of the clock provided that the clock enable line, $\overline{CK\ EN}$, is low. Like other 8-bit interface devices, the 'S383 is packaged in the popular 20-pin SKINNYDIP.

Ordering Information

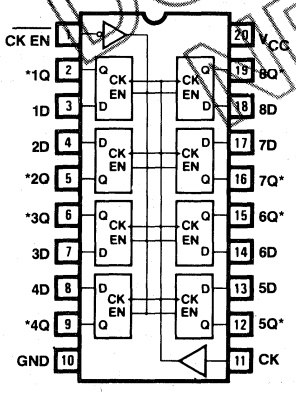
PART NUMBER	PKG	TEMP	POLARITY	CONTROL OPTIONS	POWER
SN54S383	J,L,W	Mil	Non-invert	Clock Enable	S
SN74S383	N,J	Com			

Function Table 'S383

INPUTS			OUTPUT
$\overline{CK\ EN}$	CLOCK	DATA	Q
H	X	X	Q_0
L	↑	H	H
L	↑	L	L
X	L or H or ↓	X	Q_0

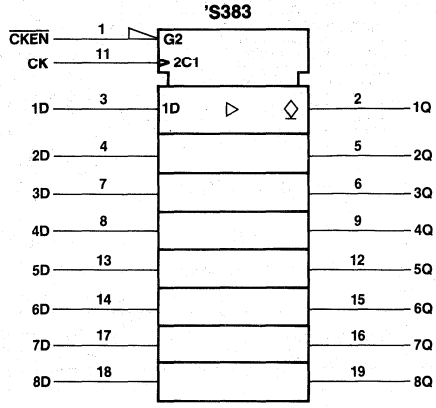
Logic Symbol

8-Bit Register with Clock Enable and Open-Collector Outputs
'S383



*Indicates Open-Collector Output

IEEE Symbol



12

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories MMI

Absolute Maximum Ratings

Supply voltage V_{CC} ..... 7.0 V
Input voltage ..... 5.5 V
Off-state output voltage ..... 5.5 V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface, Test Load/Waveforms)	FIGURE	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage			4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature			−55		125	0		75	°C
t_W	Width of clock	High-t_{WH}	1	7			7			ns
		Low-t_{WL}								
t_{su}	Setup time	Data input to CK	2	5 ↑			5 ↑			ns
		Low $\overline{CK\ EN}$ to CK		9 ↓			9 ↓			
		High $\overline{CK\ EN}$ to CK		9 ↑			9 ↑			
t_h	Hold time	Data input	2	3 ↑			3 ↑			ns
		Low $\overline{CK\ EN}$ to CK		3 ↓			3 ↓			
		High $\overline{CK\ EN}$ to CK		0 ↑			0 ↑			

↑↓ The arrow indicates the transition of the clock/enable input used for reference: ↑ for the low-to-high transition, ↓ for the high-to-low transition.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IH}	High-level input voltage			2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−1.2			−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.5V			-250			-250	μA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7V			50			50	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OL} = 24mA			0.5			0.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	V_{OH} = 5.5 V			250			250	μA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	Outputs HIGH			160			160	mA
			Outputs LOW			160			160	

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	'S383 MIN	'S383 TYP	'S383 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 15 pF R_L = 280Ω	75	110		MHz
t_{PLH}	Clock to output delay			10	17	ns
t_{PHL}				14	22	ns

Test Waveforms

CLOCK PULSE WIDTH AND
CLOCK TO OUTPUT DELAYS

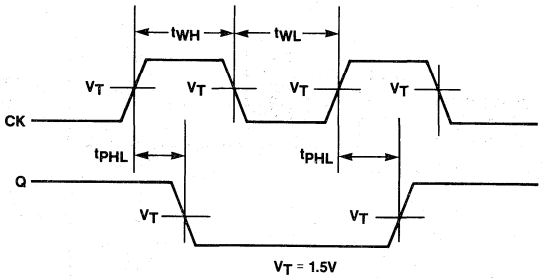


Figure 1

DATA AND CLOCK ENABLE
SETUP AND HOLD TIMES

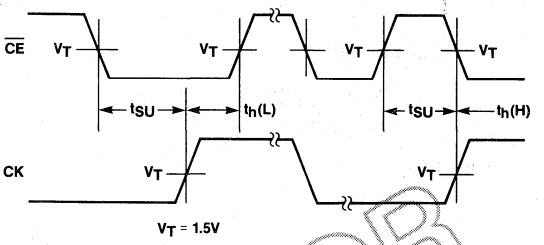
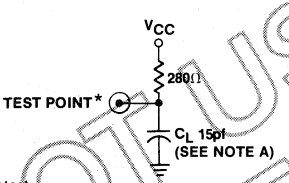


Figure 2

Test Load



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

LOAD CIRCUIT FOR
OPEN-COLLECTOR OUTPUTS

A. Includes probe and jig capacitance.

B. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤1 MHz, Z_{out} = 50Ω and:
For Series 54/74S, t_R ≤2.5 ns, t_F ≤2.5 ns.

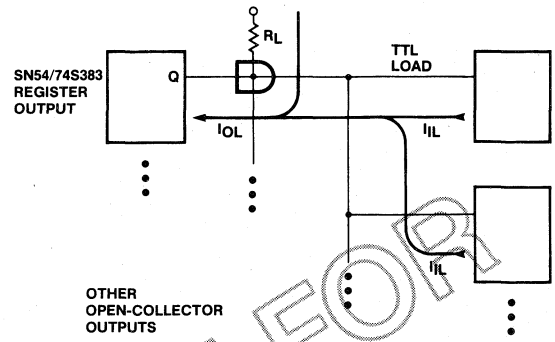
12

Open Collector Bus Application Information For Determination of R_L For Wired-And Applications

1. **CALCULATE R_L(Min):**

$$R_L(\text{Min}) = \frac{V_{CC} - V_{OL}(\text{Max})}{I_{OL} - (\text{TOTAL } I_{IL})}$$

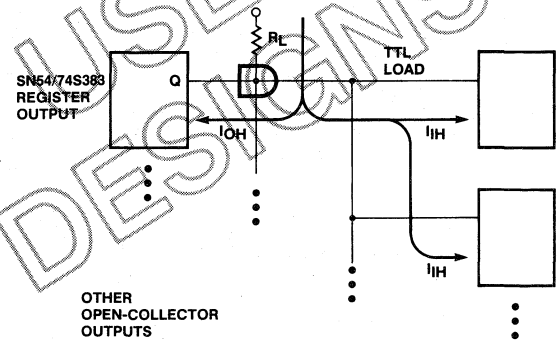
where I_{OL} = 24 mA at
V_{OL}(Max) = 0.5 V



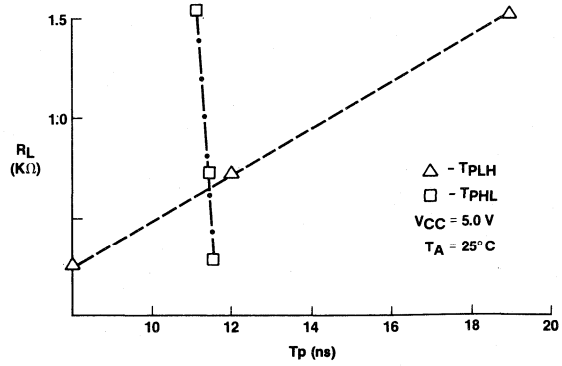
2. **CALCULATE R_L(Max):**

$$R_L(\text{Max}) = \frac{V_{CC} - V_{OH}(\text{Min})}{(\text{TOTAL } I_{OH} + \text{TOTAL } I_{IH})}$$

where I_{OH} = 250 μA at
V_{OH}(Min) = 2.5V



3. **SELECT** a value for R_L in the range of R_L(Min) to R_L(Max), based on power consumption and speed requirements:



RL vs. Tp FOR SN54/74S383

8-Bit Latches, 8-Bit Registers with Inverting Outputs

SN54/74LS533 SN54/74S533
SN54/74LS534 SN54/74S534

Features/Benefits

- Inverting outputs
- Three-state outputs drive bus lines
- 20-pin SKINNYDIP® saves space
- 8-bit data path matches byte boundaries
- Hysteresis improves noise margin
- Low current PNP inputs reduce loading
- Ideal for microprocessor interface
- Pin-compatible with SN54/74LS373/4 or SN54/74S373/4 — can be direct replacement when bus polarity must be changed

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	POWER
54LS533 74LS533	J,W,L N,J	Mil Com	Invert	Latch	LS
54LS534 74LS534	J,W,L N,J	Mil Com		Register	
54S533 74S533	J,W,L N,J	Mil Com		Latch	S
54S534 74S534	J,W,L N,J	Mil Com		Register	

Description

In addition to the standard S and LS latches and registers, Monolithic Memories provides inverting outputs instead of non-inverting outputs. The inverting outputs are intended for bus applications that require inversion as in interfacing the Am2901A 4-bit slice to an assertive-low bus.

The latch passes eight bits of data from the inputs (D) to the outputs (Q) when the gate (G) is high. The data is "latched" when the gate (G) goes low. The register loads eight bits of input data and passes it to the output on the "rising edge" of the clock.

The three-state outputs are active when $\overline{OE}$ is low, and high-impedance when $\overline{OE}$ is high. Schmitt-trigger buffers at the gate/clock inputs improve system noise margin by providing typically 400 mV of hysteresis.

All of the 8-bit devices are packaged in the popular 20-pin SKINNYDIP.

Function Tables

'533 8-Bit Latch (Inverting)

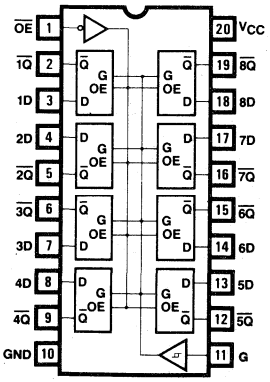
$\overline{OE}$	G	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

'534 8-Bit Register (Inverting)

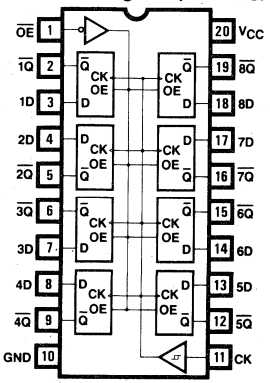
$\overline{OE}$	CK	D	$\overline{Q}$
L	↑	H	H
L	↑	L	L
L	L or H or ↓	X	Q_0
H	X	X	Z

Logic Symbols

'533 8-Bit Latch (Inverting)



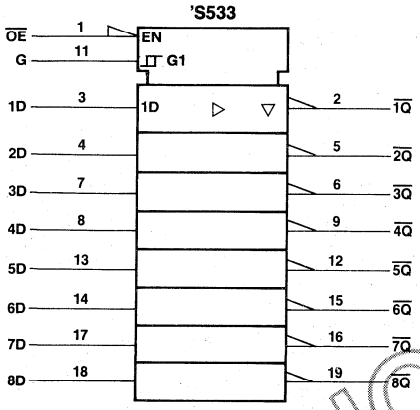
'533 8-Bit Register (Inverting)

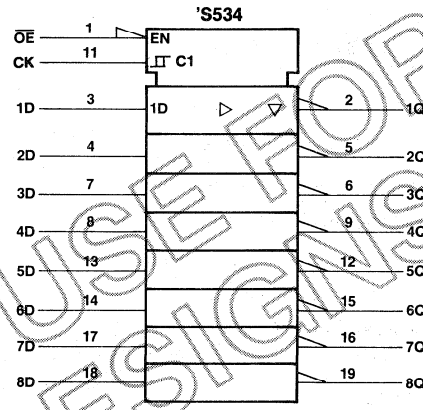


12

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories MMI

IEEE Symbols





Absolute Maximum Ratings

Supply voltage V_{CC} ..... 7 V
Input voltage ..... 7 V
Off-state output voltage ..... 5.5 V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		−55		125	0		75	°C
t_w	Width of Clock/Gate	High	15			15			ns
		Low	15			15			
t_{su}	Setup time	LS533	3↓			3↓			ns
		LS534	20↑			20↑			
t_h	Hold time	LS533	10↓			10↓			ns
		LS534	0↑			0↑			

↑↓ The arrow indicates the transition of the clock/enable input used for reference. ↑ for the low-to-high transition, ↓ for the high-to-low transition.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IH}	High-level input voltage			2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−1.5			−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V			−0.4			−0.4	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7V			20			20	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 7V			0.1			0.1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OL} = 12mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24mA					0.35	0.5	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OH} = −1mA	2.4	3.4					V
			I_{OH} = −2.6mA				2.4	3.1		
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2V	V_O = 0.4V						−20	μA
I_{OZH}			V_O = 2.7V			20			20	μA
I_{OS}	Output short-circuit current *	V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	LS533		36	48		36	48	mA
			LS534		27	48		27	48	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	LS533 MIN	LS533 TYP	LS533 MAX	LS534 MIN	LS534 TYP	LS534 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 45pF R_L = 667Ω				35	50		MHz
t_{PLH}	Data to Output delay			17	25				ns
t_{PHL}				12	25				ns
t_{PLH}	Clock/Gate to output delay			20	35		19	30	ns
t_{PHL}				18	35		15	30	ns
t_{PZL}	Output Enable delay			25	36		21	30	ns
t_{PZH}				17	30		20	30	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 667Ω		18	29		18	29	ns
t_{PHZ}				16	24		16	24	ns

12

Absolute Maximum Ratings

Supply voltage V_{CC} ..... 7 V
Input voltage ..... 5.5 V
Off-state output voltage ..... 5.5 V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		−55		125	0		75	°C
t_w	Width of Clock/Gate	High	6			6			ns
		Low	7.3			7.3			
t_{su}	Setup time	S533	0↓			0↓			ns
		S534	5↑			5↑			
t_h	Hold time	S533	10↓			10↓			ns
		S534	5↑			5↑			

↑↓ The arrow indicates the transition of the clock/enable input used for reference. ↑ for the low-to-high transition, ↓ for the high-to-low transition.

Electrical Characteristics Over Operating Conditions

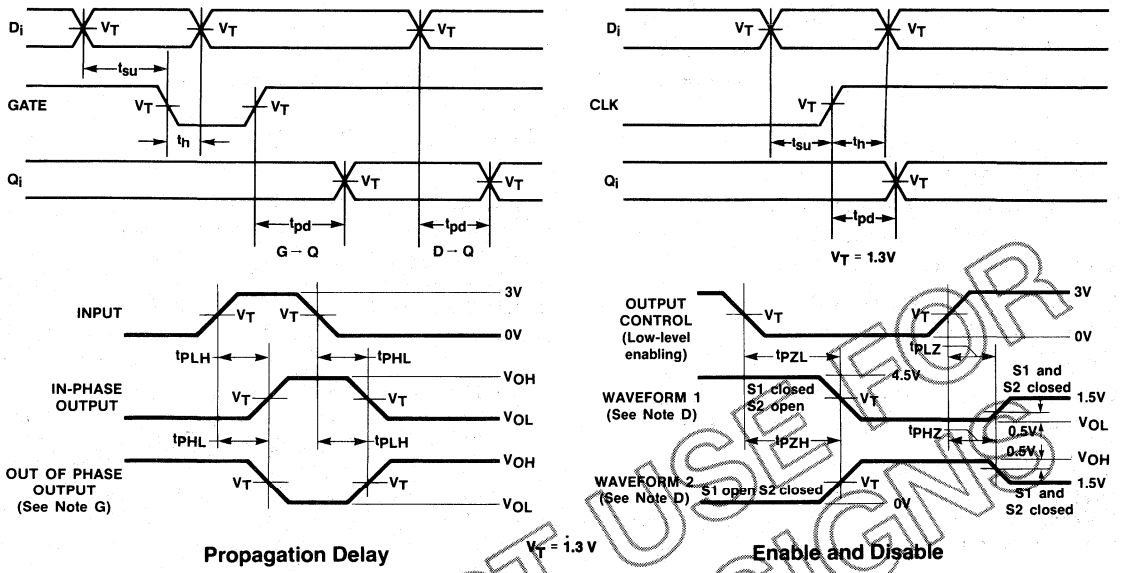
SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IH}	High-level input voltage			2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN,	I_I = −18mA			−1.2			−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5V			−0.25			−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7V			50			50	μA
I_I	Maximum input current	V_{CC} = MAX,	V_I = 5.5V			1			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 20mA			0.5			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = −2mA	2.4	3.4					V
			I_{OH} = −6.5mA				2.4	3.1		
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 0.5V			−50			−50	μA
I_{OZH}			V_O = 2.4V			50			50	μA
I_{OS}	Output short-circuit current *	V_{CC} = MAX		−40		−100	−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	S533		105	160		105	160	mA
			S534		90	140		90	140	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

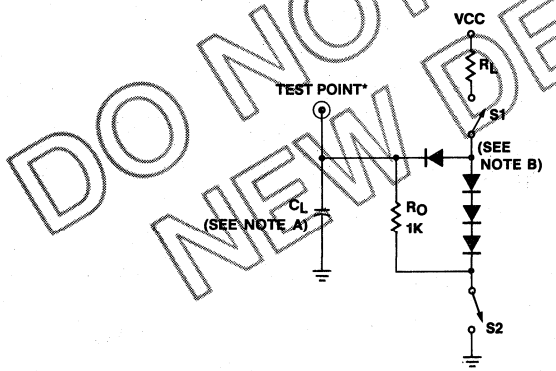
Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	S533 MIN	S533 TYP	S533 MAX	S534 MIN	S534 TYP	S534 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 15pF R_L = 280Ω				75	100		MHz
t_{PLH}	Data to Output delay			9	18				ns
t_{PHL}				5	16				ns
t_{PLH}	Clock/Gate to output delay			12	22		11	20	ns
t_{PHL}				7	20		8	18	ns
t_{PZL}	Output Enable delay			11	20		11	20	ns
t_{PZH}				8	17		8	17	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 280Ω		8	16		7	16	ns
t_{PHZ}				6	13		5	13	ns

Test Waveforms



Test Load



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

NOTES:
A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. For Series 54/74S, R_O = 1K, V_T = 1.5 V.
For Series 54/74LS, R_O = 5K, V_T = 1.3 V.
D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{OUT} = 50Ω and:
For Series 54/74S, $t_R \leq 2.5$ ns, $t_F \leq 2.5$ ns.
For Series 54/74LS and PALs, $t_R \leq 15$ ns. $t_F \leq 6$ ns.
G. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

8-Bit Latch, 8-Bit Register with 32 mA Outputs

SN74S531 SN74S532

Features/Benefits

- **High drive capability (I_{OL} = 32 mA)**
- **Three-state outputs drive bus lines**
- **20-pin SKINNYDIP® saves space**
- **8-bit data path matches byte boundaries**
- **Hysteresis improves noise margin**
- **Low current PNP inputs reduce loading**
- **Ideal for microprocessor interface**
- **Pin-compatible with SN74S373/4 — can be a direct replacement when high drive capability is required**

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	POWER
SN74S531	N,J	com	Non-invert	Latch	S
SN74S532	N,J	com		Register	

Description

In addition to the standard S and LS latches and registers, Monolithic Memories provides increased output sink current (I_{OL}) from the standard Schottky I_{OL} of 20 mA to an improved 32 mA.

The higher I_{OL} is intended for upgrading systems which presently satisfy 32-mA requirements with the SN54/74365A/366A/367A/368A hex buffers.

The latch passes eight bits of data from the inputs (D) to the outputs (Q) when the gate (G) is high. The data is "latched" when the gate (G) goes low. The register loads eight bits of input data and passes it to the output on the rising edge of the clock.

The three-state outputs are active when $\overline{OE}$ is low, and high-impedance when $\overline{OE}$ is high. Schmitt-trigger buffers at the gate/clock inputs improve system noise margin by providing typically 400 mV of hysteresis.

All of the 8-bit devices are packaged in the popular 20-pin SKINNYDIP®.

Function Tables

'S531 8-Bit Latch

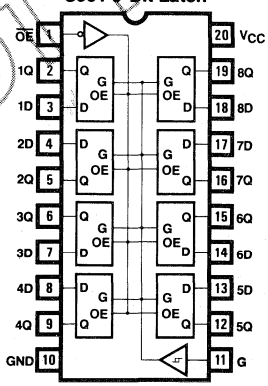
$\overline{OE}$	G	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

'S532 8-Bit Register

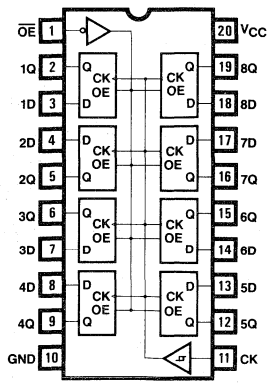
$\overline{OE}$	CK	D	Q
L	↑	H	H
L	↑	L	L
L	L or H or ↓	X	Q_0
H	X	X	Z

Logic Symbols

'S531 8-Bit Latch



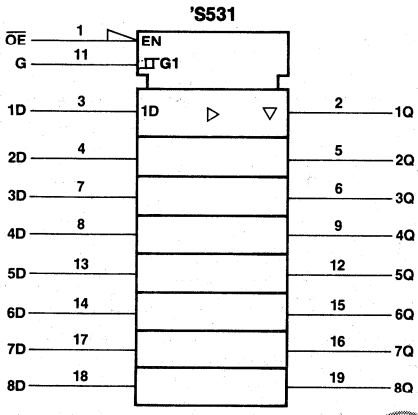
'S532 8-Bit Register

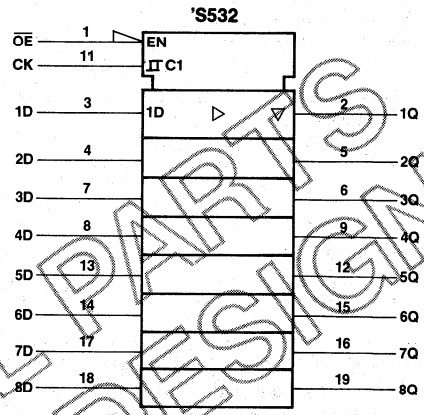


SKINNYDIP® is a registered trademark of Monolithic Memories.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories

IEEE Symbols





12

Absolute Maximum Ratings

Supply voltage V_{CC} ..... 7 V
Input voltage ..... 5.5 V
Off-state output voltage ..... 5.5 V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free air temperature		0		75	°C
t_w	Width of Clock/Enable	High	6	6		ns
		Low	7.3	7.3		
t_{su}	Setup time	S531	0↓	0↓		ns
		S532	5↑	5↑		
t_h	Hold time	S531	10↓	10↓		ns
		S532	2↑	2↑		

↑↓ The arrow indicates the transition of the clock/enable input used for reference. ↑ for the low-to-high transition, ↓ for the high-to-low transition.

Electrical Characteristics Over Operating Conditions

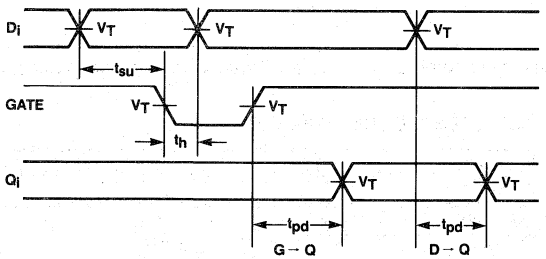
SYMBOL	PARAMETER	TEST CONDITIONS		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN,	I_I = −18mA			−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5V			−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7V			50	μA
I_I	Maximum input current	V_{CC} = MAX,	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 32mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = −6.5mA	2.4	3.1		V
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 0.5V			−50	μA
I_{OZH}			V_O = 2.4V			50	μA
I_{OS}	Output short-circuit current *	V_{CC} = MAX,		−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	S531		105	160	mA
			S532		90	140	

*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

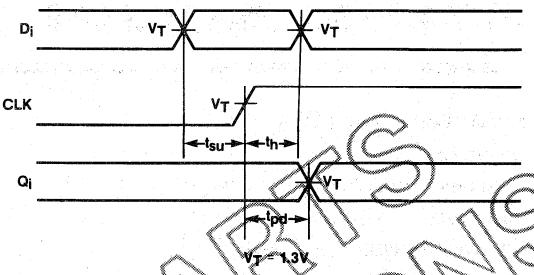
Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	S531 MIN	S531 TYP	S531 MAX	S532 MIN	S532 TYP	S532 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 15pF R_L = 280Ω				75	100		MHz
t_{PLH}	Data to Output delay			7	12				ns
t_{PHL}				7	12				ns
t_{PLH}	Clock/Gate to output delay			7	14		8	15	ns
t_{PHL}				12	18		11	17	ns
t_{PZL}	Output Enable delay			11	18		11	18	ns
t_{PZH}				8	15		8	15	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 280Ω		8	12		7	12	ns
t_{PHZ}				6	9		5	9	ns

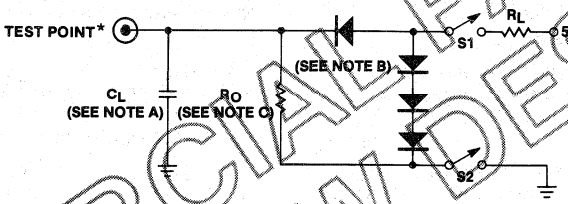
'S531 Timing Diagrams



'S532 Timing Diagrams

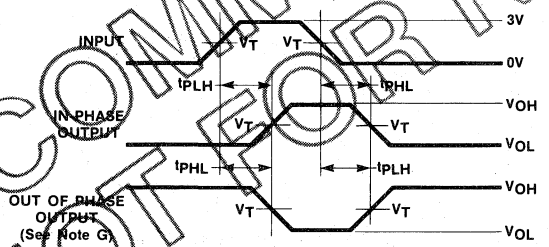


Test Load



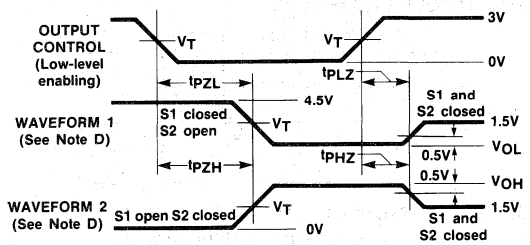
* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Test Waveforms



Propagation Delay

V_T = 1.3 V



Enable and Disable

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. For Series 54/74S, R_O = 1K, V_T = 1.5 V.
D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{OUT} = 50Ω and:
For Series 54/74S, $t_R \leq 2.5$ ns, $t_F \leq 2.5$ ns.
For Series 54/74LS and PALs, $t_R \leq 15$ ns. $t_F \leq 6$ ns.
G. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

12

8-Bit Latch, 8-Bit Register with Inverting, 32 mA Outputs

SN74S535 SN74S536

Features/Benefits

- **Inverting outputs**
- **High-drive capability (I_{OL} = 32 mA)**
- **Three-state outputs drive bus lines**
- **20-pin SKINNYDIP® saves space**
- **8-bit data path matches byte boundaries**
- **Hysteresis improves noise margin**
- **Low current PNP inputs reduce loading**
- **Ideal for microprocessor interface**
- **Pin-compatible with SN74S533/4 — can be a direct replacement when high-drive capability is required**

Description

In addition to the standard S and LS latches and registers, Monolithic Memories provides increased output sink current (I_{OL}) from the standard Schottky I_{OL} of 20 mA to an improved 32 mA; also, inverting outputs instead of the standard noninverting outputs.

The higher I_{OL} is intended for upgrading systems which presently satisfy 32-mA requirements with the SN54/74365/366/367/368 hex buffers. The inverting outputs are intended for bus applications that require inversion as in interfacing the Am2901A 4-bit slice to an assertive low.

The latch passes eight bits of data from the inputs (D) to the outputs (Q) when the gate (G) is high. The data is "latched" when the gate (G) goes low. The register loads eight bits of input data and passes it to the output on the rising edge of the clock.

The three-state outputs are active when $\overline{OE}$ is low, and high-impedance when $\overline{OE}$ is high. Schmitt-trigger buffers at the gate/clock inputs improve system noise margin by providing typically 400 mV of hysteresis.

All of the 8-bit devices are packaged in the popular 20-pin SKINNYDIP®.

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	POWER
SN74S535	N,J	Com	Invert	Latch	S
SN74S536	N,J	Com		Register	

Function Tables

'S535 8-Bit Latch (Inverting)

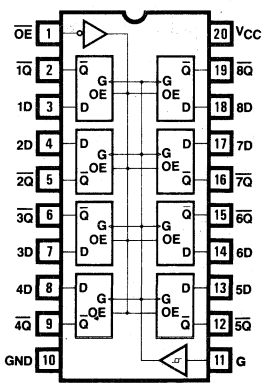
$\overline{OE}$	G	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

'S536 8-Bit Register (Inverting)

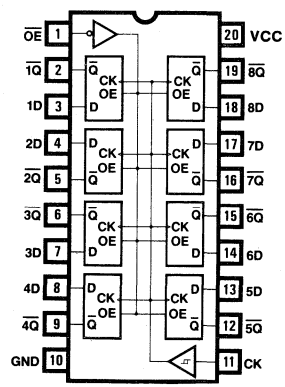
$\overline{OE}$	CK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L or H or ↓	X	Q_0
H	X	X	Z

Logic Symbols

'S535 8-Bit Latch (Inverting)



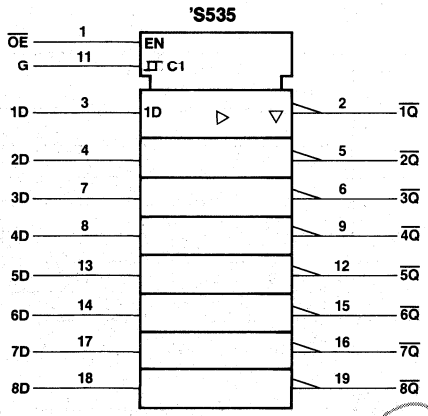
'S536 8-Bit Register (Inverting)

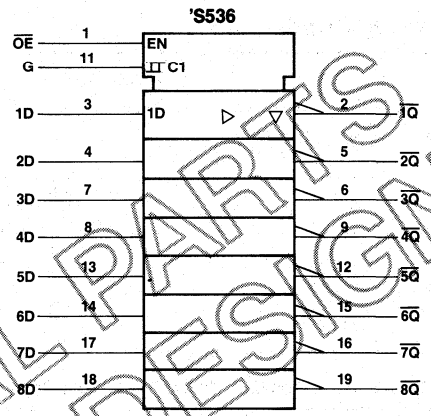


SKINNYDIP® is a registered trademark of Monolithic Memories.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories

IEEE Symbols





12

Absolute Maximum Ratings

Supply voltage V_{CC} ..... 7 V
Input voltage ..... 5.5 V
Off-state output voltage ..... 5.5 V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free air temperature		0		75	°C
t_w	Width of Clock/Enable	High	6	6		ns
		Low	7.3	7.3		
t_{su}	Setup time	S535	0↓	0↓		ns
		S536	5↑	5↑		
t_h	Hold time	S535	10↓	10↓		ns
		S536	5↑	2↑		

Electrical Maximum Ratings Over Operating Conditions

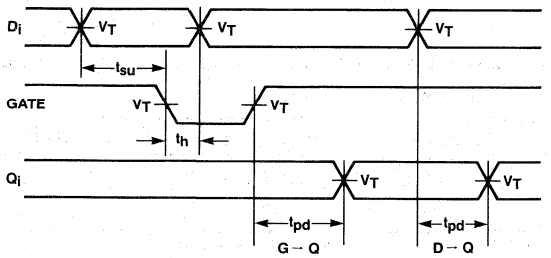
SYMBOL	PARAMETER	TEST CONDITIONS		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.5V			−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7V			50	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 32mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = −6.5mA	2.4	3.1		V
I_{OZL}	Off-state output current	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 0.5V			−50	μA
I_{OZH}			V_O = 2.4V			50	μA
I_{OS}	Output short-circuit current *	V_{CC}		−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	S535		105	160	mA
			S536		90	140	

*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

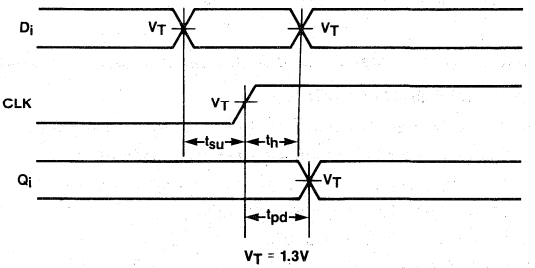
Switching Charcteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	S535 MIN	S535 TYP	S535 MAX	S536 MIN	S536 TYP	S536 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 15pF R_L = 280Ω				75	100		MHz
t_{PLH}	Data to Output delay			9	18				ns
t_{PHL}				5	16				ns
t_{PLH}	Clock/Enable to output delay			12	22		11	20	ns
t_{PHL}				7	20		8	18	ns
t_{PZL}	Output Enable delay			11	20		11	20	ns
t_{PZH}				8	17		8	17	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 280Ω		8	16		7	16	ns
t_{PHZ}				6	13		5	13	ns

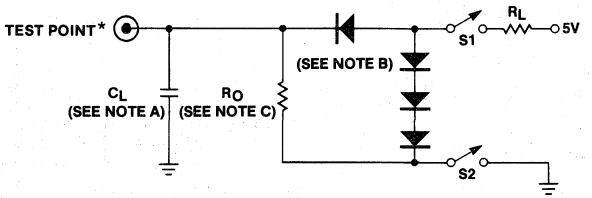
'S535 Timing Diagrams



'S536 Timing Diagrams

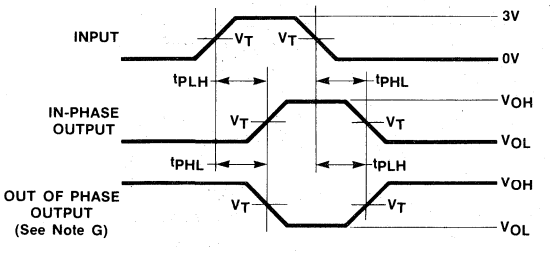


Test Load

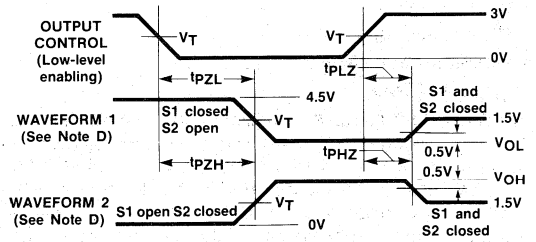


* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Test Waveforms



Propagation Delay



Enable and Disable

V_T = 1.3 V

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. For Series 54/74S, R_O = 1K, V_T = 1.5 V.
D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{OUT} = 50Ω and:
For Series 54/74S, $t_R \leq 2.5$ ns, $t_F \leq 2.5$ ns.
For Series 54/74LS and PALs, $t_R \leq 15$ ns. $t_F \leq 6$ ns.
G. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

12

8-Bit Diagnostic Register
SN54/74S818

FOR MORE DETAIL SEE SECTION 13

Features/Benefits

- High-drive capability: I_{OL} = 32 mA (Com), 24 mA (Mil)
- Assists on-line and off-line system diagnostic testing
- Swaps the content of shadow register and output register
- Shadow register for diagnostic testing
- Edge-triggered "D" registers
- Cascadable for wide control words for use in microprogramming
- Features RAM write-back for writable control store initialization
- PNP inputs for low-input current
- 24-pin SKINNYDIP® saves space

Applications

- Register for microprogram control store
- Status register
- Data register
- Instruction register
- Address register
- Interrupt mask register
- Pipeline register
- General purpose register
- Parallel-serial/Serial-parallel converter

Description

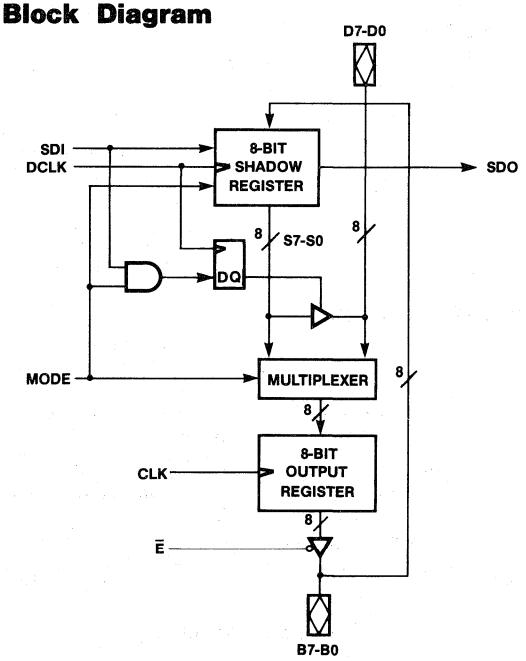
The SN54/74S818 is an 8-bit register with diagnostic features. There is a shadow register in each diagnostic register. Diagnostic data is shifted in serially into the shadow register (S7-S0), while the output register is loaded with either the content of the shadow register or the input data (D7-D0). Moreover, D7-D0 can also be used as the outputs from the shadow register to the data bus, while the outputs (B7-B0) can also be converted to inputs when disabled.

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN54S818	JS,F,L	Mil
SN74S818	NS,JS	Com

NOTE: L package here is L28. The other packages are 24-pin.

Block Diagram



Function Table

INPUTS				OUTPUTS			OPERATION	SEE FIG.
MODE	SDI	CLK	DCLK	B7-B0	S7-S0	SDO		
L	X	↑	*	Bn ← Dn	HOLD	S7	Load output register from input bus	1
L	X	*	↑	HOLD	Sn ← Sn-1 S0 ← SDI	S7	Shift shadow register data	2
L	X	↑	↑	Bn ← Dn	Sn ← Sn-1 S0 ← SDI	S7	Load output register from input bus while shifting shadow register data	1 & 2
H	X	↑	*	Bn ← Sn	HOLD	SDI	Load output register from shadow register	2,3,4
H	L	*	↑	HOLD	Sn ← Bn	SDI	Load shadow register from output bus	3
H	L	↑	↑	Bn ← Sn	Sn ← Bn	SDI	Swap shadow register and output register	
H	H	*	↑	HOLD	HOLD	SDI	Enable D7-D0 as outputs for RAM write-back	4

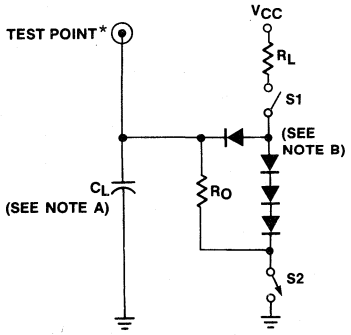
* Clock must be steady or falling.

SKINNYDIP® is a registered trademark of Monolithic Memories

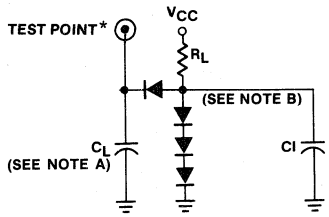
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Monolithic Memories MMI

Test Load



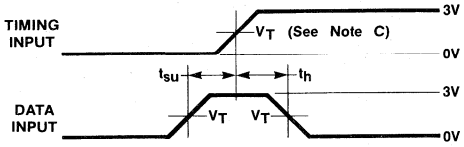
LOAD CIRCUIT FOR THREE-STATE OUTPUTS



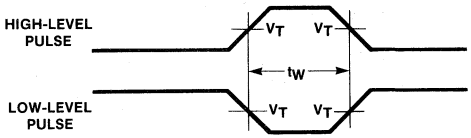
LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS

* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

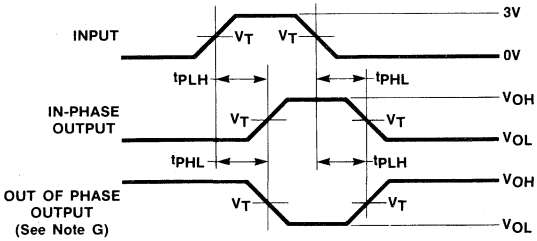
Test Waveforms



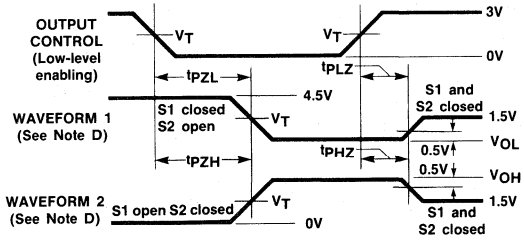
SETUP AND HOLD



PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE

Notes: A. C_L includes probe and jig capacitance.

B. All diodes are 1N916 or 1N3064.

C. For Series 54, R_O = 1K, V_T = 1.5V.
For Series 54LS, R_O = 5K, V_T = 1.3V.

D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

F. All input pulses are supplied by generators having the following characteristics:
PRR ≤ 1 MHz. Z_{OUT} = 50 Ω and:
For Series 54, $t_R \leq 2.5$ ns, $t_F \leq 2.5$ ns.
For Series 54S and PALs, $t_R \leq 15$ ns, $t_F \leq 6$ ns.

G. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.


IMPORTANT
NOTES

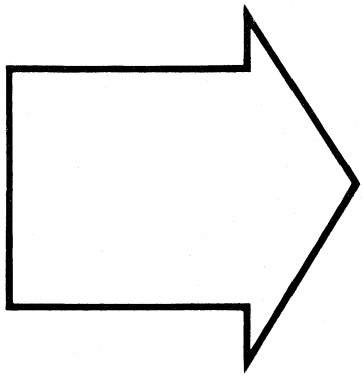


Table of Contents

DOUBLE-DENSITY-PLUS™ INTERFACE

13

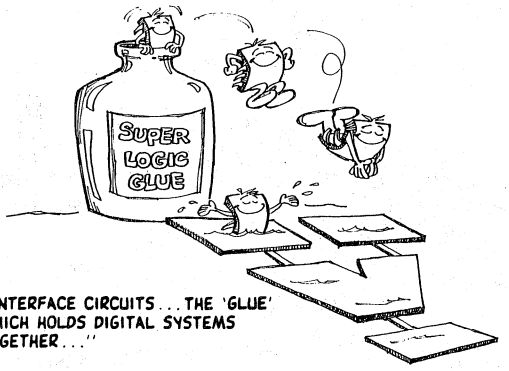
Double-Density PLUS Selection Guide

PART NUMBER	PART DESCRIPTION			POWER	POLARITY	OUTPUT	I_{OL}
COMMERCIAL	ARCHITECTURE	FUNCTION	FEATURE				
74LS546	Transceiver	Register	Independent enable controls	LS	Noninvert	Three-state	32 mA
74LS566	Transceiver	Register		LS	Invert	Three-state	32 mA
74LS547	Transceiver	Latch		LS	Noninvert	Three-state	32 mA
74LS567	Transceiver	Latch		LS	Invert	Three-state	32 mA
74LS646	Transceiver	Front load latch	Direction control	LS	Noninvert	Three-state	24 mA
74LS647	Transceiver	Front load latch		LS	Noninvert	Open-collector	24 mA
74LS648	Transceiver	Front load latch		LS	Invert	Three-state	24 mA
74LS649	Transceiver	Front load Latch		LS	Invert	Open-collector	24 mA
74LS651	Transceiver	Front load latch	Independent enable controls	LS	Invert	Three-state	24 mA
74LS652	Transceiver	Front load latch		LS	Noninvert	Three-state	24 mA
74LS653	Transceiver	Front load latch		LS	Invert	A: Open-collector B: Three-state	24 mA
74LS654	Transceiver	Fr/load latch		LS	Noninvert		24 mA
74ACT547	Transceiver	Latch	Independent enable controls	CMOS	Noninvert	Three-state	12 mA
74ACT567	Transceiver	Latch		CMOS	Invert	Three-state	12 mA
74ACT646	Transceiver	Front load latch	Direction control	CMOS	Noninvert	Three-state	12 mA
74ACT648	Transceiver	Front load latch		CMOS	Invert	Three-state	12 mA
74ACT651	Transceiver	Front load latch	Independent enable controls	CMOS	Invert	Three-state	12 mA
74ACT652	Transceiver	Front load latch		CMOS	Noninvert	Three-state	12 mA
74ACT793	Readback	Latch	Readback enable control	CMOS	Noninvert	Three-state	12 mA
74ACT794	Readback	Register		CMOS	Noninvert	Three-state	12 mA
74LS793	Readback	Latch	Readback enable control	LS	Noninvert	Three-state	24 mA
74LS794	Readback	Register		LS	Noninvert	Three-state	24 mA
74LS548	Two-stage pipeline	Register	Input, Output individual select controls	LS	Noninvert	Three-state	32 mA
74LS549	Two-stage pipeline	Latch		LS	Noninvert	Three-state	32 mA
74S818	Pipeline	Register	Mode controls	S	Noninvert	Three-state	32 mA

Small But Mighty; New Components Give You More Logic in Less Chips*

Chuck Hastings and Suneel Rajpal

Interface circuits are generally thought of as unglamorous bread-and-butter items. They have the humble role of being the "glue" which holds digital systems together. Contemporary custom-LSI wizards often claim to be on the point of getting rid of all these bothersome little low-complexity circuits, and yet *more* interface circuits are sold with each passing year. According to recent estimates, during 1983 the personal computer industry *alone* consumed one-fourth as many interface circuits as *all* users consumed during 1982. Figure 1 graphically portrays a realistic scenario for interface for the next few years—everything else will shrink, so interface will grab an *increasing* share of board area in the future!



"INTERFACE CIRCUITS ... THE 'GLUE' WHICH HOLDS DIGITAL SYSTEMS TOGETHER..."

What this means to you is that, if interface does its part and does some shrinking too, you'll get some *major* shrinkage in your overall system. Interface is low-complexity stuff to start with, and over the years it has stubbornly resisted being shrunk. Nonetheless, today Monolithic Memories offers a broad line of interface parts which arose from commonly-encountered circumstances, and which — where they fit your design — shrink parts count by a factor of 2:1. Unsurprisingly, they are called "Double-Density PLUS Interface." Actually, under optimal conditions certain of these parts can shrink your parts count by as much as 4:1.

Double-Density PLUS™ Interface can do wonders to compress the physical size of your logic. Consider, for example, a simple sychronous cross-connection between two 8-bit microprocessor buses, capable of transferring information in either direction one byte at time. This cross-connection can be implemented using two 'LS374 8-bit noninverting registers, connected "back-to-back" — that is, each 'LS374 has all of its eight outputs tied respectively to the eight inputs of the other one. Together, these two parts total 40 pins and 2 (0.6*1.1) = 2 (0.66) = 1.32 square inches, allowing for 100 mils end clearance and 300 mils side clearance as is common practice in board layout.

"... DOUBLE-DENSITY PLUS™ INTERFACE CAN DO WONDERS TO COMPRESS THE PHYSICAL SIZE OF YOUR LOGIC..."

You may notice that, when these two parts are considered as a functional block, far fewer than 40 pins go to the outside world; there are only the 16 data pins corresponding to the two 8-bit buses, two clock pins, two output-enable pins, and power and ground. Now, since Monolithic Memories also noticed back-to-back 'LS374s as an attractive low-pin-count combination a couple of years ago, today you have the option of replacing both of these 'LS374's with a single 24-pin, 300-mil "SKINNYDIP®" 'LS546, which takes up only (0.6*1.3) = 0.78 square inches of your board — slightly more than half as much board area as the two 'LS374s. To summarize:

DESIGN SOLUTION	BOARD AREA		WIRE ENDS	
	Sq. In.	Normalized	Pin Count	Normalized
Two 'LS374s	1.32	1.00	40	1.00
One 'LS546	0.78	0.59	24	0.60

Table 1. Board Area and Wire Savings Using 'LS546

*Note: This article is a portion of Monolithic Memories Conference Paper CP-112, which may be found in its entirety in the second edition of the *Systems Design Handbook*.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

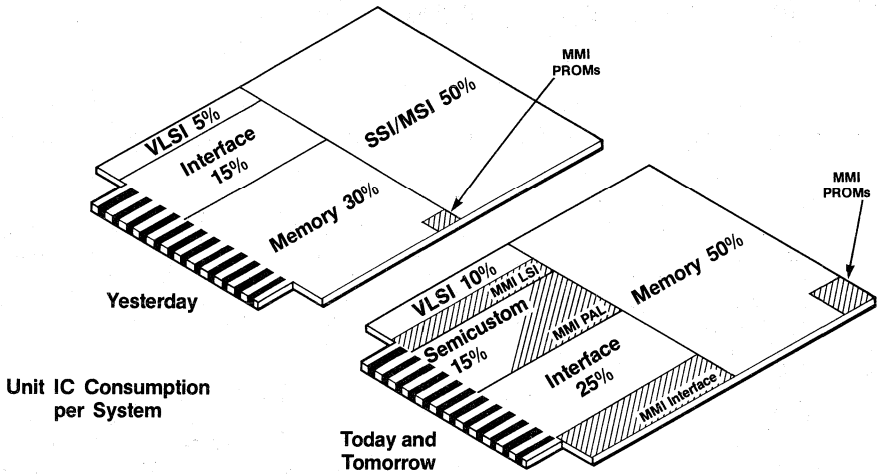


Figure 1. Logic Distribution on a Typical Board

You also pick up some other benefits along the way making this swap. The two registers within the 'LS546 are appreciably faster than the 'LS374s, and also have a higher output drive — 32 mA sinking current instead of 24 mA. The 'LS546 and 'LS566 have clock enables which operate independently for each register. The 'LS546 also has a cleaned-up "structured" pinout with the 8 pins for each data bus together, each bus having its own side of the 24-pin dual-inline package.

The 'LS546 is comprised of two non-inverting edge-triggered registers. If you are dealing with assertive-low buses and need inverting registers, use an 'LS566. If you prefer latches to registers, use either an 'LS547 (non-inverting) or an 'LS567 (inverting). All of these parts have a common "back-to-back" internal architecture, as shown in Figure 2.

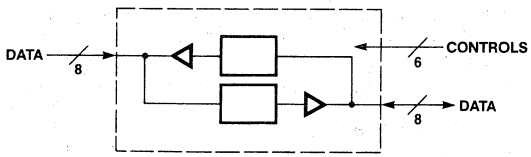


Figure 2. The 546/547/566/567 Block Diagram

Two more families of back-to-back parts also come in the same pinout: the 'LS646/7/8/9 family, and the 'LS651/2/3/4 family. These differ from each other in enable structure; the 'LS646 et. al. have a "direction-control line" so that you can't perform certain operations on both sides of the part simultaneously, whereas the 'LS651 et. al. have generally independent operations on both sides. In each of these families there are two non-inverting parts and two inverting parts; in each case, there is a three-state part and an open-collector part. All of the parts from both families are comprised of "front-loading-latch" individual elements (see

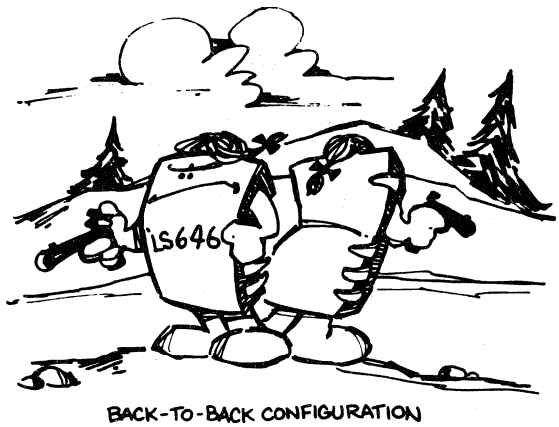


Figure 3); a front-loading latch is an edge-triggered flipflop in parallel with a buffer, so that the data can be piped through the buffer to reach the output rapidly and then can be *subsequently* recorded in the flipflop. It is also possible, in a front-loading-latch structure, to pipe data temporarily around the flipflop to the output without *ever* recording it in the flipflop. The 'LS646/7/8/9 feature hysteresis on their data inputs as well as on their control inputs, which makes them function well in high-noise environments. The 'LS653/4 are open-collector in one direction, but three-state in the other direction.

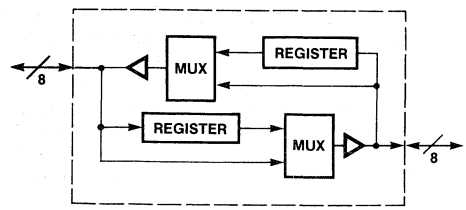


Figure 3. The '646-Series/'651-Series Block Diagram

Then there are two "readback" parts, which consists of a latch or register back-to-back with a buffer: the 'LS793 readback latch, and the 'LS794 readback register. Both of these are just 20-pin, and hence offer a full 2:1 saving in board area as well as in parts count. They have structured pinouts compatible with those of the 'LS573 and 'LS574, but a very different internal architecture; each of the 8 elements (latch or flipflop) has 2 outputs, one of which is totem-pole and goes to the presumed "output pin" of that element, and the other of which is three-state and goes back to the "input pin" for the element (see Figure 4). Thus, it is possible to read the contents of an 'LS793 or 'LS794 from its *input* lines by enabling its three-state outputs.

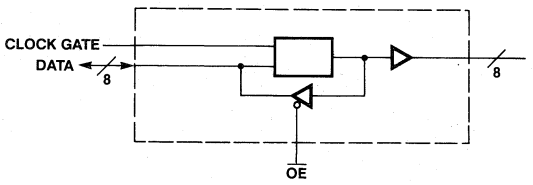


Figure 4. The '793/'794 Block Diagram

The 'LS793 and 'LS794 are intended for use in decentralized systems, for instance industrial-control systems in which a large number of slowly-changing setpoints and displays are under the control of a central microprocessor. The readback feature permits reading one of these, updating it, and replacing it. Without the readback feature, the system would have to keep a *redundant* copy of the setpoint or display value in main memory, which could cause additional system overhead due to the time-slicing of the microprocessor's activities, or even due to virtual-memory page-faulting in larger systems. Moreover, there is the reliability issue of whether the alleged redundant copy always agrees exactly with the real thing out there in the register controlling the actuator or the display, and what happens whenever it doesn't.

CONFIGURATION	LATCHES	REGISTERS
Back-to-Back L/R	'547('373) '567('533)	'546('374) '566('534)
Back-to-Back Front-Loading Latches		'646/7('374) '648/9('534) '652/4('374) '651/3('534)
Readback L/R	'793('373)	'794('374)

Table 2. Double-Density PLUS Interface Product

Note that the bracketed part numbers represent the element *inside* the Double-Density PLUS Interface. For example, a '245 can replace two '244s and a '546 can replace two '374s. The same holds true for the '646 and '651 series. However the '793/'794 are the equivalent of a '373/'374 and a readback buffer such as a '244.

Table 2 is a summary of the Double-Density PLUS Interface product presently available from Monolithic Memories.

Two other common and intuitively-plausible combinations of a couple of 8-bit latches or registers are "nose-to-tail" (one after the other), and "side-by-side" (alternate). If two registers are used in a nose-to-tail combination, for instance, data from the inputs enters the first register when it is clocked, and the outputs of the first register are the inputs of the second register, and thus the same data finally reach the outputs of the combination when the second register is subsequently clocked. And, if two registers are used in a side-by-side combination, their inputs come from the same input bus, and their outputs go to the same output bus, but they can be controlled separately and the output bus can be driven from either one.

Although the nose-to-tail configuration and the side-by-side configuration seem quite different, with the provision of some internal multiplexing the same Double-Density PLUS™ Interface part can satisfy both requirements. Such a part is called a pipeline — register or latch, as the case may be. The internal architecture of a two-level pipeline is shown in Figure 5.

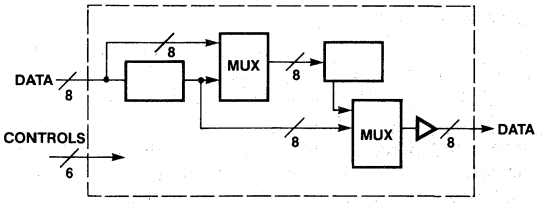


Figure 5. The '548/9 Block Diagram

The 'LS548, with the edge-triggered registers, and the 'LS549, with latches, follow the Figure 5 block diagram exactly. Their pinouts resemble those of 'LS546, 'LS646, and 'LS651 families. Their speeds are similar, and they also feature 32-mA-I_{OL} outputs.

Typical applications for Double-Density PLUS Interface include computer peripherals, minicomputers, and microcomputers. Applications for the open-collector parts are in the telecommunication and games areas. The drive of these parts enables them to drive heavily-loaded buses, and flat cables.

13

8-Bit Buffer Transceiver
SN54LS245

Features/Benefits

- Three-state outputs drive bus lines
- Low current PNP inputs reduce loading
- Symmetric — equal driving capability in each direction
- 8-bit data path matches byte boundaries
- Ideal for microprocessor interface
- Pin-compatible with SN54LS645 — improved speed, I_{IL} and I_{OZL} specifications

Ordering Information

PART NUMBER	TYPE	TEMP	POLARITY	POWER
SN54LS245	J,L,W	Mil	Noninvert	LS

Description

These 8-bit bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

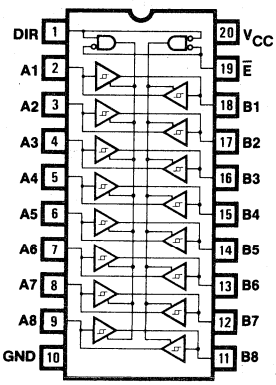
The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The enable input ($\overline{E}$) can be used to disable the device so that the buses are effectively isolated.

Function Table

ENABLE $\overline{E}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolated

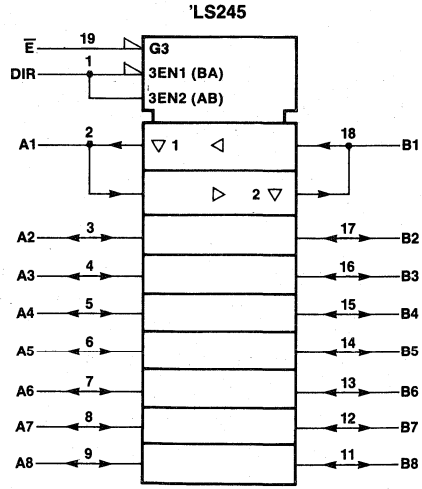
Logic Symbol

'LS245



IEEE Symbol

'LS245



2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories AMD

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
T_A	Operating free-air temperature	-55		125	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	UNIT
V_{IL}	Low-level input voltage						0.7	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = -18 mA			-1.5	V
ΔV_T	Hysteresis (V_{T+}-V_{T-}) A or B		V_{CC} = MIN		0.2	0.4		V
I_{IL}	Low-level input current		V_{CC} = MAX	V_I = 0.4 V			-0.2	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7 V			20	μA
I_I	Maximum input current	A or B	V_{CC} = MAX	V_I = 5.5 V			0.1	mA
		DIR or $\overline{E}$		V_I = 7.0 V				
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OL} = 12 mA		0.25	0.4	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OH} = -3 mA	2.4	3.4		V
				I_{OH} = -12 mA	2			
I_{OZL}	Off-state output current		V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2 V	V_O = 0.4 V			-200	μA
I_{OZH}				V_O = 2.7 V			20	μA
I_{OS}	Output short-circuit current*		V_{CC} = MAX		-40		-225	mA
I_{CC}	Supply Current	Outputs High	V_{CC} = MAX. Outputs open			48	70	mA
		Outputs Low				62	90	
		Outputs Disabled				64	95	

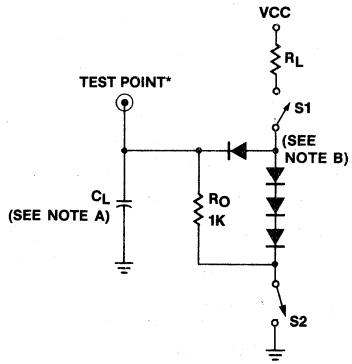
* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	A to B DIRECTION MIN	A to B DIRECTION TYP	A to B DIRECTION MAX	B to A DIRECTION MIN	B to A DIRECTION TYP	B to A DIRECTION MAX	UNIT
t_{PLH}	Data to output delay	C_L = 45 pF R_L = 667 Ω		8	12		8	12	ns
t_{PHL}				8	12		8	12	ns
t_{PZL}	Output enable delay			27	40		27	40	ns
t_{PZH}				25	40		25	40	ns
t_{PZL}	Output disable delay	C_L = 5 pF R_L = 667 Ω		15	25		15	25	ns
t_{PHZ}				15	25		15	25	ns

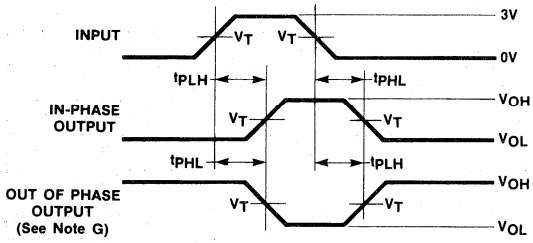
13

Test Load



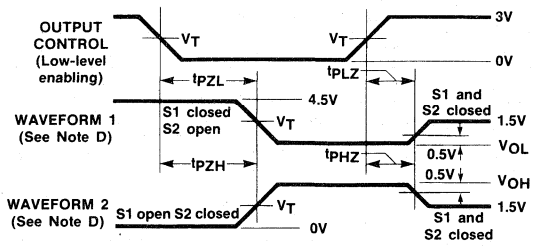
* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Test Waveforms



Propagation Delay

V_T = 1.3 V



Enable and Disable

Notes: A. C_L includes probe and jig capacitance.

B. All diodes are 1N916 or 1N3064.

C. For Series 54LS, R_O = 5 K, V_T = 1.3 V.

D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz. Z_{OUT} = 50 Ω and:
For series 54S, $t_R \leq 2.5$ ns, $t_F \leq 2.5$ ns.
For Series 54LS, $t_R \leq 15$ ns, $t_F \leq 6$ ns.

G. When measuring propagation delay times of three-state outputs, switches S1 and S2 are closed.

8-Bit Buffer Transceivers
SN54LS645

Features/Benefits

- **Three-state outputs drive bus lines**
- **Low current PNP inputs reduce loading**
- **Symmetric — equal driving capability in each direction**
- **8-bit data path matches byte boundaries**
- **Ideal for microprocessor interface**

Ordering Information

PART NUMBER	TYPE	TEMP	POLARITY	POWER
SN54LS645	J,L,W	Mil	Noninvert	LS

Description

These 8-bit bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

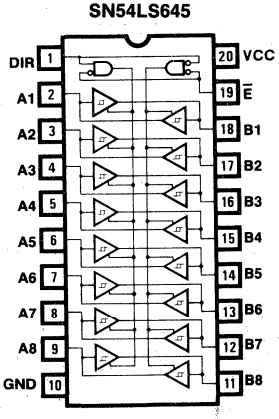
The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The enable input ($\overline{E}$) can be used to disable the device so that the buses are effectively isolated.

All of the 8-bit devices are packaged in the popular 20-pin SKINNYDIP.

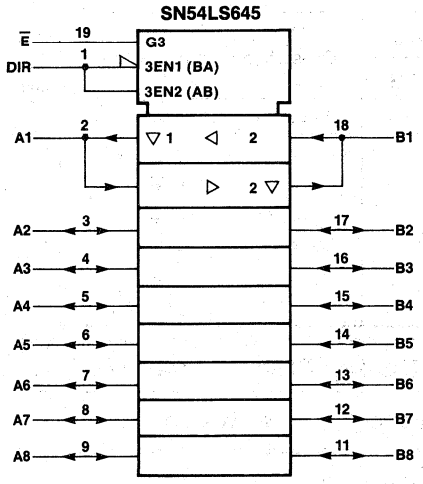
Function Table

ENABLE $\overline{E}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolated

Logic Symbol



IEEE Symbol



13

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories MMI

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
T_A	Operating free-air temperature	-55		125	°C

Electrical Characteristics Over Operating Conditions

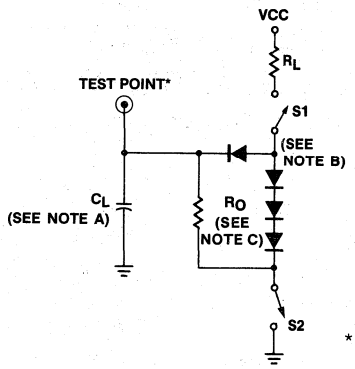
SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	UNIT
V_{IL}	Low-level input voltage						0.7	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = -18 mA			-1.5	V
ΔV_T	Hysteresis (V_{T+}-V_{T-}) A or B		V_{CC} = MIN		0.2	0.4		V
I_{IL}	Low-level input current		V_{CC} = MAX	V_I = 0.4 V			-0.2	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7 V			20	μA
I_I	Maximum input current	A or B	V_{CC} = MAX	V_I = 5.5 V			0.1	mA
		DIR or $\overline{E}$		V_I = 7.0 V				
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OL} = 12 mA		0.25	0.4	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OH} = -3 mA	2.4	3.4		V
				I_{OH} = -12 mA	2			
I_{OZL}	Off-state output current		V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2 V	V_O = 0.4 V			-200	μA
I_{OZH}				V_O = 2.7 V			20	μA
I_{OS}	Output short-circuit current*		V_{CC} = MAX		-40		-225	mA
I_{CC}	Supply Current	Outputs High	V_{CC} = MAX. Outputs open			48	70	mA
		Outputs Low				62	90	
		Outputs Disabled				64	95	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

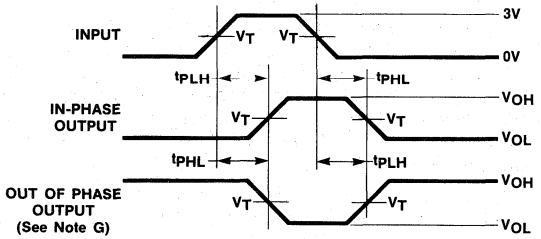
SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	A to B DIRECTION MIN	A to B DIRECTION TYP	A to B DIRECTION MAX	B to A DIRECTION MIN	B to A DIRECTION TYP	B to A DIRECTION MAX	UNIT
t_{PLH}	Data to output delay	C_L = 45 pF R_L = 667 Ω		8	15		8	15	ns
t_{PHL}				11	15		11	15	ns
t_{PZL}	Output enable delay			31	40		31	40	ns
t_{PZH}				26	40		26	40	ns
t_{PLZ}	Output disable delay	C_L = 5 pF R_L = 667 Ω		15	25		15	25	ns
t_{PHZ}				15	25		15	25	ns

Test Load



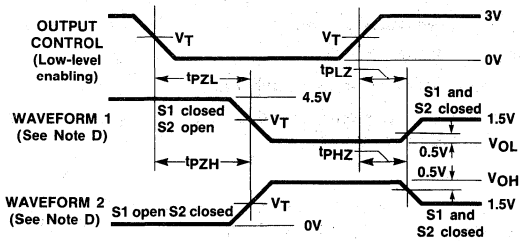
* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Test Waveforms



Propagation Delay

V_T = 1.3 V



Enable and Disable

Notes: A. C_L includes probe and jig capacitance.

B. All diodes are 1N916 or 1N3064.

C. For Series 54LS, R_O = 5 K, V_T = 1.3 V.

D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz. Z_{OUT} = 50 Ω and:
For series 54S, $t_R \leq 2.5$ ns, $t_F \leq 2.5$ ns.
For Series 54LS, $t_R \leq 15$ ns, $t_F \leq 6$ ns.

G. When measuring propagation delay times of three-state outputs, switches S1 and S2 are closed.

13

8-Bit Bus Register Transceivers and Latch Transceivers

SN54/74LS546 SN54/74LS547 SN54/74LS566 SN54/74LS567

Features/Benefits

- **Bidirectional transceivers utilizing registers or latches**
- **Faster than other LS-TTL registers/latches**
- **Independent registers/latches for A bus and B bus**
- **Data can be swapped between internal registers/latches**
- **8-bit data paths match byte boundaries**
- **'LS546/547/566/567 can replace two 'LS374/373/534/533 devices**
- **Independent clock/gate enables for rank A and rank B**
- **High drive capability: I_{OL} = 32 mA (COM), 24 mA (MIL)**
- **24-pin SKINNYDIP® saves space**
- **Three-state outputs drive bus lines**
- **The clock, clock-enable, and latch-enable inputs typically have 300 mV hysteresis**

There are independent clock and clock enable controls for the two directions namely CKA, CKB, CKEA, CKEB for 'LS546/'LS566, and independent gate enable control GA1, GA2, GB1 and $\overline{GB2}$ for 'LS547/'LS567. The CKA/B and $\overline{CKEA/B}$ can control the internal registers A/B to load data or hold data. Similarly, the GA1, $\overline{GA2}$, GB1 and $\overline{GB2}$ can govern the internal latches, A/B to pass or hold data.

Description

These devices are comprised of a pair of 8-bit registers ('LS546, 'LS566), or a pair of 8-bit latches ('LS547, 'LS567).

The direction of operation is controlled by $\overline{OEAB}$ and $\overline{OEBA}$. When $\overline{OEAB}$ is Low and $\overline{OEBA}$ is High, the operation of the registers/latches is A-to-B direction; when $\overline{OEAB}$ is High and $\overline{OEBA}$ is low, the operation of the registers/latches is B-to-A direction; when $\overline{OEAB}$ and $\overline{OEBA}$ both are High, the A, B buses both are inputs, data will be stored into registers/latches; when $\overline{OEAB}$ and $\overline{OEBA}$ both are Low, the A, B buses both are outputs, data will transfer from internal registers/latches to A, B buses.

There are independent clock and clock enable controls for the two directions: namely CKA, CKB, $\overline{CKEA}$ and $\overline{CKEB}$ for 'LS546/'LS566, and independent gate enable control GA1, $\overline{GA2}$, GB1 and $\overline{GB2}$ for 'LS547/'LS567. The CKA/B and $\overline{CKEA/B}$ can control the internal registers A/B to load data or hold data. Similarly, the GA1, $\overline{GA2}$, GB1 and $\overline{GB2}$ govern the internal latches, A/B to pass or hold data.

The 'LS546/'547 provide non-inverting polarity; the 'LS566/'LS567 provide inverting polarity. The 'LS546/'LS547/'LS566/'LS567 all have 3-state outputs, and have 32-mA output drive I_{OL} (COM) over the commercial temperature range and 24-mA output drive I_{OL} (MIL), over the military temperature range.

All of the devices are packaged in the popular 24-pin SKINNYDIP package.

Ordering Information

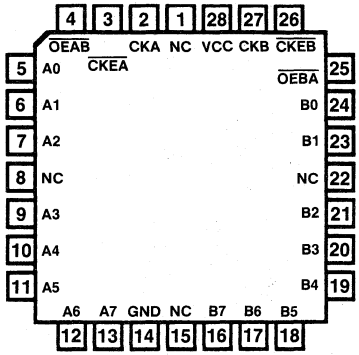
PART NUMBER	PACKAGE	TEMPERATURE	POLARITY	TYPE	POWER
SN54LS546	JS, W, L (28)	Mil	Non-invert	Register	LS
SN74LS546	NS, JS, NL (28)	Com			
SN54LS547	JS, W, L (28)	Mil		Latch	
SN74LS547	NS, JS, NL (28)	Com			
SN54LS566	JS, W, L (28)	Mil	Invert	Register	
SN74LS566	NS, JS, NL (28)	Com			
SN54LS567	JS, W, L (28)	Mil		Latch	
SN74LS567	NS, JS, NL (28)	Com			

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Monolithic Memories MMI

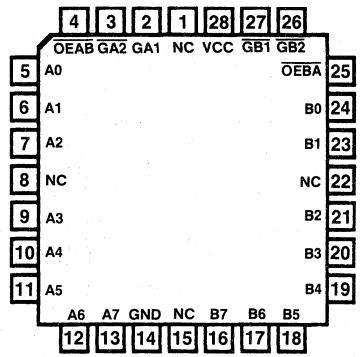
Pin Configurations

SN74LS546



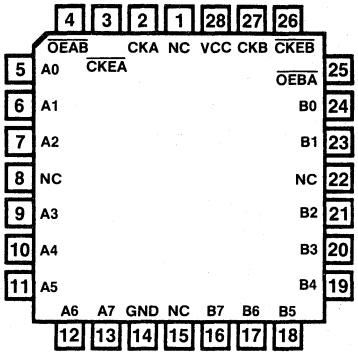
Plastic Chip Carrier

SN74LS547



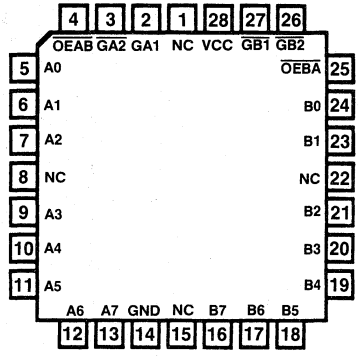
Plastic Chip Carrier

SN74LS566



Plastic Chip Carrier

SN74LS567

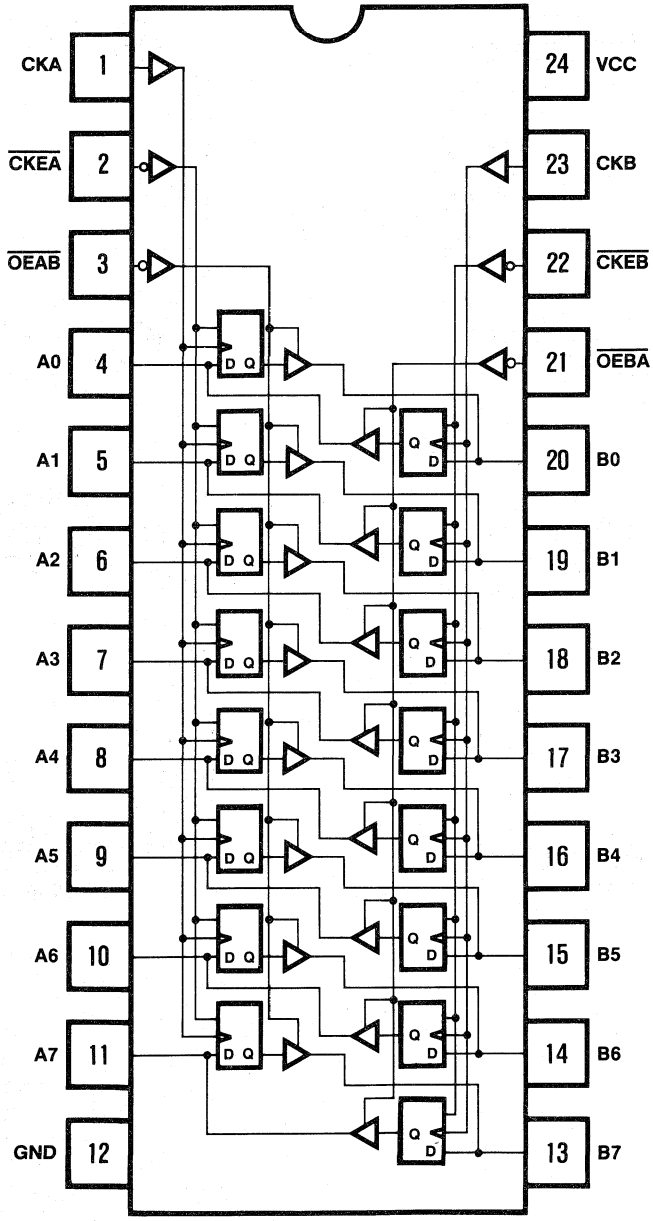


Plastic Chip Carrier

13

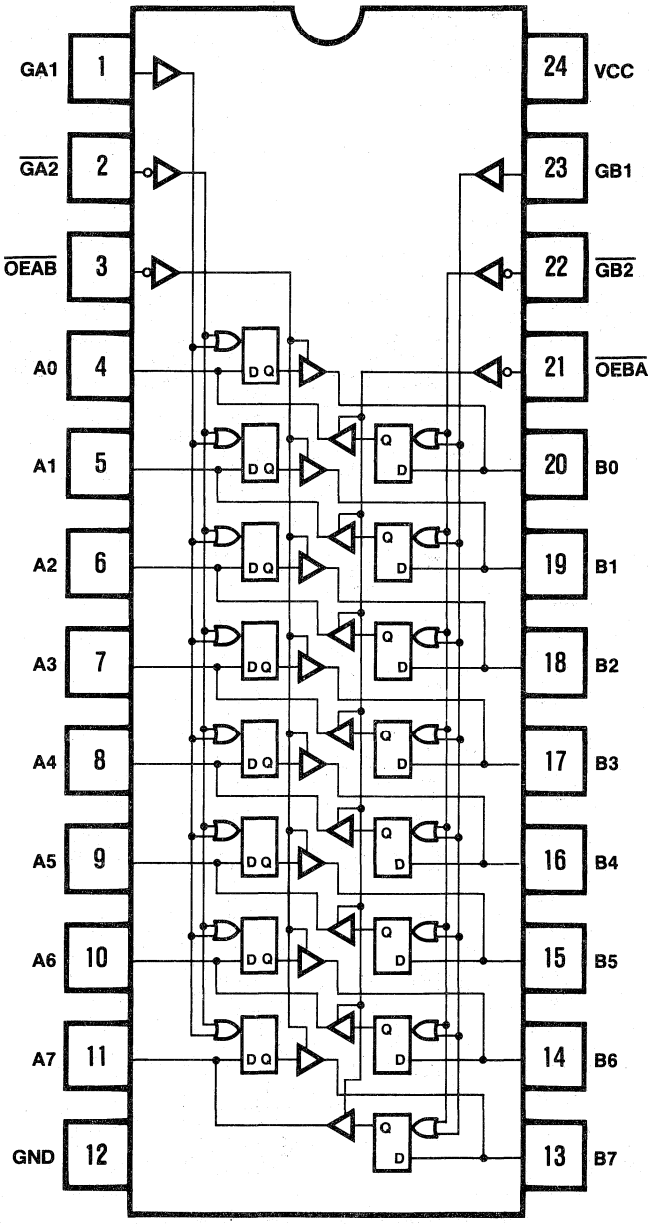
Logic Diagram

SN54/74LS546
REGISTER TRANSCEIVER
NON-INVERTING OUTPUTS



Logic Diagram

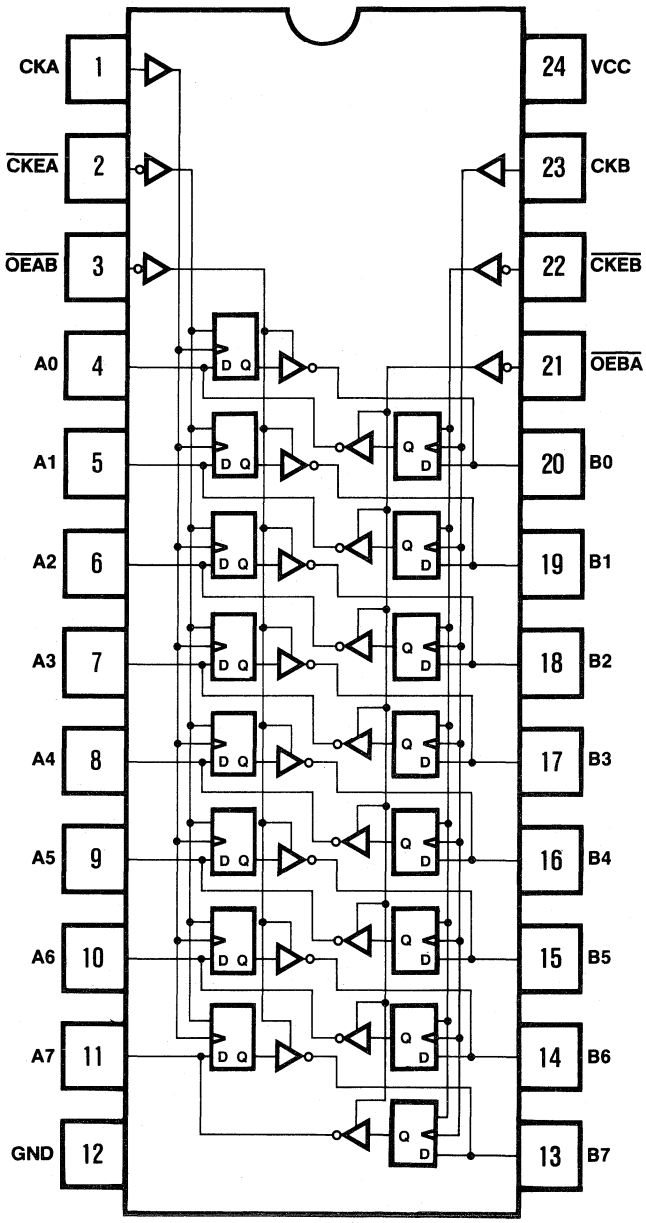
SN54/74LS547
LATCH TRANSCEIVER
NON-INVERTING OUTPUTS



13

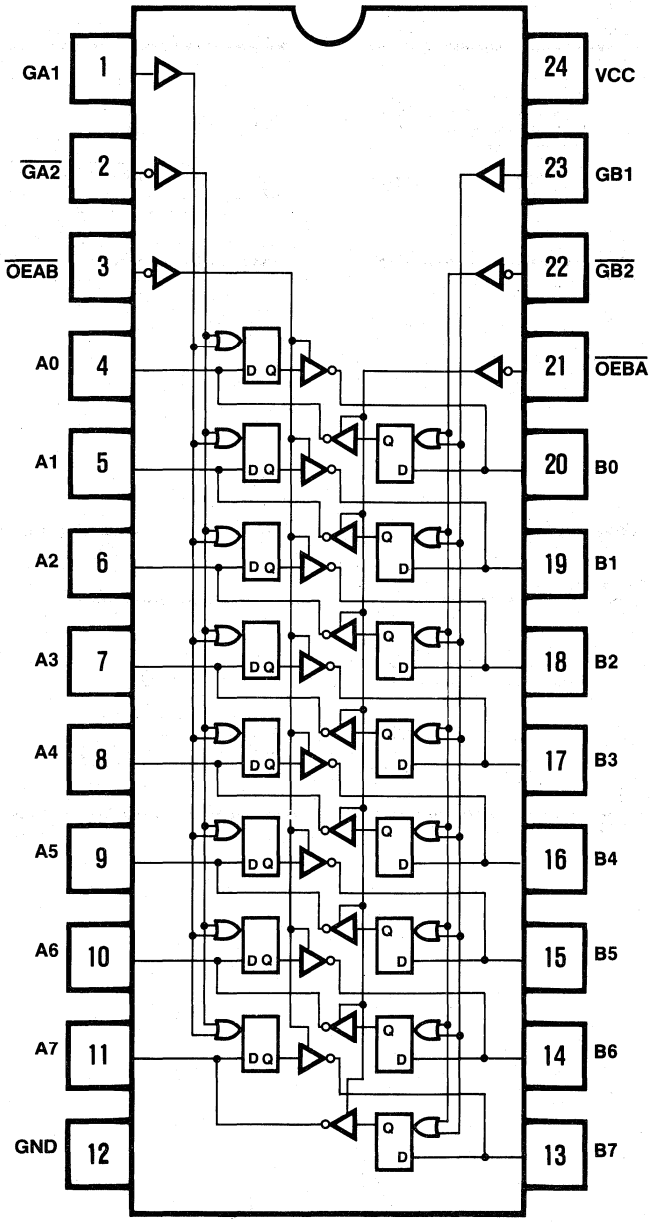
Logic Diagram

SN54/74LS566
REGISTER TRANSCEIVER
INVERTING OUTPUTS



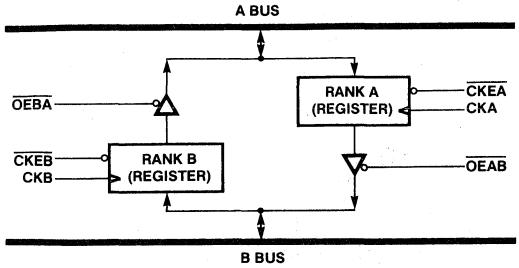
Logic Diagram

SN54/74LS567
LATCH TRANSCEIVER
INVERTING OUTPUTS

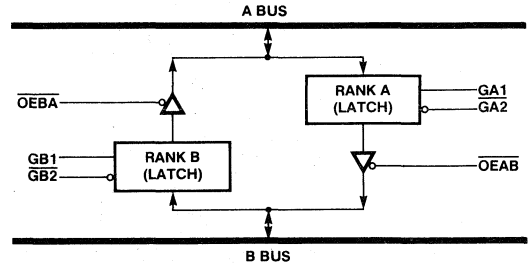


Block Diagrams

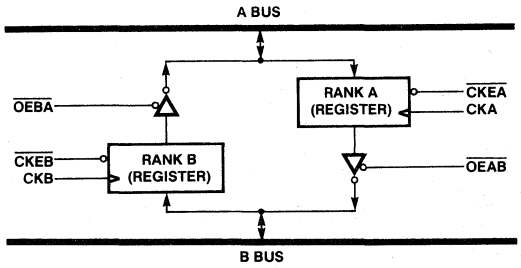
'LS546 (Non-inverting)



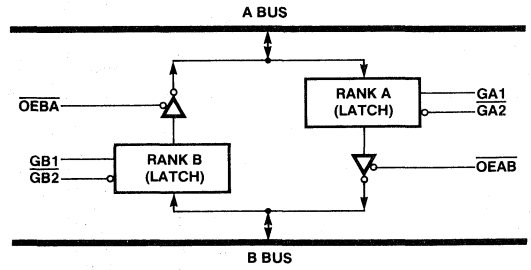
'LS547 (Non-inverting)



'LS566 (Inverting)

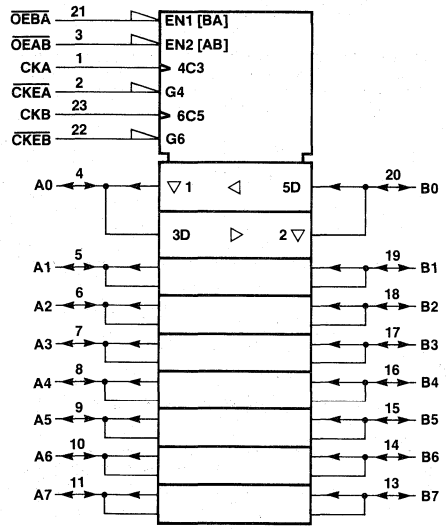


'LS567 (Inverting)

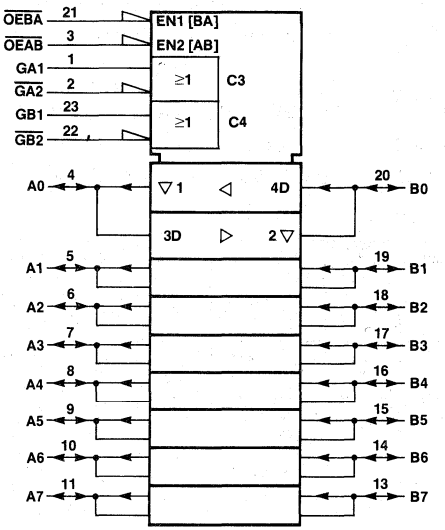


IEEE Symbols

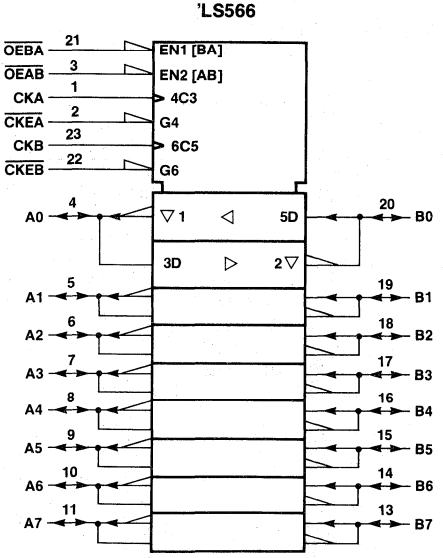
'LS546



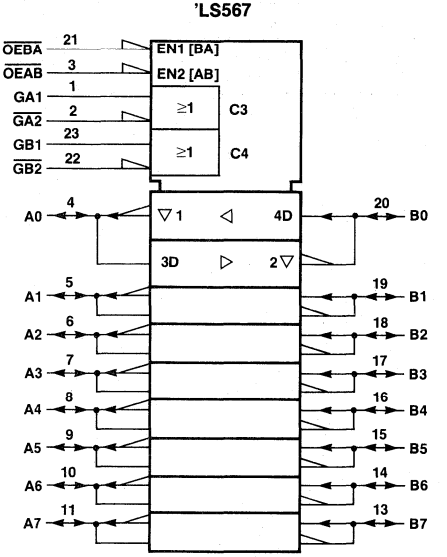
'LS547



'LS566



'LS567



13

Function Table Nomenclature Description

A0-A7: Eight input/output pins on the A side.

B0-B7: Eight input/output pins on the B side.

X: H or L state irrelevant ("Don't Care" conditions).

GA1/$\overline{GA2}$: Gate enables for rank A of 'LS547/'LS567.

GB1/$\overline{GB2}$: Gate enables for rank B of 'LS547/'LS567.

QoA/QoB: Previous data of the internal rank A/B.

GA1	$\overline{GA2}$	RANK A	GB1	$\overline{GB2}$	RANK B
X	L	Enabled (Flush)	X	L	Enabled (Flush)
X	L	Enabled (Flush)	L	H	Disabled (Freeze)
X	L	Enabled (Flush)	H	X	Enabled (Flush)
L	H	Disabled (Freeze)	H	X	Enabled (Flush)
L	H	Disabled (Freeze)	X	L	Enabled (Flush)
L	H	Disabled (Freeze)	L	H	Disabled (Freeze)
H	X	Enabled (Flush)	X	L	Enabled (Flush)
H	X	Enabled (Flush)	L	H	Disabled (Freeze)
H	X	Enabled (Flush)	H	X	Enabled (Flush)

$\overline{CKEA}$/$\overline{CKEB}$: Clock enable for rank A/B of 'LS546/'LS566.

CKA/CKB: Clock for rank A/B of 'LS546/'LS566.

UC: H or L or ↓ case (nonclocked operation).

↑: Positive edge of CK causes clocking, if clock enable is asserted.

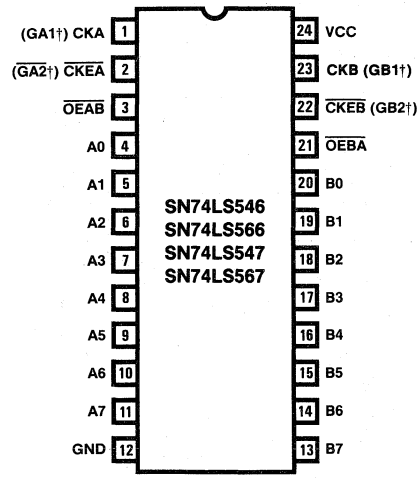
CKA	$\overline{CKEA}$	RANK A	CKB	$\overline{CKEB}$	RANK B
UC	X	Disabled	UC	X	Disabled
↑	L	Enabled	↑	L	Enabled
↑	L	Enabled	↑	H	Disabled
↑	H	Disabled	↑	L	Enabled
↑	H	Disabled	↑	H	Disabled

$\overline{OEAB}$: To enable the A-to-B operation.

$\overline{OEBA}$: To enable the B-to-A operation.

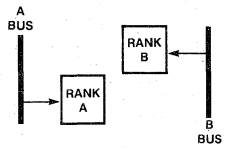
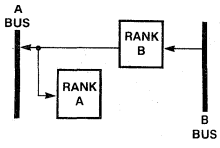
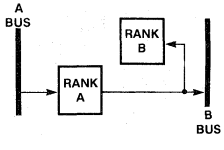
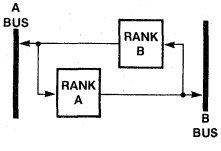
$\overline{OEAB}$	$\overline{OEBA}$	OPERATION DIRECTION
L	L	A, B buses both are outputs (Transfer stored data to bus stored)
L	H	A-to-B
H	L	B-to-A
H	H	A, B buses both are inputs (storage)

Pin Configuration



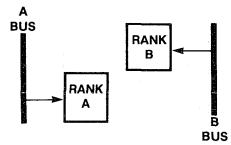
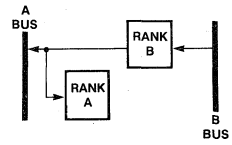
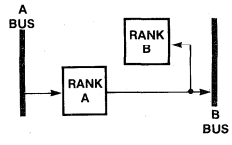
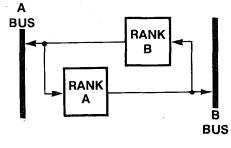
†For SN74LS547, SN74LS567

Bus Operation For 'LS546

OPERATION	DIRECTION CONTROL		DATA I/O		BLOCK DIAGRAM	CLOCK ENABLE (A)		RANK A	CLOCK ENABLE (B)		RANK B
	$\overline{OEAB}$	$\overline{OEBA}$	A0-A7	B0-B7		CKA	$\overline{CKEA}$		CKB	$\overline{CKEB}$	
Storage	H	H	Input	Input		UC	X	QoA	UC	X	QoB
						UC	X	QoA	↑	L	B bus
						UC	X	QoA	↑	H	QoB
						↑	L	A bus	UC	X	QoB
						↑	L	A bus	↑	L	B bus
						↑	L	A bus	↑	H	QoB
						↑	H	QoA	UC	X	QoB
						↑	H	QoA	↑	L	B bus
						↑	H	QoA	↑	H	QoB
B-to-A Operation	H	L	Output of Rank B	Input		UC	X	QoA	UC	X	QoB
						UC	X	QoA	↑	L	B bus
						UC	X	QoA	↑	H	QoB
						↑	L	Rank B	UC	X	QoB
						↑	L	Rank B	↑	L	B bus
						↑	L	Rank B	↑	H	QoB
						↑	H	QoA	UC	X	QoB
						↑	H	QoA	↑	L	B bus
						↑	H	QoA	↑	H	QoB
A-to-B Operation	L	H	Input	Output of Rank A		UC	X	QoA	UC	X	QoB
						UC	X	QoA	↑	L	Rank A
						UC	X	QoA	↑	H	QoB
						↑	L	A bus	UC	X	QoB
						↑	L	A bus	↑	L	Rank A
						↑	L	A bus	↑	H	QoB
						↑	H	QoA	UC	X	QoB
						↑	H	QoA	↑	L	Rank A
						↑	H	QoA	↑	H	QoB
Transfer Stored Data	L	L	Output of Rank B	Output of Rank A		UC	X	QoA	UC	X	QoB
						UC	X	QoA	↑	L	Rank A
						UC	X	QoA	↑	H	QoB
						↑	L	Rank B	UC	X	QoB
						↑	L	Rank B	↑	L	Rank A
						↑	L	Rank B	↑	H	QoB
						↑	H	QoA	UC	X	QoB
						↑	H	QoA	↑	L	Rank A
						↑	H	QoA	↑	H	QoB

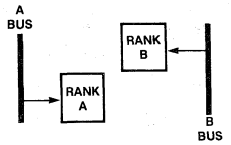
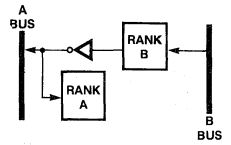
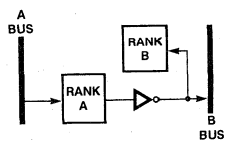
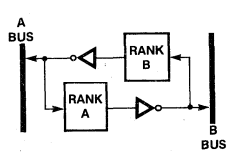
13

Bus Operation For 'LS547

OPERATION	DIRECTION CONTROL		DATA I/O		BLOCK DIAGRAM	GATE ENABLE (A)		RANK A	GATE ENABLE (B)		RANK B
	$\overline{OEAB}$	$\overline{OEBA}$	A0-A7	B0-B7		GA1	$\overline{GA2}$		GB1	$\overline{GB2}$	
Storage	H	H	Input	Input		L	H	QoA	L	H	QoB
						L	H	QoA	H	X	B bus
						L	H	QoA	X	L	B bus
						H	X	A bus	L	H	QoB
						H	X	A bus	H	X	B bus
						H	X	A bus	X	L	B bus
						X	L	A bus	L	H	QoB
						X	L	A bus	H	X	B bus
						X	L	A bus	X	L	B bus
B-to-A Operation	H	L	Output of Rank B	Input		L	H	QoA	L	H	QoB
						L	H	QoA	H	X	B bus
						L	H	QoA	X	L	B bus
						H	X	Rank B	L	H	QoB
						H	X	Rank B	H	X	B bus
						H	X	Rank B	X	L	B bus
						X	L	Rank B	L	H	QoB
						X	L	Rank B	H	X	B bus
						X	L	Rank B	X	L	B bus
A-to-B Operation	L	H	Input	Output of Rank A		L	H	QoA	L	H	QoB
						L	H	QoA	H	X	Rank A
						L	H	QoA	X	L	Rank A
						H	X	A bus	L	H	QoB
						H	X	A bus	H	X	Rank A
						H	X	A bus	X	L	Rank A
						X	L	A bus	L	H	QoB
						X	L	A bus	H	X	Rank A
						X	L	A bus	X	L	Rank A
Transfer Stored Data	L	L	Output of Rank B	Output of Rank A		L	H	QoA	L	H	QoB
						L	H	QoA	H	X	Rank A
						L	H	QoA	X	L	Rank A
						H	X	Rank B	L	H	QoB
						H*	X	Rank B	H	X	Rank A
						H*	X	Rank B	X	L	Rank A
						X	L	Rank B	L	H	QoB
						X*	L	Rank B	H	X	Rank A
						X*	L	Rank B	X	L	Rank A

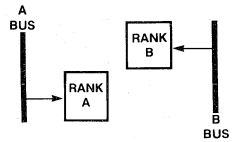
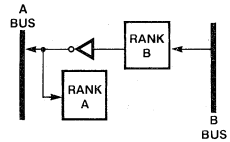
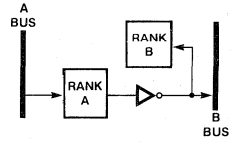
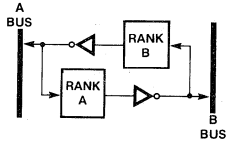
* NOTE: These controls for $\overline{OEAB}$, $\overline{OEBA}$, GA1, $\overline{GA2}$, GB1 and $\overline{GB2}$ can cause race conditions.

Bus Operation For 'LS566

OPERATION	DIRECTION CONTROL		DATA I/O		BLOCK DIAGRAM	CLOCK ENABLE (A)		RANK A	CLOCK ENABLE (B)		RANK B
	$\overline{OEAB}$	$\overline{OEBA}$	A0-A7	B0-B7		CKA	$\overline{CKEA}$		CKB	$\overline{CKEB}$	
Storage	H	H	Input	Input		UC	X	QoA	UC	X	QoB
						UC	X	QoA	↑	L	B bus
						UC	X	QoA	↑	H	QoB
						↑	L	A bus	UC	X	QoB
						↑	L	A bus	↑	L	B bus
						↑	L	A bus	↑	H	QoB
						↑	H	QoA	UC	X	QoB
						↑	H	QoA	↑	L	B bus
						↑	H	QoA	↑	H	QoB
B-to-A Operation	H	L	Output of $\overline{\text{Rank B}}$	Input		UC	X	QoA	UC	X	QoB
						UC	X	QoA	↑	L	B bus
						UC	X	QoA	↑	H	QoB
						↑	L	$\overline{\text{Rank B}}$	UC	X	QoB
						↑	L	$\overline{\text{Rank B}}$	↑	L	B bus
						↑	L	$\overline{\text{Rank B}}$	↑	H	QoB
						↑	H	QoA	UC	X	QoB
						↑	H	QoA	↑	L	B bus
						↑	H	QoA	↑	H	QoB
A-to-B Operation	L	H	Input	Output of $\overline{\text{Rank A}}$		UC	X	QoA	UC	X	QoB
						UC	X	QoA	↑	L	$\overline{\text{Rank A}}$
						UC	X	QoA	↑	H	QoB
						↑	L	A bus	UC	X	QoB
						↑	L	A bus	↑	L	$\overline{\text{Rank A}}$
						↑	L	A bus	↑	H	QoB
						↑	H	QoA	UC	X	QoB
						↑	H	QoA	↑	L	$\overline{\text{Rank A}}$
						↑	H	QoA	↑	H	QoB
Transfer Stored Data	L	L	Output of $\overline{\text{Rank B}}$	Output of $\overline{\text{Rank A}}$		UC	X	QoA	UC	X	QoB
						UC	X	QoA	↑	L	$\overline{\text{Rank A}}$
						UC	X	QoA	↑	H	QoB
						↑	L	$\overline{\text{Rank B}}$	UC	X	QoB
						↑	L	$\overline{\text{Rank B}}$	↑	L	$\overline{\text{Rank A}}$
						↑	L	$\overline{\text{Rank B}}$	↑	H	QoB
						↑	H	QoA	UC	X	QoB
						↑	H	QoA	↑	L	$\overline{\text{Rank A}}$
						↑	H	QoA	↑	H	QoB

13

Bus Operation For 'LS567

OPERATION	DIRECTION CONTROL		DATA I/O		BLOCK DIAGRAM	GATE ENABLE (A)		RANK A	GATE ENABLE (B)		RANK B
	$\overline{OEAB}$	$\overline{OEBA}$	A0-A7	B0-B7		GA1	$\overline{GA2}$		GB1	$\overline{GB2}$	
Storage	H	H	Input	Input		L	H	QoA	L	H	QoB
						L	H	QoA	H	X	B bus
						L	H	QoA	X	L	B bus
						H	X	A bus	L	H	QoB
						H	X	A bus	H	X	B bus
						H	X	A bus	X	L	B bus
						X	L	A bus	L	H	QoB
						X	L	A bus	H	X	B bus
						X	L	A bus	X	L	B bus
B-to-A Operation	H	L	Output of $\overline{\text{Rank B}}$	Input		L	H	QoA	L	H	QoB
						L	H	QoA	H	X	B bus
						L	H	QoA	X	L	B bus
						H	X	$\overline{\text{Rank B}}$	L	H	QoB
						H	X	$\overline{\text{Rank B}}$	H	X	B bus
						H	X	$\overline{\text{Rank B}}$	X	L	B bus
						X	L	$\overline{\text{Rank B}}$	L	H	QoB
						X	L	$\overline{\text{Rank B}}$	H	X	B bus
						X	L	$\overline{\text{Rank B}}$	X	L	B bus
A-to-B Operation	L	H	Input	Output of $\overline{\text{Rank A}}$		L	H	QoA	L	H	QoB
						L	H	QoA	H	X	$\overline{\text{Rank A}}$
						L	H	QoA	X	L	$\overline{\text{Rank A}}$
						H	X	A bus	L	H	QoB
						H	X	A bus	H	X	$\overline{\text{Rank A}}$
						H	X	A bus	X	L	$\overline{\text{Rank A}}$
						X	L	A bus	L	H	QoB
						X	L	A bus	H	X	$\overline{\text{Rank A}}$
						X	L	A bus	X	L	$\overline{\text{Rank A}}$
Transfer Stored Data	L	L	Output of $\overline{\text{Rank B}}$	Output of $\overline{\text{Rank A}}$		L	H	QoA	L	H	QoB
						L	H	QoA	H	X	$\overline{\text{Rank A}}$
						L	H	QoA	X	L	$\overline{\text{Rank A}}$
						H	X	$\overline{\text{Rank B}}$	L	H	QoB
						H*	X	$\overline{\text{Rank B}}$	H	X	$\overline{\text{Rank A}}$
						H*	X	$\overline{\text{Rank B}}$	X	L	$\overline{\text{Rank A}}$
						X	L	$\overline{\text{Rank B}}$	L	H	QoB
						X*	L	$\overline{\text{Rank B}}$	H	X	$\overline{\text{Rank A}}$
						X*	L	$\overline{\text{Rank B}}$	X	L	$\overline{\text{Rank A}}$

* NOTE: These controls for $\overline{OEAB}$, $\overline{OEBA}$, GA1, $\overline{GA2}$, GB1 and $\overline{GB2}$ can cause race conditions.

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER				MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage				4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature				-55		125	0		75	°C
T_W	Width of clock/gate	'LS546, 'LS566	High	CK	11			8			ns
			Low		19			15			
		'LS547, 'LS567	High	GA1,GB1	10			8			
			Low	$\overline{GA2}$,$\overline{GB2}$	18			16			
T_{su}	Setup time	'LS546	CKA, CKB		14↑			11↑			ns
		'LS547	GA1, GB1		5↓			5↓			
			$\overline{GA2}$, $\overline{GB2}$		15↑			15↑			
		'LS566	CKA, CKB		14↑			11↑			
		'LS567	GA1, GB1		13↓			13↓			
			$\overline{GA2}$, $\overline{GB2}$		22↑			22↑			
T_h	Hold time	'LS546	CKA, CKB		0↑			0↑			ns
		'LS547	GA1, GB1		13↓			13↓			
			$\overline{GA2}$, $\overline{GB2}$		5↑			5↑			
		'LS566	CKA, CKB		0↑			0↑			
		'LS567	GA1, GB1		11↓			11↓			
			$\overline{GA2}$, $\overline{GB2}$		5↑			5↑			
T_{suce}	Setup time for $\overline{CKEA}$, $\overline{CKEB}$, ('LS546, 'LS566 only)				15↑			11↑			ns
T_{hce}	Hold time for $\overline{CKEA}$, $\overline{CKEB}$ ('LS546, 'LS566 only)				5↑			4↑			ns

↑ ↓ the arrow indicates the transition of the clock/gate input used for reference:
↑ for the low-to-high transitions.
↓ for the high-to-low transitions.

13

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IH}	High-level input voltage				2			2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18 mA			−1.5			−1.5	V
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4 V	A or B			−250			−250	μA
				All others			−400			−400	
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7 V			20			20	μA
I_I	Maximum input current	A or B	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
		All others		V_I = 7.0 V							
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OL} = 24 mA			0.5				V
				I_{OL} = 32 mA					0.35	0.5	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OH} = −1 mA	2.4	3.4					V
				I_{OH} = −2.6 mA				2.4	3.1		
I_{OZL}	Off-state output current		V_{CC} = MAX	V_O = 0.4 V			−250			−250	μA
I_{OZH}				V_O = 2.4 V			20			20	
I_{OS}	Output short-circuit current*		V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply current		V_{CC} = MAX, Outputs open	'LS546			180			180	mA
				'LS547			180			180	
				'LS566			180			180	
				'LS567			180			180	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY		COMMERCIAL		UNIT
			'LS546 MIN MAX	'LS547 MIN MAX	'LS546 MIN MAX	'LS547 MIN MAX	
f_{MAX}	Maximum clock frequency	C_L = 45 pF R_L = 280 Ω $\overline{OE}$ = L	33		43		MHz
t_{PLH}/t_{PHL}	CK to output delay ('LS546 only)		26		21		ns
t_{PLH}/t_{PHL}	$\overline{GA1}$, $\overline{GA2}$, GB1 or $\overline{GB2}$ to output delay ('LS547 only)			27		24	ns
t_{PLH}/t_{PHL}	Data D to output delay ('LS547 only)			23		18	ns
t_{PZL}/t_{PZH}	Output enable delay	C_L = 45 pF R_L = 280 Ω	25	25	21	21	ns
t_{PLZ}/t_{PHZ}	Output disable delay	C_L = 5 pF R_L = 280 Ω	22	22	19	19	ns

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS	'LS546 MIN MAX	'LS547 MIN MAX	UNIT
f_{MAX}	Maximum clock frequency	C_L = 45 pF R_L = 280 Ω $\overline{OE}$ = L	50		MHz
t_{PLH}/t_{PHL}	CK to output delay ('LS546 only)		19		ns
t_{PLH}/t_{PHL}	GA1, $\overline{GA2}$, GB1 or $\overline{GB2}$ to output delay ('LS547 only)			23	ns
t_{PLH}/t_{PHL}	Data D to output delay ('LS547 only)			17	ns
t_{PZL}/t_{PZH}	Output enable delay	C_L = 45 pF R_L = 280 Ω	19	19	ns
t_{PLZ}/t_{PHZ}	Output disable delay	C_L = 5 pF R_L = 280 Ω	17	17	ns

13

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY		COMMERCIAL		UNIT
			'LS566 MIN MAX	'LS567 MIN MAX	'LS566 MIN MAX	'LS567 MIN MAX	
f_{MAX}	Maximum clock frequency	C_L = 45 pF R_L = 280 Ω $\overline{OE}$ = L	33		43		MHz
t_{PLH}/t_{PHL}	CK to output delay ('LS566 only)		26		21		ns
t_{PLH}/t_{PHL}	$\overline{GA1}$, $\overline{GA2}$, GB1 or $\overline{GB2}$ to output delay ('LS567 only)			26		24	ns
t_{PLH}/t_{PHL}	Data D to output delay ('LS567 only)			29		23	ns
t_{PZL}/t_{PZH}	Output enable delay	C_L = 45 pF R_L = 280 Ω	25	25	21	21	ns
t_{PLZ}/t_{PHZ}	Output disable delay	C_L = 5 pF R_L = 280 Ω	22	22	19	19	ns

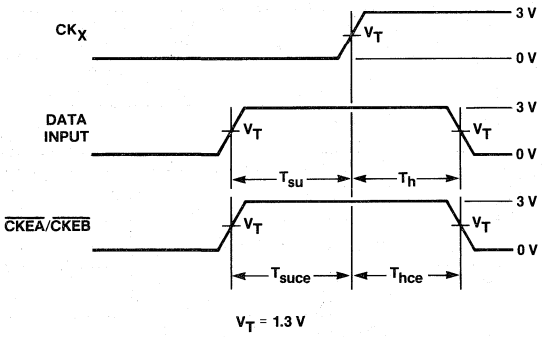
Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS	'LS566 MIN MAX	'LS567 MIN MAX	UNIT
f_{MAX}	Maximum clock frequency	C_L = 45 pF R_L = 280 Ω $\overline{OE}$ = L	50		MHz
t_{PLH}/t_{PHL}	CK to output delay ('LS566 only)		19		ns
t_{PLH}/t_{PHL}	GA1, $\overline{GA2}$, GB1 or $\overline{GB2}$ to output delay ('LS567 only)			21	ns
t_{PLH}/t_{PHL}	Data D to output delay ('LS567 only)			19	ns
t_{PZL}/t_{PZH}	Output enable delay	C_L = 45 pF R_L = 280 Ω	19	19	ns
t_{PLZ}/t_{PHZ}	Output disable delay	C_L = 5 pF R_L = 280 Ω	17	17	ns

Definition of Waveforms

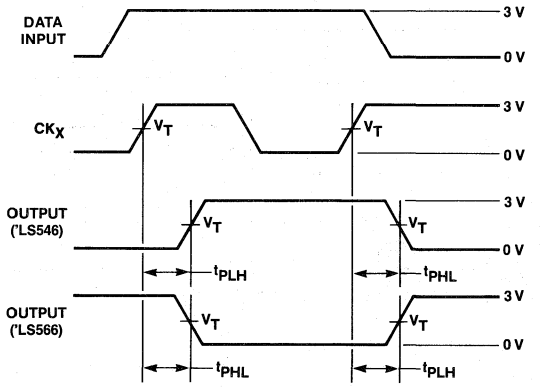
'LS546/566

Setup and Hold



V_T = 1.3 V

Clock CK to Output Delay



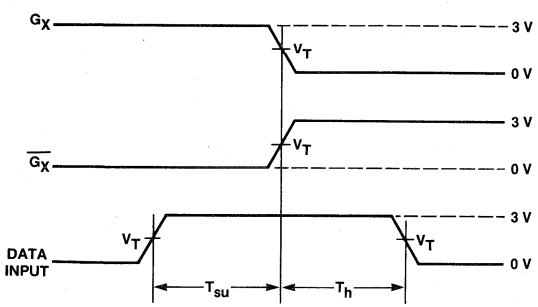
V_T = 1.3 V

13

Definition of Waveforms

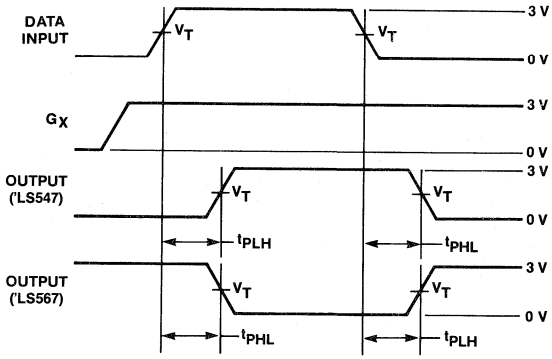
'LS547/567

Setup and Hold



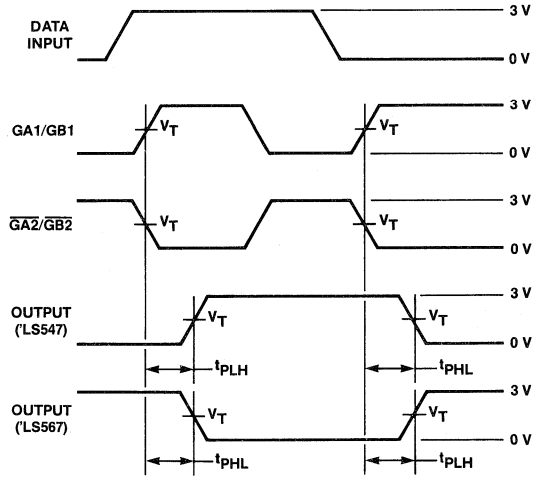
V_T = 1.3 V

Data D to Output Delay



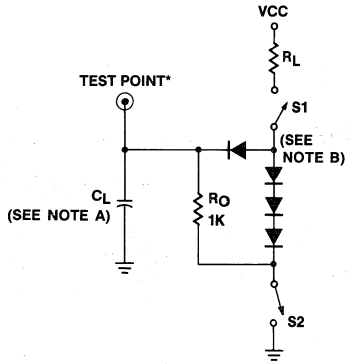
V_T = 1.3 V

GA1, $\overline{GA2}$, GB1 or $\overline{GB2}$ to Output Delay

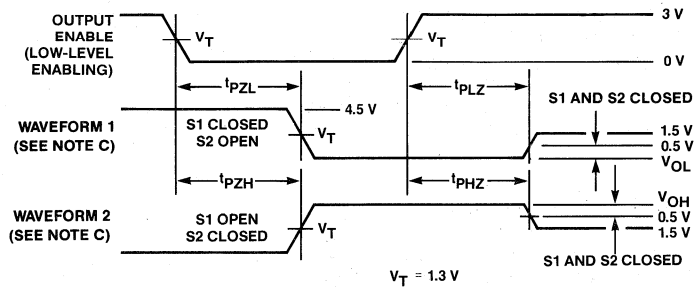


V_T = 1.3 V

Test Load



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.



ENABLE AND DISABLE

NOTES: A. C_L includes probe and jig capacitance.

B. All diodes are 1N916 or 1N3064.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} = 50Ω and t_R ≤ 15 ns t_F ≤ 6 ns.

F. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

13

8-Bit Bus Front-Loading-Latch Transceivers

SN54/74LS646
SN54/74LS648
SN54/74LS647
SN54/74LS649

Features/Benefits

- **Bidirectional bus transceivers and registers**
- **Independent registers for A and B buses**
- **Real-time data transfer or stored data transfer**
- **24-pin SKINNYDIP® saves space**
- **8-bit data path matches byte boundaries**
- **Three-state or open-collector outputs drive bus lines**

Description

The 8-bit bus transceivers with 3-state ('LS646, 'LS648) or open-collector ('LS647, 'LS649) outputs have 16 D-type flip-flops and multiplexers. The bus-oriented pinout of the parts is shown in the Pin Configuration. The internal gate-level hardware configurations for the 'LS646/647 and 'LS648/649 are given in their respective Logic Diagrams. The basic repeated element, consisting of an edge-triggered flip-flop paralleled with a bypassing path or "feed-through" into a two-way mux, is sometimes called a "front-loading latch."

A pair of multiplexers are used to distribute two bytes of data through the part. The data-routing combinations offered by the multiplexers provide flexibility in directing data to or from either bus, and/or either register. Data is loaded into registers A or B upon the rising edge of the appropriate clock signals. CKA clocks register A, which receives data from the B bus directly at its inputs. Similarly, CKB clocks register B, which has the A bus available directly at its inputs. Control of the multiplexers is provided by two select lines (one per register), SRA and SRB. Command of the outputs is performed by enable line $\overline{E}$, and direction line DIR.

When $\overline{E}$ is High data from the buses can be stored into register A and B. When $\overline{E}$ is Low and DIR is High, the direction of operation is from A to B; when $\overline{E}$ and DIR are LOW, the direction of operation is from B to A.

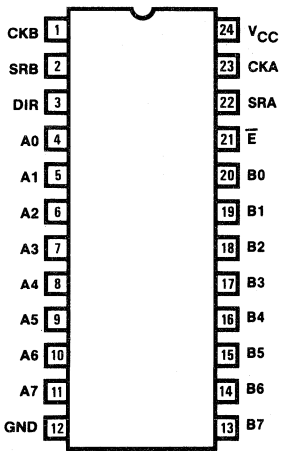
SRA is used to select between register A and the B bus, and then to route the data to a controlled buffer connected to the A bus. Likewise, SRB selects between register B and the A bus, and then routes the data to the B bus through a controlled buffer.

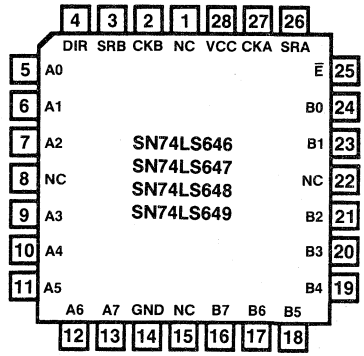
Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	O/P	PWR
SN54LS646	JS,W,L (28)	Mil	Noninvert	Three-state	LS
SN54LS646	NS,JS NL (28)	Com	Noninvert	Three-state	LS
SN54LS647	JS,W,L (28)	Mil	Noninvert	Open-collector	LS
SN74LS647	NS,JS NL (28)	Com	Noninvert	Open-collector	LS
SN54LS648	JS,W,L (28)	Mil	Invert	Three-state	LS
SN54LS648	NS,JS NL (28)	Com	Invert	Three-state	LS
SN54LS649	JS,W,L (28)	Mil	Invert	Open-collector	LS
SN74LS649	NS,JS NL (28)	Com	Invert	Open-collector	LS

Pin Configurations

'LS646/647/648/649
8-Bit Bus Front-Loading-Latch Transceivers





Plastic Chip Carrier

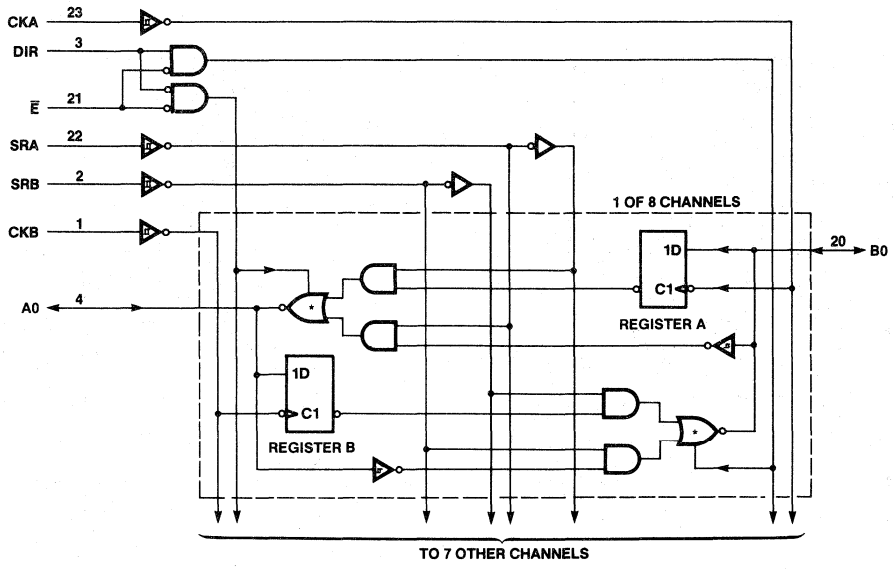
SKINNYDIP® is a registered trademark of Monolithic Memories.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Monolithic Memories MMI

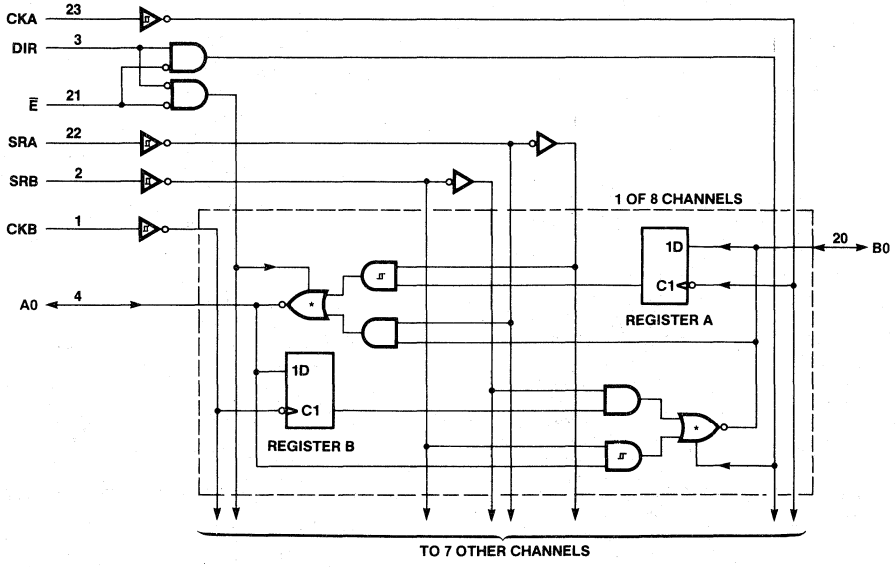
Logic Diagrams

'LS646/647 (Non-Inverting)



* For the 'LS646 devices, the A and B bus outputs are 3-state.
For the 'LS647 devices, the A and B bus outputs are open-collector.

'LS648/649 (Inverting)

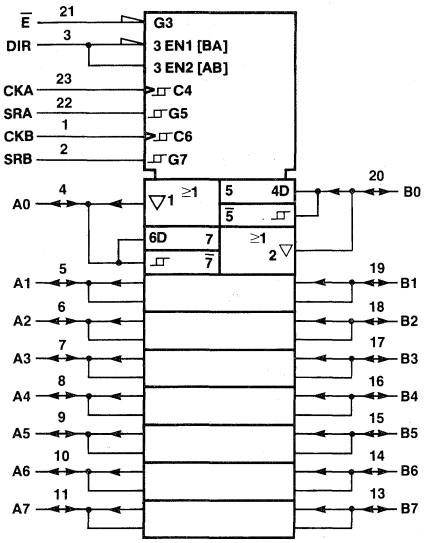


* For the 'LS648 devices, the A and B bus outputs are 3-state.
For the 'LS649 devices, the A and B bus outputs are open-collector.

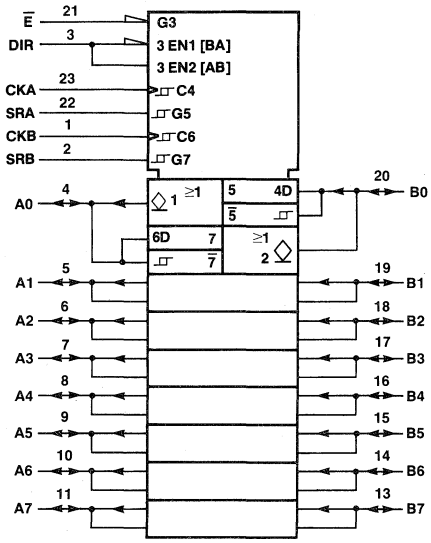
13

IEEE Symbols

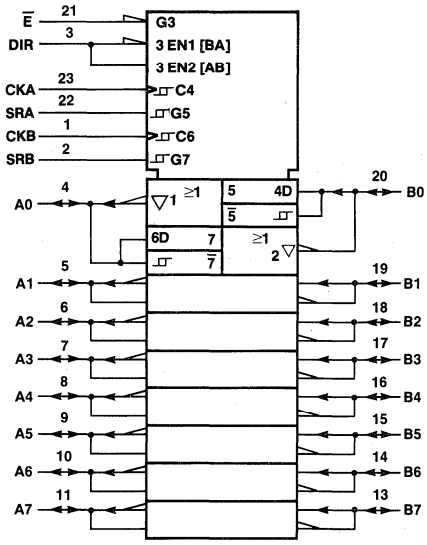
'LS646



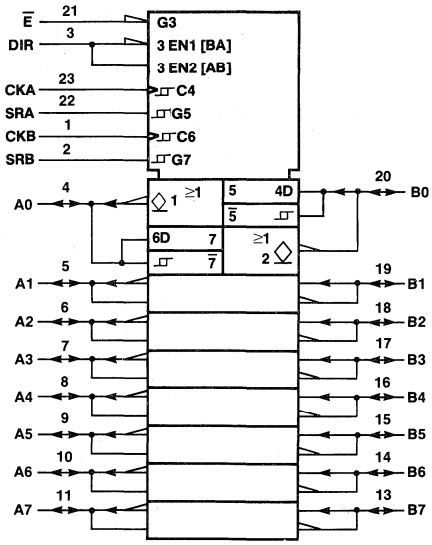
'LS647



'LS648

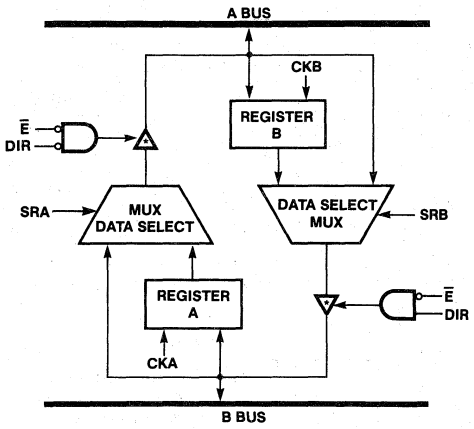


'LS649

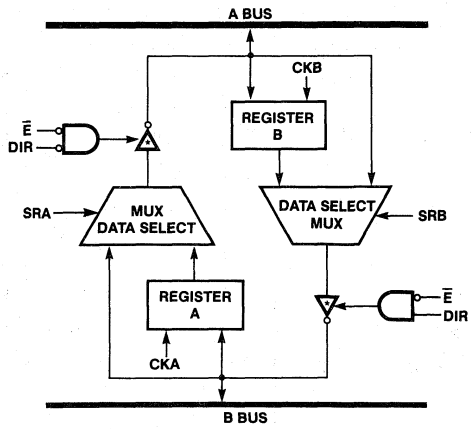


Block Diagrams

'LS646/647 (Non-Inverting)



'LS648/649 (Inverting)



* For the 'LS646/648 devices, the A and B bus outputs are 3-state.
For the 'LS647/649 devices, the A and B bus outputs are open-collector.

Function Table Nomenclature Description

Ē: To enable the A-to-B or B-to-A operation.

DIR: To select the direction of operation.

Ē	DIR	OPERATION DIRECTION
L	L	B-to-A
L	H	A-to-B
H	X	A and B buses both are inputs (storage)

SRA/SRB: To select the output data coming from the A/B register if SRA/SRB is a High level; otherwise, directly from the input data bus.

A0-A7: Eight input/output pins on the A side.

B0-B7: Eight input/output pins on the B side.

CKA/CKB: Clock for Register A/B.

X: H or L state irrelevant ("Don't Care" conditions).

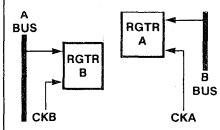
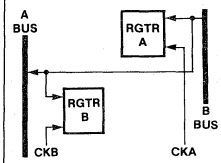
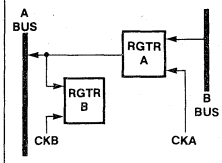
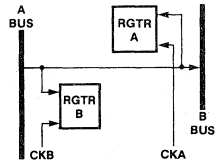
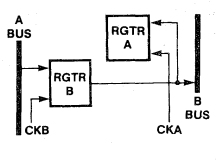
↑: Positive edge of CK causes clocking, if clock enable is asserted.

UC: H or L or ↓ case (nonclocked operation).

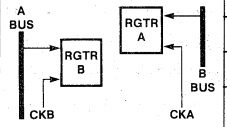
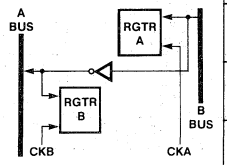
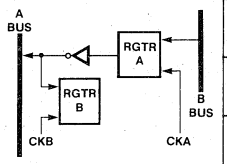
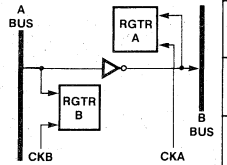
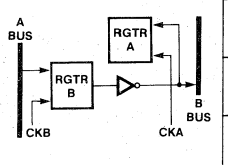
RGTR: Register.

13

Bus Operation for 'LS646/647

OPERATION	CONTROL				DATA I/O		BLOCK DIAGRAM	CLOCK ENABLE		'LS646/647
	$\overline{E}$	DIR	SRA	SRB	A0-A7	B0-B7		CKA	CKB	
Storage	H	X	X	X	Input	Input		UC	UC	No operation
								UC	↑	Real time A bus data → RGTR B
								↑	UC	Real time B bus data → RGTR A
								↑	↑	Real time A bus data → RGTR B Real time B bus data → RGTR A
Real time B-to-A Operation	L	L	L	X	Output	Input		UC	UC	Real time B bus data → A bus
								UC	↑	Real time B bus data → A bus Real time B bus data → RGTR B
								↑	UC	Real time B bus data → A bus Real time B bus data → RGTR A
								↑	↑	Real time B bus data → A bus Real time B bus data → RGTR A Real time B bus data → RGTR B
Stored data B-to-A Operation	L	L	H	X	Output	Input		UC	UC	RGTR A data → A bus
								UC	↑	RGTR A data → A bus RGTR A data → RGTR B
								↑	UC	Real time B bus data → RGTR A RGTR A data → A bus
								↑	↑	Real time B bus data → RGTR A RGTR A data → A bus RGTR A data → RGTR B
Real time A-to-B Operation	L	H	X	L	Input	Output		UC	UC	Real time A bus data → B bus
								UC	↑	Real time A bus data → B bus Real time A bus data → RGTR B
								↑	UC	Real time A bus data → B bus Real time A bus data → RGTR A
								↑	↑	Real time A bus data → B bus Real time A bus data → RGTR A Real time A bus data → RGTR B
Stored data A-to-B Operation	L	H	X	H	Input	Output		UC	UC	RGTR B data → B bus
								UC	↑	Real time A bus data → RGTR B RGTR B data → B bus
								↑	UC	RGTR B data → B bus RGTR B data → RGTR A
								↑	↑	Real time A bus data → RGTR B RGTR B data → B bus RGTR B data → RGTR A

Bus Operation for 'LS648/649

OPERATION	CONTROL				DATA I/O		BLOCK DIAGRAM	CLOCK ENABLE		'LS648/649
	$\overline{E}$	DIR	SRA	SRB	A0-A7	B0-B7		CKA	CKB	
Storage	H	X	X	X	Input	Input		UC	UC	No operation
								UC	↑	Real time A bus data → RGTR B
								↑	UC	Real time B bus data → RGTR A
								↑	↑	Real time A bus data → RGTR B Real time B bus data → RGTR A
Real time B-to-A Operation	L	L	L	X	Output	Input		UC	UC	Real time $\overline{B}$ bus data → A bus
								UC	↑	Real time $\overline{B}$ bus data → A bus Real time $\overline{B}$ bus data → RGTR B
								↑	UC	Real time $\overline{B}$ bus data → A bus Real time B bus data → RGTR A
								↑	↑	Real time $\overline{B}$ bus data → A bus Real time B bus data → RGTR A Real time $\overline{B}$ bus data → RGTR B
Stored data B-to-A Operation	L	L	H	X	Output	Input		UC	UC	RGTR $\overline{A}$ data → A bus
								UC	↑	RGTR $\overline{A}$ data → A bus RGTR $\overline{A}$ data → RGTR B
								↑	UC	Real time B bus data → RGTR A RGTR $\overline{A}$ data → A bus
								↑	↑	Real time B bus data → RGTR A RGTR $\overline{A}$ data → A bus RGTR $\overline{A}$ data → RGTR B
Real time A-to-B Operation	L	H	X	L	Input	Output		UC	UC	Real time $\overline{A}$ bus data → B bus
								UC	↑	Real time $\overline{A}$ bus data → B bus Real time A bus data → RGTR B
								↑	UC	Real time $\overline{A}$ bus data → B bus Real time $\overline{A}$ bus data → RGTR A
								↑	↑	Real time $\overline{A}$ bus data → B bus Real time $\overline{A}$ bus data → RGTR A Real time A bus data → RGTR B
Stored data A-to-B Operation	L	H	X	H	Input	Output		UC	UC	RGTR $\overline{B}$ data → B bus
								UC	↑	Real time A bus data → RGTR B RGTR $\overline{B}$ data → B bus
								↑	UC	RGTR $\overline{B}$ data → B bus RGTR $\overline{B}$ data → RGTR A
								↑	↑	Real time A bus data → RGTR B RGTR $\overline{B}$ data → B bus RGTR $\overline{B}$ data → RGTR A

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature		-55		125	0		75	°C
t_w	Width of clock	High	20			20			ns
		Low	20			20			
t_{su}	Setup time	'LS646	20 ↑			20 ↑			ns
		'LS648	20 ↑			20 ↑			
t_h	Hold time	'LS646	0 ↑			0 ↑			ns
		'LS648	0 ↑			0 ↑			
I_{OH}	High-level output current				-12			-15	mA
I_{OL}	Low-level output current				12			24	mA

↑ ↓ The arrow indicates the transition of the clock input used for reference. ↑ for the low-to-high transitions. ↓ for the high-to-low transitions.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IH}	High-level input voltage				2			2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = -18 mA			-1.5			-1.5	V
ΔV_T	Hysteresis (V_{T+}-V_{T-})		V_{CC} = MIN		0.1	0.4		0.2	0.4		V
I_{IL}	Low-level input current		V_{CC} = MAX	V_I = 0.4 V			-0.4			-0.4	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7 V			20			20	μA
I_I	Maximum input current	A or B	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
		All others		V_I = 7 V							
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OH} = -3 mA	2.4	3.4		2.4	3.4		V
				I_{OH} = MAX	2			2			
I_{OZL}	Off-state output current		V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2 V	V_O = 0.4 V			-400			-400	μA
I_{OZH}				V_O = 2.7 V			20			20	μA
I_{OS}	Output short-circuit current*		V_{CC} = MAX		-40		-225	-40		-225	mA
I_{CC}	Supply current		V_{CC} = MAX	'LS646 Outputs High			145			145	mA
				'LS646 Outputs Low			165			165	
				'LS646 Outputs Disabled			165			165	
				'LS648 Outputs High			145			145	
				'LS648 Outputs Low			165			165	
				'LS648 Outputs Disabled			165			165	

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	'LS646 MIN	'LS646 MAX	'LS648 MIN	'LS648 MAX	UNIT
t_{PLH}	Data to output delay	C_L = 45pF R_L = 667Ω		18		18	ns
t_{PHL}				20		25	ns
t_{PLH}	Clock to output delay			25		25	ns
t_{PHL}				35		40	ns
t_{PLH}	Select to output delay (data input High)			40		55	ns
t_{PHL}				35		40	ns
t_{PLH}	Select to output delay (data input Low)			50		40	ns
t_{PHL}				25		40	ns
t_{PZL}	Output enable delay			65		55	ns
t_{PZH}				55		50	ns
t_{PLZ}	Output disable delay	C_L = 5pF R_L = 667Ω		35		35	ns
t_{PHZ}				35		45	ns
t_{PZL}	Direction enable delay	C_L = 45pF R_L = 667Ω		60		45	ns
t_{PZH}				45		40	ns
t_{PLZ}	Direction disable delay	C_L = 5pF R_L = 667Ω		30		30	ns
t_{PHZ}				30		35	ns

Switching Characteristics Over Operating Range

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	MIL 'LS646 MIN	MIL 'LS646 MAX	MIL 'LS648 MIN	MIL 'LS648 MAX	COM 'LS646 MIN	COM 'LS646 MAX	COM 'LS648 MIN	COM 'LS648 MAX	UNIT
t_{PLH}	Data to output delay	C_L = 45pF R_L = 667Ω		25		18		25		18	ns
t_{PHL}				25		25		25		25	ns
t_{PLH}	Clock to output delay			28		25		28		25	ns
t_{PHL}				35		40		35		40	ns
t_{PLH}	Select to output delay † (data input High)			40		55		40		55	ns
t_{PHL}				35		40		35		40	ns
t_{PLH}	Select to output delay † (data input Low)			50		40		50		40	ns
t_{PHL}				30		40		30		40	ns
t_{PZL}	Output enable delay			65		55		65		55	ns
t_{PZH}				55		50		55		50	ns
t_{PLZ}	Output disable delay	C_L = 5pF R_L = 667Ω		45		35		45		35	ns
t_{PHZ}				45		50		45		50	ns
t_{PZL}	Direction enable delay	C_L = 45pF R_L = 667Ω		60		45		60		45	ns
t_{PZH}				45		40		45		40	ns
t_{PLZ}	Direction disable delay	C_L = 5pF R_L = 667Ω		40		30		40		30	ns
t_{PHZ}				45		45		45		45	ns

† See Figure 4.

13

Absolute Maximum Ratings

Supply voltage, V_{CC} ..... 7.0 V
Input voltage, ... 7.0 V
Off-state output voltage ..... 5.5 V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature		−55		125	0		75	°C
t_w	Width of clock	High	20			20			ns
		Low	20			20			
t_{su}	Setup time	'LS647	20↑			20↑			ns
		'LS649	20↑			20↑			
t_h	Hold time	'LS647	0↑			0↑			ns
		'LS649	0↑			0↑			
V_{OH}	High-level output voltage				5.5			5.5	V
I_{OL}	Low-level output current				12			24	mA

↑ ↓ The arrow indicates the transition of the clock input used for reference. ↑ for the low-to-high transitions. ↓ for the high-to-low transitions.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IH}	High-level input voltage				2			2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18 mA			−1.5			−1.5	V
ΔV_T	Hysteresis (V_{T+}-V_{T-})		V_{CC} = MIN		0.1	0.4		0.2	0.4		V
I_{IL}	Low-level input current		V_{CC} = MAX	V_I = 0.4 V			−0.4			−0.4	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7 V			20			20	μA
I_I	Maximum input current	A or B	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
		All others		V_I = 7 V							
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	V_{OH} = 5.5 V			100			100	μA
I_{CC}	Supply current		V_{CC} = MAX	'LS-647, Outputs High			130			130	mA
				'LS-647, Outputs Low			150			150	
				'LS-647, Outputs Disabled			150			150	
				'LS-649, Outputs High			130			130	
				'LS-649, Outputs Low			150			150	
				'LS-649, Outputs Disabled			150			150	

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	'LS647 MIN	'LS647 MAX	'LS649 MIN	'LS649 MAX	UNIT
t_{PLH}	Data to output delay	C_L = 45pF R_L = 667Ω		26		25	ns
t_{PHL}				27		30	ns
t_{PLH}	Clock to output delay			35		30	ns
t_{PHL}				45		45	ns
t_{PLH}	Select to output delay† (data input High)			50		55	ns
t_{PHL}				45		45	ns
t_{PLH}	Select to output delay† (data input Low)			60		45	ns
t_{PHL}				30		40	ns
t_{PLH}	Output enable delay			40		40	ns
t_{PHL}				50		50	ns
t_{PLH}	Direction enable delay			35		30	ns
t_{PHL}				40		45	ns

Switching Characteristics Over Operating Range

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	MIL 'LS647 MIN	MIL 'LS647 MAX	MIL 'LS649 MIN	MIL 'LS649 MAX	COM 'LS647 MIN	COM 'LS647 MAX	COM 'LS649 MIN	COM 'LS649 MAX	UNIT
t_{PLH}	Data to output delay	C_L = 45pF R_L = 667Ω		32		35		32		35	ns
t_{PHL}				27		30		27		30	ns
t_{PLH}	Clock to output delay			35		40		35		40	ns
t_{PHL}				45		45		45		45	ns
t_{PLH}	Select to output delay† (data input High)			50		55		50		55	ns
t_{PHL}				45		45		45		45	ns
t_{PLH}	Select to output delay† (data input Low)			60		50		60		50	ns
t_{PHL}				30		40		30		40	ns
t_{PLH}	Output enable delay			40		45		40		45	ns
t_{PHL}				50		50		50		50	ns
t_{PLH}	Direction enable delay			40		45		40		45	ns
t_{PHL}				40		45		40		45	ns

† See Figure 4.

13

Test Waveforms

Setup Time/Hold Time

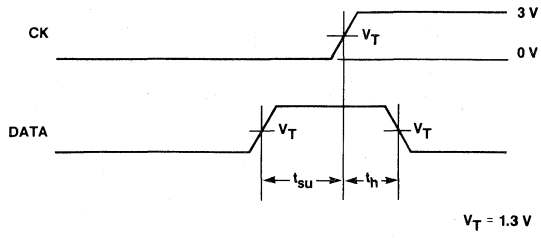


Figure 1.

Bus Data To Bus Output Delay

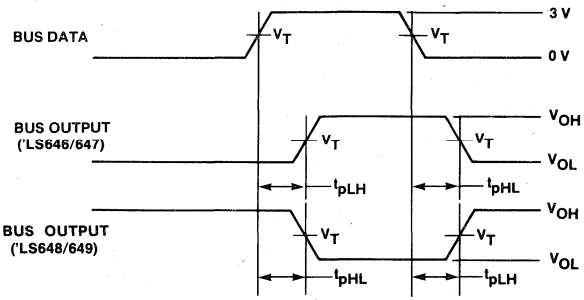


Figure 2. V_T = 1.3 V

CK To Bus Output Propagation Delay Time

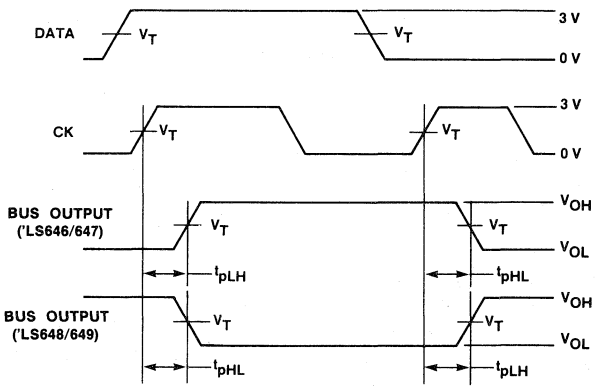


Figure 3 V_T = 1.3 V

Select To Output Delay

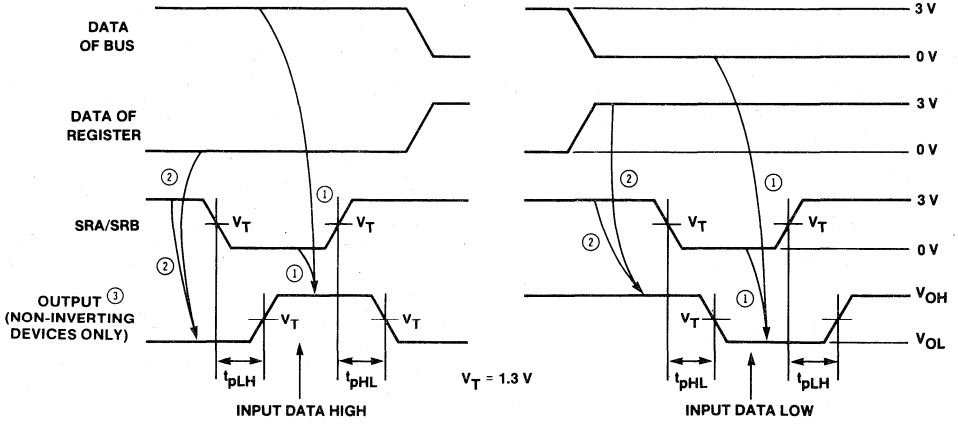


Figure 4

NOTES: 1. When SRA/SRB is low, the input data will transfer to output bus.
2. When SRA/SRB is high, the data of register will transfer to output bus.
3. For the inverting devices, the timing is similar, but the output is opposite to that for the non-inverting devices.

Enable/Disable/Direction-Change Delay

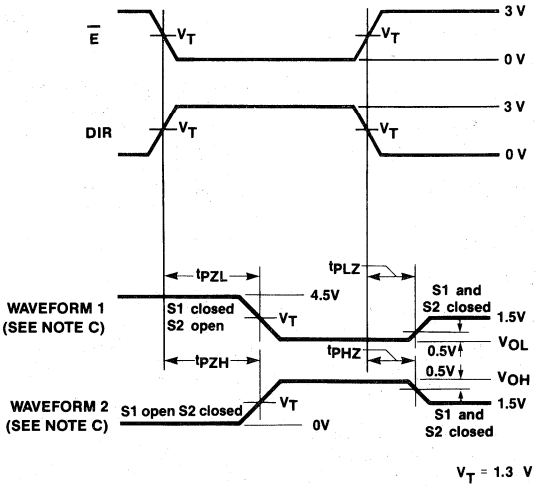
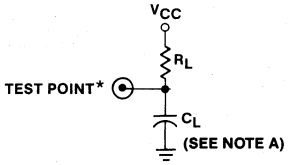
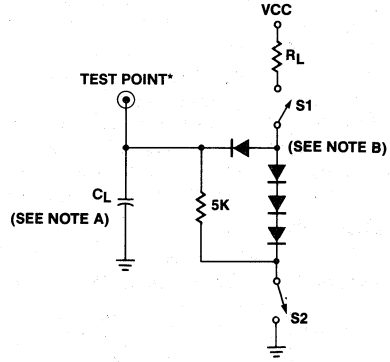


Figure 5

Test Loads



Load Circuit For
Open-Collector Outputs



Load Circuit For
Three-State Outputs

* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Notes: A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz. Z_{OUT} = 50 Ω and t_R = 15 ns t_F ≤ 6 ns.
F. When measuring propagation delay times of three-state outputs, switches S1 and S2 are closed.

13

8-Bit Bus Front-Loading-Latch Transceivers

SN54/74LS651
SN54/74LS653
SN54/74LS652
SN54/74LS654

Features/Benefits

- **Bidirectional bus transceivers and registers**
- **Independent registers for A and B buses**
- **Real-time data transfer or stored data transfer**
- **Simultaneous outputs on both buses**
- **24-pin SKINNYDIP® saves space**
- **8-bit data path matches byte boundaries**
- **Three-state or open-collector outputs drive bus lines**
- **'LS653/4 are open-collector in A direction, three-state in B direction**

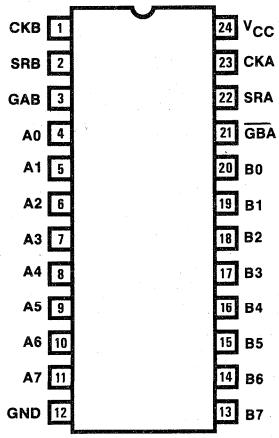
Description

These 8-bit bus transceivers with 3-state ('LS651, 'LS652) or open-collector ('LS653, 'LS654) outputs have 16 D-type flip-flops and multiplexers. The bus-oriented pinout of the parts is shown in the Pin Configuration. The internal gate-level hardware configurations for the 'LS651/653 and 'LS652/654 are given in their respective Logic Diagrams. The basic repeated element, consisting of an edge-triggered flip-flop paralleled with a by-passing path or "feed-through" into a two-way mux, is sometimes called a "front-loading latch."

A pair of multiplexers are used to distribute two bytes of data through the part. The data-routing combinations offered by the multiplexers provide flexibility in directing data to or from either bus, and/or either register. Data is loaded into registers A or B upon the rising edge of the appropriate clock signals. CKA clocks register A, which receives data from the B bus directly at its inputs.

Pin Configurations

'LS651/652/653/654
8-Bit Bus Front-Loading-Latch Transceivers



Ordering Information

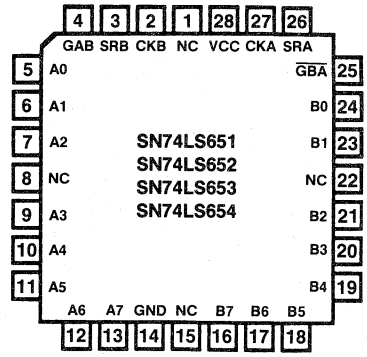
PART NUMBER	PKG	TEMP	POLARITY	OUTPUTS	POWER
SN54LS651	JS,W,L*	Mil	Invert	Three-state	LS
SN74LS651	NS,JS, NL (28)	Com	Invert	Three-state	LS
SN54LS652	JS,W,L*	Mil	Noninvert	Three-state	LS
SN74LS652	NS,JS, NL (28)	Com	Noninvert	Three-state	LS
SN54LS653	JS,W,L*	Mil	Invert	A bus open-collector; B bus three-state	LS
SN74LS653	NS,JS, NL (28)	Com	Invert		LS
SN54LS654	JS,W,L*	Mil	Noninvert		LS
SN74LS654	NS,JS, NL (28)	Com	Noninvert		LS

* L package here is L28. The other packages are 24-pin.

Similarly, CKB clocks register B, which has the A bus available directly at its inputs. Control of the multiplexers is provided by two select lines (one per register), SRA and SRB. Command of the outputs is performed by two enable lines, GAB and $\overline{GBA}$.

When GAB is Low and $\overline{GBA}$ is High, data from the buses can be loaded into registers A and B. When $\overline{GBA}$ is Low, the A bus is configured for output. When GAB is High, the B bus is configured for output. The A and B buses can be enabled at the same time, to operate as outputs simultaneously.

SRA is used to select between register A and the B bus, and then to route the data to a controlled buffer connected to the A bus. Likewise, SRB selects between register B and the A bus, and then routes the data to the B bus through a controlled buffer.



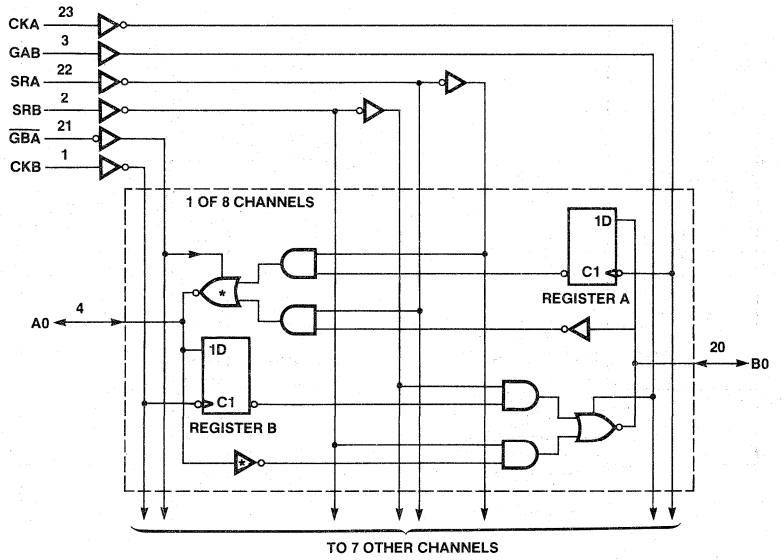
Plastic Chip Carrier

SKINNYDIP® is a registered trademark of Monolithic Memories.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories MMI

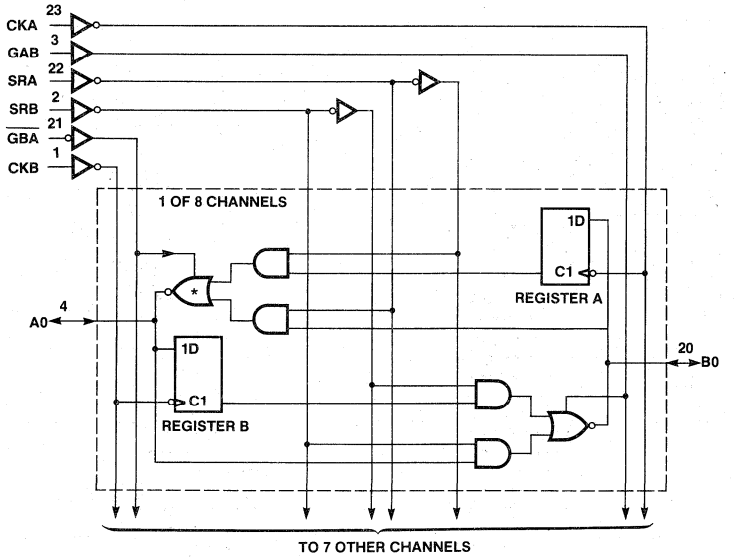
Logic Diagrams

'LS652/654 (Non-Inverting)



* For the 'LS652 devices, the A bus outputs are 3-state.
For the 'LS654 devices, the A bus outputs are open-collector.
The B bus outputs are 3-state for both devices.

'LS651/653 (Inverting)

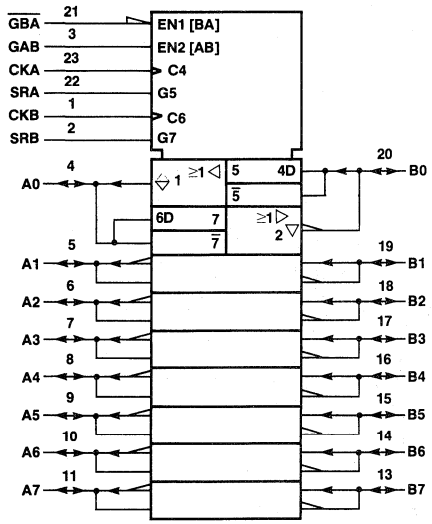


* For the 'LS651 devices, the A bus outputs are 3-state.
For the 'LS653 devices, the A bus outputs are open-collector.
The B bus outputs are 3-state for both devices.

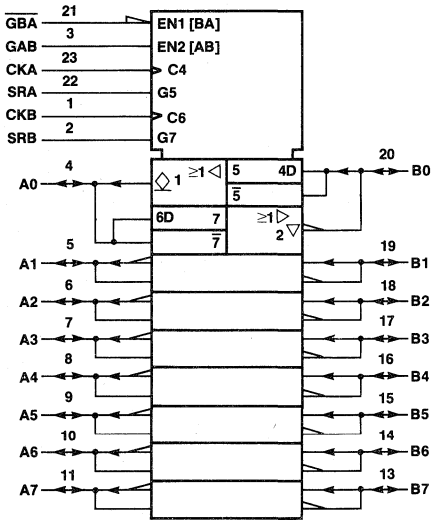
13

IEEE Symbols

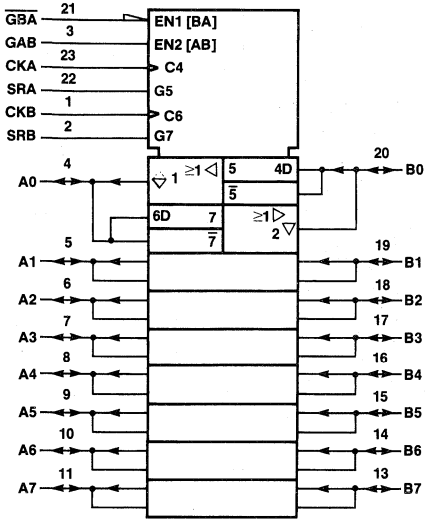
'LS651



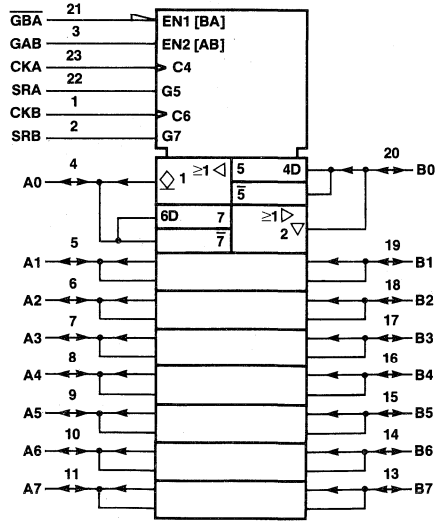
'LS653



'LS652

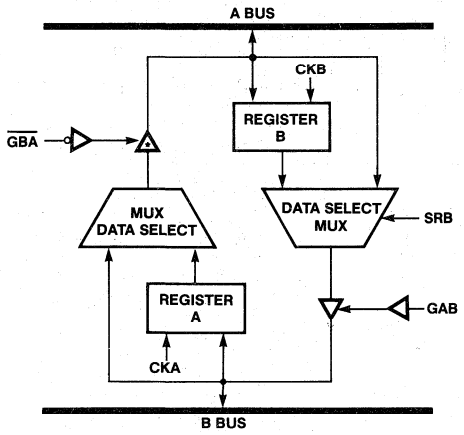


'LS654

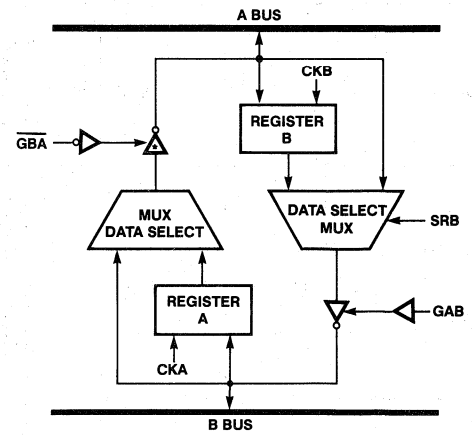


Block Diagrams

'LS652/654 (Non-Inverting)



'LS651/653 (Inverting)



* For the 'LS651/652 devices, the A bus outputs are 3-state.
For the 'LS653/654 devices, the A bus outputs are open-collector.
The B bus outputs are 3-state for both devices.

Function Table Nomenclature Description

GAB: To enable the A-to-B operation.

$\overline{GBA}$: To enable the B-to-A operation.

GAB	$\overline{GBA}$	OPERATION DIRECTION
L	L	B to A
L	H	A and B buses both are inputs (storage)
H	L	A and B buses both are outputs (Transfer stored data to bus)
H	H	A to B

SRA/SRB: To select the output data coming from the A/B register if SRA/SRB is High level; otherwise, directly from the input data bus.

A0-A7: Eight input/output pins on the A side.

B0-B7: Eight input/output pins on the B side.

CKA/CKB: Clock for Register A/B.

X: H or L state irrelevant ("Don't Care" conditions).

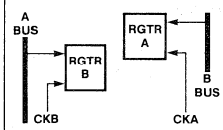
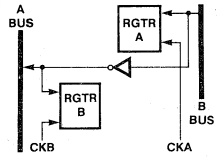
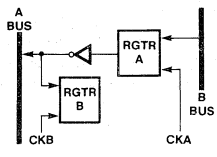
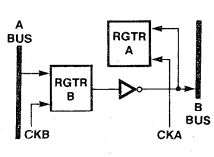
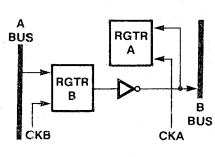
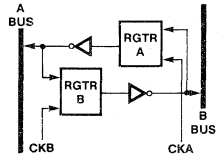
↑: Positive edge of CK causes clocking, if clocking enable is asserted.

UC: H or L or ↓ case (nonclocked operation).

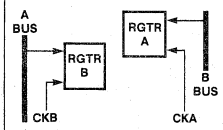
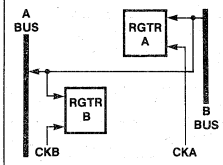
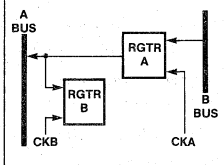
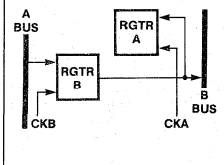
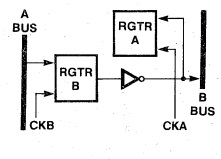
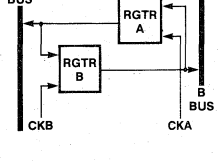
RGTR: Register.

13

Bus Operation for 'LS651/653

OPERATION	CONTROL				DATA I/O		BLOCK DIAGRAM	CLOCK ENABLE		'LS651/653
	GAB	$\overline{GBA}$	SRA	SRB	A0-A7	B0-B7		CKA	CKB	
Storage	L	H	X	X	Input	Input		UC	UC	No operation
								UC	↑	Real time A bus data → RGTR B
								↑	UC	Real time B bus data → RGTR A
								↑	↑	Real time A bus data → RGTR B Real time B bus data → RGTR A
Real time B-to-A Operation	L	L	L	X	Output	Input		UC	UC	Real time $\overline{B}$ bus data → A bus
								UC	↑	Real time $\overline{B}$ bus data → A bus Real time $\overline{B}$ bus data → RGTR B
								↑	UC	Real time $\overline{B}$ bus data → A bus Real time B bus data → RGTR A
								↑	↑	Real time $\overline{B}$ bus data → A bus Real time B bus data → RGTR A Real time $\overline{B}$ bus data → RGTR B
Stored data B-to-A Operation	L	L	H	X	Output	Input		UC	UC	RGTR $\overline{A}$ data → A bus
								UC	↑	RGTR $\overline{A}$ data → A bus RGTR $\overline{A}$ data → RGTR B
								↑	UC	Real time B bus data → RGTR A RGTR $\overline{A}$ data → A bus
								↑	↑	Real time B bus data → RGTR A RGTR $\overline{A}$ data → A bus RGTR $\overline{A}$ data → RGTR B
Real time A-to-B Operation	H	H	X	L	Input	Output		UC	UC	Real time $\overline{A}$ bus data → B bus
								UC	↑	Real time $\overline{A}$ bus data → B bus Real time A bus data → RGTR B
								↑	UC	Real time $\overline{A}$ bus data → B bus Real time $\overline{A}$ bus data → RGTR A
								↑	↑	Real time $\overline{A}$ bus data → B bus Real time $\overline{A}$ bus data → RGTR A Real time A bus data → RGTR B
Stored data A-to-B Operation	H	H	X	H	Input	Output		UC	UC	RGTR $\overline{B}$ data → B bus
								UC	↑	Real time A bus data → RGTR B RGTR $\overline{B}$ data → B bus
								↑	UC	RGTR $\overline{B}$ data → B bus RGTR $\overline{B}$ data → RGTR A
								↑	↑	Real time A bus data → RGTR B RGTR $\overline{B}$ data → B bus RGTR $\overline{B}$ data → RGTR A
Transfer Stored Data	H	L	H	H	Output	Output		UC	UC	RGTR $\overline{A/B}$ data → A/B bus
								UC	↑	RGTR $\overline{A/B}$ data → A/B bus RGTR $\overline{A}$ data → RGTR B
								↑	UC	RGTR $\overline{A/B}$ data → A/B bus RGTR $\overline{B}$ data → RGTR A
								↑	↑	RGTR $\overline{A/B}$ data → A/B bus RGTR $\overline{A}$ data → RGTR B RGTR $\overline{B}$ data → RGTR A

Bus Operation for 'LS652/654

OPERATION	CONTROL				DATA I/O		BLOCK DIAGRAM	CLOCK ENABLE		'LS652/654
	GAB	$\overline{GBA}$	SRA	SRB	A0-A7	B0-B7		CKA	CKB	
Storage	L	H	X	X	Input	Input		UC	UC	No operation
								UC	↑	Real time A bus data → RGTR B
								↑	UC	Real time B bus data → RGTR A
								↑	↑	Real time A bus data → RGTR B Real time B bus data → RGTR A
Real time B-to-A Operation	L	L	L	X	Output	Input		UC	UC	Real time B bus data → A bus
								UC	↑	Real time B bus data → A bus Real time B bus data → RGTR B
								↑	UC	Real time B bus data → A bus Real time B bus data → RGTR A
								↑	↑	Real time B bus data → A bus Real time B bus data → RGTR A Real time B bus data → RGTR B
Stored data B-to-A Operation	L	L	H	X	Output	Input		UC	UC	RGTR A data → A bus
								UC	↑	RGTR A data → A bus RGTR A data → RGTR B
								↑	UC	Real time B bus data → RGTR A RGTR A data → A bus
								↑	↑	Real time B bus data → RGTR A RGTR A data → A bus RGTR A data → RGTR B
Real time A-to-B Operation	H	H	X	L	Input	Output		UC	UC	Real time A bus data → B bus
								UC	↑	Real time A bus data → B bus Real time A bus data → RGTR B
								↑	UC	Real time A bus data → B bus Real time A bus data → RGTR A
								↑	↑	Real time A bus data → B bus Real time A bus data → RGTR A Real time A bus data → RGTR B
Stored data A-to-B Operation	H	H	X	H	Input	Output		UC	UC	RGTR B data → B bus
								UC	↑	Real time A bus data → RGTR B RGTR B data → B bus
								↑	UC	RGTR B data → B bus RGTR B data → RGTR A
								↑	↑	Real time A bus data → RGTR B RGTR B data → B bus RGTR B data → RGTR A
Transfer Stored Data	H	L	H	H	Output	Output		UC	UC	RGTR A/B data → A/B bus
								UC	↑	RGTR A/B data → A/B bus RGTR A data → RGTR B
								↑	UC	RGTR A/B data → A/B bus RGTR B data → RGTR A
								↑	↑	RGTR A/B data → A/B bus RGTR A data → RGTR B RGTR B data → RGTR A

13

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature		-55		125	0		75	°C
t_w	Width of clock	High	20			20			ns
		Low	20			20			
t_{su}	Setup time	'LS651	20 ↑			20 ↑			ns
		'LS652	20 ↑			20 ↑			
t_h	Hold time	'LS651	0 ↑			0 ↑			ns
		'LS652	0 ↑			0 ↑			
I_{OH}	High-level output current				-12			-15	mA
I_{OL}	Low-level output current				12			24	mA

↑ ↓ The arrow indicates the transition of the clock input used for reference. ↑ for the low-to-high transitions. ↓ for the high-to-low transitions.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IH}	High-level input voltage				2			2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = -18 mA			-1.5			-1.5	V
I_{IL}	Low-level input current		V_{CC} = MAX	V_I = 0.4 V			-0.4			-0.4	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7 V			20			20	μA
I_I	Maximum input current	A or B	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
		All others		V_I = 7 V							
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OH} = -3 mA	2.4	3.4		2.4	3.4		V
				I_{OH} = MAX	2			2			
I_{OZL}	Off-state output current		V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2 V	V_O = 0.4 V			-400			-400	μA
I_{OZH}				V_O = 2.7 V			20			20	μA
I_{OS}	Output short-circuit current*		V_{CC} = MAX		-40		-225	-40		-225	mA
I_{CC}	Supply current		V_{CC} = MAX	'LS651 Outputs High			145			145	mA
				'LS651 Outputs Low			165			165	
				'LS651 Outputs disabled			165			165	
				'LS652 Outputs High			145			145	
				'LS652 Outputs Low			165			165	
				'LS652 Outputs disabled			165			165	

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	'LS651 MIN	'LS651 MAX	'LS652 MIN	'LS652 MAX	UNIT
t_{PLH}	Data to output delay	C_L = 45pF R_L = 667Ω		15		15	ns
t_{PHL}				15		20	ns
t_{PLH}	Clock to output delay			20		20	ns
t_{PHL}				30		30	ns
t_{PLH}	Select to output delay † (data input High)			35		35	ns
t_{PHL}				20		25	ns
t_{PLH}	Select to output delay † (data input Low)			35		35	ns
t_{PHL}				30		20	ns
t_{PZL}	$\overline{GBA}$ to A bus output enable delay			25		25	ns
t_{PZH}				20		20	ns
t_{PLZ}	$\overline{GBA}$ to A bus output disable delay	C_L = 5pF R_L = 667Ω		25		25	ns
t_{PHZ}				35		35	ns
t_{PZL}	GAB to B bus output enable delay	C_L = 45pF R_L = 667Ω		30		30	ns
t_{PZH}				25		25	ns
t_{PLZ}	GAB to B bus output disable delay	C_L = 5pF R_L = 667Ω		25		25	ns
t_{PHZ}				35		35	ns

† See Figure 4.

Switching Characteristics Over Operating Range

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	MIL 'LS651 MIN	MIL 'LS651 MAX	MIL 'LS652 MIN	MIL 'LS652 MAX	COM 'LS651 MIN	COM 'LS651 MAX	COM 'LS652 MIN	COM 'LS652 MAX	UNIT
t_{PLH}	Data to output delay	C_L = 45pF R_L = 667Ω		20		20		15		20	ns
t_{PHL}				20		25		17		22	ns
t_{PLH}	Clock to output delay			25		25		22		22	ns
t_{PHL}				35		35		30		30	ns
t_{PLH}	Select to output delay † (data input High)			40		40		35		35	ns
t_{PHL}				25		30		25		28	ns
t_{PLH}	Select to output delay † (data input Low)			40		40		35		35	ns
t_{PHL}				35		25		30		22	ns
t_{PZL}	$\overline{GBA}$ to A bus output enable delay			30		30		25		25	ns
t_{PZH}				25		25		20		20	ns
t_{PLZ}	$\overline{GBA}$ to A bus output disable delay	C_L = 5pF R_L = 667Ω		35		30		30		28	ns
t_{PHZ}				40		45		40		40	ns
t_{PZL}	GAB to B bus output enable delay	C_L = 45pF R_L = 667Ω		35		35		30		32	ns
t_{PZH}				30		30		25		25	ns
t_{PLZ}	GAB to B bus output disable delay	C_L = 5pF R_L = 667Ω		35		35		30		30	ns
t_{PHZ}				40		45		35		40	ns

† See Figure 4.

13

Absolute Maximum Ratings

Supply voltage V_{CC} ..... −0.5 V to 7 V
Input voltage ..... −1.5 V to 7 V
Off-state output voltage ..... −0.5 V to 5.5 V
Storage temperature ..... −65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature		−55		125	0		75	°C
t_w	Width of clock	High	20			20			ns
		Low	20			20			
t_{su}	Setup time	'LS653	20 ↑			20 ↑			ns
		'LS654	20 ↑			20 ↑			
t_h	Hold time	'LS653	0 ↑			0 ↑			ns
		'LS654	0 ↑			0 ↑			
V_{OH}	High-level output voltage (A bus only)				5.5			5.5	V
I_{OH}	High-level output current (B bus only)				−12			−15	mA
I_{OL}	Low-level output current				12			24	mA

↑ ↓ The arrow indicates the transition of the clock input used for reference. ↑ for the low-to-high transitions, ↓ for the high-to-low transitions.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IH}	High-level input voltage				2			2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18 mA			−1.5			−1.5	V
I_{IL}	Low-level input current		V_{CC} = MAX	V_I = 0.4 V			−0.4			−0.4	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7 V			20			20	μA
I_I	Maximum input current	A or B	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
		All others		V_I = 7 V							
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
V_{OH}	High-level output voltage (B bus only)		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
				I_{OH} = MAX	2			2			
I_{OH}	High-level output current (A bus only)		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	V_{OH} = 5.5 V			100			100	μA
I_{OZL}	Off-state output current (B bus only)		V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2 V	V_O = 0.4 V			−400			−400	μA
I_{OZH}				V_O = 2.7 V (B bus only)			20			20	μA
I_{OS}	Output short-circuit current* (B bus only)		V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply current		V_{CC} = MAX	'LS-653, Outputs High			145			145	mA
				'LS-653, Outputs Low			165			165	
				'LS-653, Outputs disabled			165			165	
				'LS-654, Outputs High			145			145	
				'LS-654, Outputs Low			165			165	
				'LS-654, Outputs disabled			165			165	

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

13

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS* (See Test Load/Waveforms)	'LS653 MIN	'LS653 MAX	'LS654 MIN	'LS654 MAX	UNIT
t_{PLH}	Data to A bus output delay	C_L = 45pF R_L = 667Ω		25		25	ns
t_{PHL}				20		25	ns
t_{PLH}	Data to B bus output delay			15		15	ns
t_{PHL}				15		20	ns
t_{PLH}	Clock to A bus output delay			30		30	ns
t_{PHL}				30		30	ns
t_{PLH}	Clock to B bus output delay			20		20	ns
t_{PHL}				30		30	ns
t_{PLH}	Select to A bus † output delay (data input High)			45		45	ns
t_{PHL}				25		30	ns
t_{PLH}	Select to A bus † output delay (data input Low)			40		45	ns
t_{PHL}				30		25	ns
t_{PLH}	Select to B bus † output delay (data input High)			35		35	ns
t_{PHL}				25		25	ns
t_{PLH}	Select to B bus † output delay (data input Low)			35		35	ns
t_{PHL}				30		20	ns
t_{PLH}	$\overline{GBA}$ to A bus output enable delay			35		35	ns
t_{PHL}				25		30	ns
t_{PZL}	GAB to B bus output enable delay			30		30	ns
t_{PZH}				25		25	ns
t_{PLZ}	GAB to B bus output disable delay	C_L = 5pF R_L = 667Ω		25		25	ns
t_{PHZ}				35		35	ns

* For A bus, the test load will refer to the open-collector test load. See Figure 6.
For B bus, the test load will refer to the three-state test load. See Figure 7.

† See Figure 4.

Switching Characteristics Over Operating Range

SYMBOL	PARAMETER	TEST CONDITIONS* (See Test Load/Waveforms)	MIL		COM		UNIT
			'LS653 MIN MAX	'LS654 MIN MAX	'LS653 MIN MAX	'LS654 MIN MAX	
t_{PLH}	Data to A bus output delay	C_L = 45pF R_L = 667Ω	30	30	28	30	ns
t_{PHL}			25	30	23	28	ns
t_{PLH}	Data to B bus output delay		20	20	18	18	ns
t_{PHL}			20	25	18	20	ns
t_{PLH}	Clock to A bus output delay		40	40	35	35	ns
t_{PHL}			40	40	35	35	ns
t_{PLH}	Clock to B bus output delay		25	25	23	23	ns
t_{PHL}			35	35	30	30	ns
t_{PLH}	Select to A bus output † delay (data input High)		50	50	45	48	ns
t_{PHL}			30	40	25	35	ns
t_{PLH}	Select to A bus output † delay (data input Low)		45	55	43	50	ns
t_{PHL}			35	30	30	28	ns
t_{PLH}	Select to B bus output † delay (data input High)		40	35	35	35	ns
t_{PHL}			25	35	25	30	ns
t_{PLH}	Select to B bus output † delay (data input Low)		40	45	35	40	ns
t_{PHL}			35	25	30	23	ns
t_{PLH}	$\overline{GBA}$ to A bus output enable delay		40	35	35	35	ns
t_{PHL}			30	40	28	35	ns
t_{PZL}	GAB to B bus output enable delay		35	35	30	33	ns
t_{PZH}			30	30	25	28	ns
t_{PLZ}	GAB to B bus output disable delay	C_L = 5pF R_L = 667Ω	35	35	30	30	ns
t_{PHZ}			40	45	38	40	ns

* For A bus, the test load will refer to the open-collector test load. See Figure 6.
For B bus, the test load will refer to the three-state test load. See Figure 7.

† See Figure 4.

13

Test Waveforms

Setup Time/Hold Time

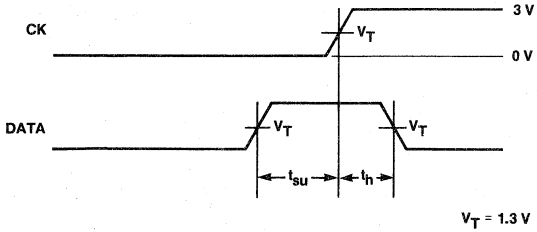


Figure 1.

Bus Data To Bus Output Delay

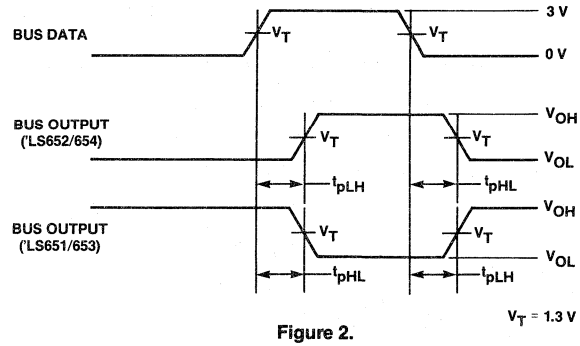


Figure 2.

CK To Bus Output Propagation Delay Time

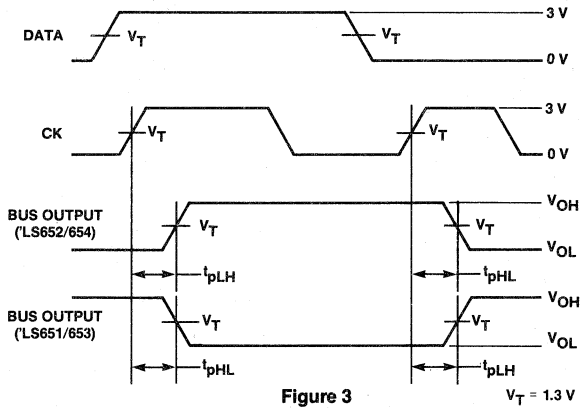


Figure 3

Select To Output Delay

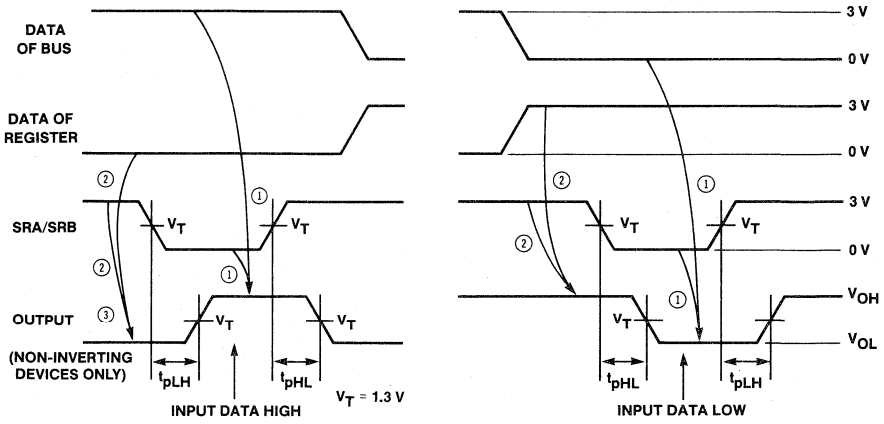


Figure 4

NOTES: 1. When SRA/SRB is low, the input data will transfer to output bus.
2. When SRA/SRB is high, the data of register will transfer to output bus.
3. For the inverting devices, the timing is similar, but the output is opposite to that for the non-inverting devices.

Enable/Disable Delay

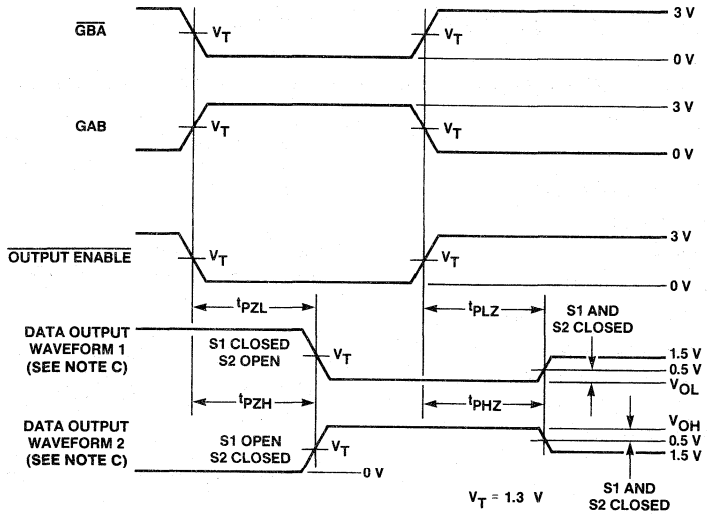
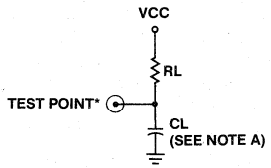
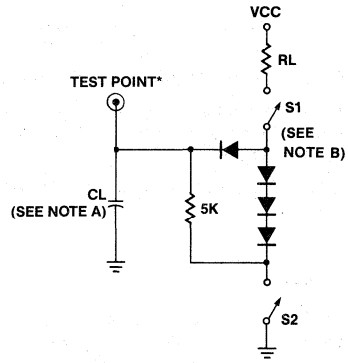


Figure 5

Test Loads



Load Circuit For Open-Collector Outputs



Load Circuit For Three-State Outputs

* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Notes: A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz. Z_{OUT} = 50 Ω and t_R = 15 ns t_F ≤ 6 ns.
F. When measuring propagation delay times of three-state outputs, switches S1 and S2 are closed.

13

8-Bit Two-Stage Pipelined Register/Latch

SN54/74LS548 SN54/74LS549

Feature/Benefits

- Two 8-bit high-speed registers/latches
- Faster than other LS-TTL registers/latches
- Three-state outputs drive bus lines
- 24-pin SKINNYDIP® saves space
- 8-bit data path matches byte boundaries
- Multiplexer selects either rank at input/output
- Output can drive bus directly: I_{OL} 32 mA (com), 24 mA (mil)
- Registers/latches configurable for nose-to-tail or side-by-side operation
- Individual clock/gate enables for each rank

Applications

- Registers for pipelined arithmetic units or digital signal processors
- Bus monitor for popular 8-bit microprocessors to restart instructions upon virtual memory page fault
- Video display character/attribute pipelined registers
- Sequence/state generator for systems: dual-rank registers/latches allow storing a backup previous state for redundancy, or diagnostics
- Two-stage buffer for pipelined interfacing input/output

Description

The 54/74LS548 and 54/74LS549 contain a pair of high-speed 8-bit registers ('LS548) or latches ('LS549) which perform various pipeline storage functions. Two control pins govern a pair of internal multiplexers, as shown in the block diagrams; using these, several useful data paths can be configured. The input selection multiplexer determines the source of data to the second register/latch, as controlled by the INSEL line. In this way, data from either the D7-D0 inputs, or the outputs of the first register/latch, are stored in the second register/latch. The output selection multiplexer determines the source of data that will be sent to the outputs Y7-Y0. This multiplexer is controlled by the OUTSEL line, and allows either the first or second register/latch data to be output. The outputs are fully buffered, provide high-drive current, and allow three-state control through the $\overline{OE}$ line.

Ordering Information

PART NUMBER	PKG	TEMP	TYPE	POWER
SN54LS548	JS,W,L(28)	Mil	Register	LS
SN74LS548	NS,JS,NL(28)	Com	Register	LS
SN54LS549	JS,W,L(28)	Mil	Latch	LS
SN74LS549	NS,JS,NL(28)	Com	Latch	LS

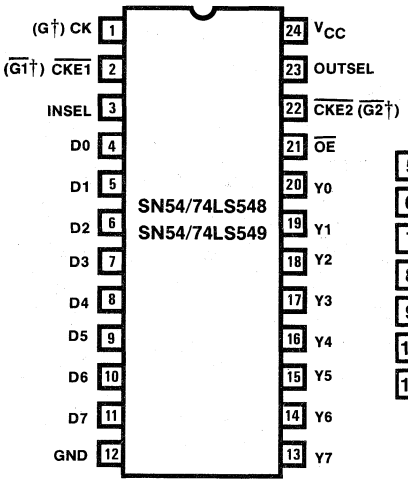
The arrangement of registers/latches within the 'LS548/'LS549 can be thought of a two 8-bit storage ranks, rank 1 and rank 2. The 'LS548 has a common clock line CK, and separate clock enables $\overline{CKE1}$ and $\overline{CKE2}$ for rank 1 and rank 2 respectively. In contrast, the 'LS549 operates as a flow-through latch, and has separate latch enables $\overline{G1}$ and $\overline{G2}$ for each rank, as well as a common latch-enable input G.

In the 'LS548, data present at the D7-D0 inputs are stored in rank 1 on the positive edge of CK, if $\overline{CKE1}$ has been previously asserted. Data for rank 2 are stored similarly, if $\overline{CKE2}$ is asserted prior to the clock. In the 'LS549, data pass through the latches when the latch controls ($\overline{G1}$ or $\overline{G2}$) for either rank are enabled simultaneously with the common latch enable G. Data remain in a rank when the latch controls are disabled, or 'unasserted'.

The clock/gate control lines are used with the INSEL and OUTSEL controls for flexible data storage and movement operations. Two representative examples are shown in Figure 1 (a) and 1 (b). The first example is a classical 2-stage pipelined register, or 'nose-to-tail' configuration. Data at D7-D0 are first stored in rank 1, then stored in rank 2 on the next clock/gate. If the clock/gate enable for either rank becomes unasserted, then the previously-stored data are simply retained. In the second example, data at D7-D0 are stored in either or both ranks if the respective clock/gate enable signals are asserted. In this 'side-by-side' configuration, data sent to the Y7-Y0 outputs are selected from either rank 1 or rank 2, under control of the OUTSEL line.

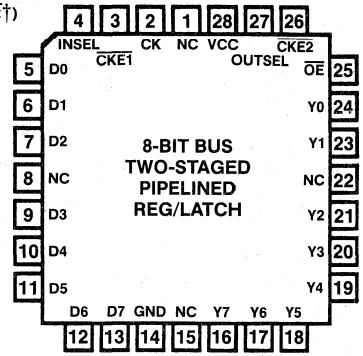
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories MMI

Pin Configurations



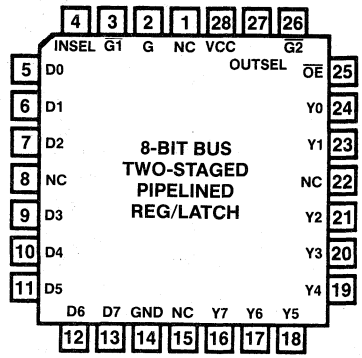
† For SN54/74LS549.

SN54/74LS548



Plastic Chip Carrier

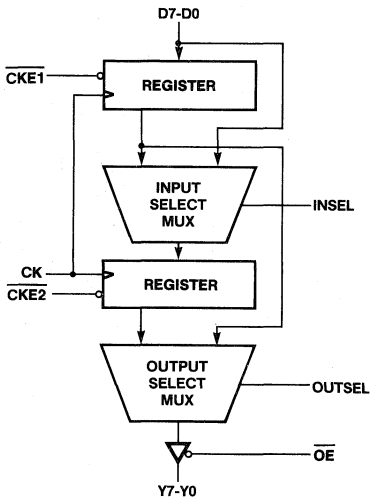
SN54/74LS549



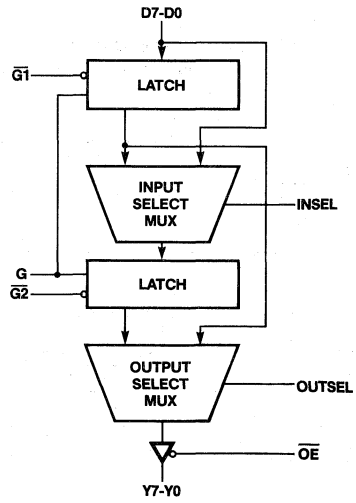
Plastic Chip Carrier

Block Diagrams

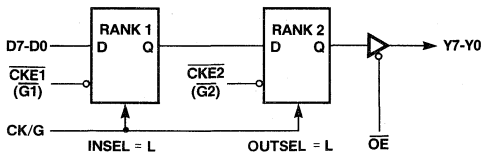
'LS548



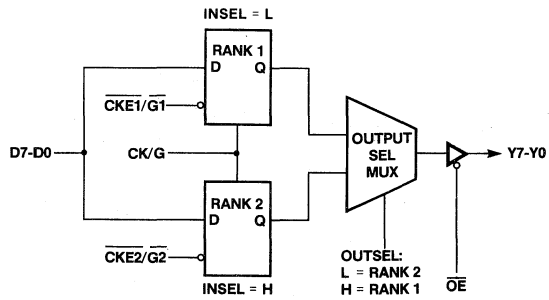
'LS549



Typical Configurations



(a) Nose-to-Tail



(b) Side-by-Side

Figure 1

Function Table Nomenclature Description

Rank 1-Q or Rank 2-Q = Data available at the internal flip-flop/latch outputs for the 8 rank 1 or rank 2 registers/latches respectively.

D = Data at the D0-D7 input pins.

Y = Data at the Y0-Y7 output pins.

X = H or L state irrelevant ("don't care" conditions)

Q_0 = Previous states of the internal register/latch data are retained.

Z = Indicates that the Y0-Y7 outputs are in high-impedance state.

INSEL = Input select mux control pin; determines the source of input data for rank 2.

INSEL	RANK 2 INPUT
L	Rank 1
H	D

OUTSEL = Output select mux control pin; selects either rank 1 or rank 2 for output.

OUTSEL	OUTPUT
L	Rank 2
H	Rank 1

$\overline{OE}$ = Output enable pin.

$\overline{OE}$	OUTPUT
L	Rank 1 or Rank 2
H	Hi-Z

↑ = Positive edge of CK causes clocking, if clocking is enabled.

CK = The common clock line for the 54/74LS548.

$\overline{CKE1}/\overline{CKE2}$ = Clock enable line for the rank 1/ rank 2 register in the 54/74LS548.

CK	$\overline{CKE1}$	$\overline{CKE2}$	RANK 1	RANK 2
L or H or ↓	X	X	Disabled	Disabled
↑	L	L	Enabled	Enabled
↑	L	H	Enabled	Disabled
↑	H	L	Disabled	Enabled
X	H	H	Disabled	Disabled

G = The common latch control line for the 54/74LS549.

$\overline{G1}/\overline{G2}$ = Latch enable line for the rank 1/ rank 2 latch in the 54/74LS549.

G	$\overline{G1}$	$\overline{G2}$	RANK 1	RANK 2
L	L	L	Enabled (Flush)	Enabled (Flush)
L	L	H	Enabled (Flush)	Disabled (Freeze)
L	H	L	Disabled (Freeze)	Enabled (Flush)
L	H	H	Disabled (Freeze)	Disabled (Freeze)
H	X	X	Enabled (Flush)	Enabled (Flush)

'LS548 Function Table

CK	$\overline{CKE1}$	RANK 1	$\overline{CKE2}$	INSEL	RANK 2
L or H or ↓	X	Q0	X	X	Q0
↑	H	Q0	H	X	Q0
↑	L	D	H	X	Q0
↑	L	D	L	L	Rank 1-Q
↑	L	D	L	H	D
↑	H	Q0	L	L	Rank 1-Q
↑	H	Q0	L	H	D

'LS549 Function Table

G	$\overline{G1}$	RANK 1	$\overline{G2}$	INSEL	RANK 2
L	L	D	L	L	Rank 1-Q
L	L	D	L	H	D
L	L	D	H	X	Q0
L	H	Q0	L	L	Rank 1-Q
L	H	Q0	L	H	D
L	H	Q0	H	X	Q0
H	X	D	X	L	Rank 1-Q
H	X	D	X	H	D

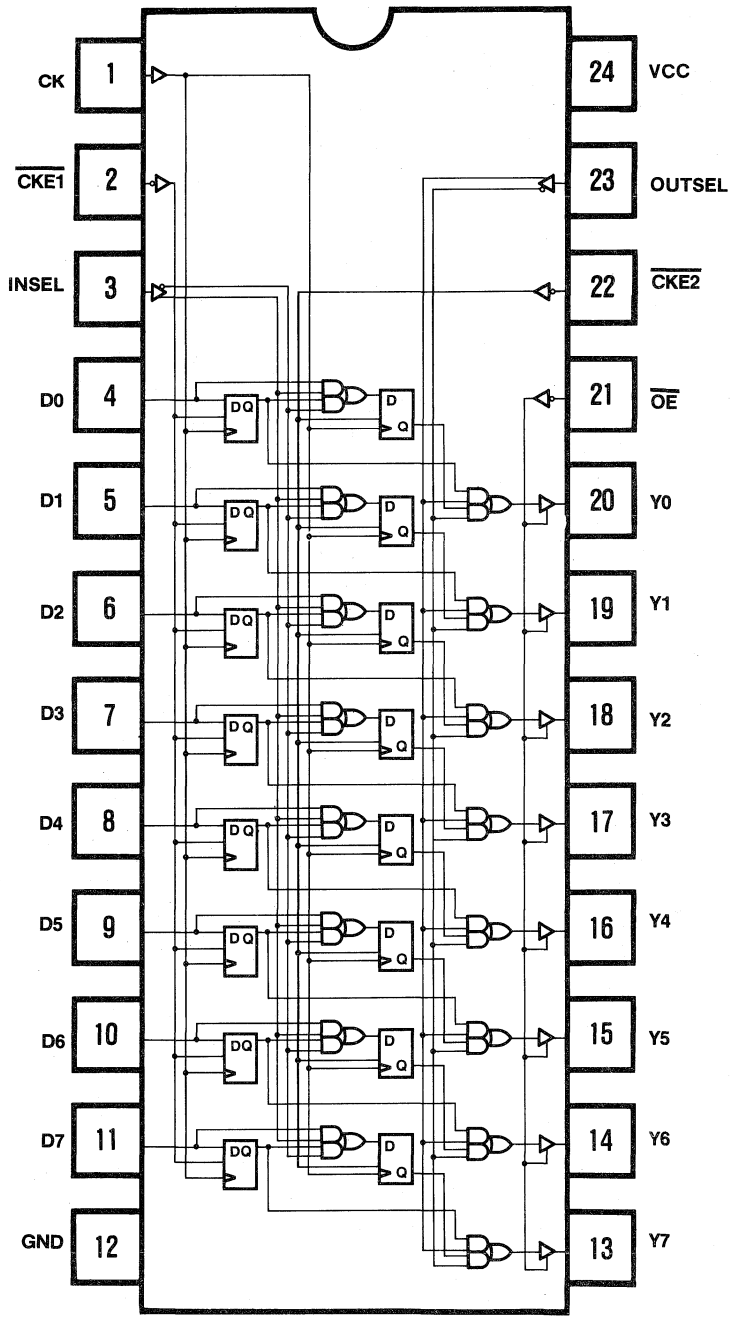
'LS548/549 Output Function Table

OUTSEL	$\overline{OE}$	Y
L	L	Rank 2-Q
H	L	Rank 1-Q
X	H	Hi-Z

13

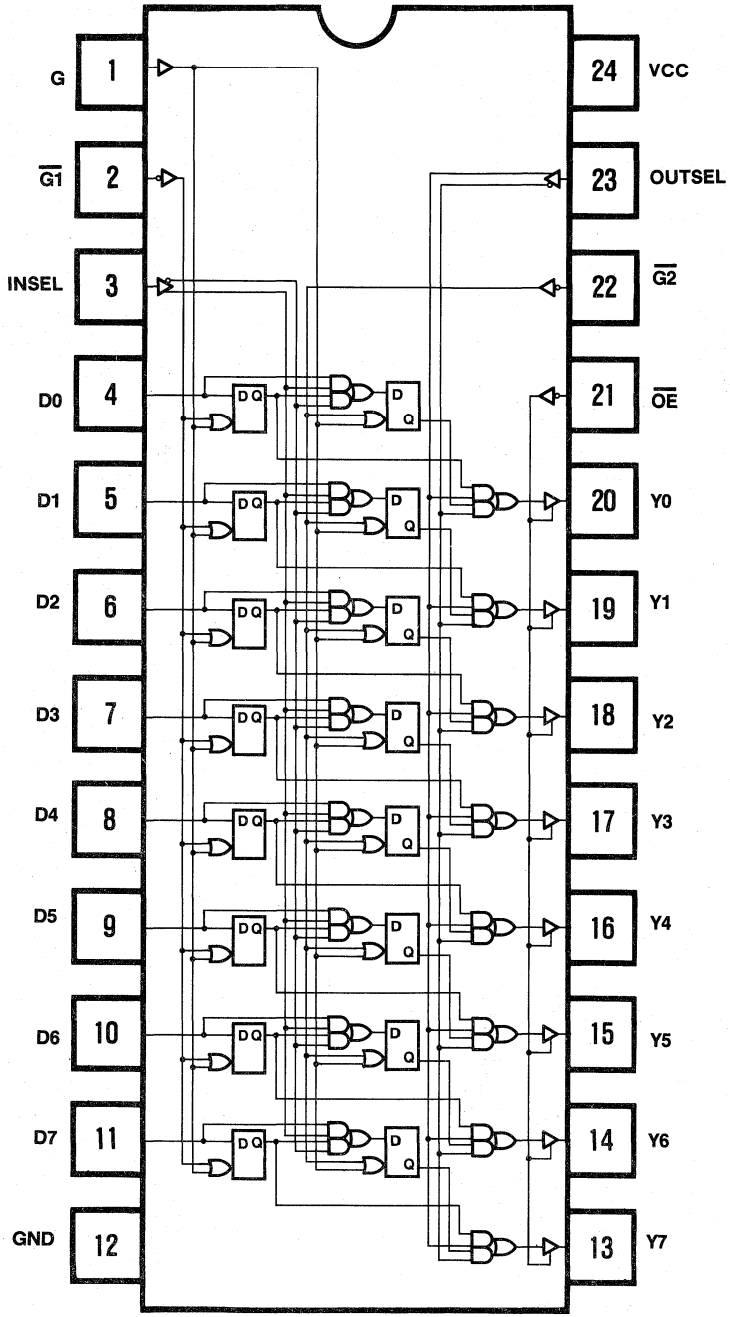
Logic Diagram

54/74LS548 Pipelined Register



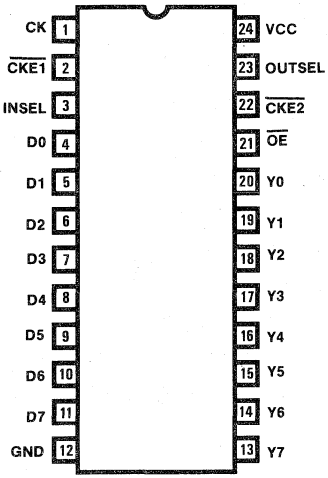
Logic Diagram

54/74LS549 Pipelined Latch

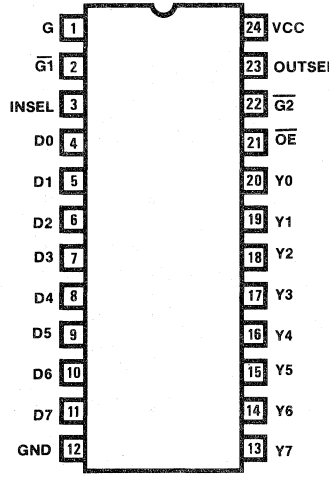


Pin Configurations

'LS548

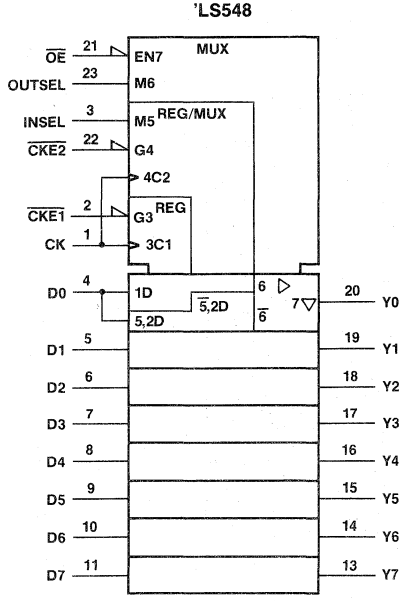


'LS549

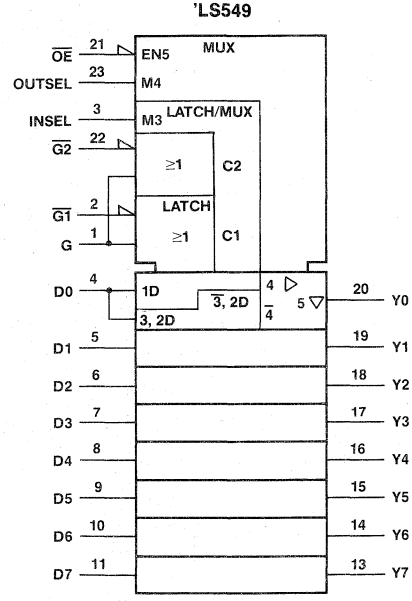


IEEE Symbols

'LS548



'LS549



Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER				MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage				4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature				-55		125	0		75	°C
t_w	Width of CK, G, $\overline{G1}$, $\overline{G2}$	High	'LS548	CK	15			11			ns
			'LS549	G							
		Low	'LS548	CK	15			11			ns
			'LS548	$\overline{G1}$, $\overline{G2}$	18			16			
t_{su}	Setup time for Data		'LS548	CK	20↑			15↑			ns
			'LS549	G	10↓			6↓			
				$\overline{G1}$, $\overline{G2}$	17↑			4↑			
t_h	Hold time for Data		'LS548	CK	0↑			0↑			ns
			'LS549	G	12↓			10↓			
				$\overline{G1}$, $\overline{G2}$	5↑			5			
$t_{su\text{-}CKEX}$	Setup time for clock enables $\overline{CKE1}$, $\overline{CKE2}$ ('LS548 only)				15↑			10↑			ns
$t_{h\text{-}CKEX}$	Hold time for clock enable $\overline{CKE1}$, $\overline{CKE2}$, ('LS548 only)				8↑			5↑			ns
$t_{su\text{-}INSEL}$	Setup time for INSEL[1]				30			25			ns
$t_{h\text{-}INSEL}$	Hold time for INSEL[2]				0			0			ns

NOTES: 1. This is the minimum setup time needed for INSEL prior to the rising edge of the clock/$\overline{GX}$, and to the falling edge of the G, to ensure data transfer to rank 2.
2. This is the minimum hold time needed for INSEL after the rising edge of the clock/$\overline{GX}$, and to the falling edge of the G, to ensure data transfer to rank 2.
↑↓ the arrow indicates the transition of the clock/gate input used for reference:
↑ for the low-to-high transitions,
↓ for the high-to-low transitions.

13

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IH}	High-level input voltage				2.0			2.0			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18 mA			−1.5			−1.5	V
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4 V	D or Y			−250			−250	μA
				All others			−400			−400	
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7 V			20			20	μA
I_I	Maximum input current	D or Y	V_{CC} = MIN	V_I = 5.5 V			0.1			0.1	mA
		All others		V_I = 7 V							
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OL} = 32 mA					0.35	0.5	V
				I_{OL} = 24 mA			0.5				
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OH} = −1 mA	2.4	3.4					V
				I_{OH} = −2.6 mA				2.4	3.1		
I_{OZL}	Off-State output current		V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2V	V_O = 0.4 V			−20			−20	μA
I_{OZH}				V_O = 2.7 V			20			20	
I_{OS}	Output short-circuit current*		V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply Current		V_{CC} = MAX, Outputs open	'LS548			150			150	mA
				'LS549			160			160	

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	'LS548 MIN	'LS548 MAX	'LS549 MIN	'LS549 MAX	UNIT
f_{MAX}	Maximum clock frequency	C_L = 45 pF, R_L = 280Ω, $\overline{OE}$ = L	50				MHz
t_{PLH}/t_{PHL}	CK, $\overline{G1}$, or $\overline{G2}$ to output delay			18		22	ns
t_{PLH}/t_{PHL}	G to output delay ('LS549)					23	ns
t_{PLH}/t_{PHL}	Data D to output delay ('LS549)					16	ns
t_{PLH}/t_{PHL}	Output multiplexer control OUTSEL to output delay			20		20	ns
t_{PZL}/t_{PZH}	Output enable delay	C_L = 45 pF, R_L = 280Ω		18		18	ns
t_{PLZ}/t_{PHZ}	Output disable delay	C_L = 5 pF, R_L = 280Ω		15		15	ns

Switching Characteristics Over Operating Conditions

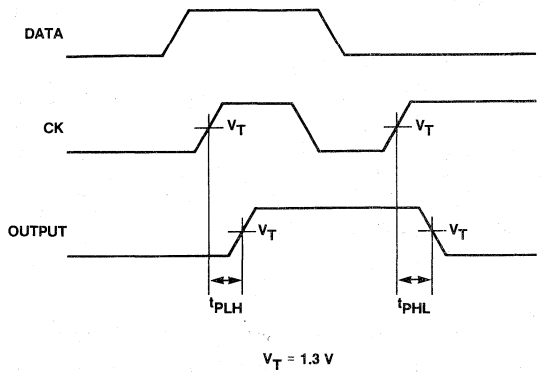
SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	MIL 'LS548 MIN	MIL 'LS548 MAX	MIL 'LS549 MIN	MIL 'LS549 MAX	COM 'LS548 MIN	COM 'LS548 MAX	COM 'LS549 MIN	COM 'LS549 MAX	UNIT
f_{MAX}	Maximum clock frequency		33				45				MHz
t_{PLH}/t_{PHL}	CK, $\overline{G1}$ or $\overline{G2}$ to output delay	C_L = 45 pF, R_L = 280Ω, $\overline{OE}$ = L		25		26		20		24	ns
t_{PLH}/t_{PHL}	G to output delay ('LS549)					28				25	ns
t_{PLH}/t_{PHL}	Data D to output delay ('LS549)					24				18	ns
t_{PLH}/t_{PHL}	Output multiplexer control OUTSEL to output delay			27		27		22		22	ns
t_{PZL}/t_{PZH}	Output enable delay	C_L = 45 pF, R_L = 280Ω		23		23		20		20	ns
t_{PLZ}/t_{PHZ}	Output disable delay	C_L = 5 pF, R_L = 280Ω		20		20		17		17	ns

13

Test Waveforms

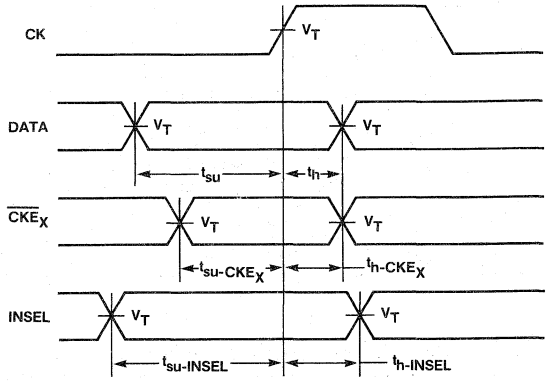
'LS548

CK to Output Delay



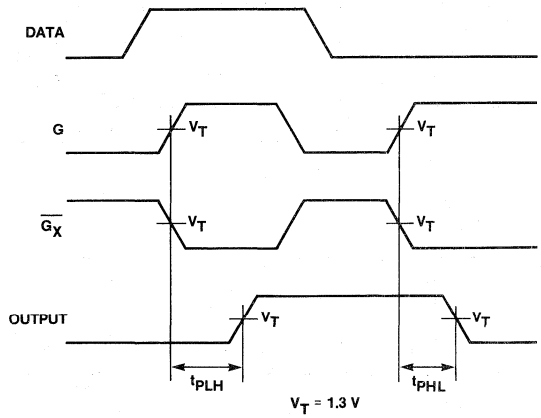
V_T = 1.3 V

Setup and Hold



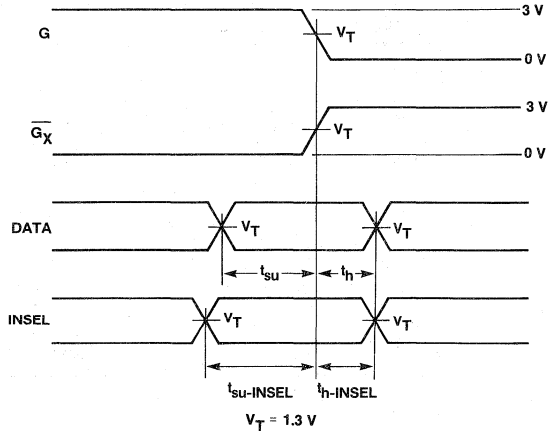
'LS549

G to Output Delay



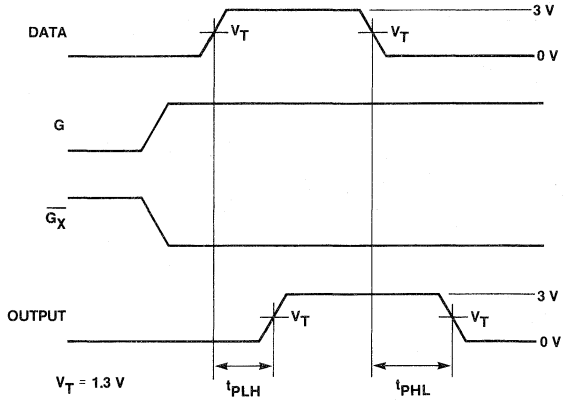
V_T = 1.3 V

Setup and Hold



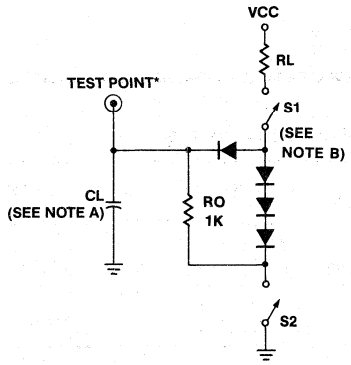
V_T = 1.3 V

Data D to Output Delay

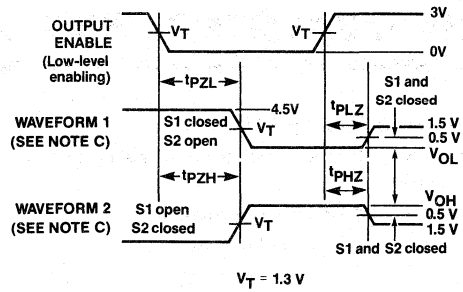


V_T = 1.3 V

Standard Test Load



Load Circuit for Three-state Outputs



'LS548/549 Enable and Disable

* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Notes: A. C_L includes probe and jig capacitance.

B. All diodes are 1N916 or 1N3064.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz. Z_{OUT} = 50 Ω and t_R = 15 ns t_F ≤ 6 ns.

F. When measuring propagation delay times of three-state outputs, switches S1 and S2 are closed.

13

8-Bit Latch/Register with Readback

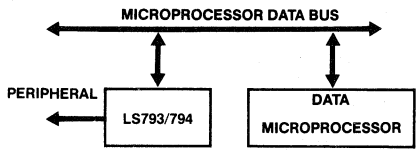
SN54/74LS793 SN54/74LS794

Features/Benefits

- **I/O port configuration enables output data back onto input bus**
- **8-bit data path matches byte boundaries**
- **Ideal for microprocessor interface**

Description

These 8-bit latches/registers are useful for I/O operations on a microprocessor bus. An image of the output data can be read back by the CPU. This operation is important in control algorithms which make decisions based on the previous status of output controls. Rather than storing a redundant copy of the output data in memory, simply reading the register as an I/O port allows the data to be retrieved from where it has been stored in an 'LS793/4, for verification and/or updating.



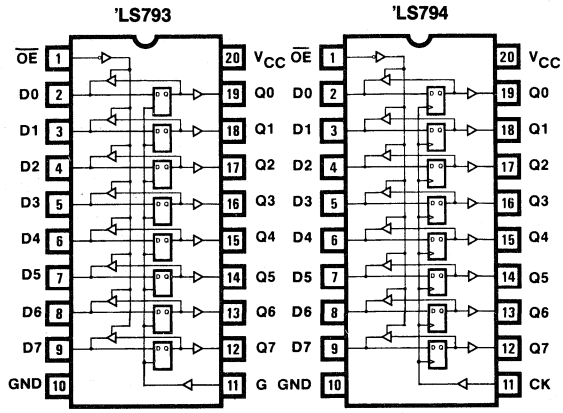
The data is loaded in the registers on the low-to-high transition of the clock (CK), for the 'LS794. The data is passed through the 'LS793 when the gate, (G), is High, and it is "latched" when G changes to Low. The output enable, $\overline{OE}$ is used to enable data on D7-D0. When $\overline{OE}$ is low the output of the latches/registers is enabled on D0-D7, enabling D as an output bus so that the host can perform a read operation. When $\overline{OE}$ is High, D7-D0 are inputs to the latches/registers configuring D as an input bus.

The output drive of these commercial parts for any output pin is I_{OL} = 24 mA.

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	POWER
SN54LS793 SN74LS793	J,W,L, N,J,NL	Mil Com	Non-invert	Latch	LS
SN54LS794 SN74LS794	J,W,L, N,J,NL	Mil Com	Non-invert	Register	LS

Logic Symbols



'LS793 Function Table

G	$\overline{OE}$	Q	D
L	L	Q_0**	Output, Q
L	H	Q_0**	Input
H†	L	D*	Output, Q*
H	H	D	Input

* In this case the output of the latch feeds the input, and a "race" condition results.

** Q_0 represents the previous "latched" state.

† This transition is not a normal mode of operation and may produce hazards.

'LS794 Function Table

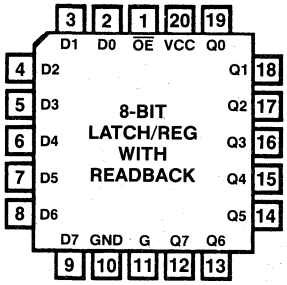
CK	$\overline{OE}$	Q	D
L or H or ↓	L	Q_0	Output, Q
L or H or ↓	H	Q_0	Input
↑	L	Q_0	Output, Q*
↑	H	D	Input

* In this case the output of the register is clocked to the inputs and the overall Q output is unchanged at Q_0.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

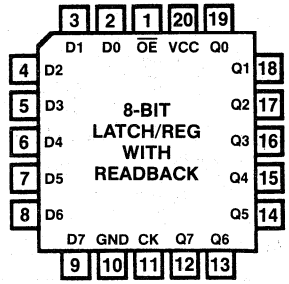
Pin Configurations

SN74LS793



Plastic Chip Carrier

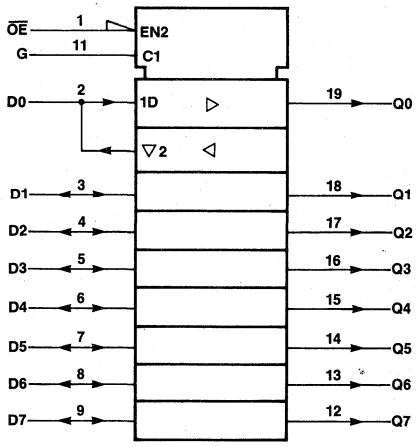
SN74LS794



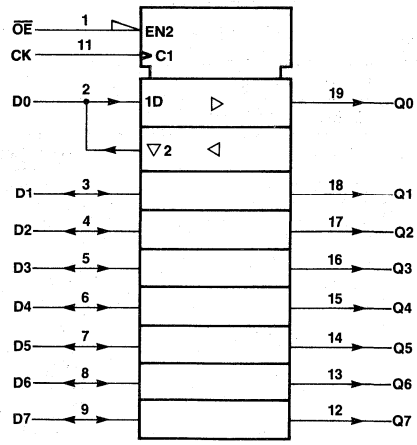
Plastic Chip Carrier

IEEE Symbols

'LS793



'LS794



13

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER			MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage			4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature			-55		125	0		75	°C
t_w	Width of Clock/Gate	High		15			15			ns
		Low ('LS794 only)		15			15			
t_{su}	Setup time		'LS793	15↓			10↓			ns
			'LS794	15↑			15↑			
t_h	Hold time		'LS793	10↓			10↓			
			'LS794	0↑			0↑			

↑ ↓ The arrow indicates the transition of the clock/gate input used for reference. ↑ for the low-to-high transitions, ↓ for the high-to-low transitions.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IH}	High-level input voltage				2			2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = -18 mA			-1.5			-1.5	V
I_{IL}	Low-level input current		V_{CC} = MAX	V_I = 0.4 V			-250			-250	μA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7 V			40			40	μA
I_I	Maximum input current	D or Q	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
		All others		V_I = 7 V							
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OH} = -1 mA	2.4	3.4					V
				I_{OH} = -2.6 mA				2.4	3.1		
I_{OZL}	Off-state output current		V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2 V	V_O = 0.4 V			-250			-250	μA
I_{OZH}				V_O = 2.7 V			40			40	
I_{OS}	Output short-circuit current*		V_{CC} = MAX		-30		-130	-30		-130	mA
I_{CC}	Supply current		V_{CC} = MAX, Outputs open	'LS793			120			120	mA
				'LS794			120			120	

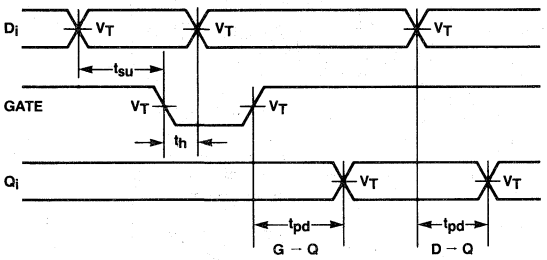
* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

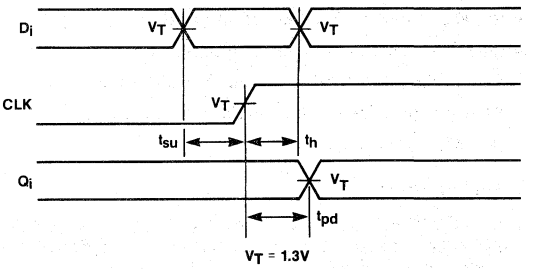
SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	'LS793 MIN	'LS793 TYP	'LS793 MAX	'LS794 MIN	'LS794 TYP	'LS794 MAX	UNIT
f_{MAX}	Maximum clock frequency	C_L = 45pF R_L = 280 Ω				35	50		MHz
t_{PLH}	Data to output delay			12	18				ns
t_{PHL}				12	18				ns
t_{PLH}	Clock/gate to output delay			17	25		9	20	ns
t_{PHL}				12	25		14	20	ns
t_{PZL}	Output enable delay†			15	20		15	20	ns
t_{PZH}				11	20		11	20	ns
t_{PLZ}	Output disable delay†	C_L = 5pF R_L = 280 Ω		8	20		8	20	ns
t_{PHZ}				9	20		9	20	ns

† For the 'LS793, G should remain LOW during these tests.

'LS793 Timing Diagrams



'LS794 Timing Diagrams

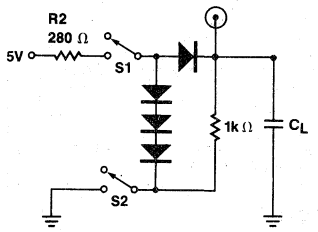


The case when gate is HIGH and data flows through the part is specified as Data to Output delay in the Switching Characteristics table. (V_T = 1.3V).

Test Loads

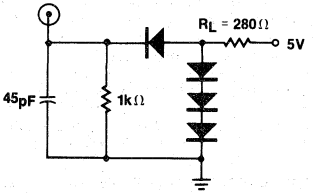
FOR D OUTPUTS-ENABLE AND DISABLE

TEST POINT FOR Di*



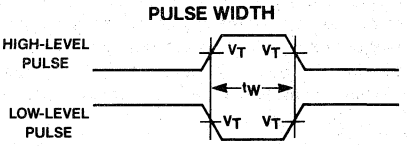
FOR Q OUTPUTS

TEST POINT FOR Qi*

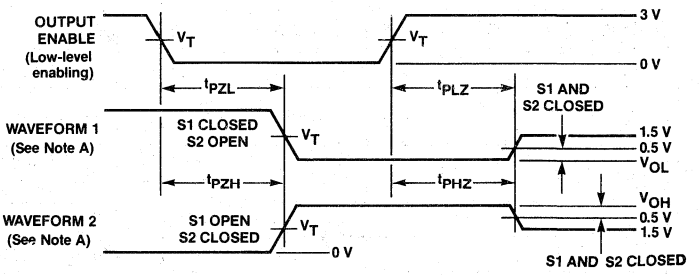


* The "TEST POINT" is drived by the output under test, and observed by instrumentation.

PULSE WIDTH



ENABLE AND DISABLE WAVEFORMS



For the 'LS793, the latch control "G" should be low while testing the enable and disable times, so that the output (Q) does not change. (V_T = 1.3V).

NOTES: A. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

13

8-Bit SERDE Pipeline Register

SN54/74S818

Features/Benefits

- High drive capability. I_{OL} = 32 mA (Com)
- Alternate source to Am29818
- Serial-parallel/Parallel-serial pipeline register
- Independent pathing and clocking controls
- Expandable in multiples of 8 bits
- Three-state outputs
- PNP inputs for low-inputcurrent
- 24-pin SKINNYDIP® saves space

Applications

- Universal interface element for systems using both serial and parallel data formats
- Serial communication and peripheral interface
- Microprogram control store output register
- Serial-parallel/Parallel-serial pipeline conversion
- State machine feedback path isolation/diagnostics
- Serial readback register

Description

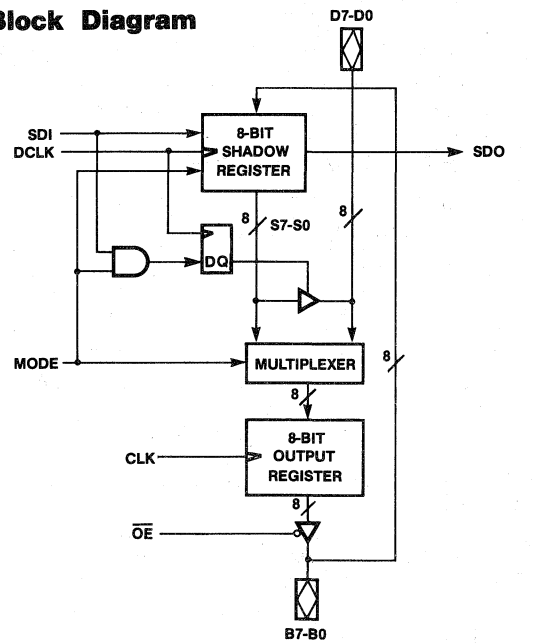
The SN54/74S818 is an 8-bit serializing/deserializing pipeline register. It can also be used as a serial readback register as well as a diagnostic register. All of these configurations are expandable in multiples of eight bits.

The 54/74S818 internally consists of a universal shift register and an 8-bit register. Its wide application results from a combination of powerful interconnection modes and independent clocking and pathing controls. It is ideally suited as a universal interface element involving both serial and parallel data formats.

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN74S818	NS, JS, NL (28)	Com
SN54S818	JS, W, L (28)	Mil

Block Diagram



Function Table

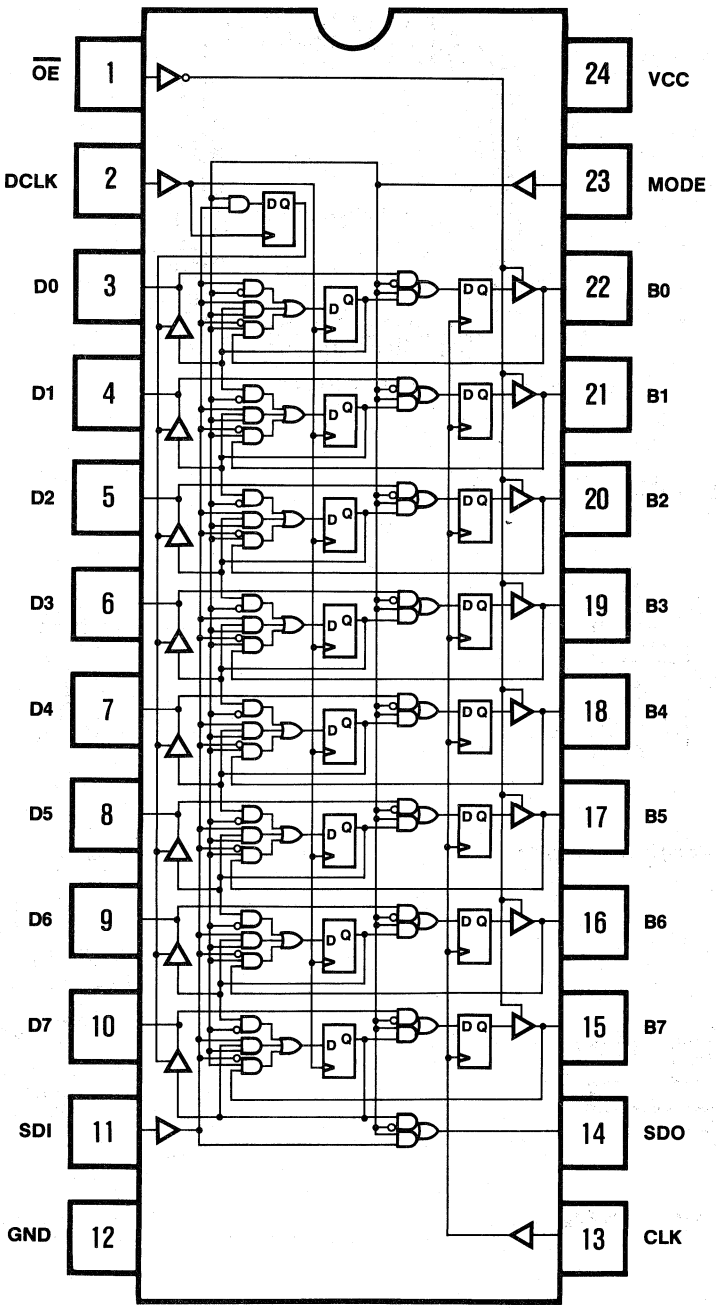
INPUTS				OUTPUTS			OPERATION	SEE FIG.
MODE	SDI	CLK	DCLK	B7-B0	S7-S0	SDO		
L	X	↑	*	Bn ← Dn	HOLD	S7	Load output register from input bus	1
L	X	*	↑	HOLD	Sn ← Sn-1 S0 ← SDI	S7	Shift shadow register data	2
L	X	↑	↑	Bn ← Dn	Sn ← Sn-1 S0 ← SDI	S7	Load output register from input bus while shifting shadow register data	1 & 2
H	X	↑	*	Bn ← Sn	HOLD	SDI	Load output register from shadow register	2,3,4
H	L	*	↑	HOLD	Sn ← Bn	SDI	Load shadow register from output bus	3
H	L	↑	↑	Bn ← Sn	Sn ← Bn	SDI	Swap shadow register and output register	
H	H	*	↑	HOLD	HOLD	SDI	Enable D7-D0 as outputs for RAM write-back	4

* Clock must be steady or falling.

SKINNYDIP® is a registered trademark of Monolithic Memories.

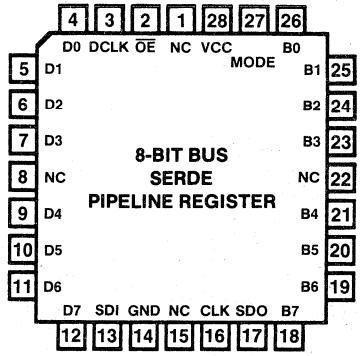
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories

Logic Diagram



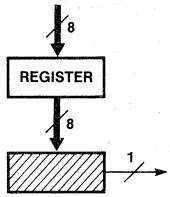
Pin Configuration

SN74S818

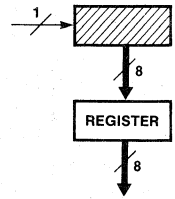


Plastic Chip Carrier

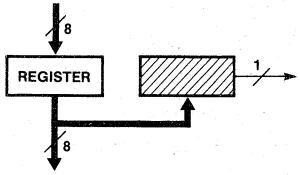
Typical Configurations



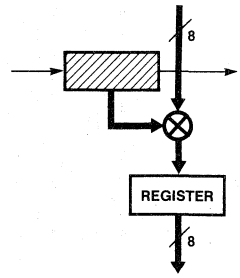
Serializing Pipeline Register



Deserializing Pipeline Register



Serial Readback Register



Diagnostic Register

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature		-55		125	0		75	°C
t_w	Width of CLK	High	15			12			ns
		Low	15			13			ns
t_{wd}	Width of DCLK	High	25			20			ns
		Low	25			20			ns
t_{suc}	Setup time from MODE to CLK		20↑			17↑			ns
t_{hc}	Hold time from CLK to MODE		0↑			0↑			ns
t_{sud}	Setup time from data to CLK		21↑			14↑			ns
t_{hd}	Hold time from CLK to data		0↑			0↑			ns
t_{sudc}	Setup time from SDI, MODE to DCLK		31↑			20↑			ns
t_{hdc}	Hold time from DCLK to SDI, MODE		0↑			0↑			ns
t_{sudq}	Setup time from output to DCLK		25↑			18↑			ns
t_{hdq}	Hold time from DLCK to output		0↑			0↑			ns

↑ ↓ The arrow indicates the transition of the clock/gate input used for reference: ↑ for the low-to-high transitions. ↓ for the high-to-low transitions.

13

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IH}	High-level input voltage				2			2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18 mA			−1.2			−1.2	V
I_{IL}	Low-level input current		V_{CC} = MAX	V_I = 0.5 V			−0.25			−0.25	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7 V			50			50	μA
I_I	Maximum input current	D or B	V_{CC} = MAX	V_I = 5.5 V			1			1	mA
		All others		V_I = 7 V							
V_{OL}	Low-level output voltage	B7-B0	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OL} = 32 mA						0.5	V
				I_{OL} = 24 mA			0.5				
		SDO D7-D0		I_{OL} = 8 mA						0.5	
				I_{OL} = 4 mA			0.5				
V_{OH}	High-level output voltage	B7-B0	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OH} = 6.5 mA	2.4			2.4			V
		SDO D7-D0		I_{OH} = −2 mA							
I_{OZL}	Off-state output current		V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2 V	V_O = 0.5 V			−250			−250	μA
I_{OZH}				V_O = 2.4 V			50			50	μA
I_{OS}	Output short-circuit current*		V_{CC} = MAX		−40		−100	−40		−100	mA
I_{CC}	Supply current		V_{CC} = MAX. Outputs open			115	155		115	145	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER		TEST CONDITIONS (See Test Load/Waveforms)	MIN	MAX	UNIT
f_{MAX}	Maximum output clock frequency		C_L = 50 pF R_L = 280Ω $\overline{OE}$ = L	40		MHz
f_{MAXD}	Maximum diagnostic clock frequency	Cascaded	C_L = 50 pF R_L = 2 KΩ	20		MHz
		Uncascaded		25		
t_{CLK}	CLK to output delay		C_L = 50 pF R_L = 280Ω $\overline{OE}$ = L		14	ns
t_{SS}	SDI to SDO delay (MODE = HIGH)		C_L = 50 pF R_L = 2 KΩ		12	ns
t_{MS}	MODE to SDO delay				17	ns
t_{DS}	DCLK to SDO delay (MODE = LOW)				28	ns
t_{DEZL}	DCLK to D7-D0 enable delay		C_L = 50 pF R_L = 2 KΩ		25	ns
t_{DEZH}					20	ns
t_{DDLZ}	DCLK to D7-D0 disable delay		C_L = 5 pF R_L = 2 KΩ		36	ns
t_{DDHZ}					60	ns
t_{DC}	DCLK to CLK separation		C_L = 50 pF R_L = 280Ω $\overline{OE}$ = L	22		ns
t_{CD}	CLK to DCLK separation			35		ns
t_{PZL}	Output enable delay		C_L = 50 pF R_L = 280Ω		19	ns
t_{PZH}					13	ns
t_{PLZ}	Output disable delay		C_L = 5 pF R_L = 280Ω		12	ns
t_{PHZ}					22	ns

Switching Characteristics Over Operating Range

SYMBOL	PARAMETER		TEST CONDITIONS (See Interface Test Load/Waveforms)	MILITARY MIN	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL MAX	UNIT
f_{MAX}	Maximum output clock frequency		C_L = 50 pF R_L = 280Ω OE = L	33		40		MHz
f_{MAXD}	Maximum diagnostic clock frequency	Cascaded	C_L = 50 pF R_L = 2 KΩ	16		20		MHz
		Uncascaded		20		25		
t_{CLK}	CLK to output delay		C_L = 50 pF R_L = 280Ω OE = L		18		14	ns
t_{SS}	SDI to SDO delay (MODE = HIGH)		C_L = 50 pF R_L = 2 KΩ		18		15	ns
t_{MS}	MODE to SDO delay				27		18	ns
t_{DS}	DCLK to SDO delay (MODE = LOW)				38		30	ns
t_{DEZL}	DCLK to D7-D0 enable delay		C_L = 50 pF R_L = 2 KΩ		35		25	ns
t_{DEZH}					30		25	ns
t_{DDLZ}	DCLK to D7-D0 disable delay		C_L = 5 pF R_L = 2 KΩ		45		45	ns
t_{DDHZ}					90		80	ns
t_{DC}	DCLK to CLK separation		C_L = 50 pF R_L = 280Ω OE = L	30		30		ns
t_{CD}	CLK to DCLK separation			45		40		ns
t_{PZL}	Output enable delay		C_L = 50 pF R_L = 280Ω		25		20	ns
t_{PZH}					20		15	ns
t_{PLZ}	Output disable delay		C_L = 5 pF R_L = 280Ω		20		15	ns
t_{PHZ}					30		25	ns

13

Timing Waveforms

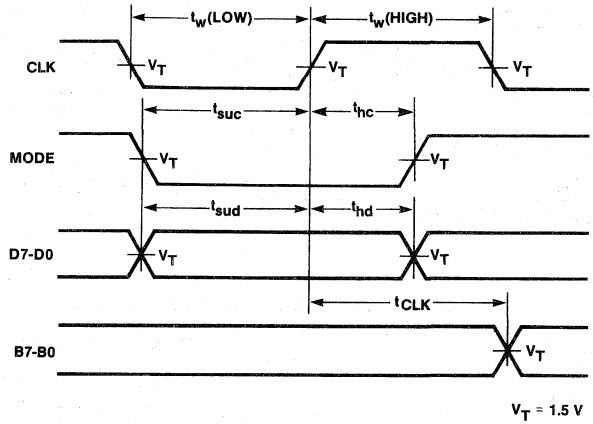


Figure 1. Switching waveforms for typical register applications ($\overline{OE}$ = L)

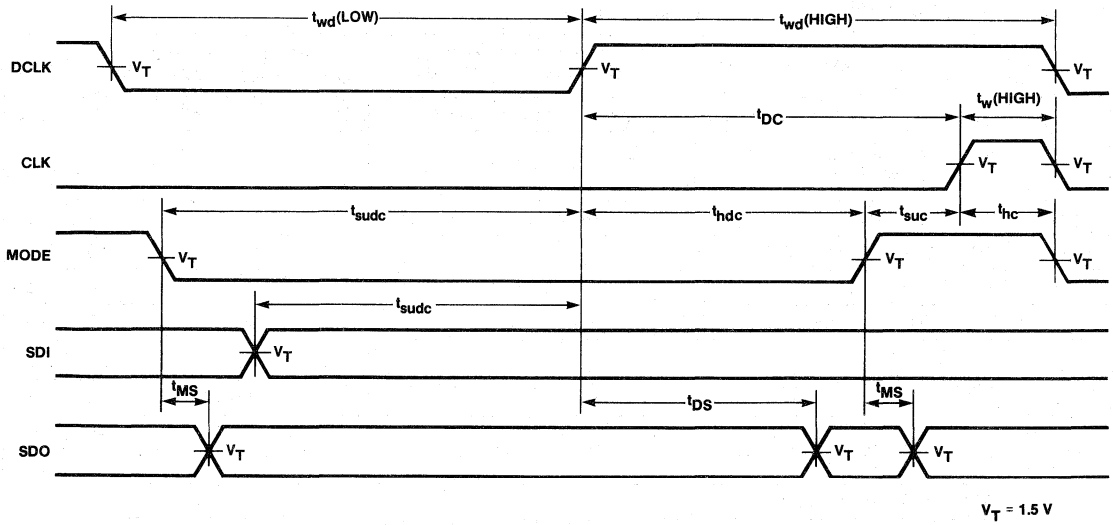


Figure 2. Switching waveforms for shift-in followed by diagnostic load

Timing Waveforms

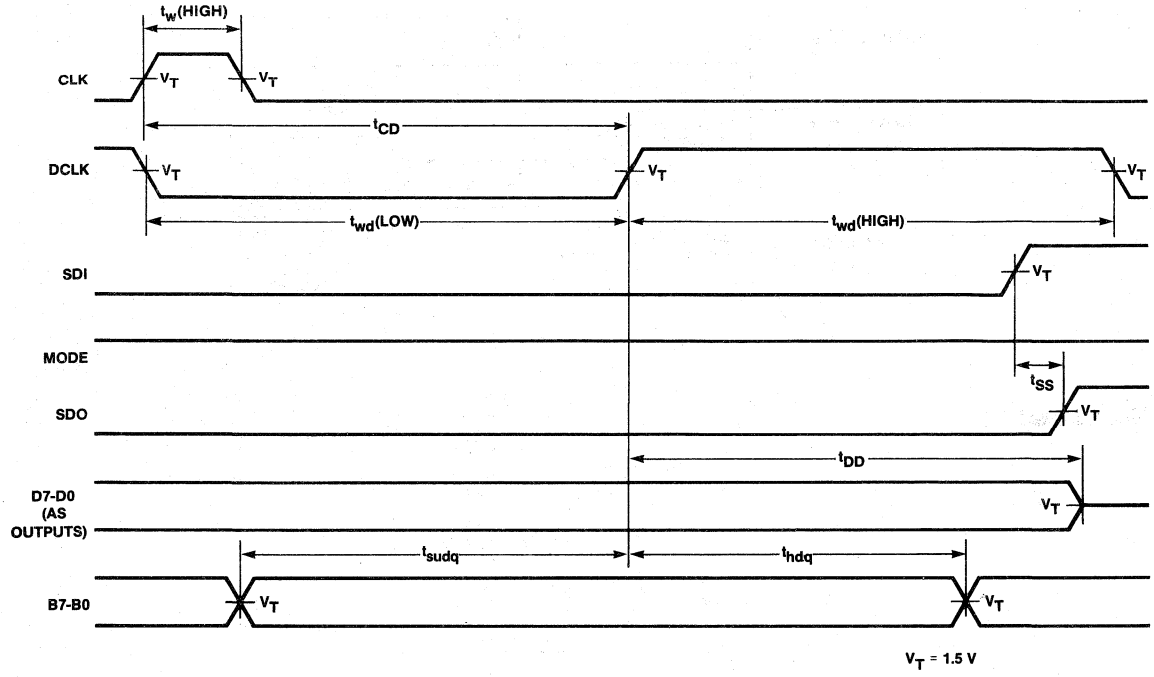
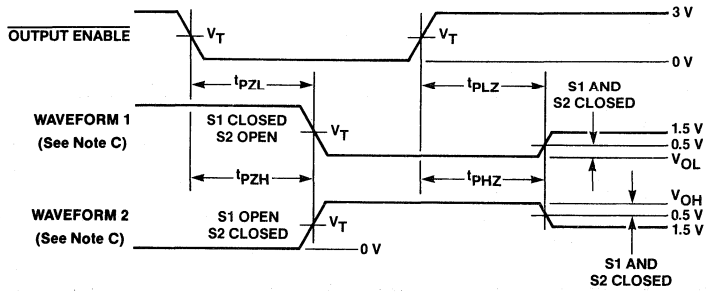


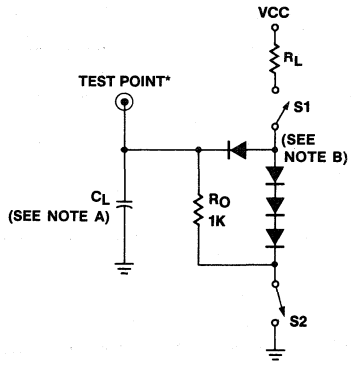
Figure 3. Switching waveforms for data bus (D7-D0) disabling

13

Enable/Disable Delay



Test Load



* The "TEST POINT" is drived by the output under test, and observed by instrumentation.

NOTES: A. C_L includes probe and jig capacitance.

B. All diodes are 1N916 or 1N3064.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. In the examples above the phase relationships between inputs and outputs have been chosen arbitrarily.

E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz Z_{out} = 50Ω and for series 54/74S t_R = 2.5 ns t_F ≤ 2.5 ns.

F. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

	B7-B0	D7-D0, SDO
R_O	1 KΩ	5 KΩ

Basics of Diagnostics

The basic theory of diagnostics is to insert test data to the inputs of a typical system and sample the test results from certain nodes of the circuits. For a combinatorial circuit, testing is very easy since the circuit has no memory of the previous states. But for a sequential circuit, the data to be sampled at a node depends not only on the inputs, but also on the current state it is in. If the previous state contains some error, it will possibly perform an illegal jump. In that case, depending on which state the system is currently in, the next state may be different. After several illegal jumps, it will be quite impossible to keep track of the jumps which it performs.

A way to solve the problem is by converting a sequential circuit to a combinatorial one. A sequential circuit can often be viewed as a network with a clock and a number of inputs and outputs, with some outputs being routed back to the inputs (see Figure 5a). If the loop is broken and inputs which are fed back from the outputs are instead fed in from some external sources (see Figure 5b), the system can be viewed as combinatorial and system testing will be easier. The "shadow register" concept involves shifting in serial data to the hidden register (the shadow register) and then loading test data to the output register. Together with other system inputs, the test results will appear on the output end of the network and can be sampled and analyzed. and analysed.

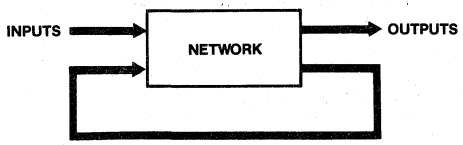


Figure 5a. A typical digital system

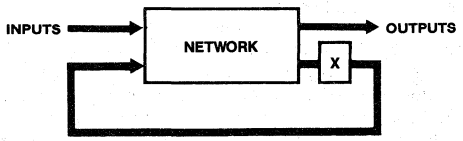


Figure 5b. The feedback of figure 5a is broken to convert the system to a non-sequential one

Diagnostic On-Chip™ (DOC™) Using Shadow Register

The diagnostic register is an 8-bit register with two levels of registers—a shadow register and an output register. A shadow register is basically a buried register with shift capability. There is also an output register whose outputs appear to the rest of the system. There is an output flipflop to each shadow flipflop. An output flipflop drives a three-state output buffer before going to the output pin. If the output is disabled, the output pin may be converted to an input pin. This feature is very important if the output is driving a bus and sampling of data on the bus is desired.

The input to a bit of the shadow register is a multiplexer which can select from one of the following nodes:

a) Output of the preceding bit of the shadow register (or SDI for the least significant bit).
b) Output of the same bit of the shadow register.
c) Data on the output pin of the same bit. This data may be the output of the corresponding bit of the output register if there is no output enable pin and the output is enabled, or the input to that pin if there is an output enable pin and output is disabled. Refer to Figure 6 for some general information on a typical diagnostic functional part with output enable ($\overline{OE}$).

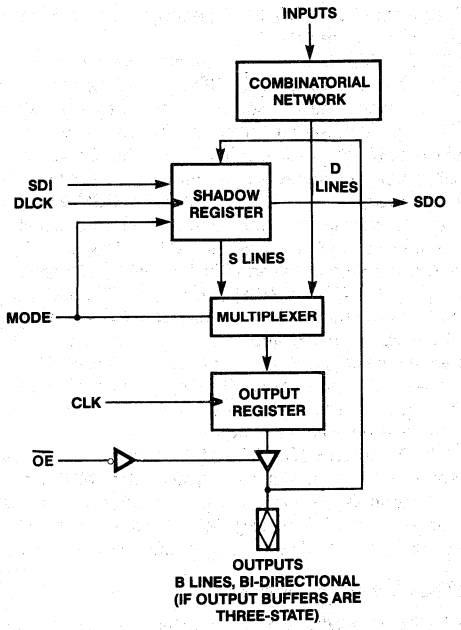


Figure 6. A typical functional block diagram for a diagnostic part

The input to any bit of the output register is also selected from one of the following nodes:
a) Corresponding input bit.
b) Corresponding output bit of the shadow register.

The reasons why a shadow register is preferred, as compared to shifting in diagnostic data directly to the output register, are:
a) The output register contains control signals for the system. Certain bits of this register may control different ports which are driving the same bus. As diagnostic data is shifted in, these bits become random and the ports they are controlling may drive a bus simultaneously. Invalid data may appear and worst of all, with a low-impedance path between the power supply, severe damage may be done to these ports.
b) As a diagnostic word is shifted in, the system is performing different tasks from what it is supposed to do. For example, when an ALU is performing an addition, diagnostic data is shifted in. The ALU then performs some other functions. The status of the system keeps changing. In some cases, illegal states may appear which produces unpredictable test results; for example, a flag may appear unpredictably.
c) The shadow register enables diagnostic data to be shifted in as background data without holding up the processor operation.

The diagnostic register is one part in a series of diagnostic products which follows a new standard for diagnostics. The basic standard is described in Figure 6 and the table on page one. This standard implies that all diagnostic parts in this series are cascadable.

Diagnostic Pins

There are several pins in the diagnostic register in addition to the regular 8-bit inputs and outputs:

1) Diagnostic Clock (DCLK)—The diagnostic clock is used to clock the shadow register.

2) MODE—This pin is used in selecting the data to the registers. For the output register, MODE = LOW indicates that the output register is being used as a normal register; MODE = HIGH means that the next state of the output register will be obtained from the shadow register. For the shadow register, MODE = LOW indicates serial data from SDI (see below) is shifted in every diagnostic clock; MODE = HIGH switches SDI from a data input to a control input. See below for details.

3) Serial Data In (SDI)—When MODE = LOW, this pin is for shifting serial data in. When MODE = HIGH, SDI serves as a control pin. If MODE = HIGH and SDI = LOW, data from the output pins will be loaded to the shadow register on the next DCLK. MODE = HIGH and SDI = HIGH indicate a reserved operation. The data from the diagnostic clock is held the same. This reserved operation will be very significant when more operations than what is described are needed. The diagnostic register gives an example of how it can be used.

4) Serial Data Out (SDO)—When MODE = LOW, this pin carries the shift-out bit of the shadow register. When MODE = HIGH, the SDI becomes a control pin and the control signal should be passed along if several diagnostic parts are connected together serially. So SDO should carry SDI along in this case.

Write-Back to RAMs

Due to the applications of a diagnostic register in a writable microprogram control store, this part also includes an additional feature to initialize the control RAMs; when necessary, the input data pins to the register can be operated as output pins. In short, a diagnostic register is an 'asymmetric register transceiver' with shift capability. The term 'asymmetric register transceiver' means that there are two bidirectional registered ports on a chip, and these ports are enabled with different methodologies and have different timings. One port is still primarily for inputs (D7-D0), while the other is primarily for outputs (B7-B0).

When MODE and SDI are both HIGHs, the D7-D0 will be converted to an output port on the rising edge of the next DCLK by enabling the three-state buffers driving the D7-D0. The input for the three-state buffers is from the outputs of the shadow register (S7-S0).

Applications

This part can be used as a: microprogram control store register, data register, status register, address register, instruction register, interrupt mask register, interrupt vector, program counter, stack pointer, and for other general purposes.

If the diagnostic registers are used in a system using microprogram control words, status registers, and instruction registers, etc., one way to connect them together is shown in Figure 7. There is only one data input and one data output to the diagnostic parts. When serial data is shifted in or shifted out, data has to be passed from one diagnostic chip to another. Since SDI must be passed from chip-to-chip if it is used for control, it is necessary for logic designers to make sure the fall-through time of SDI to the last chip and the setup time from SDI to DCLK are satisfied.

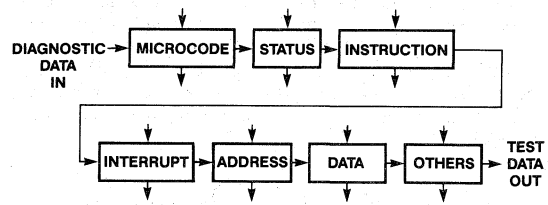


Figure 7. One way diagnostic registers can be linked together

The diagnostic registers are basically used for diagnostic purposes, although they may also function as parallel-to-serial and serial-to-parallel converters.

Two examples of how the diagnostic parts can be built into a system are shown in Figures 8, 9. The diagnostic registers are used to substitute the instruction register, memory data registers, status register, memory address registers, and the registers for a non-writable (Figure 8) or a writable (Figure 9) microprogram control store. The only additional block to a typical system without diagnostic features is the diagnostics controller. The diagnostics controller should be able to supply the system with signals like MODE, SDI, DCLK, and the register clock (CLK). In order words, the diagnostics controller in itself is a supercontroller of the processing unit. It should also be noted that all sequential paths, except for the register files, should be converted to combinatorial paths if all the diagnostic parts are to break the sequential loops.

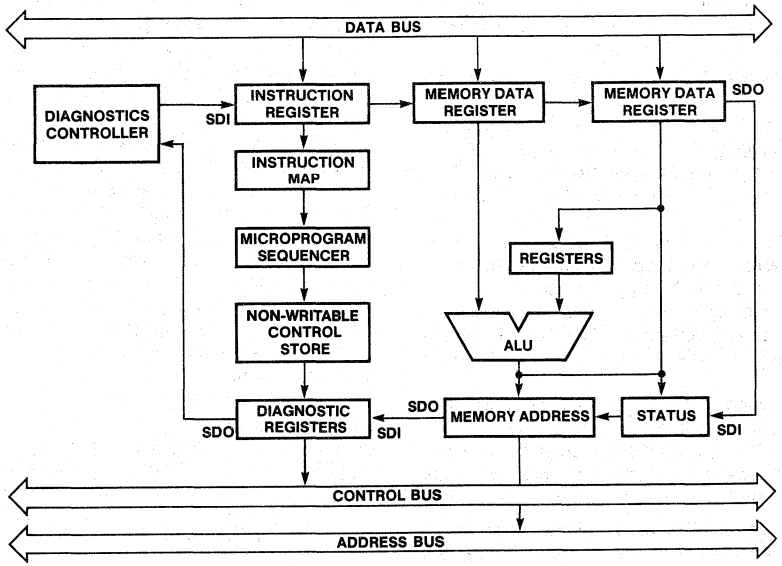


Figure 8. An application example of using diagnostic registers in a CPU using non-writable control store

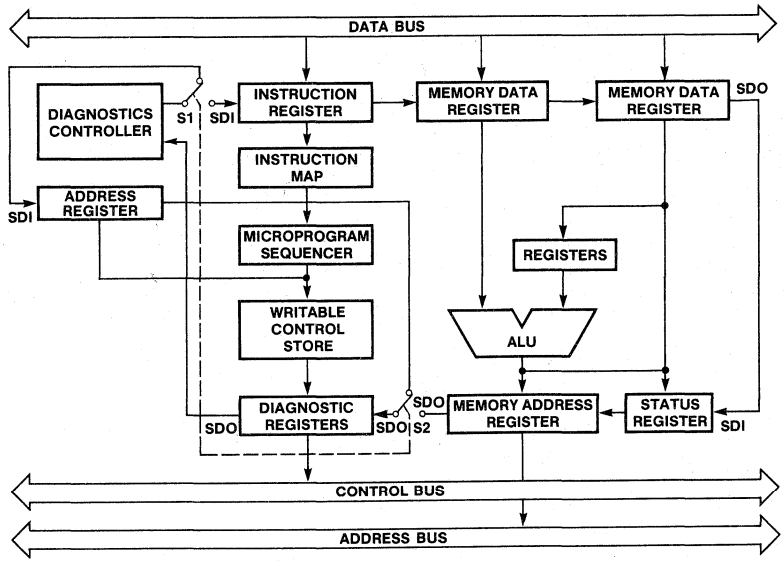


Figure 9. An application example of using diagnostic registers in a CPU using writable control store

13

In normal operation, the diagnostic controller will make the diagnostic feature inactive by setting MODE = LOW and disabling DCLK and have the CLK free running.

When diagnostics are needed, the following sequence is performed:

1) Shift in diagnostic test data bit-by-bit. In order to perform this operation, CLK is disabled; MODE remains LOW; SDI contains the bit to be shifted in, and the diagnostic clock is enabled. This will continue until a full test vector is shifted into the shadow register.
2) MODE switches to HIGH. Then DCLK is disabled and CLK is enabled. The contents of the shadow register, which is the test vector, will be loaded into the output register.
3) The test result is set up at the inputs of the diagnostic registers. MODE switches to LOW again. DCLK is still disabled and CLK is still enabled. The test result will be clocked into the output register.
4) With MODE HIGH and DCLK enabled and CLK disabled, the test result will be clocked to the shadow register.
5) With MODE held LOW and DCLK still enabled and CLK still disabled, the test result can be shifted out and analyzed while another test vector is shifted in.

A block diagram of such a diagnostics controller is shown in Figure 10. The central control unit of this controller may be a disk-based unit or even a diagnostic PROM. Note that, in normal operation, MODE remains LOW and only CLK is active.

Figure 9 is an example with writable programmable control store where initialization of the control RAMs is necessary. This can be done by loading in a sequence of data and address through the diagnostics controller. What this controller must be able to do, in addition to what is described above (see Figure 10), is to disable the outputs from the microprogram sequencer and feed in the address through another diagnostic register. There is a switch, S1, which switches the SDI to the registers of the writable control store from some other register (in Figure 9, it is the memory address register) to the diagnostic 'control store address' register. The initialization data is shifted into the shadow register by resetting MODE to LOW and enabling DCLK. After all data is shifted into the shadow register, MODE and SDI are set HIGH and then followed by a CLK, a DCLK, and a write to control store. The CLK loads the present control store address in the output registers of the 'control store address' register, and the MODE = HIGH and SDI = HIGH will enable the inputs to the diagnostic register as outputs, so that the data in the shadow register can be written back to the control store.

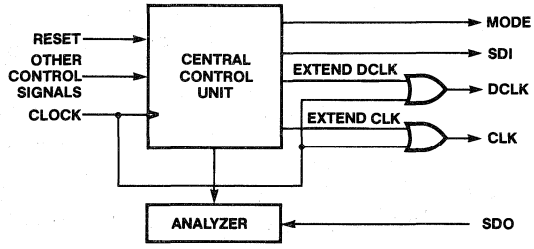


Figure 10. A diagnostic controller unit

8-Bit Bus Latch Transceivers- Advanced CMOS-TTL Compatible

74ACT547 74ACT567

Features/Benefits

- **Bidirectional transceivers utilizing latches**
- **Independent latches for A bus and B bus**
- **Data can be swapped between internal latches**
- **8-bit data paths match byte boundaries**
- **'547/'567 devices can replace two '373 devices**
- **Independent gate enables for rank A and rank B**
- **Low quiescent supply current of < 10 μA (typical)**
- **Active supply current at about 20% LS equivalent**
- **Wide commercial operating supply and temperature ranges 4.5 V to 5.5 V; -40°C to +85°C**
- **24-pin SKINNYDIP® saves space.**

Description

These transceivers have a pair of 8-bit latches connected back-to-back, i.e. the bus pins are used for input or output. The latches are followed by either non-inverting ('ACT547) or inverting ('ACT567) three-state buffers.

Both devices have independent gate enable inputs for ranks A and B (GA1, $\overline{GA2}$, GB1, $\overline{GB2}$), and independent output enables for ranks A and B ($\overline{OEAB}$, $\overline{OEBA}$).

The direction of operation is controlled by $\overline{OEAB}$ and $\overline{OEBA}$. When $\overline{OEAB}$ is Low and $\overline{OEBA}$ is High, the devices operate in the A-to-B direction. When OEAB is High and $\overline{OEBA}$ is Low, the devices operate in the B-to-A direction. When $\overline{OEAB}$ and $\overline{OEBA}$ are both High, the A and B buses are configured as inputs. When $\overline{OEAB}$ and $\overline{OEBA}$ are both Low, the A and B buses are configured as outputs. See the Bus Operation Tables for the detailed operation.

Data is passed through the latch whenever either of the gate enables for the respective rank (GA1 or $\overline{GA2}$, GB1 or $\overline{GB2}$) are asserted.

All of the 8-bit devices are packaged in the popular 24-pin SKINNYDIP® package.

Ordering Information

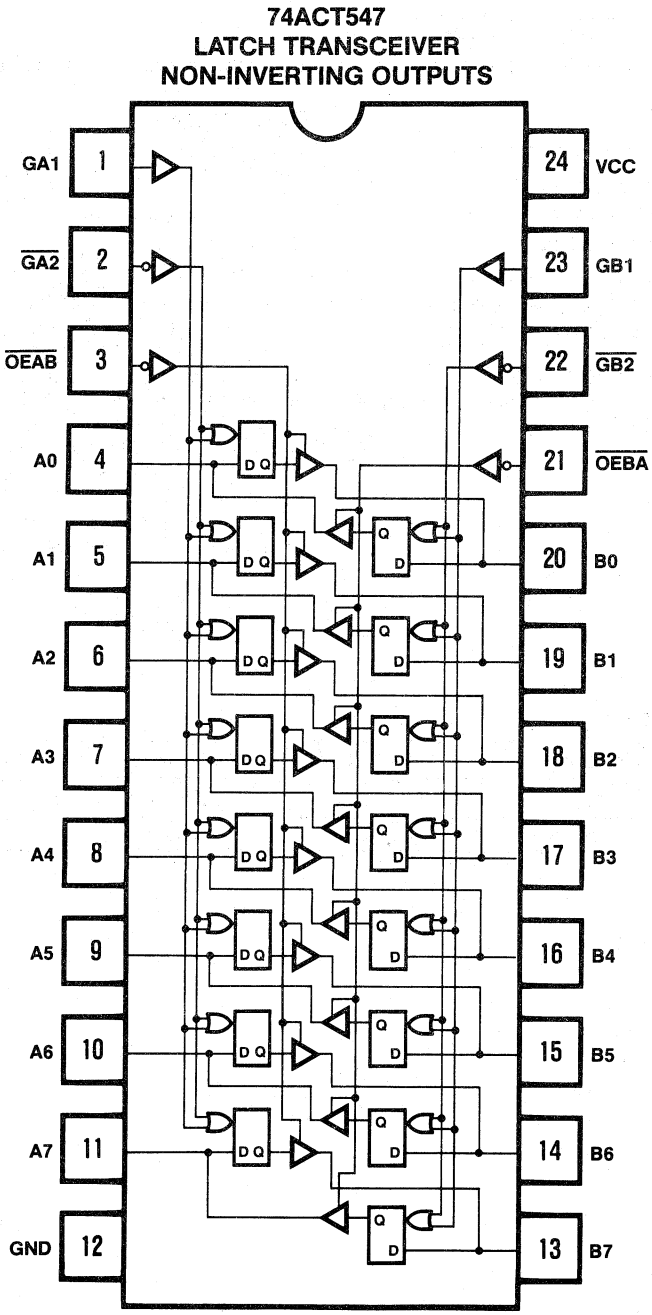
PART NUMBER	PACKAGE	TEMPERATURE	POLARITY	TYPE	TECH
74ACT547	NS, JS	Commercial	Noninvert	Latch	CMOS
74ACT567	NS, JS	Commercial	Invert		

13

SKINNYDIP® is a registered trademark of Monolithic Memories.

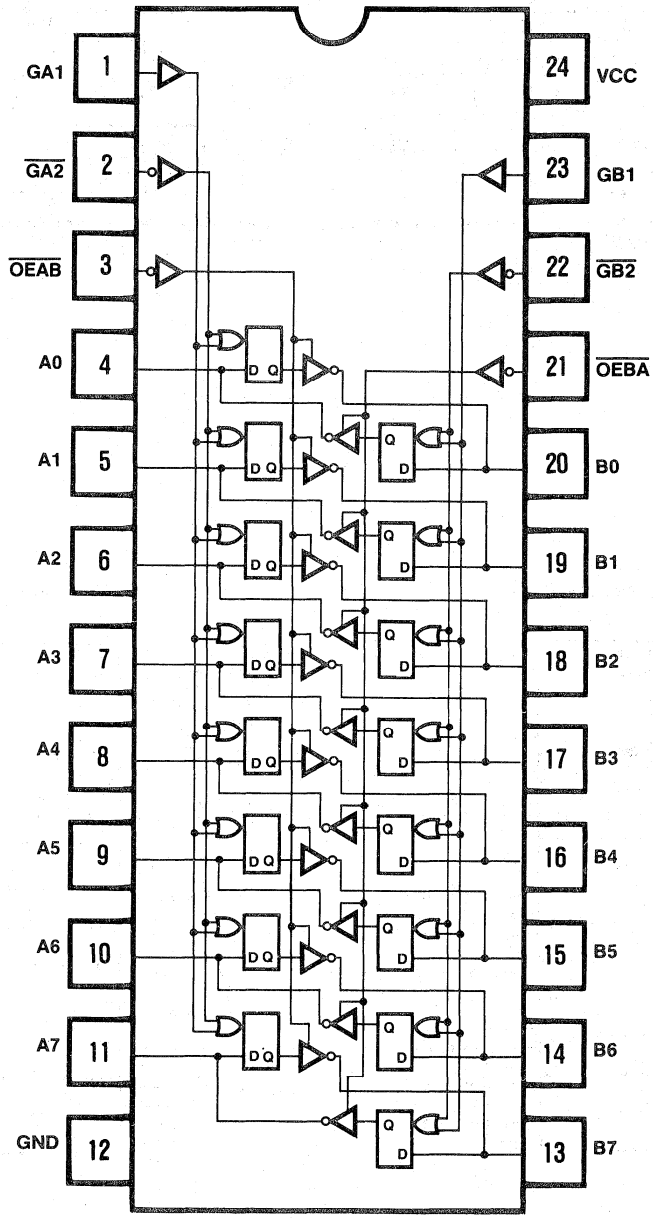
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374
Monolithic Memories MMI

Logic Symbol



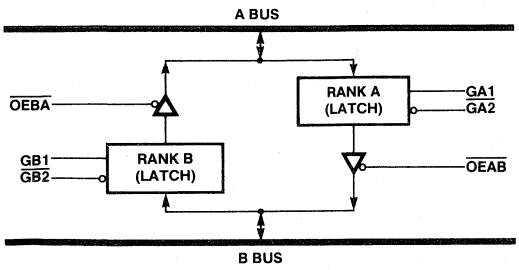
Logic Symbol

74ACT567
LATCH TRANCEIVER
INVERTING OUTPUTS

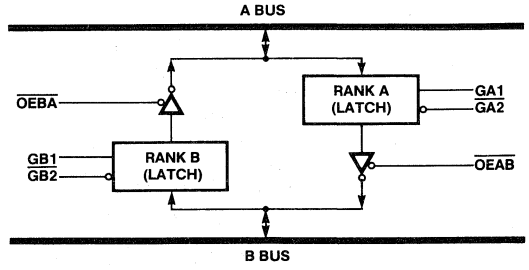


Block Diagrams

'ACT547 (Non-inverting)

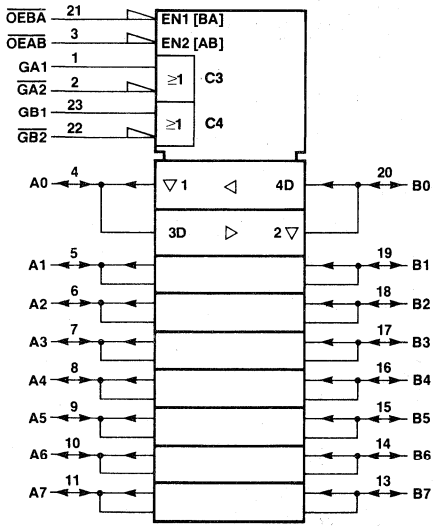


'ACT567 (Inverting)

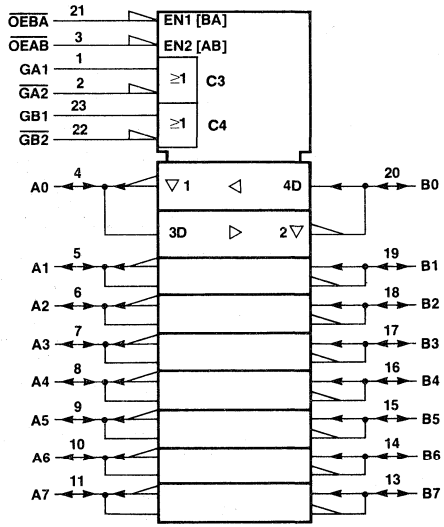


IEEE Symbols

'ACT547 (Non-inverting)



'ACT567 (Inverting)



Function Table Nomenclature Description

A0-A7: Eight input/output pins on the A side.

B0-B7: Eight input/output pins on the B side.

X: H or L state irrelevant ("Don't Care" conditions).

GA1/$\overline{GA2}$: Gate enables for rank A of 'ACT547/'ACT567.

GB1/$\overline{GB2}$: Gate enables for rank B of 'ACT547/'ACT567.

QoA/QoB: Previous data of the internal rank A/B.

GA1	$\overline{GA2}$	RANK A	GB1	$\overline{GB2}$	RANK B
X	L	Enabled (Flush)	X	L	Enabled (Flush)
X	L	Enabled (Flush)	L	H	Disabled (Freeze)
L	H	Disabled (Freeze)	X	L	Enabled (Flush)
L	H	Disabled (Freeze)	L	H	Disabled (Freeze)
H	X	Enabled (Flush)	X	L	Enabled (Flush)
H	X	Enabled (Flush)	L	H	Disabled (Freeze)
H	X	Enabled (Flush)	H	X	Enabled (Flush)

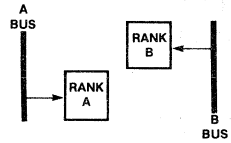
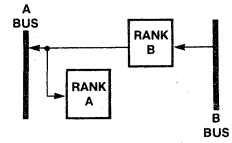
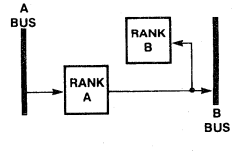
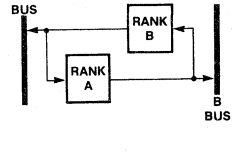
$\overline{OEAB}$: To enable the A-to-B operation.

$\overline{OEBA}$: To enable the B-to-A operation.

$\overline{OEAB}$	$\overline{OEBA}$	OPERATION DIRECTION
L	L	A, B buses both are outputs (Transfer stored data to bus stored)
L	H	A-to-B
H	L	B-to-A
H	H	A, B buses both are inputs (storage)

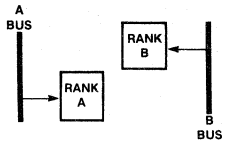
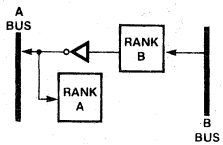
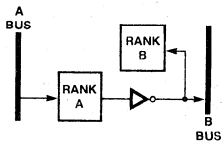
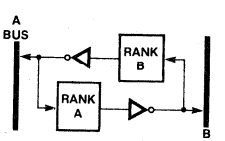
13

Bus Operation for 'ACT547

OPERATION	DIRECTION CONTROL		DATA I/O		BLOCK DIAGRAM	GATE ENABLE (A)		RANK A	GATE ENABLE (B)		RANK B
	$\overline{OEAB}$	$\overline{OEBA}$	A0-A7	B0-B7		GA1	$\overline{GA2}$		GB1	$\overline{GB2}$	
Storage	H	H	Input	Input		L	H	QoA	L	H	QoB
						L	H	QoA	H	X	B bus
						L	H	QoA	X	L	B bus
						H	X	A bus	L	H	QoB
						H	X	A bus	H	X	B bus
						H	X	A bus	X	L	B bus
						X	L	A bus	L	H	QoB
						X	L	A bus	H	X	B bus
						X	L	A bus	X	L	B bus
B-to-A Operation	H	L	Output of Rank B	Input		L	H	QoA	L	H	QoB
						L	H	QoA	H	X	B bus
						L	H	QoA	X	L	B bus
						H	X	Rank B	L	H	QoB
						H	X	Rank B	H	X	B bus
						H	X	Rank B	X	L	B bus
						X	L	Rank B	L	H	QoB
						X	L	Rank B	H	X	B bus
						X	L	Rank B	X	L	B bus
A-to-B Operation	L	H	Input	Output of Rank A		L	H	QoA	L	H	QoB
						L	H	QoA	H	X	Rank A
						L	H	QoA	X	L	Rank A
						H	X	A bus	L	H	QoB
						H	X	A bus	H	X	Rank A
						H	X	A bus	X	L	Rank A
						X	L	A bus	L	H	QoB
						X	L	A bus	H	X	Rank A
						X	L	A bus	X	L	Rank A
Transfer Stored Data	L	L	Output of Rank B	Output of Rank A		L	H	QoA	L	H	QoB
						L	H	QoA	H	X	Rank A
						L	H	QoA	X	L	Rank A
						H	X	Rank B	L	H	QoB
						H*	X	Rank B	H	X	Rank A
						H*	X	Rank B	X	L	Rank A
						X	L	Rank B	L	H	QoB
						X*	L	Rank B	H	X	Rank A
						X*	L	Rank B	X	L	Rank A

* Note: These controls for $\overline{OEAB}$, $\overline{OEBA}$, GA1, $\overline{GA2}$, GB1 and $\overline{GB2}$ can cause race conditions.

Bus Operation for 'ACT567

OPERATION	DIRECTION CONTROL		DATA I/O		BLOCK DIAGRAM	GATE ENABLE (A)		RANK A	GATE ENABLE (B)		RANK B
	$\overline{OEAB}$	$\overline{OEBA}$	A0-A7	B0-B7		GA1	$\overline{GA2}$		GB1	$\overline{GB2}$	
Storage	H	H	Input	Input		L	H	QoA	L	H	QoB
						L	H	QoA	H	X	B bus
						L	H	QoA	X	L	B bus
						H	X	A bus	L	H	QoB
						H	X	A bus	H	X	B bus
						H	X	A bus	X	L	B bus
						X	L	A bus	L	H	QoB
						X	L	A bus	H	X	B bus
						X	L	A bus	X	L	B bus
B-to-A Operation	H	L	Output of $\overline{\text{Rank B}}$	Input		L	H	QoA	L	H	QoB
						L	H	QoA	H	X	B bus
						L	H	QoA	X	L	B bus
						H	X	$\overline{\text{Rank B}}$	L	H	QoB
						H	X	$\overline{\text{Rank B}}$	H	X	B bus
						H	X	$\overline{\text{Rank B}}$	X	L	B bus
						X	L	$\overline{\text{Rank B}}$	L	H	QoB
						X	L	$\overline{\text{Rank B}}$	H	X	B bus
						X	L	$\overline{\text{Rank B}}$	X	L	B bus
A-to-B Operation	L	H	Input	Output of $\overline{\text{Rank A}}$		L	H	QoA	L	H	QoB
						L	H	QoA	H	X	$\overline{\text{Rank A}}$
						L	H	QoA	X	L	$\overline{\text{Rank A}}$
						H	X	A bus	L	H	QoB
						H	X	A bus	H	X	$\overline{\text{Rank A}}$
						H	X	A bus	X	L	$\overline{\text{Rank A}}$
						X	L	A bus	L	H	QoB
						X	L	A bus	H	X	$\overline{\text{Rank A}}$
						X	L	A bus	X	L	$\overline{\text{Rank A}}$
Transfer Stored Data	L	L	Output of $\overline{\text{Rank B}}$	Output of $\overline{\text{Rank A}}$		L	H	QoA	L	H	QoB
						L	H	QoA	H	X	$\overline{\text{Rank A}}$
						L	H	QoA	X	L	$\overline{\text{Rank A}}$
						H	X	$\overline{\text{Rank B}}$	L	H	QoB
						H*	X	$\overline{\text{Rank B}}$	H	X	$\overline{\text{Rank A}}$
						H*	X	$\overline{\text{Rank B}}$	X	L	$\overline{\text{Rank A}}$
						X	L	$\overline{\text{Rank B}}$	L	H	QoB
						X*	L	$\overline{\text{Rank B}}$	H	X	$\overline{\text{Rank A}}$
						X*	L	$\overline{\text{Rank B}}$	X	L	$\overline{\text{Rank A}}$

* Note: These controls for $\overline{OEAB}$, $\overline{OEBA}$, GA1, $\overline{GA2}$, GB1, and $\overline{GB2}$ can cause race conditions.

13

Absolute Maximum Ratings

Supply voltage, V_{CC} ..... −0.5 V to 7.0 V
DC input voltage, V_I ..... −0.5 V to V_{CC} + 0.5 V
DC output voltage, V_O ..... −0.5 V to V_{CC} + 0.5 V
DC output source/sink current per output pin, I_O ..... ±35 mA
DC V_{CC} or ground current, I_{CC} or I_{GND} ..... ±200 mA
Input diode current, I_{IK}:
V_I<0 ..... −20 mA
V_I>V_{CC} ..... +20 mA
Output diode current, I_{OK}:
V_O<0 ..... −20 mA
V_O>V_{CC} ..... +20 mA
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER			COMMERCIAL MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage			4.5	5	5.5	V
T_A	Operating free air temperature			−40		85	°C
t_w	Width of gate	High		12			ns
		Low		12			
t_{su}	Setup time	'ACT547	GA1, GB1	8↓			ns
			$\overline{GA2}$, $\overline{GB2}$	8↑			
		'ACT567	GA1, GB1	8↓			
			$\overline{GA2}$, $\overline{GB2}$	8↑			
t_h	Hold time	'ACT547	GA1, GB1	8↓			ns
			$\overline{GA2}$, $\overline{GB2}$	8↑			
		'ACT567	GA1, GB1	8↓			
			$\overline{GA2}$, $\overline{GB2}$	↑			
t_r	Input rise time at V_I = 4.5 V			0		500	ns
t_f	Input fall time at V_I = 4.5 V			0		500	ns

↑ ↓ The arrows indicate the transition of the gate control input used as reference: ↑ for the LOW-to-HIGH transitions, ↓ for the HIGH-to-LOW transitions.

Electrical Characteristics Over Operating Conditions

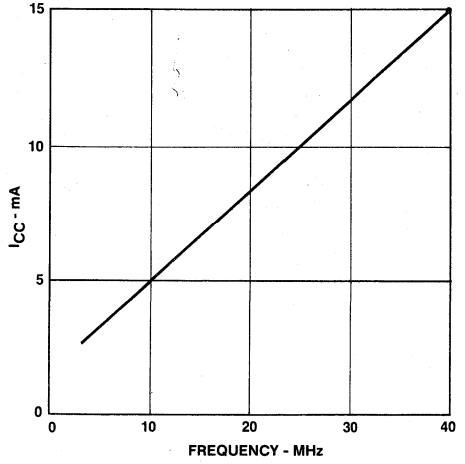
SYMBOL	PARAMETER	TEST CONDITIONS		COMMERCIAL MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
I_{IN}	Input current	V_{CC} = MAX	V_I = V_{CC} or GND			± 1.0	µA
V_{OL}	Low-level output voltage	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 20 µA			0.1	V
			I_{OL} = 6 mA			0.37	
			I_{OL} = 12 mA			0.4	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -20 µA	3.4			V
			I_{OH} = -6 mA	2.4			
I_{OZ}	Off-state output current	V_{CC} = MAX	V_O = V_{CC} or GND			± 30	µA
I_{CC}	Quiescent supply current	V_{CC} = MAX	V_I = V_{CC} or GND			80	µA

Switching Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveform)	COMMERCIAL MIN	MAX	UNIT
t_{PLH}	GA1, $\overline{GA2}$, GB1 or $\overline{GB2}$ to output delay	C_L = 50 pF		32	ns
t_{PHL}				32	
t_{PLH}	Data to output delay			32	ns
t_{PHL}				32	
t_{PZL}	Output enable delay	R_L = 1 KΩ, C_L = 50 pF		34	ns
t_{PZH}				34	
t_{PLZ}	Output disable delay			34	ns
t_{PHZ}				34	

Typical I_{CC} vs Frequency

74ACT547/567

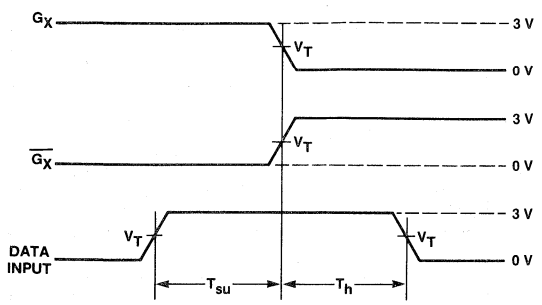


13

Definition of Waveforms

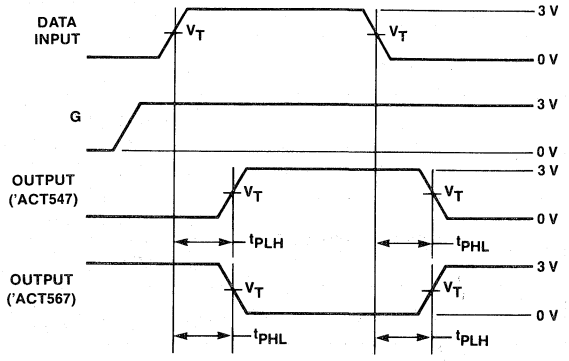
'ACT547/567

Setup and Hold



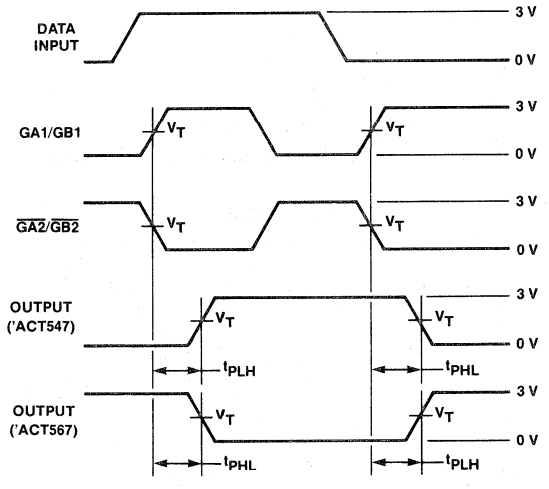
V_T = 1.3 V

Data D to Output Delay



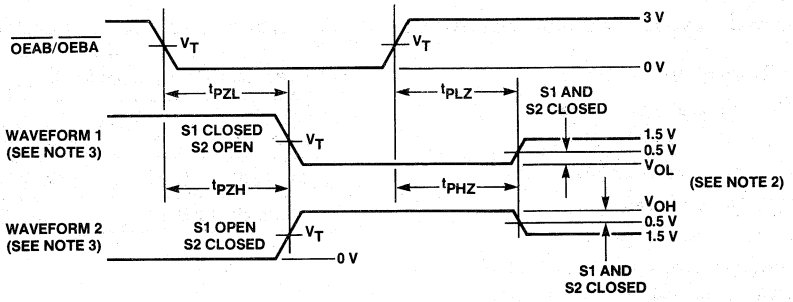
V_T = 1.3 V

GA1, $\overline{GA2}$, GB1 or $\overline{GB2}$ to Output Delay

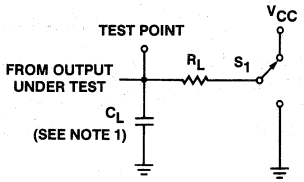


V_T = 1.3 V

Enable/Disable Waveforms



Test Load



13

Notes: 1. C_L includes probe and jig capacitance.

2. When measuring t_{PZL}, $S_1$1 is tied to V_{CC}. When measuring t_{PHZ} and t_{PZH}, S_1 is tied to ground.
   When measuring propagation delay times of three-state outputs, S_1 is open, i.e. not connected to V_{CC} or ground.
3. Waveform 1 is for an output with internal conditions such that the output is Low except when disabled by the output control.
   Waveform 1 is for an output with internal conditions such that the output is High except when disabled by the output control.
4. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
5. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_{out} = 50\ \Omega$.

8-Bit Bus Front-Loading Latch Transceivers — Advanced CMOS-TTL Compatible

74ACT646 74ACT648

Features/Benefits

- Bidirectional bus transceiver and register
- Independent registers for A and B buses
- Real-time data transfer or stored data transfer
- 24-pin SKINNYDIP® saves space
- Three-state outputs drive bus lines
- Low quiescent supply current of <10 μA (typical)
- Active supply current at about 20% LS equivalent
- Wide commercial operating supply and temperature ranges 4.5 V to 5.5 V; -40°C to +85°C

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	OUTPUT	TECH
74ACT646	NS,JS	Com	Noninvert	Three-state	CMOS
74ACT648	NS,JS	Com	Invert		

Description

This 8-bit bus transceiver with three-state outputs has sixteen D-type flip-flops and multiplexers. The bus-oriented pinout of the part is shown in the Pin Configuration. The internal gate-level hardware configurations for the 'ACT646/648 are given in the Logic Diagram. The basic repeated element, consisting of an edge-triggered flip-flop paralleled with a bypassing path, or "feed-through", into a two-way multiplexer is sometimes called a "front-loading latch."

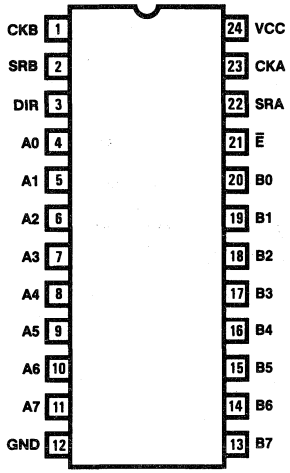
A pair of multiplexers are used to distribute two bytes of data through the part. The data-routing combinations offered by the multiplexers provide flexibility in directing data to or from either bus, and/or either register. Data is loaded into registers A or B upon the rising edge of the appropriate clock signals. CKA clocks register A, which receives data from the B bus directly at its inputs. Similarly, CKB clocks register B, which has the A bus available directly at its inputs. Control of the multiplexers is provided by two select lines (one per register), SRA and SRB. Command of the outputs is performed by enable line $\overline{E}$, and direction line DIR.

When $\overline{E}$ is High, data from the buses can be stored into register A and B. When $\overline{E}$ is Low and DIR is High, the direction of operation is from A to B, when $\overline{E}$ and DIR are Low, the direction of operation is from B to A.

SRA is used to select between register A and the B bus, and then to route the data to a controlled buffer connected to the A bus. Likewise, SRB selects between register B and the A bus, and then routes the data to the B bus through a controlled buffer.

Pin Configurations

'ACT646/648
8-Bit Bus Front-Loading Latch Transceiver

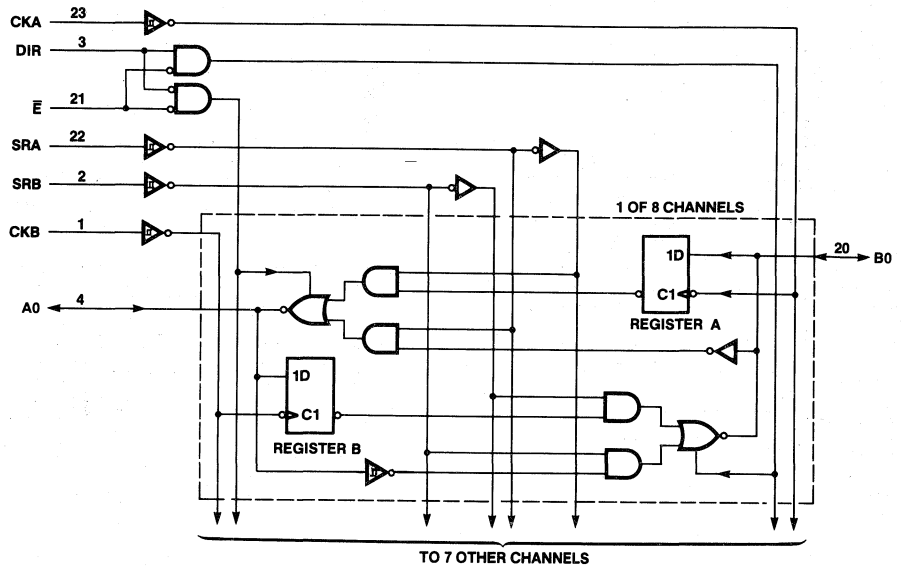


SKINNYDIP® is a registered trademark of Monolithic Memories.

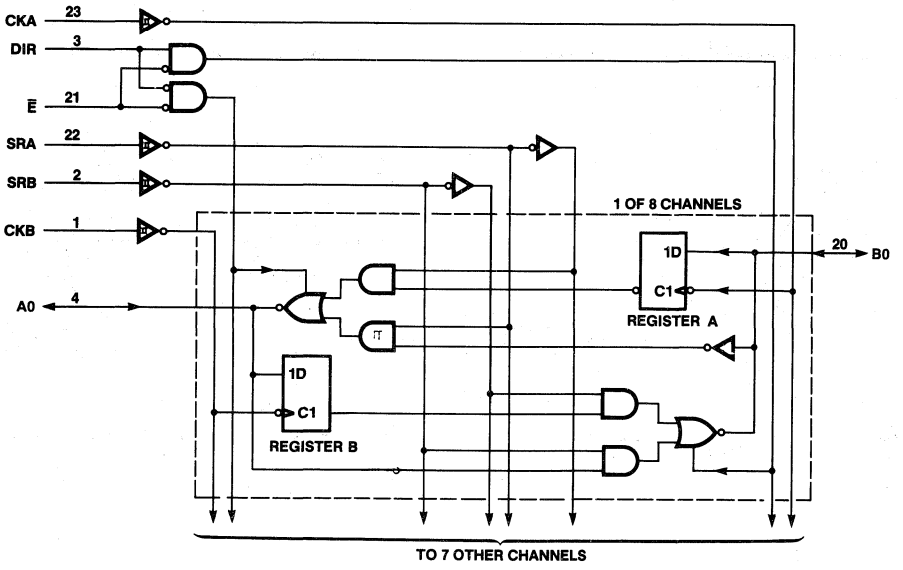
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374
Monolithic Memories

Logic Diagrams

'ACT646 (Non-Inverting)



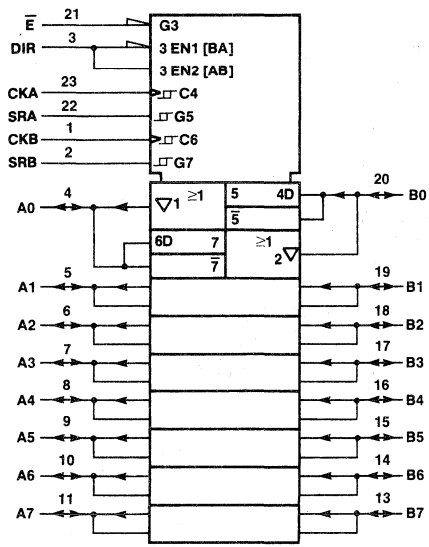
'ACT648 (Inverting)



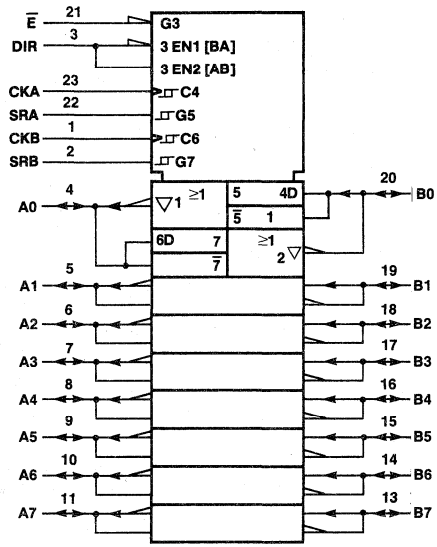
13

IEEE Symbols

'ACT646

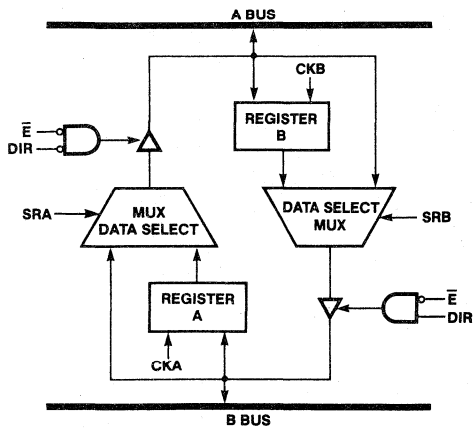


'ACT648

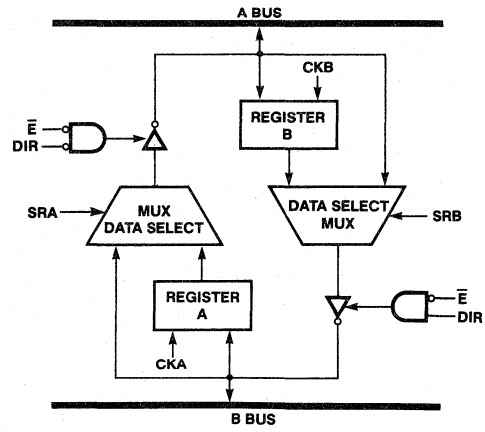


Block Diagrams

'ACT646 (Non-inverting)



'ACT648 (Inverting)



Function Table Nomenclature Description

$\overline{E}$: To enable A-to-B or B-to-A operation.

DIR: To select the direction of operation.

$\overline{E}$	DIR	OPERATION DIRECTION
L	L	B-to-A
L	H	A-to-B
H	X	A and B buses both are inputs (Storage)

SRA/SRB: To select the output data coming from the A/B register if SRA/SRB is a High level; otherwise, directly from the input data bus.

A0-A7: Eight input/output pins on the A side.

B0-B7: Eight input/output pins on the B side.

CKA/CKB: Clock for Register A/B.

X: H or L state irrelevant ("Don't Care" condition).

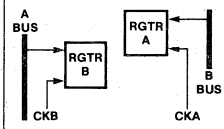
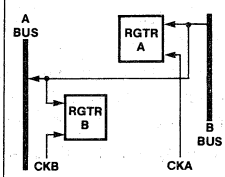
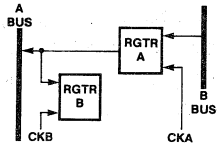
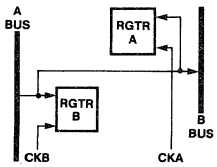
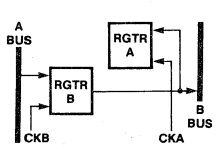
↑: Positive edge of clock causes clocking, if clock enable is asserted.

UC: H or L or ↓ case (nonclocked operation).

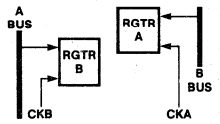
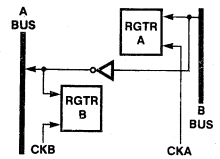
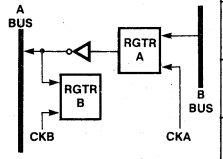
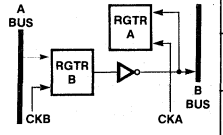
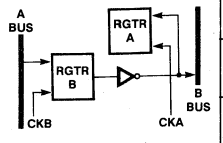
RGTR: Register.

13

Bus Operation for 'ACT646

OPERATION	CONTROL				DATA I/O		BLOCK DIAGRAM	CLOCK ENABLE		'ACT646
	$\overline{E}$	DIR	SRA	SRB	A0-A7	B0-B7		CKA	CKB	
Storage	H	X	X	X	Input	Input		UC	UC	No operation
								UC	↑	Real time A bus data → RGTR B
								↑	UC	Real time B bus data → RGTR A
								↑	↑	Real time A bus data → RGTR B Real time B bus data → RGTR A
Real time B-to-A Operation	L	L	L	X	Output	Input		UC	UC	Real time B bus data → A bus
								UC	↑	Real time B bus data → A bus Real time B bus data → RGTR B
								↑	UC	Real time B bus data → A bus Real time B bus data → RGTR A
								↑	↑	Real time B bus data → A bus Real time B bus data → RGTR A Real time B bus data → RGTR B
Stored data B-to-A Operation	L	L	H	X	Output	Input		UC	UC	RGTR A data → A bus
								UC	↑	RGTR A data → A bus RGTR A data → RGTR B
								↑	UC	Real time B bus data → RGTR A RGTR A data → A bus
								↑	↑	Real time B bus data → RGTR A RGTR A data → A bus RGTR A data → RGTR B
Real time A-to-B Operation	L	H	X	L	Input	Output		UC	UC	Real time A bus data → B bus
								UC	↑	Real time A bus data → B bus Real time A bus data → RGTR B
								↑	UC	Real time A bus data → B bus Real time A bus data → RGTR A
								↑	↑	Real time A bus data → B bus Real time A bus data → RGTR A Real time A bus data → RGTR B
Stored data A-to-B Operation	L	H	X	H	Input	Output		UC	UC	RGTR B data → B bus
								UC	↑	Real time A bus data → RGTR B RGTR B data → B bus
								↑	UC	RGTR B data → B bus RGTR B data → RGTR A
								↑	↑	Real time A bus data → RGTR B RGTR B data → B bus RGTR B data → RGTR A

Bus Operation for 'ACT648

OPERATION	CONTROL				DATA I/O		BLOCK DIAGRAM	CLOCK ENABLE		'ACT648
	$\overline{E}$	DIR	SRA	SRB	A0-A7	B0-B7		CKA	CKB	
Storage	H	X	X	X	Input	Input		UC	UC	No operation
								UC	↑	Real time A bus data → RGTR B
								↑	UC	Real time B bus data → RGTR A
								↑	↑	Real time A bus data → RGTR B Real time B bus data → RGTR A
Real time B-to-A Operation	L	L	L	X	Output	Input		UC	UC	Real time $\overline{B}$ bus data → A bus
								UC	↑	Real time $\overline{B}$ bus data → A bus Real time $\overline{B}$ bus data → RGTR B
								↑	UC	Real time $\overline{B}$ bus data → A bus Real time B bus data → RGTR A
								↑	↑	Real time $\overline{B}$ bus data → A bus Real time $\overline{B}$ bus data → RGTR A Real time $\overline{B}$ bus data → RGTR B
Stored data B-to-A Operation	L	L	H	X	Output	Input		UC	UC	RGTR $\overline{A}$ data → A bus
								UC	↑	RGTR $\overline{A}$ data → A bus RGTR $\overline{A}$ data → RGTR B
								↑	UC	Real time B bus data → RGTR A RGTR $\overline{A}$ data → A bus
								↑	↑	Real time B bus data → RGTR A RGTR $\overline{A}$ data → A bus RGTR $\overline{A}$ data → RGTR B
Real time A-to-B Operation	L	H	X	L	Input	Output		UC	UC	Real time $\overline{A}$ bus data → B bus
								UC	↑	Real time $\overline{A}$ bus data → B bus Real time A bus data → RGTR B
								↑	UC	Real time $\overline{A}$ bus data → B bus Real time $\overline{A}$ bus data → RGTR A
								↑	↑	Real time $\overline{A}$ bus data → B bus Real time $\overline{A}$ bus data → RGTR A Real time A bus data → RGTR B
Stored data A-to-B Operation	L	H	X	H	Input	Output		UC	UC	RGTR $\overline{B}$ data → B bus
								UC	↑	Real time A bus data → RGTR B RGTR $\overline{B}$ data → B bus
								↑	UC	RGTR $\overline{B}$ data → B bus RGTR $\overline{B}$ data → RGTR A
								↑	↑	Real time A bus data → RGTR B RGTR $\overline{B}$ data → B bus RGTR $\overline{B}$ data → RGTR A

Absolute Maximum Ratings

Supply voltage, V_{CC} ..... −0.5 V to 7.0 V
DC input voltage, V_I ..... −0.5 V to V_{CC} +0.5 V
DC output voltage, V_O ..... −0.5 V to V_{CC}+0.5 V
DC output source/sink current per output pin, I_O ..... ±35 mA
DC V_{CC} or ground current, I_{CC} or I_{GND} ..... ±100 mA
Input diode current, I_{IK}:
V_I <0 ..... −20 mA
V_I >V_{CC} ..... +20 mA
Output diode current, I_{OK}:
V_O <0 ..... −20 mA
V_O >V_{CC} ..... +20 mA
Storage temperature ..... −65 to +150°C

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
T_A	Operating free-air temperature		−40		85	°C
t_w	Width of clock	High	20			ns
		Low	20			
t_{su}	Set up time		25↑			ns
t_h	Hold time		0↑			ns
t_r	Input rise time at V_I = 4.5 V		0		500	ns
t_f	Input fall time at V_I = 4.5 V		0		500	ns
I_{OH}	High-level output current				−6	mA
I_{OL}	Low-level output current				12	mA

↑ The arrow indicates the Low-to-High transition of the clock input used as reference.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		25°C MIN	25°C TYP	25°C MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IH}	High-level input voltage			2			2			V
I_{IN}	Input current	V_{CC} = MAX	V_I = V_{CC} or GND			±1.0			±1.0	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 20 μA			0.1			0.1	V
			I_O = 6 mA			0.32			0.37	
			I_{OL} = 12 mA			0.4			0.4	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -20 μA	3.4			3.4			V
			I_{OH} = -6 mA	2.4			2.4			
I_{OZ}	Off-state output current	V_{CC} = MAX	V_O = V_{CC} or GND			±10			±30	μA
I_{CC}*	Quiescent supply current	V_{CC} = MAX	V_I = V_{CC} or GND			10			40	μA

* See I_{CC} vs. Frequency chart.

Switching Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveform)	COMMERCIAL T_A = 25°C MIN	COMMERCIAL T_A = 25°C MAX	COMMERCIAL MIN	COMMERCIAL MAX	UNIT
t_{PLH}	Data to output delay	C_L = 50 pF		38		45	ns
t_{PHL}				38		45	
t_{PLH}	Clock to output delay			32		38	ns
t_{PHL}				32		38	
t_{PLH}	Select to output delay* (data input high)			32		35	ns
t_{PHL}				32		35	
t_{PLH}	Select to output delay* (data input low)			32		35	ns
t_{PHL}				32		35	
t_{PZL}	Output enable delay	R_L = 1KΩ, C_L = 50 pF		40		45	ns
t_{PZH}				40		45	
t_{PLZ}	Output disable delay			35		40	ns
t_{PHZ}				35		40	
t_{PZL}	Direction enable delay			40		45	ns
t_{PZH}				35		40	
t_{PLZ}	Direction disable delay			30		35	ns
t_{PHZ}				30		35	

* See Figure 4.

13

Test Waveforms

Setup Time/Hold Time

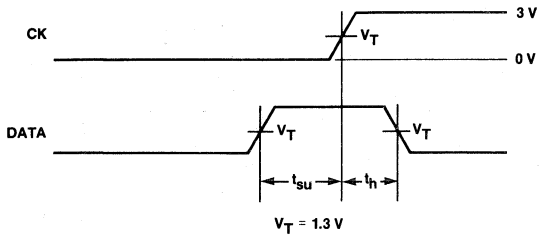


Figure 1.

Bus Data To Bus Output Delay

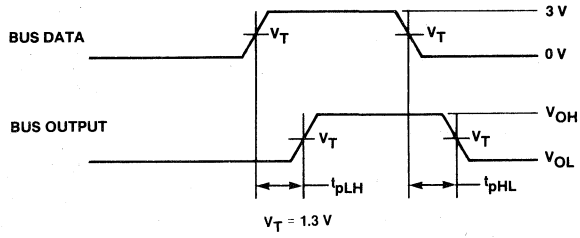


Figure 2.

CK To Bus Output Propagation Delay Time

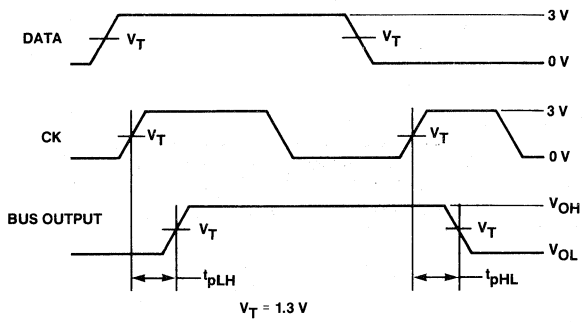
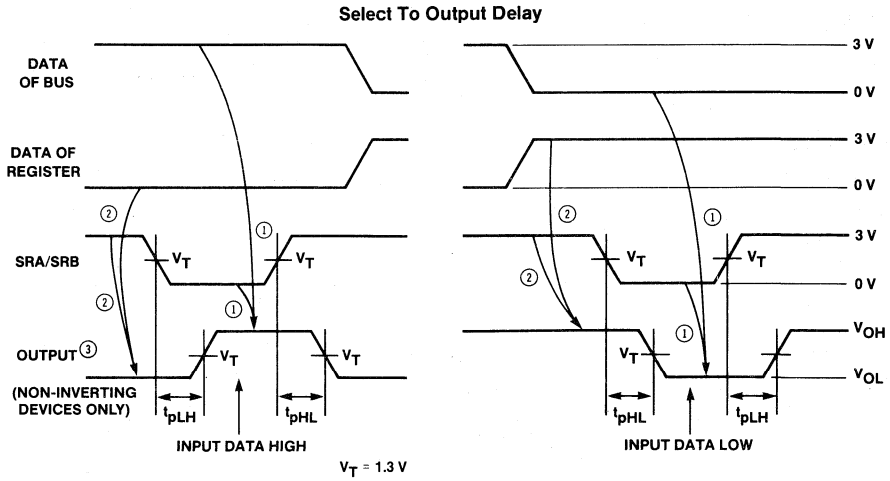


Figure 3.

Select To Output Delay



NOTES: 1. When SRA/SRB is low, the input data will transfer to output bus.
2. When SRA/SRB is high, the data of register will transfer to output bus.
3. For the inverting devices, the timing is similar, but the output is opposite to that for the non-inverting devices.

Figure 4.

Enable/Disable/Direction-Change Delay

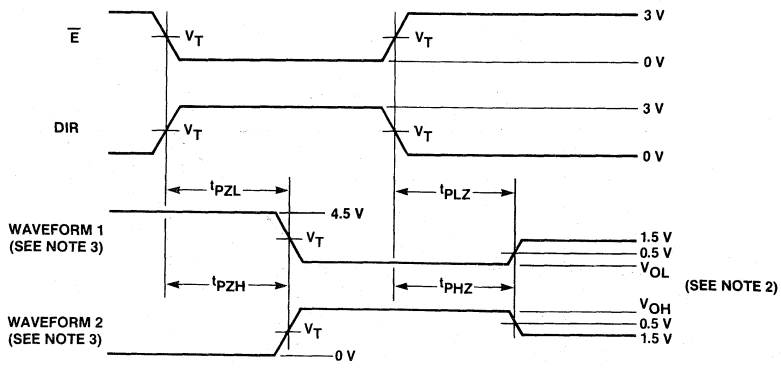


Figure 5.

Test Load

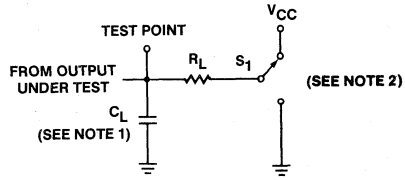


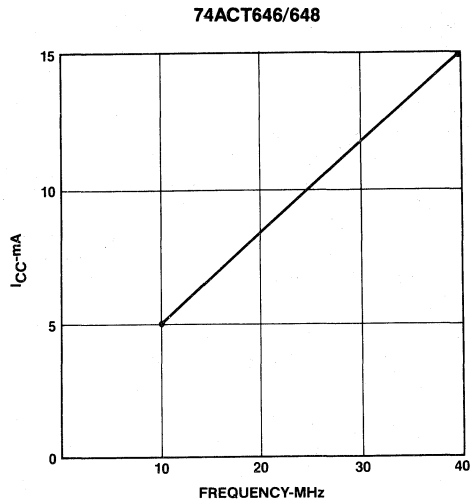
Figure 6.

NOTES 1. C_L includes probe and jig capacitance.

2. When measuring t_{PLZ} and t_{PZL}, S_1 is tied to V_{CC}. When measuring t_{PHZ} and t_{PZH}, S_1 is tied to ground.
   When measuring propagation delay times of three-state outputs, S_1 is open, i.e., not connected to V_{CC} or ground.
3. Waveform 1 is for an output with internal conditions such that the output is Low except when disabled by the output control.
   Waveform 2 is for an output with internal conditions such that the output is High except when disabled by the output control.
4. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
5. All input pulses are supplied by generators having the following characteristics: PRR ≤1 MHz, t_r ≤6 ns, t_f ≤6 ns, Z_{out} = 50 Ω.

13

Typical ICC vs. Frequency



8-Bit Bus Front-Loading Latch Transceivers — Advanced CMOS-TTL Compatible

74ACT651 74ACT652

Features/Benefits

- **Bidirectional bus transceiver and register**
- **Independent registers for A and B buses**
- **Real-time data transfer or stored data transfer**
- **Simultaneous outputs on both buses**
- **24-pin SKINNYDIP® saves space**
- **Three-state outputs drive bus lines**
- **Low quiescent supply current of <10 μA (typical)**
- **Active supply current at about 20% LS equivalent**
- **Wide commercial operating supply and temperature ranges 4.5 V to 5.5 V; -40°C to +85°C**

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	OUTPUT	TECH
74ACT651	NS,JS	Com	Noninvert	Three-state	CMOS
74ACT652	NS,JS	Com	Invert		

Description

This 8-bit bus transceiver with three-state outputs has sixteen D-type flip-flops and multiplexers. The bus-oriented pinout of the part is shown in the Pin Configuration. The internal gate-level hardware configurations for the 'ACT651/652 are given in the Logic Diagrams. The basic repeated element, consisting of an edge-triggered flip-flop paralleled with a bypassing path, or "feed-through", into a two-way multiplexer is sometimes called a "front-loading latch."

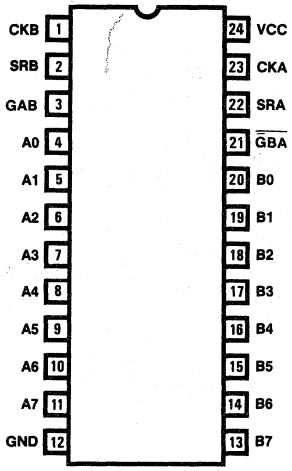
A pair of multiplexers are used to distribute two bytes of data through the part. The data-routing combinations offered by the multiplexers provide flexibility in directing data to or from either bus, and/or either register. Data is loaded into registers A or B upon the rising edge of the appropriate clock signals. CKA clocks register A, which receives data from the B bus directly at its inputs. Similarly, CKB clocks register B, which has the A bus available directly at its inputs. Control of the multiplexers is provided by two select lines (one per register), SRA and SRB. Command of the outputs is performed by two enable lines, GAB and $\overline{GBA}$.

When GAB is low and $\overline{GBA}$ is high, data from the buses can be loaded into registers A and B. When $\overline{GBA}$ is low, the A bus is configured for output. When GAB is high, the B bus is configured for output. The A and B buses can be enabled at the same time, to operate as outputs simultaneously.

SRA is used to select between register A and the B bus, and then to route the data to a controlled buffer connected to the A bus. Likewise, SRB selects between register B and the A bus, and then routes the data to the B bus through a controlled buffer.

Pin Configurations

'ACT651/652
8-Bit Bus Front-Loading Latch Transceiver



13

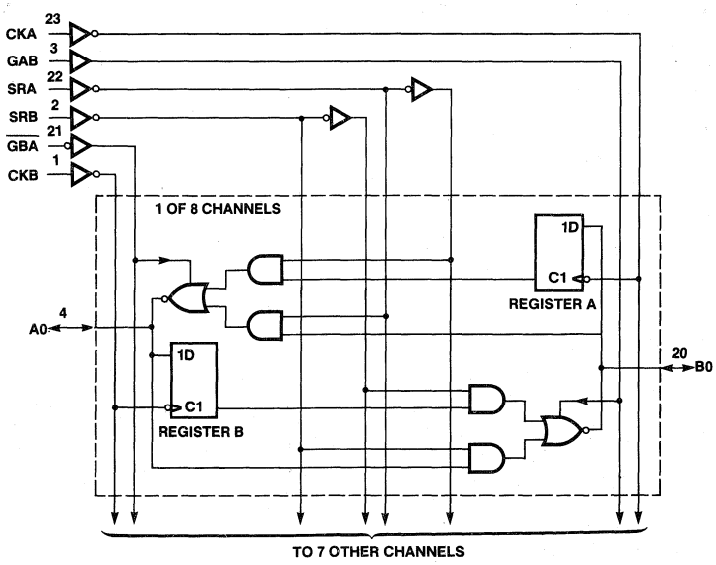
SKINNYDIP® is a registered trademark of Monolithic Memories.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

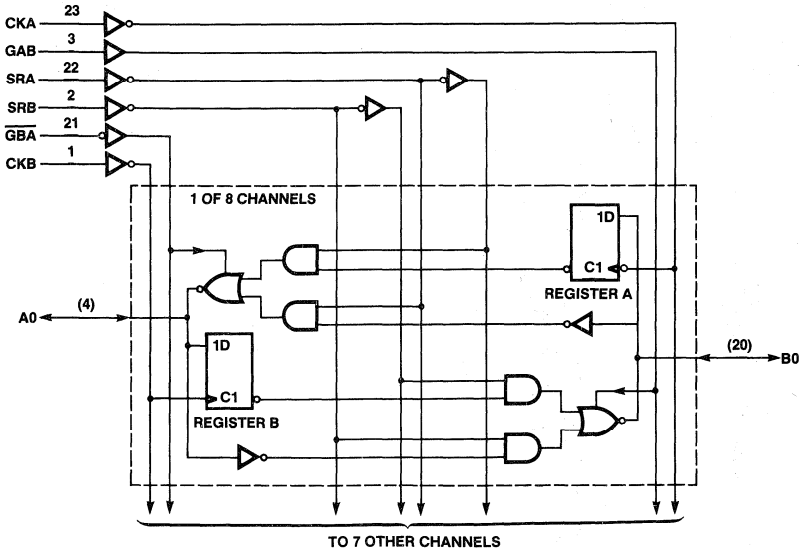
Monolithic Memories MMI

Logic Diagrams

'ACT651 (Inverting)

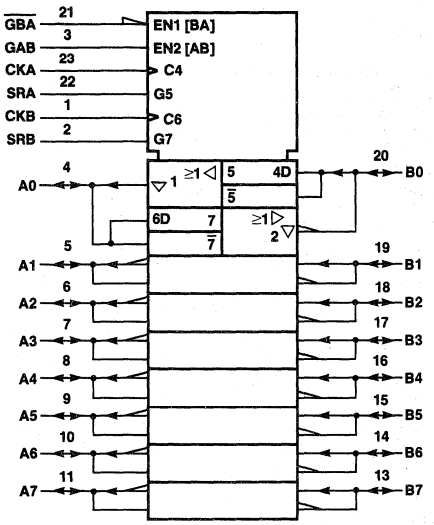


'ACT652 (Non-Inverting)

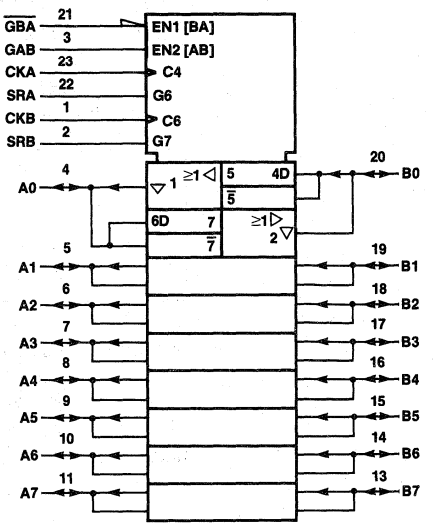


IEEE Symbols

'ACT651

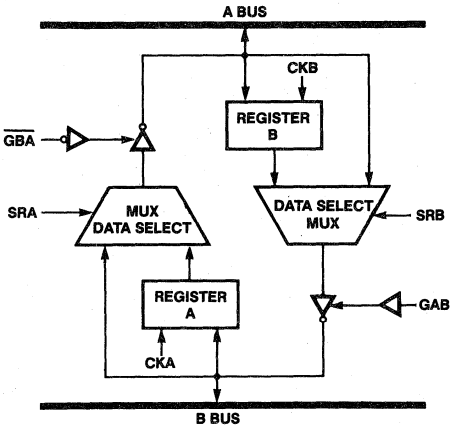


'ACT652

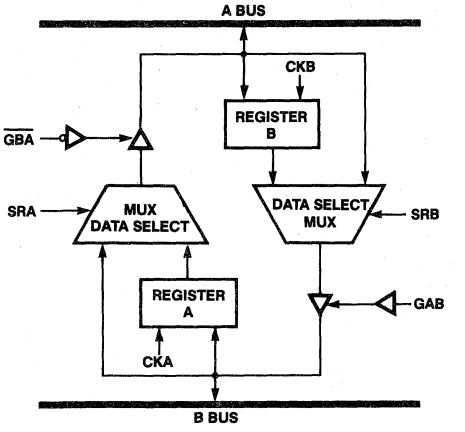


Block Diagrams

'ACT651 (Inverting)



'ACT652 (Non-inverting)



13

Function Table
Nomenclature Description

GAB: To enable A-to-B operation.

$\overline{GBA}$: To enable B-to-A operation.

GAB	$\overline{GBA}$	OPERATION DIRECTION
L	L	B-to-A
L	H	A and B buses both are inputs (Storage)
H	L	A and B buses both are outputs (Transfer stored data to bus)
H	H	A-to-B

SRA/SRB: To select the output data coming from the A/B register if SRA/SRB is a High level; otherwise, directly from the input data bus.

A0-A7: Eight input/output pins on the A side.

B0-B7: Eight input/output pins on the B side.

CKA/CKB: Clock for register A/B.

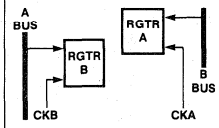
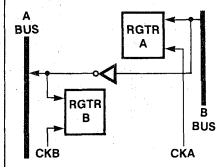
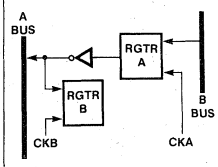
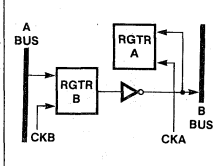
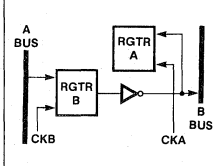
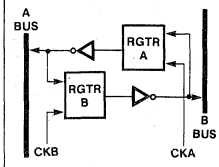
X: H or L state irrelevant ("Don't Care" condition).

↑: Positive edge of CK causes clocking, if clock enable is asserted.

UC: H or L or ↓ case (nonclocked operation).

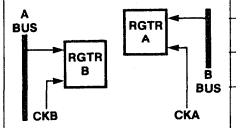
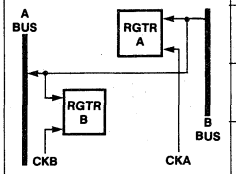
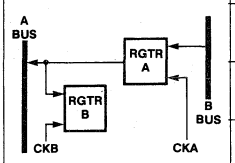
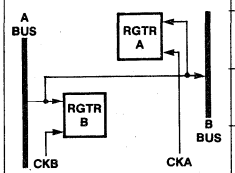
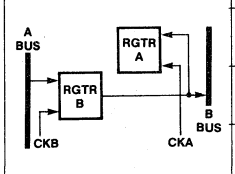
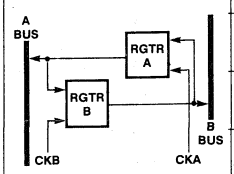
RGTR: Register.

Bus Operation for 'ACT651

OPERATION	CONTROL				DATA I/O		BLOCK DIAGRAM	CLOCK ENABLE		'ACT651
	GAB	$\overline{GBA}$	SRA	SRB	A0-A7	B0-B7		CKA	CKB	
Storage	L	H	X	X	Input	Input		UC	UC	No operation
								UC	↑	Real time A bus data → RGTR B
								↑	UC	Real time B bus data → RGTR A
								↑	↑	Real time A bus data → RGTR B Real time B bus data → RGTR A
Real time B-to-A Operation	L	L	L	X	Output	Input		UC	UC	Real time $\overline{B}$ bus data → A bus
								UC	↑	Real time $\overline{B}$ bus data → A bus Real time $\overline{B}$ bus data → RGTR B
								↑	UC	Real time $\overline{B}$ bus data → A bus Real time B bus data → RGTR A
								↑	↑	Real time $\overline{B}$ bus data → A bus Real time B bus data → RGTR A Real time $\overline{B}$ bus data → RGTR B
Stored data B-to-A Operation	L	L	H	X	Output	Input		UC	UC	RGTR $\overline{A}$ data → A bus
								UC	↑	RGTR $\overline{A}$ data → A bus RGTR $\overline{A}$ data → RGTR B
								↑	UC	Real time B bus data → RGTR A RGTR $\overline{A}$ data → A bus
								↑	↑	Real time B bus data → RGTR A RGTR $\overline{A}$ data → A bus RGTR $\overline{A}$ data → RGTR B
Real time A-to-B Operation	H	H	X	L	Input	Output		UC	UC	Real time $\overline{A}$ bus data → B bus
								UC	↑	Real time $\overline{A}$ bus data → B bus Real time A bus data → RGTR B
								↑	UC	Real time $\overline{A}$ bus data → B bus Real time $\overline{A}$ bus data → RGTR A
								↑	↑	Real time $\overline{A}$ bus data → B bus Real time $\overline{A}$ bus data → RGTR A Real time A bus data → RGTR B
Stored data A-to-B Operation	H	H	X	H	Input	Output		UC	UC	RGTR $\overline{B}$ data → B bus
								UC	↑	Real time A bus data → RGTR B RGTR $\overline{B}$ data → B bus
								↑	UC	RGTR $\overline{B}$ data → B bus RGTR $\overline{B}$ data → RGTR A
								↑	↑	Real time A bus data → RGTR B RGTR $\overline{B}$ data → B bus RGTR $\overline{B}$ data → RGTR A
Transfer Stored Data	H	L	H	H	Output	Output		UC	UC	RGTR $\overline{A}$/$\overline{B}$ data → A/B bus
								UC	↑	RGTR $\overline{A}$/$\overline{B}$ data → A/B bus RGTR $\overline{A}$ data → RGTR B
								↑	UC	RGTR $\overline{A}$/$\overline{B}$ data → A/B bus RGTR $\overline{B}$ data → RGTR A
								↑	↑	RGTR $\overline{A}$/$\overline{B}$ data → A/B bus RGTR $\overline{A}$ data → RGTR B RGTR $\overline{B}$ data → RGTR A

13

Bus Operation for 'ACT652

OPERATION	CONTROL				DATA I/O		BLOCK DIAGRAM	CLOCK ENABLE		'ACT652
	GAB	$\overline{GBA}$	SRA	SRB	A0-A7	B0-B7		CKA	CKB	
Storage	L	H	X	X	Input	Input		UC	UC	No operation
								UC	↑	Real time A bus data → RGTR B
								↑	UC	Real time B bus data → RGTR A
								↑	↑	Real time A bus data → RGTR B Real time B bus data → RGTR A
Real time B-to-A Operation	L	L	L	X	Output	Input		UC	UC	Real time B bus data → A bus
								UC	↑	Real time B bus data → A bus Real time B bus data → RGTR B
								↑	UC	Real time B bus data → A bus Real time B bus data → RGTR A
								↑	↑	Real time B bus data → A bus Real time B bus data → RGTR A Real time B bus data → RGTR B
Stored data B-to-A Operation	L	L	H	X	Output	Input		UC	UC	RGTR A data → A bus
								UC	↑	RGTR A data → A bus RGTR A data → RGTR B
								↑	UC	Real time B bus data → RGTR A RGTR A data → A bus
								↑	↑	Real time B bus data → RGTR A RGTR A data → A bus RGTR A data → RGTR B
Real time A-to-B Operation	H	H	X	L	Input	Output		UC	UC	Real time A bus data → B bus
								UC	↑	Real time A bus data → B bus Real time A bus data → RGTR B
								↑	UC	Real time A bus data → B bus Real time A bus data → RGTR A
								↑	↑	Real time A bus data → B bus Real time A bus data → RGTR A Real time A bus data → RGTR B
Stored data A-to-B Operation	H	H	X	H	Input	Output		UC	UC	RGTR B data → B bus
								UC	↑	Real time A bus data → RGTR B RGTR B data → B bus
								↑	UC	RGTR B data → B bus RGTR B data → RGTR A
								↑	↑	Real time A bus data → RGTR B RGTR B data → B bus RGTR B data → RGTR A
Transfer Stored Data	H	L	H	H	Output	Output		UC	UC	RGTR A/B data → A/B bus
								UC	↑	RGTR A/B data → A/B bus RGTR A data → RGTR B
								↑	UC	RGTR A/B data → A/B bus RGTR B data → RGTR A
								↑	↑	RGTR A/B data → A/B bus RGTR A data → RGTR B RGTR B data → RGTR A

Absolute Maximum Ratings

Supply voltage, V_{CC} ..... −0.5 V to 7.0 V
DC input voltage, V_I ..... −0.5 V to V_{CC} +0.5 V
DC output voltage, V_O ..... −0.5 V to V_{CC}+0.5 V
DC output source/sink current per output pin, I_O ..... ±35 mA
DC V_{CC} or ground current, I_{CC} or I_{GND} ..... ±100 mA
Input diode current, I_{IK}:
V_I <0 ..... −20 mA
V_I >V_{CC} ..... +20 mA
Output diode current, I_{OK}:
V_O <0 ..... −20 mA
V_O >V_{CC} ..... +20 mA
Storage temperature ..... −65 to +150°C

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
T_A	Operating free-air temperature		−40		85	°C
t_w	Width of clock	High	20			ns
		Low	20			
t_{su}	Set up time		25↑			ns
t_h	Hold time		0↑			ns
t_r	Input rise time at V_I = 4.5 V		0		500	ns
t_f	Input fall time at V_I = 4.5 V		0		500	ns
I_{OH}	High-level output current				−6	mA
I_{OL}	Low-level output current				12	mA

↑ The arrow indicates the Low-to-High transition of the clock input used as reference.

13

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		25°C MIN TYP MAX	COMMERCIAL MIN TYP MAX	UNIT
V_{IL}	Low-level input voltage			0.8	0.8	V
V_{IH}	High-level input voltage			2	2	V
I_{IN}	Input current	V_{CC} = MAX	V_I = V_{CC} or GND	±1.0	±1.0	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 20 μA	0.1	0.1	V
			I_O = 6 mA	0.32	0.37	
			I_{OL} = 12 mA	0.4	0.4	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -20 μA	3.4	3.4	V
			I_{OH} = -6 mA	2.4	2.4	
I_{OZ}	Off-state output current	V_{CC} = MAX	V_O = V_{CC} or GND	±10	±30	μA
I_{CC}*	Quiescent supply current	V_{CC} = MAX	V_I = V_{CC} or GND	10	40	μA

* See I_{CC} vs. Frequency chart.

Switching Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveform)	COMMERCIAL T_A = 25°C MIN	MAX	COMMERCIAL MIN	MAX	UNIT
t_{PLH}	Data to output delay	C_L = 50 pF		39		48	ns
t_{PHL}				35		42	
t_{PLH}	Clock to output delay			35		44	ns
t_{PHL}				35		40	
t_{PLH}	Select to output delay* (data input high)			32		40	ns
t_{PHL}				32		40	
t_{PLH}	Select to output delay* (data input low)			35		44	ns
t_{PHL}				32		36	
t_{PZL}	$\overline{GBA}$ to A bus output enable delay	R_L = 1KΩ, C_L = 50 pF		28		32	ns
t_{PZH}				28		32	
t_{PLZ}	$\overline{GBA}$ to A bus output disable delay			28		32	ns
t_{PHZ}				35		38	
t_{PZL}	GAB to B bus output enable delay			30		33	ns
t_{PZH}				28		32	
t_{PLZ}	GAB to B bus output disable delay			28		32	ns
t_{PHZ}				35		38	

* See Figure 4.

Test Waveforms

Setup Time/Hold Time

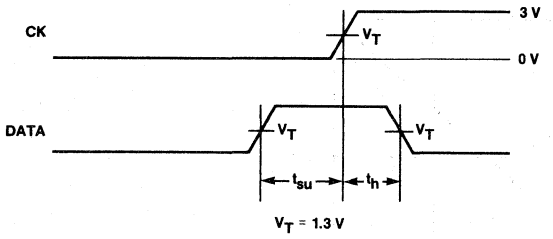


Figure 1

Bus Data To Bus Output Delay

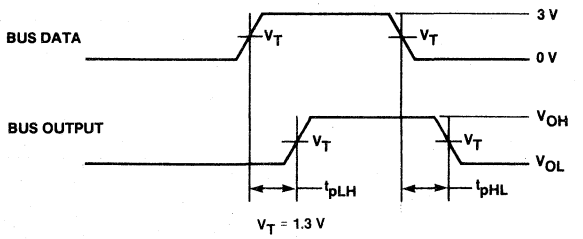


Figure 2

CK To Bus Output Propagation Delay Time

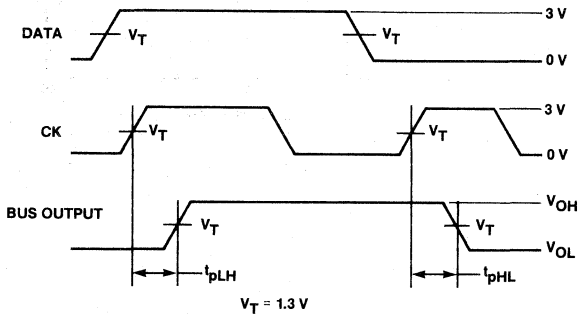
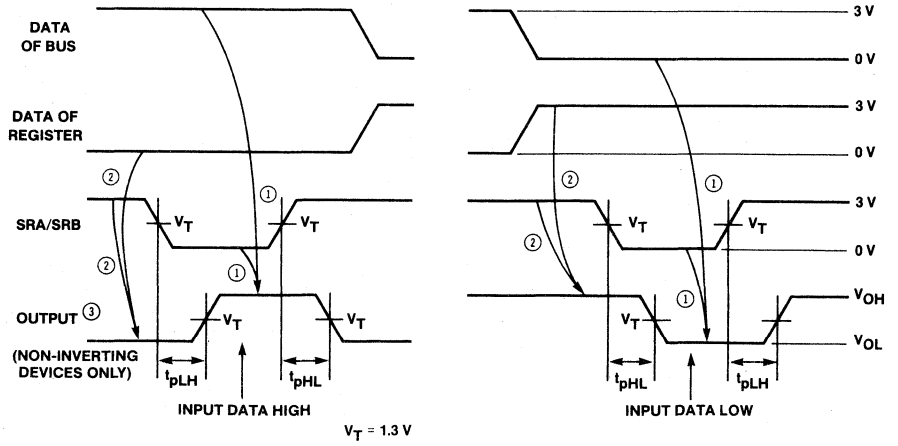


Figure 3

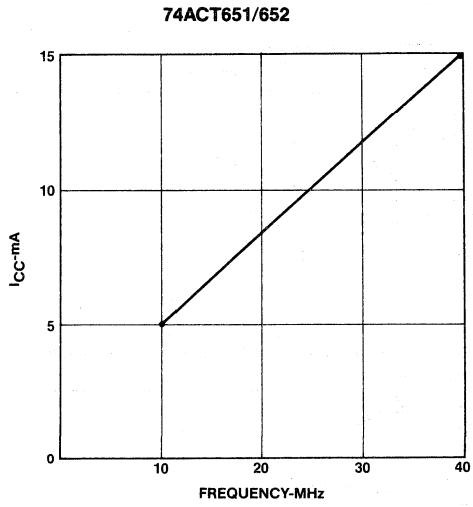
Select To Output Delay



NOTES: 1. When SRA/SRB is low, the input data will transfer to output bus.
2. When SRA/SRB is high, the data of register will transfer to output bus.
3. For the inverting devices, the timing is similar, but the output is opposite to that for the non-inverting devices.

Figure 4

Typical ICC vs. Frequency



Enable/Disable/Direction-Change Delay

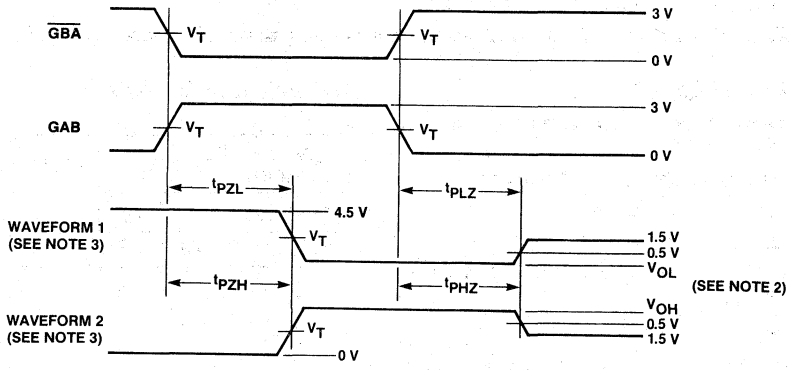


Figure 5

Standard Test Load

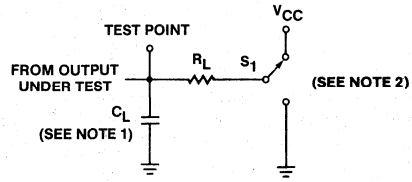


Figure 6

NOTES 1. C_L includes probe and jig capacitance.

2. When measuring t_{PLZ} and t_{PZL}, S_1 is tied to V_{CC}. When measuring t_{PHZ} and t_{PZH}, S_1 is tied to ground.
   When measuring propagation delay times of three-state outputs, S_1 is open, i.e., not connected to V_{CC} or ground.
3. Waveform 1 is for an output with internal conditions such that the output is Low except when disabled by the output control.
   Waveform 2 is for an output with internal conditions such that the output is High except when disabled by the output control.
4. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
5. All input pulses are supplied by generators having the following characteristics: PRR ≤1 MHz, t_r ≤6 ns, t_f ≤6 ns, Z_{out} = 50 Ω.

8-Bit Latches/Registers with Readback-Advanced CMOS-TTL Compatible

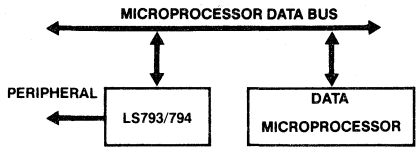
74ACT793 74ACT794

Features/Benefits

- **I/O port configuration enables output data back onto input bus**
- **Low quiescent supply current of < 10 μA (typical)**
- **Eighth bits matches byte boundaries**
- **Ideal for microprocessor interface**
- **Wide commercial operating supply and temperature ranges 4.5 V to 5.5 V; -40°C to + 85°C**

Description

These 8-bit latches/registers are useful for I/O operations on a microprocessor bus. An image of the output data can be read back by the CPU. This operation is important in control algorithms which make decisions based on the previous status of output controls. Rather than storing a redundant copy of the output data in memory, simply reading the register as an I/O port allows the data to be retrieved from where it has been stored in an ACT793/4, for verification and/or updating.



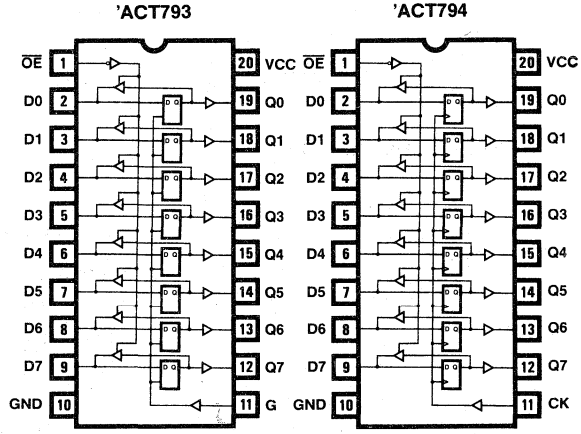
The data is loaded in the registers on the low-to-high transition of the clock (CK), for the ACT794. The data is passed through the ACT793 when the gate, (G), is High, and it is "latched" when G changes to Low. The output enable, $\overline{OE}$ is used to enable data on D7-D0. When $\overline{OE}$ is low the output of the latches/registers is enabled on D0-D7, enabling D as an outut bus so that the host can perform a read operation. When $\overline{OE}$ is High, D7-D0 are inputs to the latches/registers configuring D as an input bus.

The output drive of these commercial parts for any output pin is I_{OL} = 12 mA.

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	TECH
74ACT793	N,J	Com	Non-invert	Latch	CMOS
74ACT794	N,J	Com		Register	

Logic Symbols



'ACT793 Function Table

G	$\overline{OE}$	Q	D
L	L	Q_0**	Output, Q
L	H	Q_0**	Input
H†	L	D*	Output, Q*
H	H	D	Input

* In this case the output of the latch feeds the input, and a "race" condition results.

** Q_0 represents the previous "latched" state.

† This transition is not a normal mode of operation and may produce hazards.

'ACT794 Function Table

CK	$\overline{OE}$	Q	D
L or H or ↓	L	Q_0	Output, Q
L or H or ↓	H	Q_0	Input
↑	L	Q_0	Output, Q*
↑	H	D	Input

* In this case the output of the register is clocked to the inputs and the overall Q output is unchanged at Q_0.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Monolithic Memories

Absolute Maximum Ratings

Supply voltage, V_{CC} ..... −0.5 V to 7.0 V
DC input voltage, V_I ..... −0.5 V to V_{CC} +0.5 V
DC output voltage, V_O ..... −0.5 V to V_{CC} +0.5 V
DC output source/sink current per output pin, I_O ..... ±35 mA
DC V_{CC} or ground current, I_{CC} or I_{GND} ..... ±100 mA
Input diode current, I_{IK}:
V_I <0 ..... −20 mA
V_I >V_{CC} ..... +20 mA
Output diode current, I_{OK}:
V_O <0 ..... −20 mA
V_O >V_{CC} ..... +20 mA
Storage temperature ..... −65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
T_A	Operating free-air temperature		−40		85	°C
t_w	Width of Clock/Gate	High	15			ns
		Low	15			
t_{su}	Setup time	'ACT793	8↓			ns
		'ACT794	25↑			
t_h	Hold time	'ACT793	8↓			
		'ACT794	0↑			
t_r	Input rise time at V_I = 4.5 V		0		500	ns
t_f	Input fall time at V_I = 4.5 V		0		500	ns
I_{OH}	High-level output current				−6	mA
I_{OL}	Low-level output current				12	mA

↑ ↓ The arrows indicates the transition of the clock/gate input used for reference. ↑ for the low-to-high transitions, ↓ for the high-to-low transitions.

13

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
I_{IN}	Input current	V_{CC} = MAX	V_I = V_{CC} or GND			±1.0	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 20 μA			0.1	V
			I_{OL} = 6 mA			0.37	
			I_{OL} = 12 mA			0.4	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −20 μA	3.4			V
			I_{OH} = −6 mA	2.4			
I_{OZ}	Off-state output current	V_{CC} = MAX	V_O = V_{CC} or GND			±30	μA
I_{CC}	Quiescent supply current	V_{CC} = MAX	V_I = V_{CC} or GND			80	μA

Switching Characteristics for 'ACT793

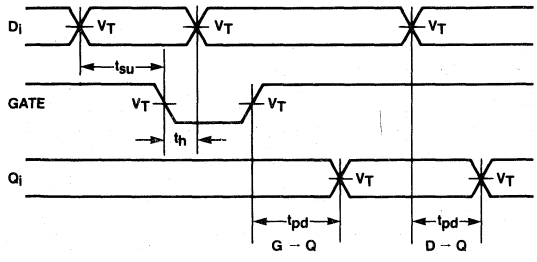
SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveform)	COMMERCIAL MIN	COMMERCIAL MAX	UNIT
t_{PLH}	Data to output delay	C_L = 50 pF		40	ns
t_{PHL}				40	
t_{PLH}	Gate to output delay			40	ns
t_{PHL}				40	
t_{PZL}	Output enable delay†	R_L = 1 K Ω C_L = 50 pF		30	ns
t_{PZH}				30	
t_{PLZ}	Output disable delay†			33	ns
t_{PHZ}				33	

† For the 'ACT793, G should remain LOW during these tests.

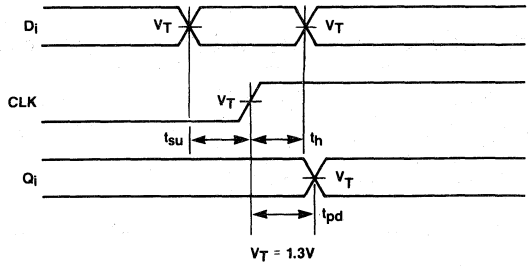
Switching Characteristics for 'ACT794

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveform)	COMMERCIAL MIN	COMMERCIAL MAX	UNIT
t_{PLH}	Clock to output delay	C_L = 50 pF		40	ns
t_{PHL}				40	
t_{PZL}	Output enable delay	R_L = 1 K Ω C_L = 50 pF		30	ns
t_{PZH}				30	
t_{PLZ}	Output disable delay			30	ns
t_{PHZ}				30	

'ACT793 Timing Diagrams

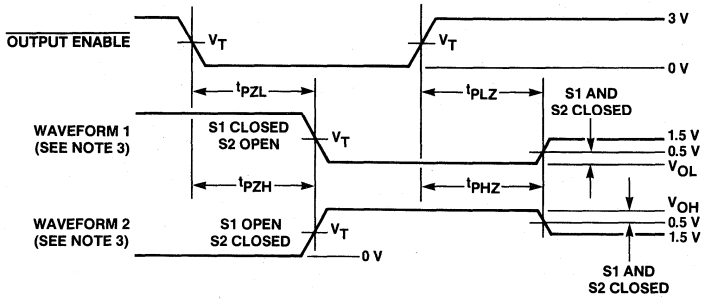


'ACT794 Timing Diagrams

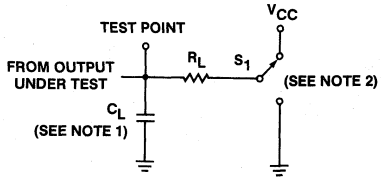


The case when gate is HIGH and data flows through the part is specified as Data to Output delay in the Switching Characteristics table. (V_T = 1.3V).

Enable/Disable Waveforms



Standard Test Load



Notes 1. C_L includes probbe and jig capacitance.

2. When measuring t_{PLZ} and t_{PZL}, S_1 is tied to V_{CC}. When measuring t_{PHZ} and t_{PZH}, S_1 is tied to ground.

   When measuring propagation delay times of three-state outputs, S_1 is open, i.e., not connected to V_{CC} or ground.

3. Waveform 1 is for an output with internal conditions such that the output is Low except when disabled by the output control.

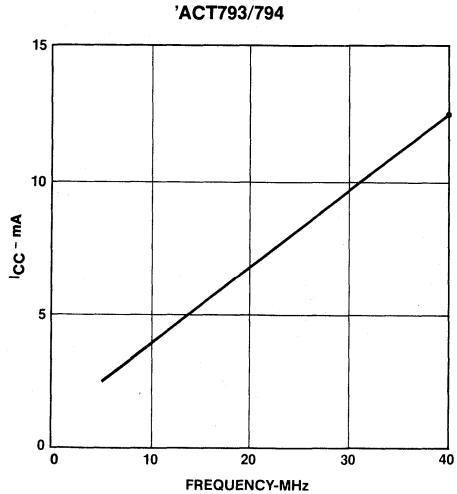
   Waveform 2 is for an output with internal conditions such that the output is High except when disabled by the output control.

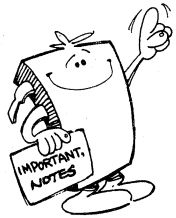
4. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

5. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, t_r ≤ 5 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.

13

Typical I_{CC} vs Frequency




IMPORTANT
NOTES

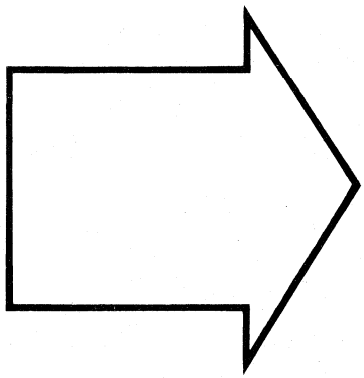


Table of Contents

ECL10KH

ECL10KH Selection Guide

DEVICE	FUNCTION	PACKAGE	PINS
	NOR Gate		
MC10H102	Quad 2-Input		
MC10H211	Dual 3-Input, 3-Output		
	OR Gate		
MC10H103	Quad 2-Input		
MC10H210	Dual 3-Input, 3-Output		
	AND Gates		
MC10H104	Quad AND		
	Complex Gates		
MC10H101	Quad OR/NOR		
MC10H105	Triple 2-3-2 Input OR/NOR		
MC10H107	Triple Exclusive OR/NOR		
MC10H109	Dual 4-5 Input OR/NOR		
MC10H117	Dual 2-Wide OR-AND/OR-AND Invert		
MC10H118	Dual 2-Wide 3-Input OR/AND		
MC10H121	4-Wide OR-AND/OR-AND Invert		
	Translators		
MC10H124	Quad TTL/ECL		
MC10H125	Quad ECL/TTL		
	Receivers		
MC10H115	Quad Line Receiver		
MC10H116	Triple Line Receiver		
	Flip-FLop Latches	J, N	16
MC10H130	Dual latch		
MC10H131	Dual D Master Slave Flip-FLop		
MC10H175	Quint Latch		
MC10H176	Hex D-Flip-Flop		
	Parity Checker		
MC10H160	12-Bit Parity Generator-Checker		
	Encoders/Decodes		
MC10H161	Binary to 1-8 (Low)		
MC10H162	Binary to 1-8 (High)		
	Data Selector Multiplexer		
MC10H158	Quad 2-Input Multiplexers (Non-inverting)		
MC10H159	Quad 2-Input Multiplexers (Inverting)		
MC10H164	8-Line Multiplexer		
MC10H173	Quad 2-Input Multiplexer Latch		
MC10H174	Dual 4-1 multiplexer		
	Counters		
MC10H016	Binary Counter		
MC10H136	Universal Hexadecimal		
	Arithmetic Functions		
MC10H179	Lookahead Carry Block		
	Special Functions		
MC10H141	Universal Shift Register		
MC10H166	5-Bit Magnitude Comparator		

ECL 10KH High-Speed Emitter-Coupled Logic Family
MC10H016
4-Bit Binary Counter

Features/Benefits

- Counting frequency, 200 MHz min.
- Power dissipation 570 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Description

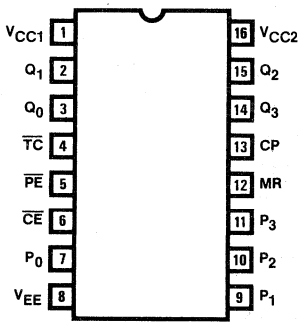
The MC10H016 is a high-speed synchronous, presettable, cascadable 4-bit Binary Counter. This device is a member of Monolithic Memories' new ECL 10KH family. It is useful for a large number of conversion, counting, and digital integration applications.

Ordering Information

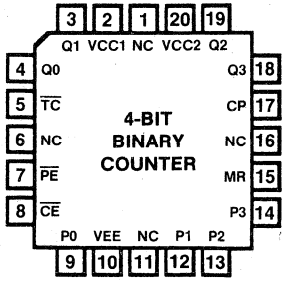
PART NUMBER	PACKAGE	TEMPERATURE
MC10H016	J, N, NL	Com

Pin Configuration

MC10H016
4-bit Binary Counter



MC10H016



Function Select Table

$\overline{CE}$	$\overline{PE}$	MR	CP	FUNCTION
L	L	L	Z	Load parallel (P_n to Q_n)
H	L	L	Z	Load parallel (P_n to Q_n)
L	H	L	Z	Count
H	H	L	Z	Hold
X	X	L	ZZ	Masters respond; slaves hold
X	X	H	X	Reset (Q_n = LOW, T_C = HIGH)

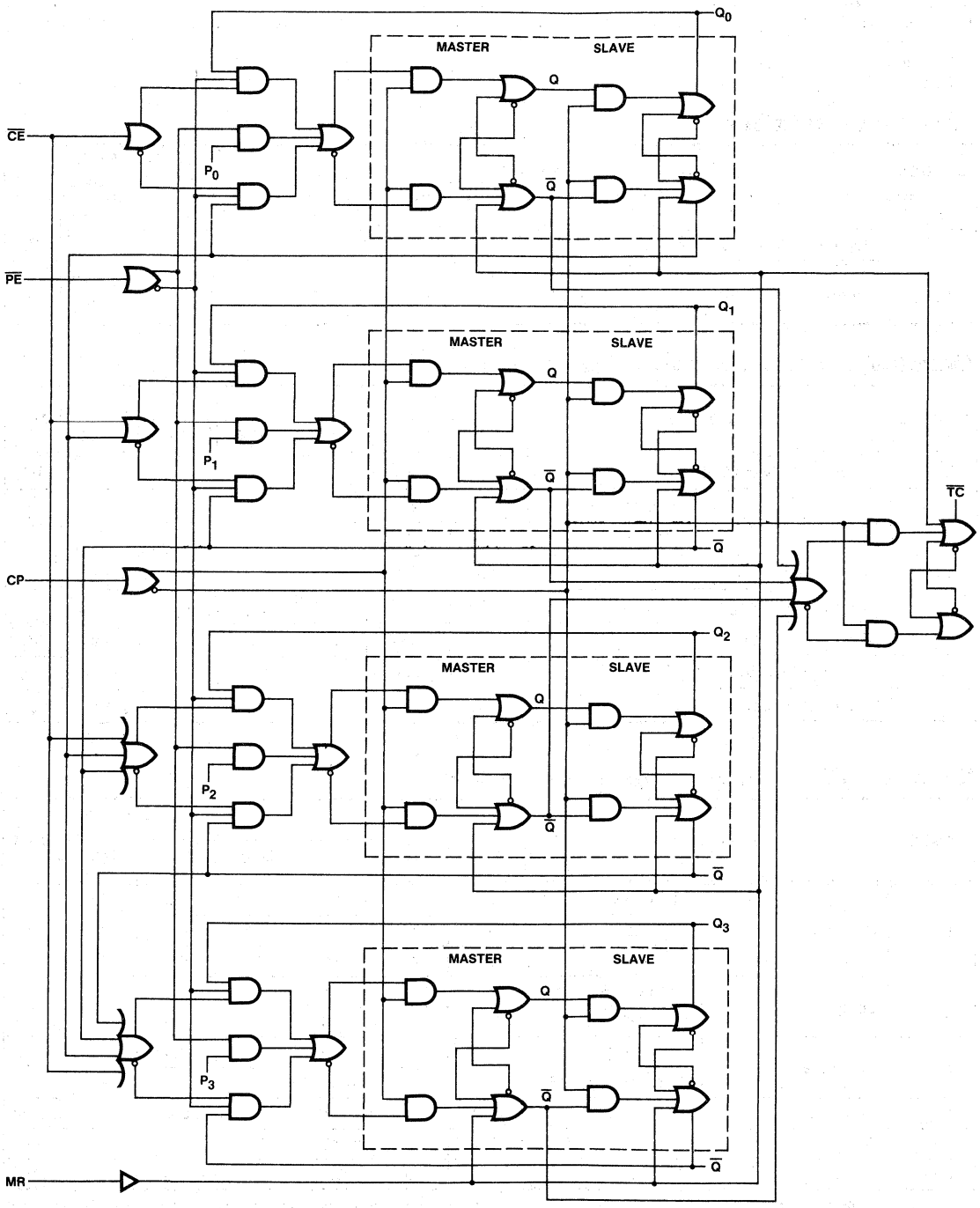
Z = Clock Pulse (Low to High)
ZZ = Clock Pulse (High to Low).

Features include assertion inputs and outputs on each of the four master/slave counting flip-flops. Terminal count is generated internally in a manner that allows synchronous loading at nearly the speed of the basic counter.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories

Logic Diagram

4-bit Binary Counter



Note: This diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

14

Absolute Maximum Ratings

Supply voltage V_{EE} (V_{CC} = 0) ..... -8.0 V to 0 Vdc
Input voltage V_I (V_{CC} = 0) ..... 0 Vdc to V_{EE}
Output Current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		-5.46	-5.2	-4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage Temperature Range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Power supply current		—	126	—	115	—	126	mA
I_{inH}	Input current HIGH	All except MR	—	450	—	265	—	265	µA
		Pin 12 MR	—	1190	—	700	—	700	
I_{inL}	Input current LOW		0.5	—	0.5	—	0.3	—	µA
V_{OH}	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	Low input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = 5.2 V, ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
t_{pd}	Propagation delay	Clock to Q	1.0	2.4	1.0	2.5	1.0	2.7	ns
		Clock to TC	0.7	2.4	0.7	2.5	0.7	2.6	
		MR to Q	0.7	2.4	0.7	2.5	0.7	2.6	
t_{set}	Setup time	Pn to Clock	2.0	—	2.0	—	2.0	—	ns
		CE or PE to Clock	2.5	—	2.5	—	2.5	—	
t_{hold}	Hold time	Clock to Pn	1.0	—	1.0	—	1.0	—	ns
		Clock to CE or PE	0.5	—	0.5	—	0.5	—	
f_{count}	Counting frequency		200	—	200	—	200	—	MHz
t_r,t+	Rise time		0.5	2.0	0.5	2.1	0.5	2.2	ns
t_f,t-	Fall time		0.5	2.0	0.5	2.1	0.5	2.2	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

ECL 10KH High Speed Emitter Coupled Logic Family
MC10H100
Quad 2-Input NOR Gate with Strobe

Features/Benefits

- Propagation delay, 1 ns typical
- 25 mW typical/gate (no load)
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Ordering Information

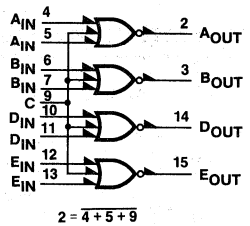
PART NUMBER	PACKAGE	TEMPERATURE
MC10H100	J, N, NL	Com

Description

The M10H100 is a member of Monolithic Memories' ECL 10KH family. This ECL device is a Quad 2-Input NOR Gate with Strobe. This device is a functional/pinout duplication of the standard ECL 10K family part, with 100% improvement in propagation delay and no increase in power supply current.

Logic Diagram

MC10H100

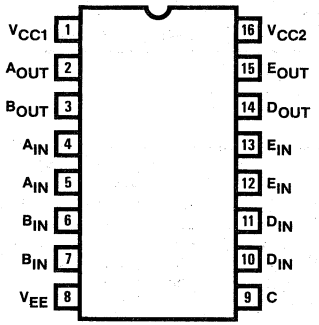


$2 = \overline{4 + 5 + 9}$

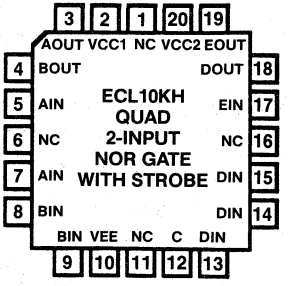
VCC1 = PIN 1
VCC2 = PIN 16
VEE = PIN 8

Pin Configuration

MC10H100
Quad 2-Input NOR Gate with Strobe



MC10H100



14

Portions of this data sheet reproduced with the courtesy of Motorola Inc.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Monolithic Memories

Absolute Maximum Ratings

Supply voltage V_{EE} (V_{CC} = 0) ..... -8.0 V to 0 V_{dc}
Input voltage V_I (V_{CC} = 0) ..... 0 V_{dc} to V_{EE}
Output current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		-5.46	-5.20	-4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Power supply current		—	29	—	26	—	29	mA
I_{inH}	Input current HIGH	Pin 9	—	900	—	560	—	560	μA
		All other pins	—	500	—	310	—	310	
I_{inL}	Input current LOW		0.5	—	0.5	—	0.3	—	μA
V_{OH}	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
t_{pd}	Propagation delay	Pin 9	0.65	1.6	0.7	1.7	0.7	1.8	ns
		All other pins	0.4	1.3	0.45	1.35	0.5	1.5	
t_r	Rise time (20%-80%)		0.5	2.0	0.5	2.1	0.5	2.2	ns
t_f	Fall time (80%-20%)		0.5	2.0	0.5	2.1	0.5	2.2	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-Ω resistor to -2.0 V.

ECL10KH High-Speed Emitter-Coupled Logic Family
MC10H101
Quad OR/NOR Gate

Features/Benefits

- **Propagation delay, 1 ns typical**
- **Power dissipation 25 mW/gate**
- **Noise margin 150 mV**
- **Voltage compensated**
- **ECL 10K-compatible.**

Ordering Information

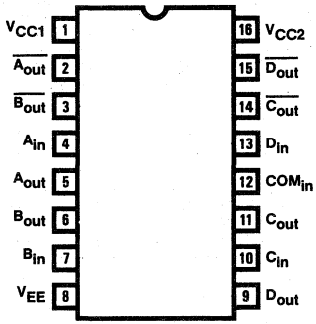
PART NUMBER	PACKAGE	TEMPERATURE
MC10H101	J,N,NL(20)	Com

Description

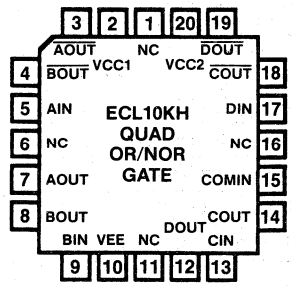
The MC10H101 is a member of Monolithic Memories' ECL family. This ECL 10KH part is a functional/pinout duplication of the standard ECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

Pin Configurations

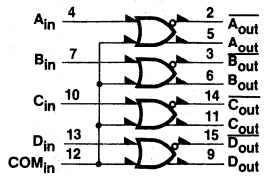
MC10H101
Quad OR/NOR Gate



MC10H101



MC10H101
Quad OR/NOR Gate



14

Portions of this Data Sheet reproduced with the courtesy of Motorola, Inc.

Absolute Maximum Ratings

Supply voltage V_{EE} (V_{CC} = 0) ..... -8.0 to 0 V_{dc}
Input voltage V_I (V_{CC} = 0) ..... 0 V_{dc} to V_{EE}
Output Current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		-5.46	-5.2	-4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ± 5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Power supply current		—	29	—	26	—	29	mA
I_{inH}	Input current high	MC10H101	—	425	—	265	—	265	μA
		MC10H101 (Pin 12 only)	—	850	—	535	—	535	
I_{inL}	Input current LOW		0.5	—	0.5	—	0.3	—	μA
V_{OH}	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
t_{pd}	Propagation delay	All others	0.5	1.45	0.5	1.5	0.5	1.6	ns
		12 Pin	0.5	1.6	0.5	1.6	0.5	1.7	
t_r, t+	Rise time		0.5	2.1	0.5	2.2	0.5	2.3	ns
t_f, t-	Fall time		0.5	2.1	0.5	2.2	0.5	2.3	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

ECL 10KH High-Speed Emitter-Coupled Logic Family
MC10H103
Quad 2-Input OR Gate

Features/Benefits

- Propagation delay, 1.0 ns typical
- Power dissipation 25 mW/gate
- Noise margin 150 mV
- Voltage compensated
- ECL 10K compatible

Ordering Information

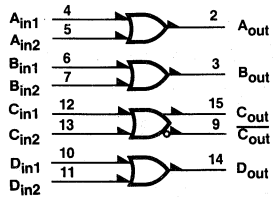
PART NUMBER	PACKAGE	TEMPERATURE
MC10H103	J,N,NL(20)	Com

Description

The MC10H103 is a member of Monolithic Memories' ECL family. This ECL 10KH part is a functional/pinout duplication of the standard ECL 10K family part with 100% improvement in propagation delay, and no increase in power-supply current.

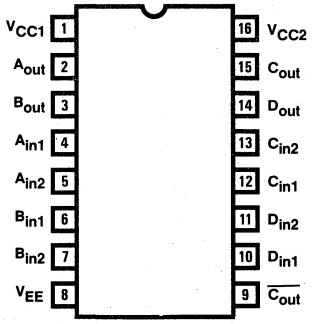
Logic Diagram

MC10H103
Quad 2-Input OR Gate

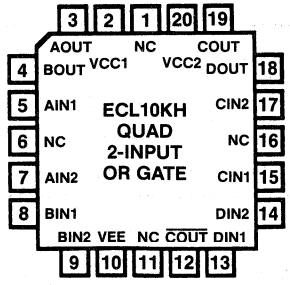


Pin Configurations

MC10H103
Quad 2-Input OR Gate



MC10H103



14

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374
Monolithic Memories

Absolute Maximum Ratings

Supply voltage V_{EE} (V_{CC} = 0) ..... -8.0 V to 0 V_{dc}
Input voltage V_I (V_{CC} = 0) ..... 0 V_{dc} to V_{EE}
Output Current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		-5.46	-5.2	-4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER	0°		25°		75°		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
I_E	Power supply current	—	29	—	26	—	29	mA
I_{inH}	Input current HIGH	—	425	—	265	—	265	μA
I_{inL}	Input current LOW	0.5	—	0.5	—	0.3	—	μA
V_{OH}	HIGH output voltage	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

SYMBOL	PARAMETER	0°		25°		75°		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	0.4	1.3	0.4	1.3	0.4	1.45	ns
t_r, t+	Rise time (20%-80%)	0.5	1.7	0.5	1.8	0.5	1.9	ns
t_f, t-	Fall time (80%-20%)	0.5	1.7	0.5	1.8	0.5	1.9	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

ECL 10KH High-Speed Emitter-Coupled Logic Family

MC10H102/Quad 2-Input NOR Gate
MC10H105/Triple 2-3-2 Input OR/NOR Gate

Features/Benefits

- Propagation delay, 1 ns typical
- Power dissipation 25 mW/gate
- Noise margin 150 mV
- Voltage compensated
- ECL 10K compatible.

Description

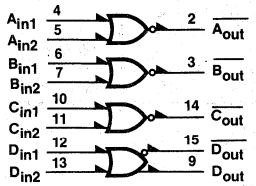
The MC10H102 and MC10H105 are members of Monolithic Memories new ECL family. These ECL 10KH parts are functional/pinout duplications of the standard ECL 10K family parts, with 100% improvement in propagation delay, and no increase in power-supply current.

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H102	J,N,NL(20)	Com
MC10H105		

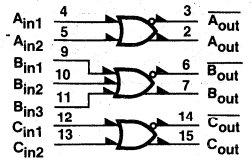
Logic Diagrams

MC10H102



Quad 2-Input NOR Gate

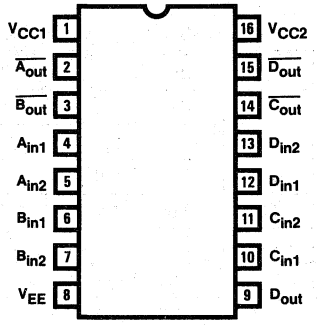
MC10H105



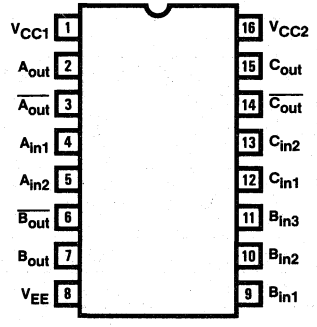
Triple 2-3-2 input OR/NOR Gate

Pin Configurations

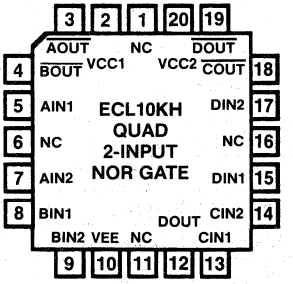
MC10H102
Quad 2-Input NOR Gate



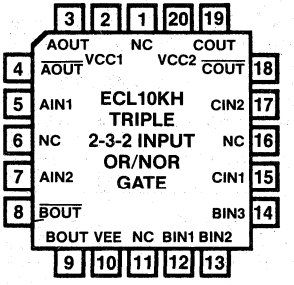
MC10H105
Triple 2-3-2 Input OR/NOR Gate



MC10H102



MC10H105



2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories MMI

Absolute Maximum Ratings

Supply voltage V_{EE} (V_{CC} = 0) ..... -8.0 V to 0 V_{dc}
Input voltage V_I (V_{CC} = 0) ..... 0 V_{dc} to V_{EE}
Output Current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		-5.46	-5.2	-4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2V ± 5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Power supply current	MC10H102	—	29	—	26	—	29	mA
		MC10H105	—	23	—	21	—	23	
I_{inH}	Input current HIGH		—	425	—	265	—	265	μA
I_{inL}	Input current LOW		0.5	—	0.5	—	0.3	—	μA
V_{OH}	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
t_{pd}	Propagation delay	MC10H102	0.4	1.25	0.4	1.25	0.4	1.4	ns
		MC10H105	0.4	1.2	0.4	1.2	0.4	1.3	
t_r, t+	Rise time	MC10H102	0.5	1.5	0.5	1.6	0.55	1.7	ns
		MC10H105	0.5	1.5	0.5	1.6	0.5	1.7	
t_f, t-	Fall time	MC10H102	0.5	1.5	0.5	1.6	0.55	1.7	ns
		MC10H105	0.5	1.5	0.5	1.6	0.5	1.7	

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

ECL 10KH High Speed Emitter Coupled Logic Family
MC10H106
Triple 4-3-3 Input NOR Gate

Features/Benefits

- Propagation delay, 1 ns typical
- 36 mW typical/gate (no load)
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Ordering Information

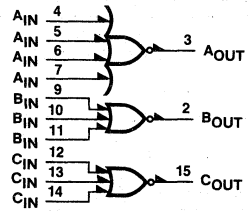
PART NUMBER	PACKAGE	TEMPERATURE
MC10H106	J, N, NL	Com

Description

The M10H106 is a member of Monolithic Memories' ECL 10KH family. This ECL device is a Triple 4-3-3 Input NOR Gate. This device is a functional/pinout duplication of the standard ECL 10K family part, with 100% improvement in propagation delay and no increase in power supply current.

Logic Diagram

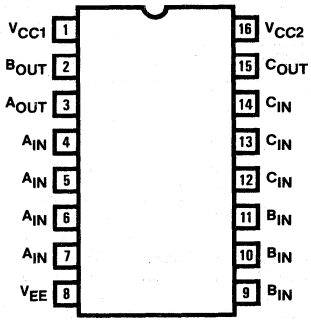
MC10H106



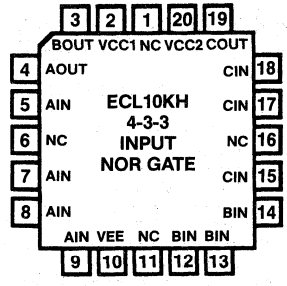
VCC1 = PIN 1
VCC2 = PIN 16
VEE = PIN 8

Pin Configuration

MC10H106
Triple 4-3-3 Input NOR Gate



MC10H106



14

Absolute Maximum Ratings

Supply voltage V_{EE} (V_{CC} = 0) ..... -8.0 V to 0 V_{dc}
Input voltage V_I (V_{CC} = 0) ..... 0 Vdc to V_{EE}
Output current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		-5.46	-5.20	-4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER	0°		25°		75°		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
I_E	Power supply current	—	23	—	21	—	23	mA
I_{inH}	Input current HIGH	—	500	—	310	—	310	μA
I_{inL}	Input current LOW	0.5	—	0.5	—	0.3	—	μA
V_{OH}	HIGH output voltage	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER	0°		25°		75°		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	0.5	1.3	0.5	1.5	0.55	1.55	ns
t_r	Rise time (20%-80%)	0.5	1.7	0.5	1.8	0.55	1.9	ns
t_f	Fall time(80%-20%)	0.5	1.7	0.5	1.8	0.55	1.9	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-Ω resistor to -2.0 V.

ECL 10KH High-Speed Emitter-Coupled Logic Family MC10H104/MC10H107 Quad 2-Input AND Gate/Triple 2-Input Exclusive OR/NOR Gate

Features/Benefits

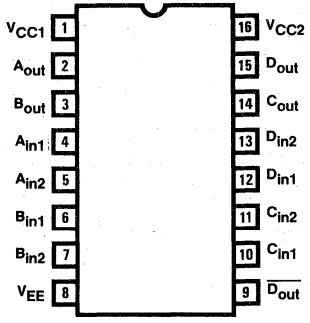
- Propagation delay, 1 ns typical
- Power dissipation 35 mW/gate typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Description

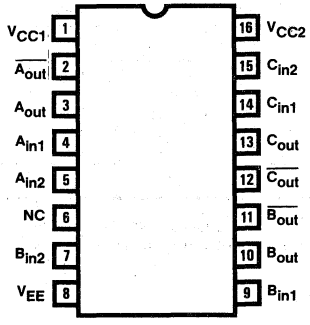
The MC10H104 and MC10H107 are members of Monolithic Memories' new ECL family. These ECL 10KH parts are functional/pinout duplications of the standard ECL 10K family parts with 100% improvement in propagation delay, and no increase in power-supply current.

Pin Configurations

MC10H104
Quad 2-Input AND Gate



MC10H107
Triple 2-Input
Exclusive OR/NOR Gate

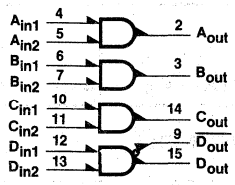


Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H104 MC10H107	J,N,NL(20)	Com

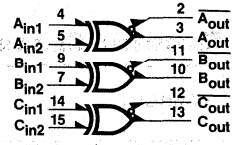
Logic Diagrams

MC10H104



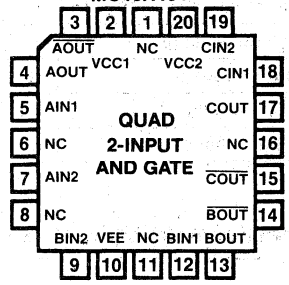
VCC1 = PIN 1
VCC2 = PIN 16
VEE = PIN 8

MC10H107

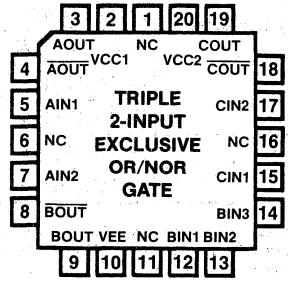


VCC1 = PIN 1
VCC2 = PIN 16
VEE = PIN 8
PIN 6 = NC

MC10H104



MC10H107



14

Absolute Maximum Ratings

Power supply V_{EE} (V_{CC} = 0) ..... −8.0 V to 0 Vdc
Input voltage V_I (V_{CC} = 0) ..... 0 Vdc to V_{EE}
Output current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply Voltage		−5.46	−5.2	−4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage temperature range	Plastic	−55		150	°C
		Ceramic	−55		165	

Electrical Characteristics V_{EE} = −5.2 V ± 5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Power supply current	MC10H104	−	39	−	35	−	39	mA
		MC10H107	−	31	−	28	−	31	
I_{inH}	Input current HIGH		−	425	−	265	−	265	μA
I_{inL}	Input current LOW		0.5	−	0.5	−	0.3	−	μA
V_{OH}	HIGH output voltage		−1.02	−0.84	−0.98	−0.81	−0.92	0.735	Vdc
V_{OL}	LOW output voltage		−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
V_{IH}	HIGH input voltage		−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
V_{IL}	LOW input voltage		−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

Switching Characteristics V_{EE} = −5.2 V, ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
t_{pd}	Propagation delay	MC10H104	0.4	1.6	0.45	1.75	0.45	1.9	ns
		MC10H107	0.4	1.5	0.4	1.6	0.4	1.7	
t_r, t+	Rise time	MC10H104	0.5	1.6	0.5	1.7	0.5	1.8	ns
		MC10H107	0.5	1.5	0.5	1.6	0.5	1.7	
t_f, t−	Fall time	MC10H104	0.5	1.6	0.5	1.7	0.5	1.8	ns
		MC10H107	0.5	1.5	0.5	1.6	0.5	1.7	

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow grater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to −2.0 V.

ECL 10KH High-Speed Emitter-Coupled Logic Family
MC10H109
Dual 4-5 Input OR/NOR Gate

Features/Benefits

- Propagation delay, 1 ns typical
- Power dissipation 35 mW/gate typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Ordering Information

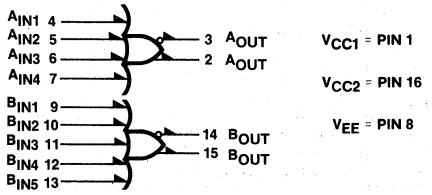
PART NUMBER	PACKAGE	TEMPERATURE
MC10H109	J,N,NL(20)	Com

Description

The MC10H109 is a member of Monolithic Memories' new ECL family. These ECL 10KH parts are functional/pinout duplications of the standard ECL 10K family parts with 100% improvement in propagation delay, and no increase in power-supply current.

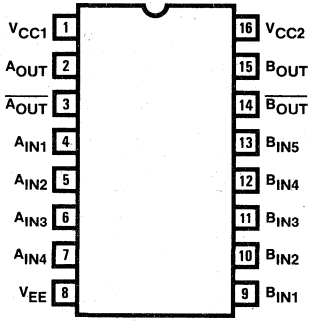
Logic Diagram

MC10H109

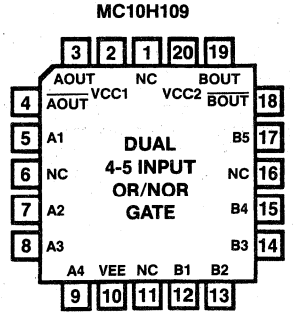


Pin Configuration

MC10H109
Dual 4-5 Input OR/NOR Gate



MC10H109



14

Portions of this Data Sheet reproduced with the courtesy of Motorola Inc.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories

Absolute Maximum Ratings

Power supply V_{EE} (V_{CC} = 0) ..... −8.0 V to 0 Vdc
Input voltage V_I (V_{CC} = 0) ..... 0 Vdc to V_{EE}
Output current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{EE}	Supply Voltage		-5.46	-5.2	-4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ± 5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Power supply current	MC10H109	–	15	–	14	–	15	mA
I_{inH}	Input current HIGH		–	425	–	265	–	265	μA
I_{inL}	Input current LOW		0.5	–	0.5	–	0.3	–	μA
V_{OH}	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	0.735	Vdc
V_{OL}	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

SYMBOL	PARAMETER	0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
t_{pd}	Propagation delay	0.4	1.3	0.4	1.3	0.45	1.45	ns
t_r, t+	Rise time	0.5	2.0	0.5	2.1	0.5	2.2	ns
t_f, t−	Fall time	0.5	2.0	0.5	2.1	0.5	2.2	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

ECL 10KH High-Speed Emitter-Coupled Logic Family
MC10H115
Quad Line Receiver

Features/Benefits

- Propagation delay 1.0 ns typical
- Power dissipation, 175 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H115	J,N,NL(20)	Com

Description

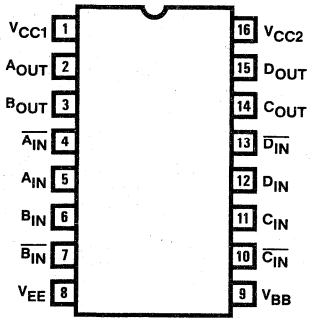
The MC10H115 is a Quad Differential Amplifier designed for use in sensing double-ended signals over long lines. This ECL 10KH part is a functional/pinout duplication of the standard ECL 10K family part, with 100% improvement in counting frequency and no increase in power-supply current.

Application Information

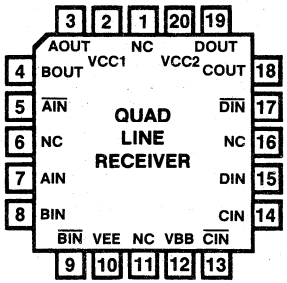
The base bias supply (V_{BB}) is made available at pin 9 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necesary. Active current sources provide the MC10H115 with excellent common mode rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} (pin 9) to prevent upsetting the current source bias network.

Pin Configuration

MC10H115
Quad Line Receiver

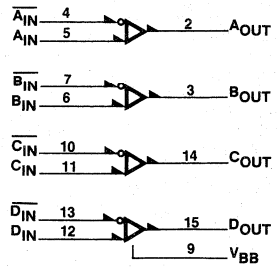


MC10H115



Logic Diagram

MC10H115



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

14

Portions of this data sheet reproduced with the courtesy of Motorola Inc.

Absolute Maximum Ratings

Supply voltage V_{EE} (V_{CC} = 0) ..... -8.0 V to 0 Vdc
Input voltage V_I (V_{CC} = 0) ..... 0 Vdc to V_{EE}
Output Current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		-5.46	-5.2	-4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER	0°		25°		75°		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
I_E	Power supply current	—	29	—	26	—	29	mA
I_{inH}	Input current HIGH	—	150	—	95	—	95	µA
I_{CBO}	Input leakage current	—	1.5	—	1.0	—	1.0	µA
V_{OH}	HIGH output voltage	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc
V_{BB}	Reference voltage	-1.42	-1.28	-1.35	-1.23	-1.295	-1.15	Vdc

Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

SYMBOL	PARAMETER	0°		25°		75°		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	0.4	1.3	0.4	1.3	0.45	1.45	ns
t_r, t+	Rise time	0.5	1.4	0.5	1.5	0.5	1.6	ns
t_f, t-	Fall time	0.5	1.4	0.5	1.5	0.5	1.6	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

ECL 10KH High-Speed Emitter-Coupled Logic Family
MC10H116
Triple Line Receiver

Features/Benefits

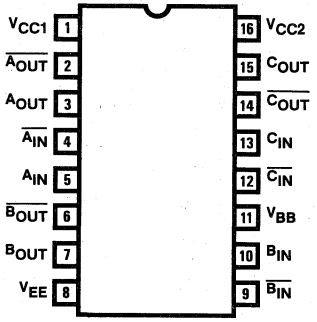
- Propagation delay 1 ns typical
- Power dissipation, 85 mW typ/pkg
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Description

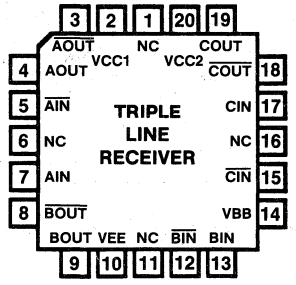
The MC10H116 is a Triple Line Receiver. This device is a member of Monolithic Memories' new ECL family. It is a functional/pinout duplication of the standard ECL 10K family part with 100% improvement in propagation delay and no increase in power-supply current.

Pin Configuration

MC10H116
Triple Line Receiver



MC10H116



Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H116	J,N,NL(20)	Com

Application Information

The MC10H116 is designed to be used in sensing differential signals over long lines. The bias supply (V_{BB}) is made available to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide these receivers with excellent common-mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} to prevent unbalancing the current-source bias network.

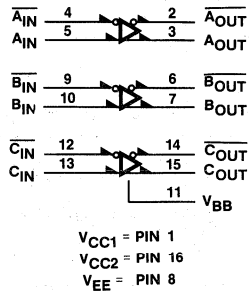
The MC10H116 does not have internal-input pull-down resistors. This provides high impedance to the amplifier input and facilitates differential connections.

Typical applications:

- Low level receiver
- Schmitt trigger
- Voltage level interface

Logic Diagram

MC10H116



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories MMI

Absolute Maximum Ratings

Supply voltage V_{EE} (V_{CC} = 0) ..... -8.0 V to 0 Vdc
Input voltage V_I (V_{CC} = 0) ..... 0 Vdc to V_{EE}
Output Current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		-5.46	-5.2	-4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER	0°		25°		75°		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
I_E	Power supply current	—	23	—	21	—	23	mA
I_{inH}	Input current HIGH	—	150	—	95	—	95	μA
I_{CBO}	Input leakage current	—	1.5	—	1.0	—	1.0	μA
V_{BB}	Reference voltage	-1.37	-1.25	-1.35	-1.23	-1.31	-1.19	Vdc
V_{OH}	HIGH output voltage	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage (1)	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage (1)	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc
V_{CMR}	Common mode range (3)	—	—	-2.85	-0.8	—	—	Vdc
V_{PP}	Input sensitivity (4)	—	—	150 typ		—	—	mVPP

Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

SYMBOL	PARAMETER	0°		25°		75°		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	0.4	1.3	0.4	1.3	0.45	1.45	ns
t_r, t+	Rise time	0.5	1.5	0.5	1.6	0.5	1.7	ns
t_f, t-	Fall time	0.5	1.5	0.5	1.6	0.5	1.7	ns

Notes: 1. When V_{BB} is used as the reference voltage.
2. Each ECL 10KH series circuit has been designed to meet the specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-Ω resistor to -2.0 V.
3. Differential input not to exceed 1.0 Vdc.
4. Differential input required to obtain full logic swing on output.

ECL 10KH High-Speed Emitter-Coupled Logic Family
MC10H117
Dual 2-Wide 2-3 Input OR-AND/OR-AND-INVERT Gate

Features/Benefits

- Propagation delay 1 ns typical
- Power dissipation, 100 mW/gate typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H117	J,N,NL(20)	Com

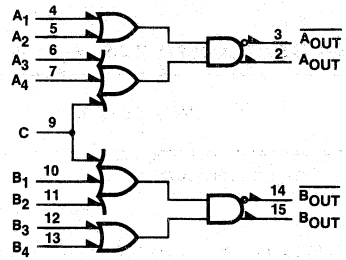
Description

The MC10H117 is a member of Monolithic Memories' ECL 10KH family. This ECL device is a Dual 2 wide 2-3 input OR-AND/OR-AND-INVERT gate designed for use in data distribution and as a data controller for digital multiplexers.

This general purpose logic element is a functional pinout duplication of the standard ECL 10K part, with 100% improvement in propagation delay, and no increase in power-supply current.

Logic Diagram

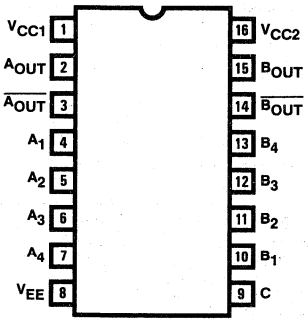
MC10H117

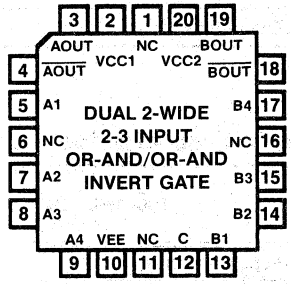


V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

Pin Configurations

MC10H117
Dual 2-Wide 2-3 Input
OR-AND/OR-AND-Invert Gate





14

Portions of this data sheet reproduced with the courtesy of Motorola Inc.

Absolute Maximum Ratings

Supply voltage V_{EE} (V_{CC} = 0) ..... -8.0 V to 0 Vdc
Input voltage (V_{CC} = 0) ..... 0 Vdc to V_{EE}
Output Current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		-5.46	-5.2	-4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Power supply current		—	29	—	26	—	29	mA
I_{inH}	Input current HIGH	Pins 3,4,5,12,13,14	—	465	—	275	—	275	µA
		Pin 6,7,10,11	—	545	—	320	—	320	
		Pin 9	—	710	—	415	—	415	
I_{inL}	Input current LOW		0.5	—	0.5	—	0.3	—	µA
V_{OH}	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	V_{dc}
V_{OL}	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	V_{dc}
V_{IH}	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	V_{dc}
V_{IL}	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	V_{dc}

Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

SYMBOL	PARAMETER	0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
t_{pd}	Propagation delay	0.45	1.35	0.45	1.35	0.5	1.5	ns
t_r, t+	Rise time	0.5	1.50	0.5	1.6	0.5	1.7	ns
t_f, t-	Fall time	0.5	1.50	0.5	1.6	0.5	1.7	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

ECL 10KH High-Speed Emitter Coupled Logic Family
MC10H118
Dual 2-Wide 3-Input OR-AND Gate

Features/Benefits

- Propagation delay 1 ns typical
- Power dissipation, 100 mW/Gate typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Ordering Information

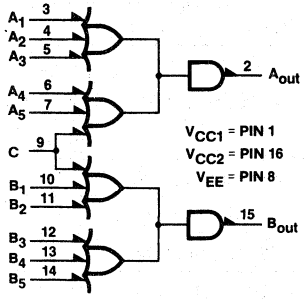
PART NUMBER	PACKAGE	TEMPERATURE
MC10H118	J,N,NL(20)	Com

Description

The MC10H118 is a member of Monolithic Memories' ECL 10KH family. This ECL device is a Dual 2-Wide 3-Input OR-AND Gate. It is a functional pinout duplication of the standard ECL 10K part with 100% improvement in propagation delay and no increase in power supply current.

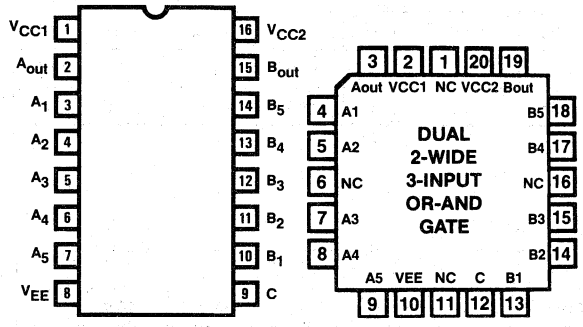
Logic Diagram

MC10H118
Dual 2-Wide
3-Input OR-AND Gate



Pin Configurations

MC10H118
Dual 2-Wide 3-Input OR-AND Gate



14

Absolute Maximum Ratings

Supply voltage V_{EE} (V_{CC} = 0) ..... -8.0 V to 0 Vdc
Input voltage V_I (V_{CC} = 0) ..... 0 Vdc to V_{EE}
Output Current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		-5.46	-5.2	-4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Power supply current		—	29	—	26	—	29	mA
I_{inH}	Input current HIGH	Pins 3,4,5,12,13,14	—	465	—	275	—	275	µA
		Pins 6,7,10,11	—	545	—	320	—	320	
		Pin 9	—	710	—	415	—	415	
I_{inL}	Input current LOW		0.5	—	0.5	—	0.3	—	µA
V_{OH}	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

SYMBOL	PARAMETER	0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
t_{pd}	Propagation delay	0.5	1.6	0.5	1.7	0.55	1.85	ns
t_r, t+	Rise time	0.5	1.5	0.5	1.6	0.5	1.7	ns
t_f, t-	Fall time	0.5	1.5	0.5	1.6	0.5	1.7	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-Ω resistor to -2.0 V.

ECL 10KH High-Speed Emitter Coupled Logic Family
MC10H119
4-Wide 4-3-3-3 Input OR-AND Gate

Features/Benefits

- Propagation delay 1 ns typical
- Power dissipation, 100 mW/Gate typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Ordering Information

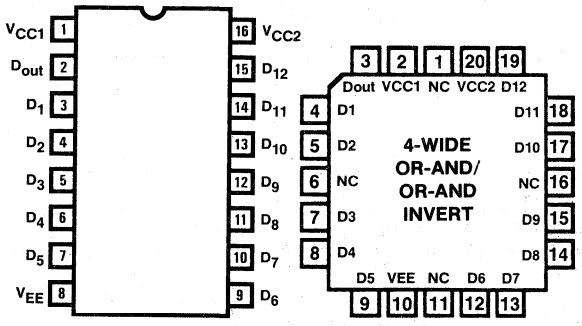
PART NUMBER	PACKAGE	TEMPERATURE
MC10H119	J,N,NL(20)	Com

Description

The MC10H119 is a member of Monolithic Memories' ECL 10KH family. This ECL device is a 4-Wide 4-3-3-3 Input OR-AND Gate. It is a functional pinout duplication of the standard ECL 10K part with 100% improvement in propagation delay and no increase in power supply current.

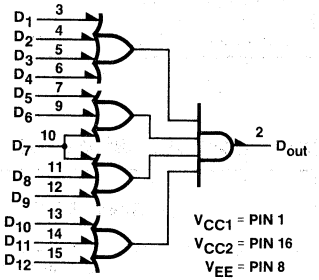
Pin Configurations

MC10H119
4-Wide 4-3-3-3
Input OR-AND Gate



Logic Diagram

MC10H119
4-Wide 4-3-3-3
Input OR-AND Gate



2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376
TWX: 910-338-2374
Monolithic Memories

Absolute Maximum Ratings

Supply voltage V_{EE} (V_{CC} = 0) ..... -8.0 V to 0 Vdc
Input voltage V_I (V_{CC} = 0) ..... 0 Vdc to V_{EE}
Output Current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		-5.46	-5.2	-4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Power supply current		—	29	—	26	—	29	mA
I_{inH}	Input current HIGH	Pins 3,4,5,6,7,9,11, 12,13,14,15	—	500	—	295	—	295	µA
		Pin 10	—	610	—	360	—	360	
I_{inL}	Input current LOW		0.5	—	0.5	—	0.3	—	µA
V_{OH}	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
t_{pd}	Propagation delay	All others	0.7	2.0	0.75	2.0	0.8	2.15	ns
		Pin 10	0.75	2.2	0.75	2.25	0.8	2.35	
t_r, t+	Rise time		0.7	2.4	0.7	2.3	0.7	2.4	ns
t_f, t-	Fall time		0.7	2.4	0.7	2.3	0.7	2.4	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

ECL 10KH High-Speed Emitter-Coupled Logic Family
MC10H121
4-Wide OR-AND/OR-AND-INVERT Gate

Features/Benefits

- Propagation delay 1 ns typical
- Power dissipation, 145 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Ordering Information

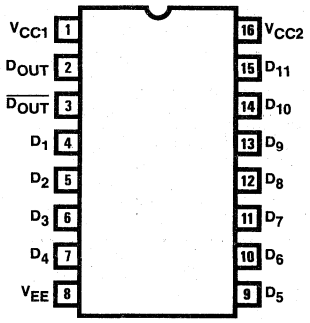
PART NUMBER	PACKAGE	TEMPERATURE
MC10H121	J, N, NL	Com

Description

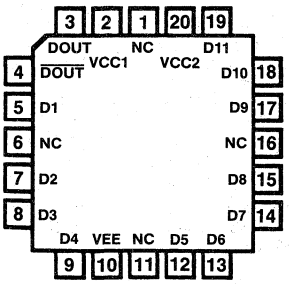
The MC10H121 is a 4-Wide OR-AND/OR-AND-INVERT Gate. This device is a member of Monolithic Memories' new ECL family. This ECL 10KH part is a functional/pinout duplication of the standard ECL 10K family part with 100% improvement in propagation delay, and no increase in power-supply current.

Pin Configuration

MC10H121
4-Wide OR-AND/OR-AND-INVERT Gate

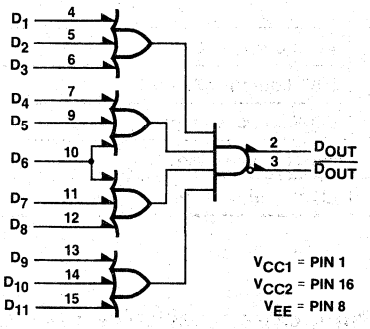


MC10H121



Logic Diagram

MC10H121



2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories

Absolute Maximum Ratings

Supply voltage V_{EE} (V_{CC} = 0) ..... −8.0 V to 0 Vdc
Input voltage V_I (V_{CC} = 0) ..... 0 Vdc to V_{EE}
Output Current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		−5.46	−5.2	−4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage temperature range	Plastic	−55		+150	°C
		Ceramic	−55		+165	

Electrical Characteristics V_{EE} = −5.2 V ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Power supply current		—	29	—	26	—	29	mA
I_{inH}	Input current HIGH	Pins 4 - 7, 9, 11 - 15	—	500	—	295	—	295	µA
		Pin 10	—	610	—	360	—	360	
I_{inL}	Input current LOW		0.5	—	0.5	—	0.3	—	µA
V_{OH}	HIGH output voltage		−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
V_{OL}	LOW output voltage		−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
V_{IH}	HIGH input voltage		−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
V_{IL}	LOW input voltage		−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

Switching Characteristics V_{EE} = −5.2 V, ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
t_{pd}	Propagation delay	All others	0.55	1.95	0.6	2.0	0.7	2.40	ns
		Pin 10	0.45	1.8	0.45	1.8	0.55	2.2	
t_r, t+	Rise time		0.5	1.7	0.5	1.8	0.5	1.9	ns
t_f, t−	Fall time		0.5	1.7	0.5	1.8	0.5	1.9	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to −2.0 V.

ECL 10KH High-Speed Emitter-Coupled Logic Family
MC10H124
Quad TTL-to-ECL Translator

Features/Benefits

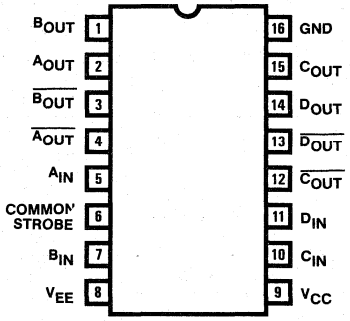
- **Propagation delay 1.5 ns typical**
- **Power dissipation 520 mW typical**
- **Noise margin 150 mV**
- **Voltage compensated**
- **ECL 10K-compatible**

Description

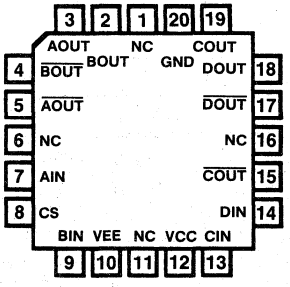
The MC10H124 is a Quad TTL-to-ECL translator. This device is a member of Monolithic Memories' new ECL family. This quad translator is used for interfacing data and control signals between a saturated logic section and the ECL section of digital systems. The 10KH part is a functional/pinout duplication of the standard ECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

Pin Configuration

MC10H124
Quad TTL-to-ECL Translator



MC10H124



Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H124	J, N, NL	Com

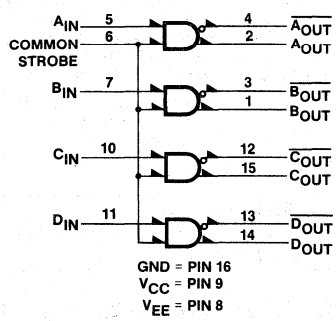
Application Information

The MC10H124 has TTL-compatible inputs and ECL complementary open-emitter outputs that allow use as an inverting/non-inverting translator or as a differential line driver. When the common strobe input is at the low logic level, it forces all true outputs to an ECL low logic state and all inverting outputs to an ECL high logic state.

An advantage of this device is that TTL-level information can be transmitted differentially, via balanced twisted-pair lines, to ECL equipment, where the signal can be received by the MC10H115 or MC10H116 differential line receivers. The power supply requirements are ground, +5.0 volts, and -5.2 volts.

Logic Diagram

MC10H124



Portions of this data sheet reproduced with the courtesy of Motorola Inc.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories MMI

Absolute Maximum Ratings

Supply voltage V_{EE} (V_{CC} = 5.0 V) ..... -8.0 V to 0 Vdc
Supply voltage, V_{CC} (V_{EE} = -5.2 V) ..... 0 to +7.0 Vdc
Input Voltage, V_I (V_{CC} = 5.0 V) ..... 0 Vdc to V_{CC}
Output Current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		-5.46	-5.2	-4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage temperature range	Plastic	-55		+150	°C
		Ceramic	-55		+165	

Electrical Characteristics V_{EE} = -5.2 V ±5% V_{CC} = 5.0 V ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Negative power supply drain current		—	72	—	66	—	72	mA
I_{CCH}	Positive power supply drain current*		—	16	—	16	—	18	mA
I_{CCL}			—	25	—	25	—	25	mA
I_{IH}	Input current HIGH (V_I = 2.4 V)	Pin 6	—	200	—	200	—	200	µA
		Pins 5, 7, 10, 11	—	50	—	50	—	50	
I_{IL}	Input current LOW (V_I = 0.4 V)	Pin 6	—	-12.8	—	-12.8	—	-12.8	mA
		Pins 5, 7, 10, 11	—	-3.2	—	-3.2	—	-3.2	
I_L	Input breakdown current (V_{in} = 5.5 V)		—	1.0	—	1.0	—	1.0	mA
V_{IC}	Input clamp voltage (-10 mA, pins 5,7,10,11) (-20 mA, pin 6)		—	-1.5	—	-1.5	—	-1.5	Vdc
V_{OH}	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage		2.0	—	2.0	—	2.0	—	Vdc
V_{IL}	LOW input voltage		—	0.8	—	0.8	—	0.8	Vdc

Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

SYMBOL	PARAMETER	0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
t_{pd}	Propagation delay	0.55	2.25	0.55	2.4	0.85	2.95	ns
t_r, t+	Rise time	0.5	1.5	0.5	1.6	0.5	1.70	ns
t_f, t-	Fall time	0.5	1.5	0.5	1.6	0.5	1.70	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

* ICCH — Current drain from V_{CC} power supply with all inputs at Logic HIGH level
ICCL — Current drain from V_{CC} power supply with all inputs at Logic LOW level.

ECL 10KH High-Speed Emitter-Coupled Logic Family
MC10H125
Quad ECL-to-TTL Translator

PRELIMINARY INFORMATION

This document contains specifications and information which are subject to change.

Features/Benefits

- Propagation delay, 2.5 ns typical
- Power Dissipation 520 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H125	J,N,NL(20)	Com

Description

The MC10H125 is a member of Monolithic Memories' ECL family. The MC10H125 is a quad translator for interfacing data and control signals between the ECL section and TTL compatible section of digital systems. The 10KH part is a functional/ pinout duplication of the standard ECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

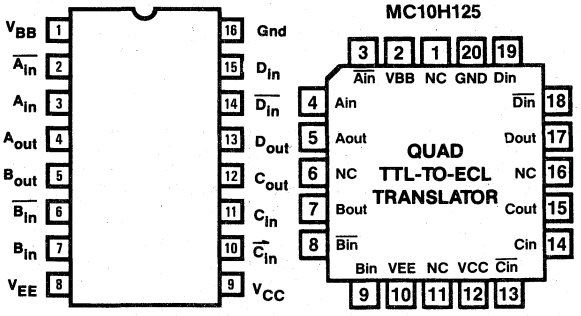
Application Information

The MC10H125 incorporates differential inputs and Schottky TTL "totem pole" outputs. The differential inputs don't have input pull-down and allow for use as an inverting/non-inverting translator or as a differential line receiver. The V_{BB} reference voltage is available from Pin 1 for use in single-ended input biasing. The outputs of the MC10H125 go to a low logic level whenever the inputs are left floating.

An advantage of this device is that ECL-level information can be received via balanced twisted pair lines in the TTL equipment. This isolates the ECL-logic from the noisy TTL environment. Power supply requirements are ground, +5.0 volts and -5.2 volts.

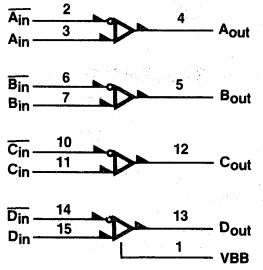
Pin Configuration

MC10H125
Quad ECL-to-TTL Translator



Logic Diagram

MC10H125
Quad ECL-to-TTL Translator



Gnd = Pin 16
V_{CC} (+ 5.0 Vdc) = Pin 9
V_{EE} (-5.2 Vdc) = Pin 8

14

Absolute Maximum Ratings

Power supply V_{EE} (V_{CC} + 5.0 V) ..... -8.0 V to 0 Vdc
Power Supply V_{CC} (V_{EE} = -5.2 V) ..... 0 V to +7.0 Vdc
Input voltage V_I (V_{CC} = 5.0 V) ..... 0 Vdc to V_{EE}

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply Voltage		-5.46	-5.2	-4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ± 5%, V_{CC} = 5.0 V ± 5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Negative power supply drain current		—	44	—	40	—	44	mAdc
I_{CCH}	Positive power supply drain current	Outputs = H	—	63	—	63	—	63	mAdc
I_{CCL}		Outputs = L	—	40	—	40	—	40	
I_{inH}	Input current		—	225	—	145	—	145	μAdc
I_{CBO}	Input leakage current		—	1.5	—	1.0	—	1.0	μAdc
V_{OH}	HIGH output voltage	I_{OH} = -1 mA	2.5	—	2.5	—	2.5	—	Vdc
V_{OL}	LOW output voltage	I_{OL} = +20 mA	—	0.5	—	0.5	—	0.5	Vdc
V_{IH}	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc
I_{OS}	Short circuit current		60	150	60	150	60	150	mAdc
V_{BB}	Reference voltage		-1.37	-1.25	-1.35	-1.23	-1.31	-1.19	Vdc

Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

SYMBOL	PARAMETER	0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
t_{pd}	Propagation delay*	0.8	3.3	0.85	3.35	0.9	3.4	ns
t_r, $t+$	Rise time	0.3	1.2	0.3	1.2	0.3	1.2	ns
t_f, $t-$	Fall time	0.3	1.2	0.3	1.2	0.3	1.2	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

* Drives a 25-pF load.

ECL 10KH High-Speed Emitter-Coupled Logic Family
Dual Latch
MC10H130

Features/Benefits

- **Propagation delay, 1 ns typical**
- **Power dissipation, 155 mW typical**
- **Noise margin 150 mV**
- **Voltage compensated**
- **ECL 10K-compatible**

Description

The MC10H130 is a dual latch which has two different mechanisms to retain data through latch control signals. Each latch can be operated separately by holding the common latch control signal ($\overline{C}$) LOW, then switching an individual latch control signal ($\overline{CE1}/\overline{CE2}$) from LOW to HIGH to cause retention of data in the relevant latch. If simultaneous operation of both latches is required, $\overline{CE1}$ and $\overline{CE2}$ are held LOW and the common latch control C is switched from LOW to HIGH.

For either latch, data present at the inputs (D1/D2) will be seen at the outputs (Q1/$\overline{Q1}$ and Q2/$\overline{Q2}$) when both latch control signals are LOW. This condition allows data to be setup within the latch, after which time causing a positive transition to the HIGH state on either or both latch control signals causes data retention. After either or both of these signals are HIGH, subsequent changes in data at an input are ignored by the latch, provided the hold time requirement is met.

An alternative means to load data in the latches is to use the direct set and reset (S1/S2 and R1/R2, respectively) lines. These inputs do not override the latch controls, or the D inputs. Instead, set or reset are only effective when either $\overline{C}$, $\overline{CE1}/\overline{CE2}$ or both, are HIGH. Note that this relationship is different than the case for a similar part, the MC10H131, which is a Dual Master-Slave D-type Flip-Flop.

Function Table

D	$\overline{C}$	$\overline{CE1}/\overline{CE2}$	R	S	$Q_{n=1}$
L	L	L	X	X	L
H	L	L	X	X	H
X	H	X	L	L	Q_n
X	H	X	L	H	H
X	H	X	H	L	L
X	H	X	H	H	N.D.
X	X	H	L	L	Q_n
X	X	H	L	H	H
X	X	H	H	L	L
X	X	H	H	H	N.D.

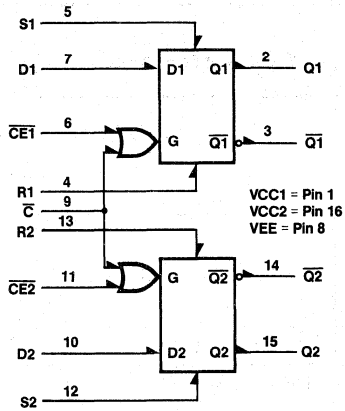
X = Don't Care
N.D. = Not Defined

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H130	J,N,NL(20)	Com

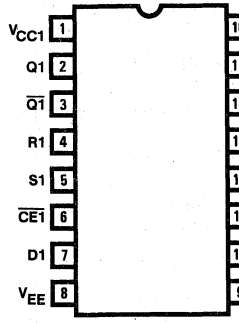
Logic Diagram

MC10H130
Dual Latch

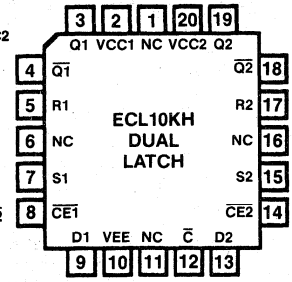


Pin Configurations

MC10H130
Dual Latch



MC10H130



2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories MMI

Absolute Maximum Ratings

Supply voltage V_{EE} (V_{CC} = 0) ..... -8.0 V to $0V_{dc}$
Input voltage V_I (V_{CC} = 0) ..... $0V_{dc}$ to V_{EE}
Output Current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		-5.46	-5.2	-4.94	V
T_A	Operating temperature range		0		75	°C
T_{stg}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Power supply current		—	38	—	35	—	38	mA
I_{inH}	Input current HIGH	Pins 6, 11	—	468	—	275	—	275	μA
		Pins 7, 9, 10	—	545	—	320	—	320	
		Pins 4, 5, 12, 13	—	434	—	255	—	255	
I_{inL}	Input current LOW		0.5	—	0.5	—	0.3	—	μA
V_{OH}	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
t_{pd}	Propagation delay	Data	0.40	1.60	0.40	1.70	0.40	1.80	ns
		Set, Reset	0.60	1.70	0.70	1.80	1.80	1.90	
		Clock, CE	0.50	1.60	0.50	1.70	1.70	1.80	
t_r,t+	Rise time (20%-80%)		0.5	1.6	0.5	1.7	0.5	1.8	ns
t_f,t-	Fall time (80%-20%)		0.5	1.6	0.5	1.7	0.5	1.8	ns
t_{set}	Setup time		0.5	1.6	0.5	1.7	0.5	1.8	ns
t_{hold}	Hold time		0.5	1.6	0.7	—	0.7	—	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

ECL 10KH High-Speed Emitter-Coupled Logic Family
MC10H131
Dual Master-Slave Type D Flip-Flop

Features/Benefits

- **Propagation delay, 1 ns typical**
- **Power dissipation, 235 mW typical**
- **Noise margin of 150 mV**
- **Voltage compensated**
- **ECL 10K-compatible**

Description

The MC10H131 is a member of Monolithic Memories' ECL family. The MC10H131 is a dual master-slave D-type flip-flop. Asynchronous Set (S) and Reset (R) override Clock (C_C) and Clock Enable ($\overline{CE}$) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking fuction. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the controlling input(s). A change in the information present at the data (D) input will not affect the data output at any other time due to master slave construction.

This ECL 10KH part is a functional/pinout duplication of the standard ECL 10K family part, with 100% improvement in clock speed and propagation delay and no increase in power supply current.

Function Tables

R-S TRUTH TABLE

R	S	$Q_n + 1$
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined.

CLOCKED TRUTH TABLE

C	D	$Q_n + 1$
L	X	Q_n
H↑	L	L
H↑	H	H

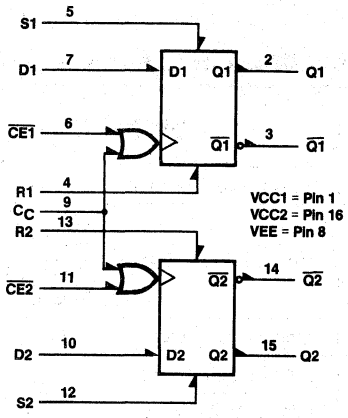
X = Don't Care.
C = $\overline{CE} + C_C$.

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H131	J,N,NL(20)	Com

Logic Diagram

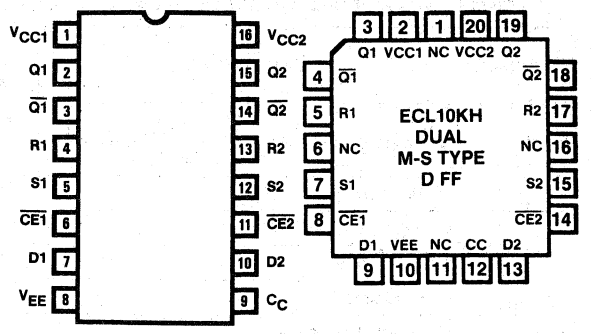
MC10H131
Dual Master-Slave Type D Flip-Flop



> : denotes edge triggered clock

Pin Configurations

MC10H131
Dual Master-Slave Type D Flip-Flop



MC10H131

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories

Absolute Maximum Ratings

Supply voltage V_{EE} (V_{CC} = 0) ..... −8.0 to 0 V_{dc}
Input voltage V_I (V_{CC} = 0) ..... 0 V_{dc} to V_{EE}
Output Current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		−5.46	−5.2	−4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Power supply current		—	62	—	56	—	62	mA
I_{inH}	Input current HIGH	Pins 6, 11	—	530	—	310	—	310	µA
		Pin 9	—	660	—	390	—	390	
		Pins 7, 10	—	485	—	285	—	285	
		Pins 4, 5, 12, 13	—	790	—	465	—	465	
I_{inL}	Input current LOW		0.5	—	0.5	—	0.3	—	µA
V_{OH}	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

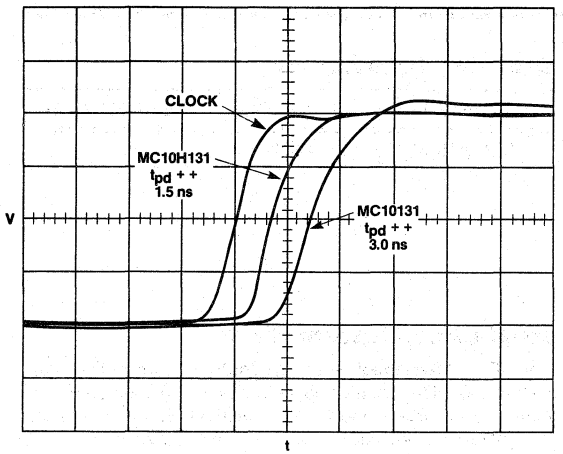
Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
t_{pd}	Propagation delay	Clock, $\overline{CE}$	0.80	1.6	0.8	1.7	0.8	1.8	ns
		Set, Reset	0.6	1.6	0.7	1.7	0.7	1.8	
t_r, $t+$	Rise time (20%-80%)		0.6	2.0	0.6	2.0	0.6	2.2	ns
t_f, $t-$	Fall time (80%-20%)		0.6	2.0	0.6	2.0	0.6	2.2	ns
t_{set}	Setup time		0.7	—	0.7	—	0.7	—	ns
t_{hold}	Hold time		0.8	—	0.8	—	0.8	—	ns
t_{tog}	Toggle frequency		250	—	250	—	250	—	MHz

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

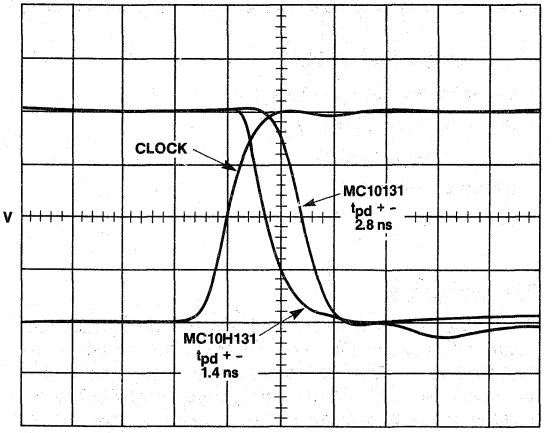
Switching Time Comparison
ECL 10KH versus ECL 10K

CLOCK TO Q



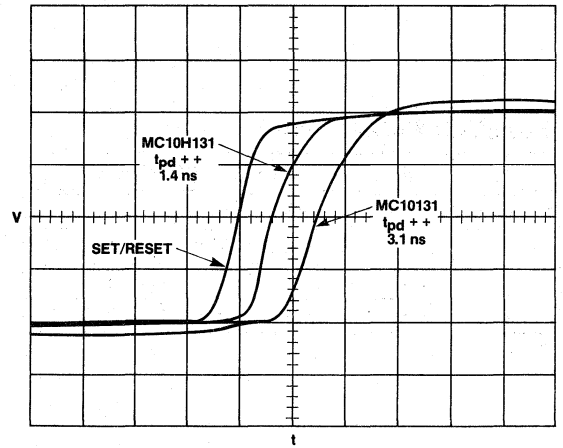
t_r FOR MC10H131: 1.4 ns
t_r FOR MC10131: 2.0 ns

CLOCK TO $\overline{Q}$



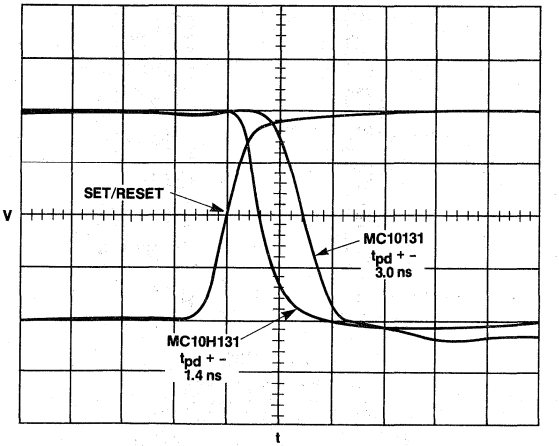
t_f FOR MC10H131: 1.2 ns
t_f FOR MC10131: 1.4 ns

SET/RESET TO Q



t_r FOR MC10H131: 1.5 ns
t_r FOR MC10131: 2.1 ns

SET/RESET TO $\overline{Q}$



t_f FOR MC10H131: 1.2 ns
t_f FOR MC10131: 1.5 ns

NOTE: t_r and t_f measured from the 20% to the 80% level of the output signal swing.
t_{pd} is measured from the 50% level of the input to the 50% level of the output.

14

ECL 10KH High-Speed Emitter-Coupled Logic Family
MC10H136
Universal Hexadecimal Counter

Features/Benefits

- Counting frequency, 250 MHz min.
- Power dissipation, 715 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H136	J, N, NL	Com

Description

The MC10H136 is a high-speed synchronous hexadecimal counter. This device is a member of Monolithic Memories' new ECL 10KH family. This 10KH part is a functional/pinout duplication of the standard ECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

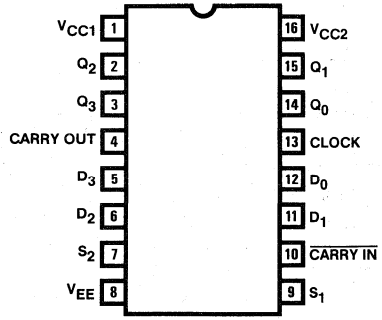
Application Information

The MC10H136 is a high-speed synchronous counter that operates at 250 MHz. Counter operating modes include count up, count down, preset and hold count. This device allows the designer to use one basic counter for many applications.

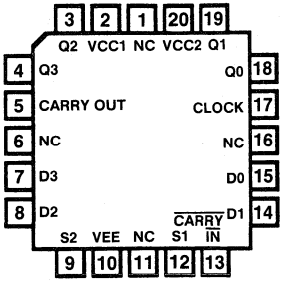
The S_1, S_2 control lines determine the operating modes of the counter. In the preset mode, a clock pulse is necessary to load the counter with the information present on the data inputs (D_0, D_1, D_2 and D_3). Carry out goes low on the terminal counter or when the counter is being preset.

Pin Configuration

MC10H136
Universal Hexadecimal Counter



MC10H136

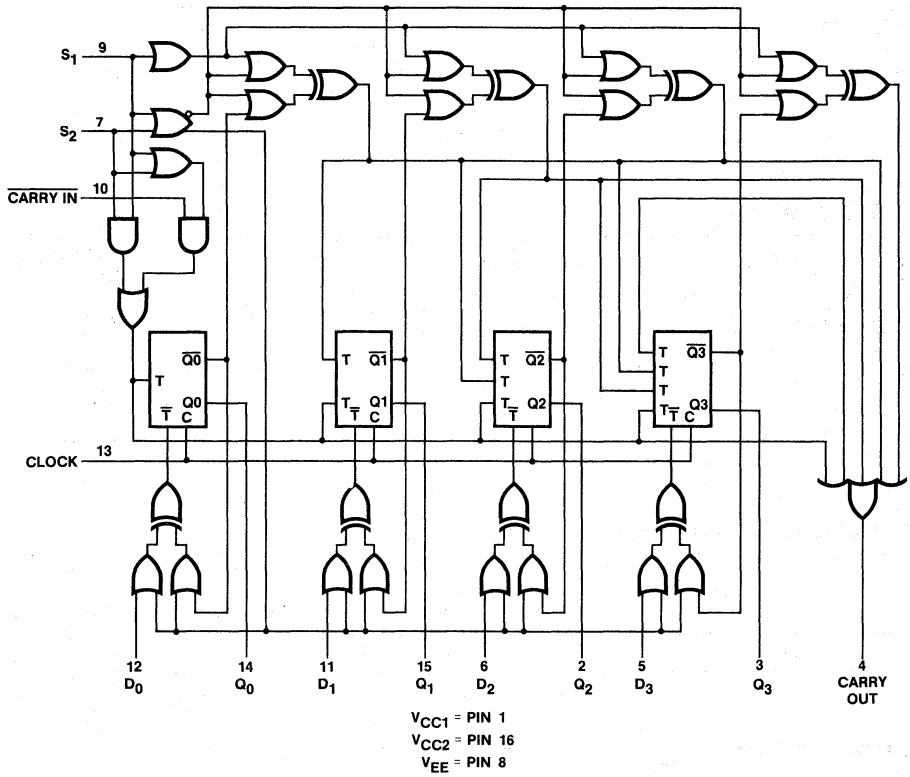


Function Select Table

S_1	S_2	OPERATING MODE
L	L	Preset (Program)
L	H	Increment (Count up)
H	L	Decrement (Count down)
H	H	Hold (Stop count)

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories

Logic Diagram



Sequential Truth Table*

INPUTS								OUTPUTS					
S_1	S_2	D_0	D_1	D_2	D_3	CARRY IN	CLOCK V_{IL} / V_{IH}	Q_0	Q_1	Q_2	Q_3	CARRY OUT	SELECT MODE
L	L	L	L	H	H	X	⌐	L	L	H	H	L	Preset
L	H	X	X	X	X	L	⌐	H	L	H	H	H	Increment
L	H	X	X	X	X	L	⌐	L	H	H	H	H	Increment
L	H	X	X	X	X	L	⌐	H	H	H	H	L	Increment
L	H	X	X	X	X	H	⌐	H	H	H	H	H	Increment
L	H	X	X	X	X	H	⌐	H	H	H	H	H	Increment
H	H	X	X	X	X	X	⌐	H	H	H	H	H	Hold
L	L	H	H	L	L	X	⌐	H	H	L	L	L	Preset
H	L	X	X	X	X	L	⌐	L	H	L	L	H	Decrement
H	L	X	X	X	X	L	⌐	H	L	L	L	H	Decrement
H	L	X	X	X	X	L	⌐	L	L	L	L	L	Decrement
H	L	X	X	X	X	L	⌐	H	H	H	H	H	Decrement

X = Don't care.

* Truth table shows logic states assuming that the inputs vary in sequence from top to bottom, as shown.
The states of the Q0-Q3 outputs are shown assuming the occurance of a L-to-H edge transition (e.g. after clocking).

14

Absolute Maximum Ratings

Supply voltage V_{EE} (V_{CC} = 0 V) ..... −8.0 V to 0 Vdc
Input voltage V_I (V_{CC} = 0 V) ..... 0 Vdc to V_{EE}
Output Current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		−5.46	−5.2	−4.94	V
T_A	Operating temperature range		0		75	
T_{STG}	Storage temperature range	Plastic	−55		+150	°C
		Ceramic	−55		+165	

Electrical Characteristics V_{EE} = −5.2 V ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Power supply current		—	165	—	150	—	165	mA
I_{inH}	Input current HIGH	Pins 5, 6, 11, 12, 13	—	430	—	275	—	275	µA
		Pin 9	—	670	—	420	—	420	
		Pin 7	—	535	—	335	—	335	
		Pin 10	—	380	—	240	—	240	
I_{inL}	Input current LOW		0.5	—	0.5	—	0.3	—	µA
V_{OH}	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The Circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

SYMBOL	PARAMETER		0°		25°		75°		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	Clock to Q	0.7	2.3	0.7	2.4	0.7	2.5	ns
		Clock to carry out	1.0	4.8	1.0	4.9	1.0	5.0	
		Carry in to carry out	0.7	2.5	0.7	2.6	0.7	2.7	
t_{set}	Setup time	Data (D0 to C)	2.0	—	2.0	—	2.0	—	ns
		Select (S to C)	3.5	—	3.5	—	3.5	—	
		Carry in (Cin to C)	2.0	—	2.0	—	2.0	—	
		Carry in (C to Cin)	0	—	0	—	0	—	
t_{hold}	Hold time	Data (C to D0)	0	—	0	—	0	—	ns
		Select (C to S)	-0.5	—	-0.5	—	-0.5	—	
		Carry in (C to Cin)	0	—	0	—	0	—	
		Carry in (Cin to C)	2.2	—	2.2	—	2.2	—	
f_{count}	Counting frequency		250	—	250	—	250	—	MHz
t_r,t+	Rise time		0.5	2.3	0.5	2.4	0.5	2.5	ns
t_f,t-	Fall time		0.5	2.3	0.5	2.4	0.5	2.5	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

ECL 10KH High-Speed Emitter-Coupled Logic Family
MC10H141
Four-Bit Universal Shift Register

PRELIMINARY INFORMATION

This document contains specifications and information which are subject to change.

Features/Benefits

- **Shift frequency, 250 MHz min**
- **Power dissipation, 425 mW typical**
- **Noise margin 150 mV**
- **Voltage compensated**
- **ECL 10K-compatible**

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H141	J,N,NL(20)	Com

Description

The MC10H141 is a four-bit universal shift register which performs shift-left, or shift-right, serial/parallel in, and serial/parallel out operations with no external gating. Inputs S1 and S2 control

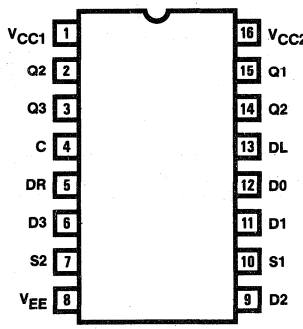
(See following page)

Function Table

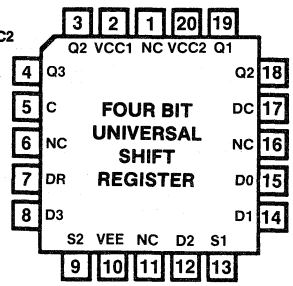
SELECT		OUTPUTS				OPERATING MODE
S1	S2	$Q0_{n-1}$	$Q1_{n-1}$	$Q2_{n-1}$	$Q3_{n-1}$	
L	L	D0	D1	D2	D3	Parallel entry
L	H	$Q1_n$	$Q2_n$	$Q3_n$	DR	Shift right*
H	L	DL	$Q0_n$	$Q1_n$	$Q2_n$	Shift left*
H	L	$Q0_n$	$Q1_n$	$Q2_n$	$Q3_n$	Stop shift

* Outputs as exist after pulse appears at "C" input with input conditions as shown (Pulse Positive transition of clock input).

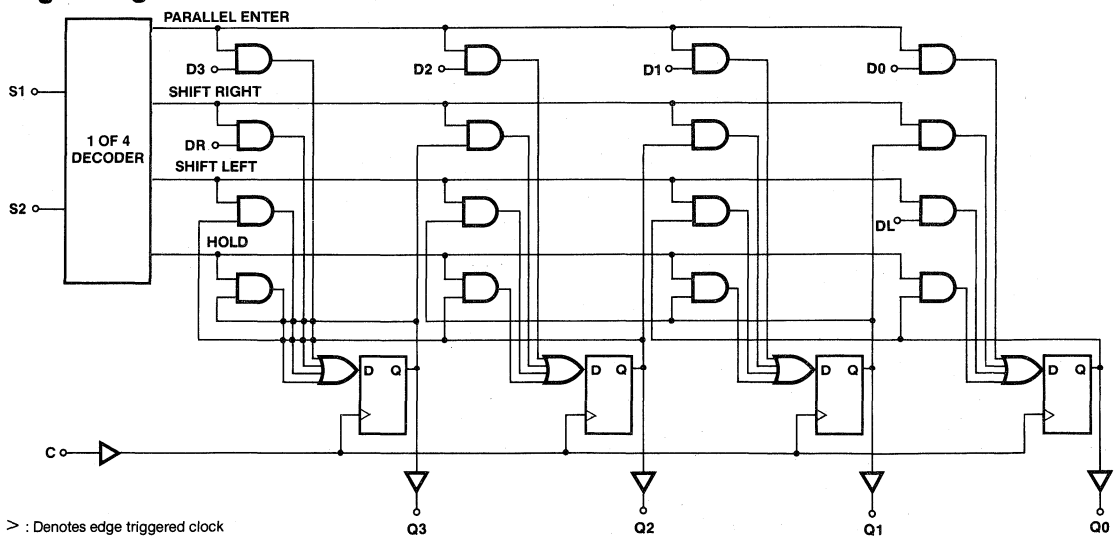
MC10H141
Four-Bit Universal Shift Register



MC10H141



Logic Diagram



> : Denotes edge triggered clock

Portions of this Data Sheet reproduced with the courtesy of Motorola Inc.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories

Absolute Maximum Ratings

Supply voltage, V_{EE} (V_{CC} = 0) ..... -8.0 V to 0 V_{dc}
Input voltage, V_I (V_{CC} = 0) ..... 0 V_{dc} to V_{EE}
Output Current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		-5.46	-5.2	-4.94	V
T_A	Operating free-air temperature		0		75	°C
T_{STG}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Power supply current		—	112	—	102	—	112	mA
I_{inH}	Input current HIGH	Pins 5, 6, 9, 11, 12, 13	—	405	—	255	—	255	µA
		Pins 7, 10	—	416	—	260	—	260	
		Pins 4,	—	510	—	320	—	320	
I_{inL}	Input current LOW		0.5	—	0.5	—	0.3	—	µA
V_{OH}	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-0.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
t_{pd}	Propagation delay		1.1	2.0	1.0	2.0	1.1	2.1	ns
t_{hold}	Hold time		1.0	—	1.0	—	1.0	—	ns
t_{set}	Setup time	Data	1.5	—	1.5	—	1.5	—	ns
		Select	3.0	—	3.0	—	3.0	—	
t_r, $t+$	Rise time		0.5	2.4	0.5	2.4	0.5	2.4	ns
t_f, $t-$	Fall time		0.5	2.4	0.5	2.4	0.5	2.4	ns
f_{shift}	Shift frequency		250	—	250	—	250	—	MHz

NOTE: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0 V.

Description (Continued)

the four possible operations of the register without external gating of the clock. The flip-flops shift information on the positive edge of the clock. The four operations are stop shift, shift-left, shift-right, and parallel entry of data. The other six inputs are all data type inputs; four for parallel entry data, and one for shifting in from the left (DL) and one for shifting in from the right (DR). This device is a functional/pinout duplication of the standard ECL 10K part, with 100% improvement in propagation delay and operation frequency and no increase in power supply current.

ECL 10KH High-Speed Emitter-Coupled Logic Family
MC10H158
QUAD 2-Input Multiplexer

PRELIMINARY INFORMATION

This document contains specifications and information which are subject to change.

Features/Benefits

- **Propagation delay, 1.5 ns typical**
- **Power dissipation, 197 mW typical**
- **Noise margin 150 mV**
- **Voltage compensated**
- **ECL 10K-Compatible**

Description

The MC10H158 is a member of Monolithic Memories' ECL Family. The MC10H158 is a quad 2-input multiplexer. When the select line (SELECT) is LOW D_1 data appear at the outputs (Q3-Q0). Conversely, when the select input is HIGH, D_0 data appear at the outputs. This ECL part is a functional/pinout duplication of the standard ECL 10K family part, with 100% improvement in propagation delay and no increase in power-supply current.

MC10H158 Function Table

SELECT	D_0*	D_1*	Q
L	X	L	L
L	X	H	H
H	L	X	L
H	H	X	H

* D_0/D_1 indicate each of four bit positions for the "zero" or "one" inputs, as controlled by the select line.

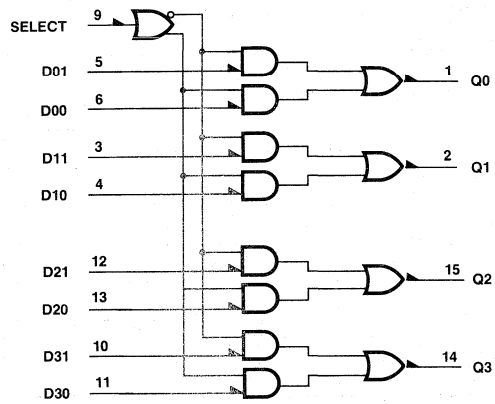
X = Don't care.

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H158	J,N,NL(20)	Com

Logic Diagram

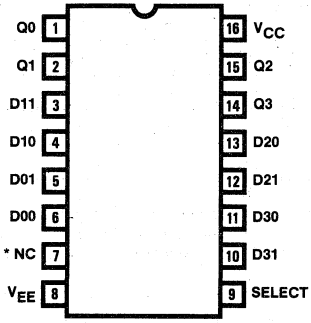
MC10H158
Quad 2-Input Multiplexer



V_{EE} Pin 8
V_{CC} Pin 16

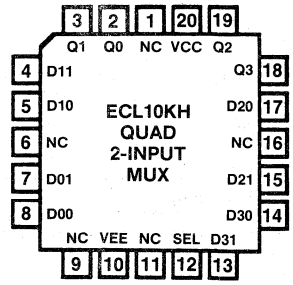
Pin Configurations

MC10H158
Quad 2-Input Multiplexer



* NC-No connection

MC10H158



Portions of this data sheet reproduced with the courtesy of Motorola Inc.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories

Absolute Maximum Ratings

Supply voltage, V_{EE} (V_{CC} = 0) ..... -8.0 to 0 V_{dc}
Input voltage, V_I (V_{CC} = 0) ..... 0 V_{dc} to V_{EE}
Output Current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply Voltage		-5.46	-5.2	-4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Power supply current		—	53	—	48	—	53	mA
I_{inH}	Input current HIGH	Pin 9	—	475	—	295	—	295	µA
		Pins 3-6 and 10-13	—	515	—	320	—	320	
I_{inL}	Input current LOW		0.5	—	0.5	—	0.3	—	µA
V_{OH}	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
t_{pd}	Propagation delay	Data	0.5	1.9	0.5	1.9	0.5	2.0	ns
		Select	1.0	2.9	1.0	2.9	1.0	2.9	
t_r, t+	Rise time		0.7	2.2	0.7	2.0	0.7	2.2	ns
t_f, t-	Fall time		0.7	2.2	0.7	2.0	0.7	2.2	ns

NOTES: Each ECL 10 KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0 V.

14

PRELIMINARY INFORMATION

This document contains specifications and information which are subject to change.

ECL 10KH High-Speed Emitter-Coupled Logic Family
MC10H159
Quad 2-Input Inverting Multiplexer with Enable

Features/Benefits

- **Propagation delay, 1.5 ns typical**
- **Power dissipation, 218 mW typical**
- **Noise margin 150 mV**
- **Voltage compensated**
- **ECL 10K-compatible**

Description

The MC10H159 is a member of Monolithic Memories' ECL family. The MC10H159 is a quad 2-input inverting multiplexer with enable. A HIGH level on the enable input (ENABLE) overrides the select input (SELECT) and forces all of the outputs (Q3-Q0) to the LOW level. A LOW level on the enable input allows multiplexer action, which is controlled by the select input. When the select input is LOW, D_1 data appear at the outputs. Conversely, when the select input is HIGH, D_0 data appear at the outputs.

MC10H159 Function Table

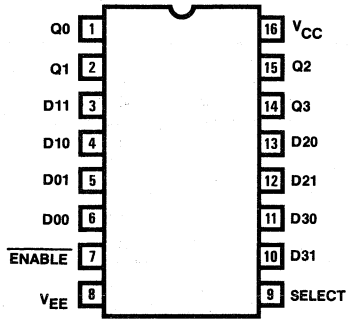
ENABLE	SELECT	D_0*	D_1*	Q
L	L	X	L	H
L	L	X	H	L
L	H	L	X	H
L	H	H	X	L
H	X	X	X	L

* D_0/D_1 indicate each of 4 bit positions for the "zero" or "one" inputs, as controlled by the select line.

X = Don't care.

Pin Configurations

MC10H159
Quad 2-Input Inverting Multiplexer with Enable

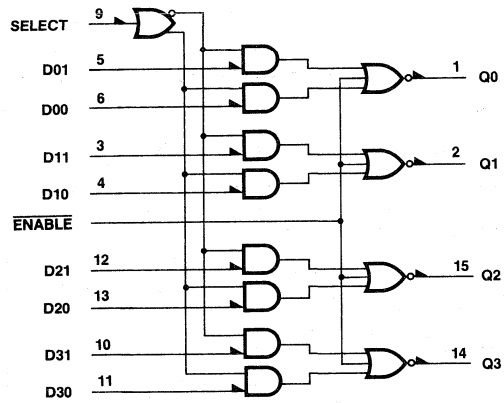


Ordering Information

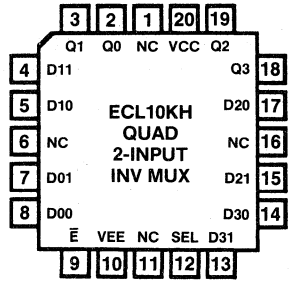
PART NUMBER	PACKAGE	TEMPERATURE
MC10H159	J,N,NL(20)	Com

Logic Diagram

MC10H159
Quad 2-Input Inverting Multiplexer with Enable



MC10H159



Portions of this Data Sheet reproduced with the courtesy of Motorola, Inc.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories

Absolute Maximum Ratings

Supply voltage V_{EE} (V_{CC} = 0) ..... −8.0 to 0 V_{dc}
Input voltage V_I (V_{CC} = 0) ..... 0 V_{dc} to V_{EE}
Output Current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		−5.46	−5.2	−4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage temperature range	Plastic	−55		150	°C
		Ceramic	−55		165	

Electrical Characteristics V_{EE} = −5.2 V ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Power supply current		—	58	—	53	—	58	mA
I_{inH}	Input current HIGH	Pin 9	—	475	—	295	—	295	μA
		Pins 3-7 and 10-13		515	—	320	—	320	
I_{inL}	Input current LOW		0.5	—	0.5	—	0.3	—	μA
V_{OH}	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.75	-1.45	Vdc

Switching Characteristics V_{EE} = −5.2 V, ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
t_{pd}	Propagation delay	Data	0.5	2.2	0.5	2.2	0.5	2.2	ns
		Select	1.0	3.2	1.0	3.2	1.0	3.2	
		Enable	1.0	3.2	1.0	3.2	1.0	3.2	
t_r,t+	Rise time		0.5	2.2	0.5	2.2	0.5	2.2	ns
t_f,t−	Fall time		0.5	2.2	0.5	2.2	0.5	2.2	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to −2.0 V.

ECL 10KH High-Speed Emitter-Coupled Logic Family
MC10H160
12-Bit Parity Generator-Checker

Features/Benefits

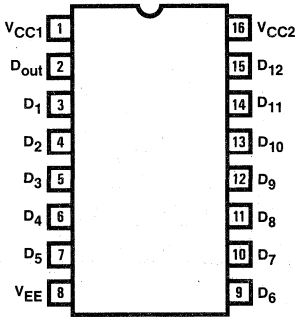
- Propagation delay, 2.5 ns typical
- Power dissipation, 320 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Description

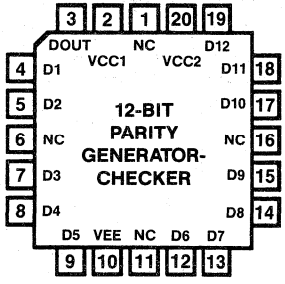
The MC10H160 is a member of Monolithic Memories' new ECL family. The MC10H160 is a 12-bit parity generator-checker. The output goes high when an odd number of inputs are high providing the odd parity function. Unconnected inputs are pulled to a logic low allowing parity detection and generation for less than 12 bits. The MC10H160 is a functional/pin out duplication of the standard ECL 10K family part with 100% improvement in propagation delay and no increase in power-supply current.

Pin Configuration

MC10H160
12-Bit Parity Generator-Checker



MC10H160

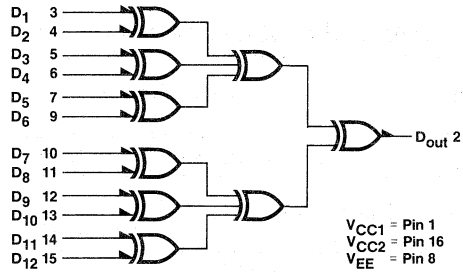


Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H160	J,N,NL(20)	Com

Logic Diagram

MC10H160
12-Bit Parity Generator-Checker



Function Table

INPUT SUM OF HIGH LEVEL INPUTS	OUTPUT PIN 2
Even	LOW
Odd	HIGH

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374
Monolithic Memories

Absolute Maximum Ratings

Power supply V_{EE} (V_{CC} = 0 V) ..... −8.0 V to 0 Vdc
Input voltage V_I (V_{CC} = 0 V) ..... 0 Vdc to V_{EE}
Output Current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		−5.46	−5.2	−4.94	V
T_A	Operating temperature range		0		+75	°C
T_{STG}	Storage temperature range	Plastic	−55		+150	°C
		Ceramic	−55		+165	

Electrical Characteristics V_{EE} = −5.2 V ± 5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Power supply current		—	88	—	78	—	86	mA
I_{inH}	Input current HIGH	Pins 3,5,7,10,12,14	—	391	—	246	—	246	μA
		Pins 4,6,9,11,13,15	—	457	—	285	—	285	
I_{inL}	Input current LOW		0.5	—	0.5	—	0.3	—	μA
V_{OH}	HIGH output voltage		−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
V_{OL}	LOW output voltage		−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
V_{IH}	HIGH input voltage		−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
V_{IL}	LOW input voltage		−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

Switching Characteristics V_{EE} = −5.2V ±5% (See Note)

SYMBOL	PARAMETER	0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
t_{pd}	Propagation delay	1.1	3.1	1.1	3.3	1.2	3.5	ns
t_r, t+	Rise time	0.55	1.5	0.55	1.6	0.75	1.7	ns
t_f, t−	Fall time	0.55	1.5	0.55	1.6	0.75	1.7	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to −2.0 V.

ECL 10KH High-Speed Emitter-Coupled Logic Family
MC10H161
Binary to 1-of-8 Decoder

Features/Benefits

- **Propagation delay, 1 ns typical**
- **Power dissipation, 315mW typical**
- **Noise margin 150 mV**
- **Voltage compensated**
- **ECL 10K-compatible**

Description

The MC10H161 is a high-speed Binary to 1-of-8 Decoder. This device is a member of Monolithic Memories' expanding ECL 10KH family. This ECL device is designed to decode a three-bit word to a one-of-eight line output. The selected output will be low while all other outputs will be high. The enable inputs, when either or both are high, force all outputs high.

The MC10H161 is a true parallel decoder. No series gating is used internally, eliminating unequal delay time found in other decoders. The MC10H161 is useful in high-speed multiplexer/demultiplexer applications.

This ECL 10KH part is a functional/pinout duplication of the standard ECL 10K part with 100% improvement in propagation delay, and no increase in power-supply current.

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H161	J,N,NL(20)	Com

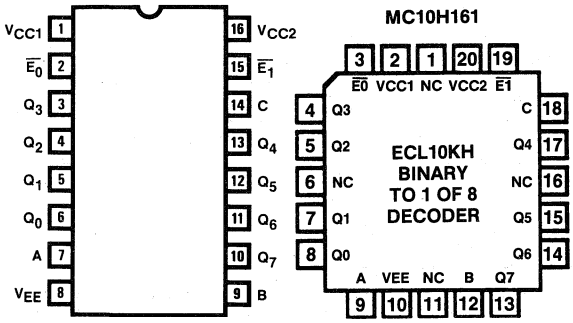
Truth Table

ENABLE INPUTS		INPUTS			OUTPUTS							
$\overline{E_1}$	$\overline{E_0}$	C	B	A	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H
L	L	L	H	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L
H	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	H	H	H	H	H	H	H	H

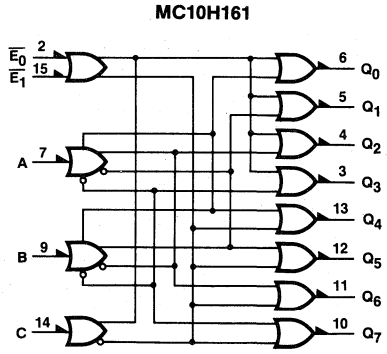
X = Don't Care

Pin Configuration

MC10H161
Binary to 1-of-8 Decoder



Logic Diagram



VCC1 = PIN 1
VCC2 = PIN 16
VEE = PIN 8

Absolute Maximum Ratings

Supply voltage V_{EE} (V_{CC} = 0) ..... -8.0 V to 0 Vdc
Input voltage V_I (V_{CC} = 0) ..... 0 Vdc to V_{EE}
Output Current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		-5.46	-5.2	-4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER	0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Power supply current	—	84	—	76	—	84	mA
I_{inH}	Input current HIGH	—	465	—	275	—	275	μA
I_{inL}	Input current LOW	0.5	—	0.5	—	0.3	—	μA
V_{OH}	HIGH output voltage	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	V_{dc}
V_{OL}	LOW output voltage	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	V_{dc}
V_{IH}	HIGH input voltage	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	V_{dc}
V_{IL}	LOW input voltage	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	V_{dc}

Switching Characteristics V_{EE} = -5.2V ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
t_{pd}	Propagation delay	Data Pins 7, 9, 14	0.6	2.0	0.65	2.1	0.7	2.2	ns
		Enable Pins 2, 15	0.8	2.3	0.8	2.4	0.9	2.5	
t_r, t+	Rise time		0.55	1.7	0.65	1.8	0.7	1.9	ns
t_f, t-	Fall time		0.55	1.7	0.65	1.8	0.7	1.9	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

14

ECL 10KH High-Speed Emitter Coupled Logic Family
MC10H162
Binary to 1-of-8 Decoder

Features/Benefits

- **Propagation delay 1 ns typical**
- **Power dissipation, 315 mW typical**
- **Noise margin 150 mV**
- **Voltage compensated**
- **ECL 10K-compatible**

Description

The MC10H162 is a high-speed Binary to 1-of-8 Decoder. This device is a member of Monolithic Memories' ECL 10KH family. This ECL device is designed to convert a three-bit word to one-of-eight output lines. The selected output will be high while all other outputs are low. The enable inputs, when either or both are high, force all outputs low.

The MC10H162 is a true parallel decoder. This eliminates unequal parallel path delay times found in other decoder designs. This device is ideally suited for high-speed multiplexer/demultiplexer applications.

This ECL 10KH part is a functional/pinout duplication of the standard ECL 10K part with 100% improvement in propagation delay and no increase in power-supply current.

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H162	J,N,NL	Com

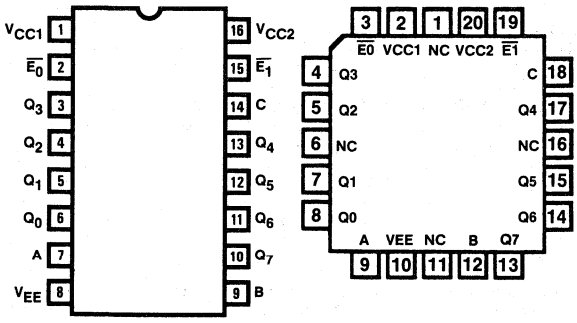
Truth Table

INPUTS					OUTPUTS							
$\overline{E0}$	$\overline{E1}$	C	B	A	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H
H	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	L	L	L	L	L	L	L	L

X = Don't Care.

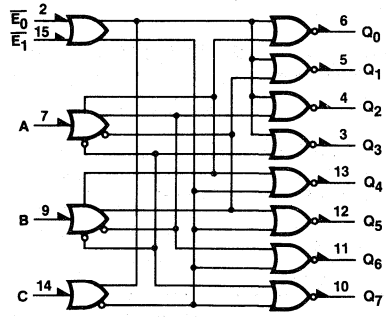
Pin Configurations

MC10H162
Binary to 1-of-8 Decoder (Inverting)



Logic Diagram

MC10H162
Binary to 1-of-8 Decoder



VCC1 = PIN 1
VCC2 = PIN 16
VEE = PIN 8

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374
Monolithic Memories

Absolute Maximum Ratings

Supply voltage V_{EE} (V_{CC} = 0) ..... -8.0 V to 0 Vdc
Input voltage V_I (V_{CC} = 0) ..... 0 Vdc to V_{EE}
Output Current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		-5.46	-5.2	-4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER	0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Power supply current	—	84	—	76	—	84	mA
I_{inH}	Input current HIGH	—	465	—	275	—	275	µA
I_{inL}	Input current LOW	0.5	—	0.5	—	0.3	—	µA
V_{OH}	HIGH output voltage	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2V ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
t_{pd}	Propagation delay	Data	0.7	2.0	0.7	2.1	0.8	2.5	ns
		Enable	0.8	2.3	0.8	2.4	0.9	2.6	
t_r, t+	Rise time		0.6	1.8	0.6	1.9	0.6	2.0	ns
t_f, t-	Fall time		0.6	1.8	0.6	1.9	0.6	2.0	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

14

Typical Applications

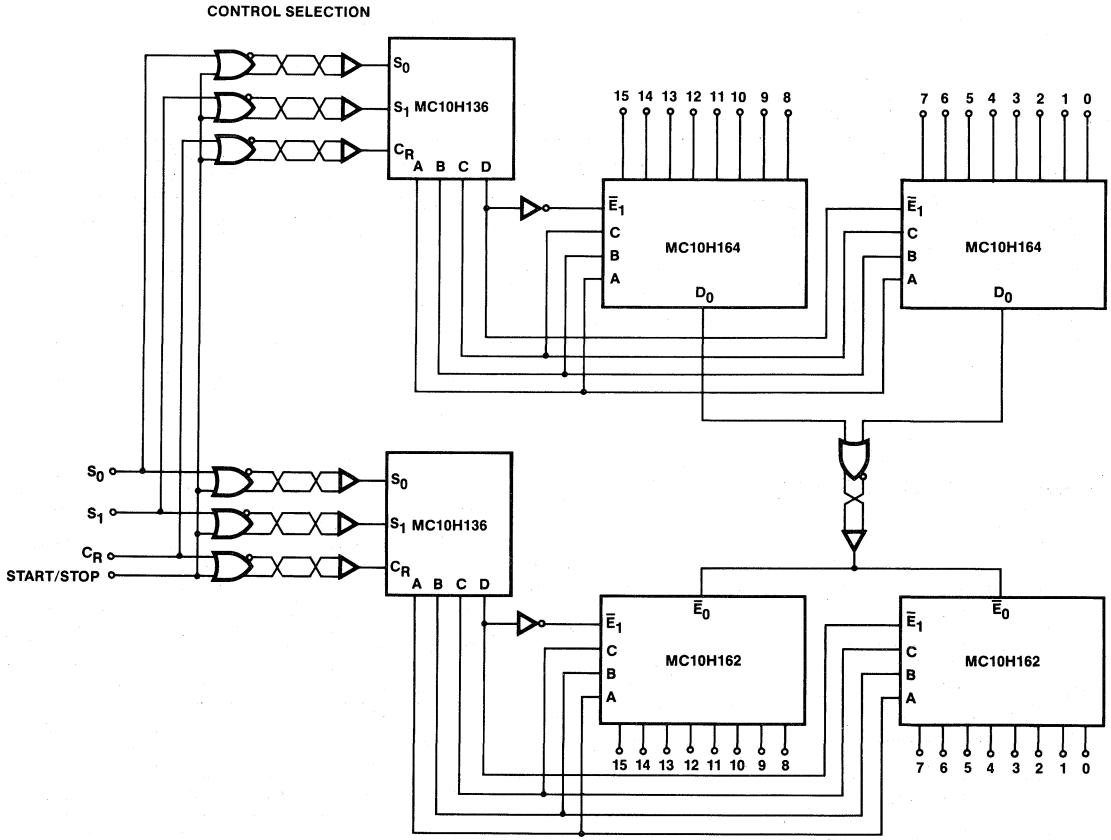


Figure 1. High Speed 16-Bit Multiplexer/Demultiplexer

ECL 10KH High-Speed Emitter-Coupled Logic Family MC10H164 8-Line Multiplexer

Features/Benefits

- Propagation delay, 1 ns typical
- Power dissipation, 310 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Description

The MC10H164 is a member of Monolithic Memories' ECL family. This ECL 10KH part is a functional/pinout duplication of the standard ECL 10K part, with 100% improvement in propagation delay, and no increase in power supply current.

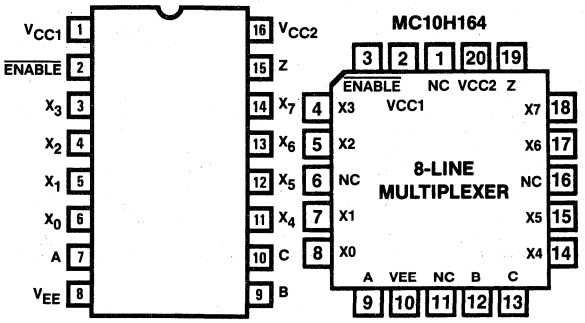
Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H164	J,N,NL(20)	Com

The MC10H164 is designed to be used in data multiplexing and parallel-to-serial conversion applications. Full parallel gating provides equal delays through any data path. The MC10H164 incorporates an output buffer, eight inputs and an enable. A high on the enable forces the output low. The open emitter output allows the MC10H164 to be connected directly to a data bus. The enable line allows an easy means of expanding to more than eight lines using additional MC10H164s.

Pin Configuration

MC10H164
8-Line Multiplexer



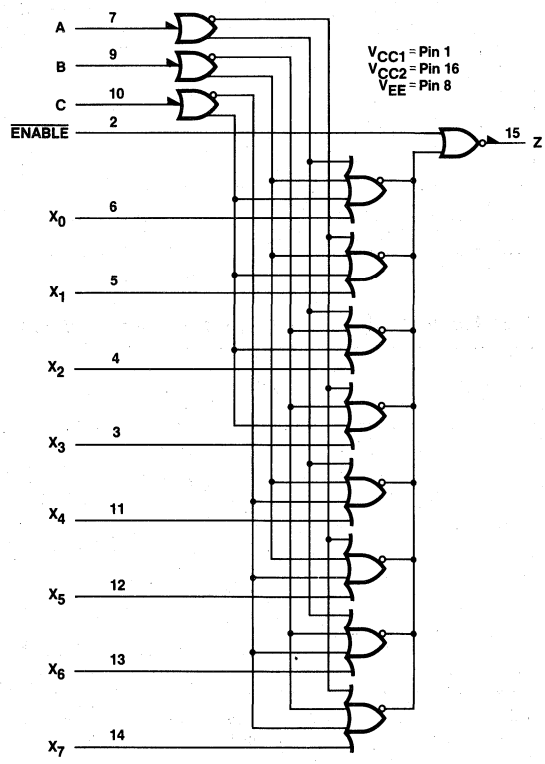
Truth Table

ENABLE	ADDRESS INPUTS			Z
	C	B	A	
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	X	X	X	L

X = Don't Care

Logic Diagram

MC10H164
8-Line Multiplexer



2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories

Absolute Maximum Ratings

Supply voltage V_{EE} (V_{CC} = 0) ..... -8.0 V to 0 V_{dc}
Input Voltage V_I (V_{CC} = 0) ..... 0 V_{dc} to V_{EE}
Output current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		-5.46	-5.2	-4.94	V
T_A	Operating free-air temperature		0		75	°C
T_{STG}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER	0°		25°		75°		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
I_E	Power supply current	—	83	—	75	—	83	mA
I_{inH}	Input current HIGH	—	512	—	320	—	320	μA
I_{inL}	Input current LOW	0.5	—	0.5	—	0.3	—	μA
V_{OH}	HIGH output voltage	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage	-1.95	-1.63	-1.95	-1.63	-0.735	-1.60	Vdc
V_{IH}	HIGH input voltage	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

SYMBOL	PARAMETER		0°		25°		75°		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	X_0-X_7	1.0	2.8	0.7	2.7	0.7	2.9	ns
		A,B,C,	1.0	3.8	0.7	3.6	0.7	3.9	
		Data	0.7	2.4	0.8	2.5	0.9	2.6	
		Address	1.0	2.8	1.1	2.9	1.2	3.2	
		Enable	0.4	1.45	0.4	1.5	0.5	1.7	
t_r,t+	Rise time		0.6	1.8	0.6	1.9	0.6	2.0	ns
t_f,t-	Fall time		0.6	1.8	0.6	1.9	0.6	2.0	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

ECL 10KH High-Speed Emitter Coupled Logic Family
MC10H166
5-Bit Magnitude Comparator

Features/Benefits

- **Propagation delay, Data-to-Output, 2.0 ns typical**
- **Power dissipation, 440 mW typical**
- **Noise margin 150 mV**
- **Voltage compensated**
- **ECL 10K-compatible**

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H166	J,N,NL	Com

Description

The MC10H166 is a member of Monolithic Memories' ECL 10KH family. This device is a 5-Bit Magnitude Comparator and is a functional/pinout duplication of the standard ECL 10K part with 100% improvement in propagation and no increase in power-supply current.

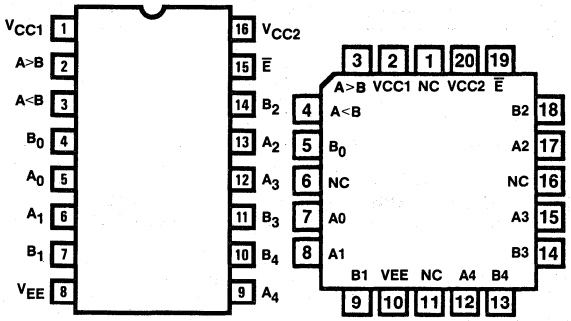
The MC10H166 is a high-speed expandable 5-bit comparator for comparing the magnitude of two binary words. Two outputs are provided: A < B and A > B. The A = B function can be obtained by wire-ORing these outputs (a low level indicates A = B) or by wire-NORing the outputs (a high level indicates A = B). A high level on the enable function forces both outputs low.

Truth Table

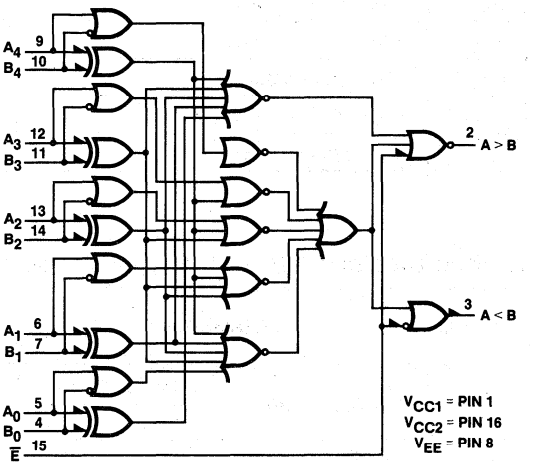
INPUTS			OUTPUTS	
$\overline{E}$	A	B	A < B	A > B
H	X	X	L	L
L	Word A = Word B		L	L
L	Word A > Word B		L	H
L	Word A < Word B		H	L

Pin Configurations

MC10H166
5-Bit Magnitude Comparator



Logic Diagram



14

Portions of this data sheet reproduced with the courtesy of Motorola Inc.

Absolute Maximum Ratings

Supply voltage V_{EE} (V_{CC} = 0) ..... -8.0 V to 0 Vdc
Input voltage V_I (V_{CC} = 0) ..... 0 Vdc to V_{EE}
Output Current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		-5.46	-5.2	-4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER	0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Power supply current	—	117	—	106	—	117	mA
I_{inH}	Input current HIGH	—	350	—	220	—	220	μA
I_{inL}	Input current LOW	0.5	—	0.5	—	0.3	—	μA
V_{OH}	HIGH output voltage	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	V_{dc}
V_{OL}	LOW output voltage	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	V_{dc}
V_{IH}	HIGH input voltage	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	V_{dc}
V_{IL}	LOW input voltage	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	V_{dc}

Switching Characteristics V_{EE} = -5.2V ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
t_{pd}	Propagation delay	Data-to-Output	1.1	3.5	1.1	3.7	1.2	4.1	ns
		Enable-to-Output	0.6	1.7	0.7	1.7	0.7	1.8	
t_r, $t+$	Rise time		0.6	1.5	0.6	1.6	0.6	1.7	ns
t_f, $t-$	Fall time		0.6	1.5	0.6	1.6	0.6	1.7	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-Ω resistor to -2.0 V.

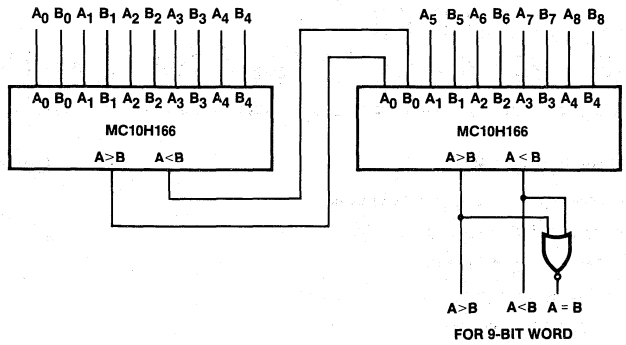


Figure 1. 9-Bit Magnitude Comparator

For longer word lengths, the MC10H166 can be serially expanded or cascaded. Figure 1 shows two devices in a serial expansion for a 9-bit word length. The A>B and A<B outputs are fed to the A_0 and B_0 inputs respectively of the next device. The connection for an A = B output is also shown. The worst case delay time of serial expansion is equal to the number of comparators times the data-to-output delay.

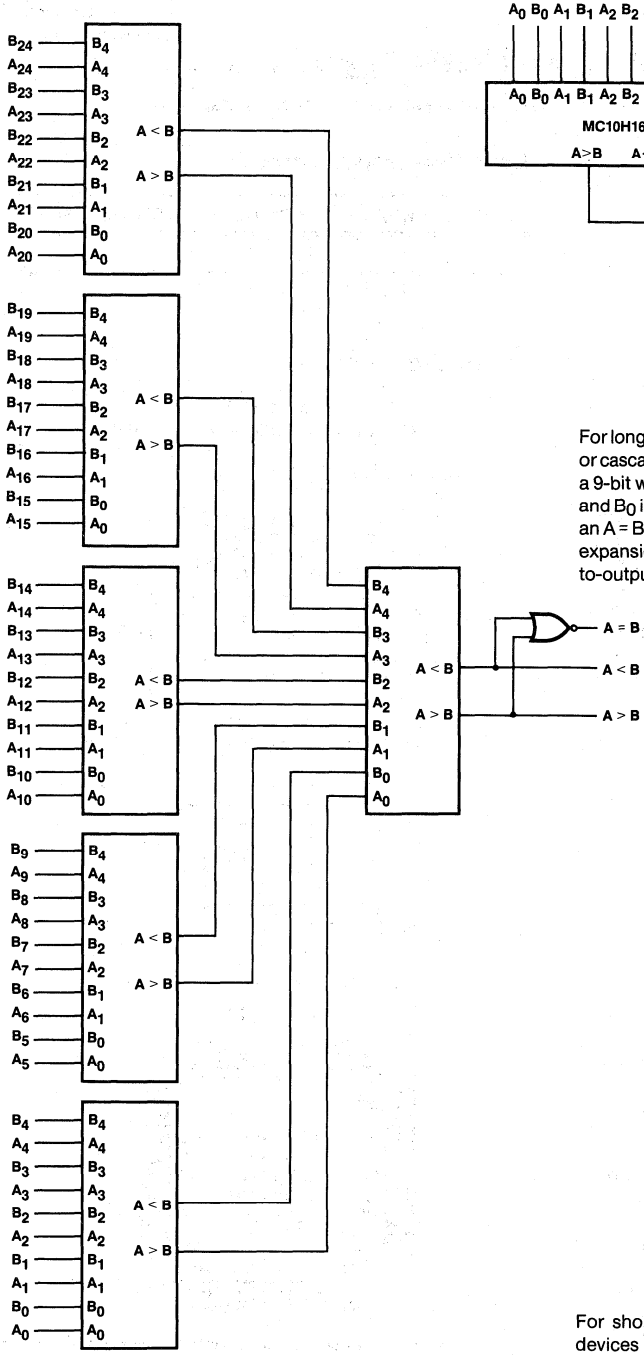


Figure 2. 25-Bit Magnitude Comparator

For shorter delay times than possible with serial expansion, devices can be cascaded. Figure 2 shows a 25-bit cascaded comparator whose worst case delay is two data-to-output delays. The cascaded scheme can be extended to longer word lengths.

ECL 10KH High-Speed Emitter-Coupled Logic Family
MC10H173
QUAD 2-Input Multiplexer With Latch

PRELIMINARY INFORMATION

This document contains specifications and information which are subject to change.

Features/Benefits

- **Propagation delay, 1.5 ns typical**
- **Power dissipation, 275 mW typical**
- **Noise margin 150 mV**
- **Voltage compensated**
- **ECL 10K-compatible**

Description

The MC10H173 is a quad 2-input multiplexer with latch. This device is a functional/pinout duplication of the standard ECL 10K part, with 100% improvement in propagation delay and no increase in power-supply current.

It incorporates common clock and common data select inputs. The select input determines which data input is enabled. A high (H) level enables data inputs D00, D10, D20, and D30 and a low (L) level enables data inputs D01, D11, D21, D31. Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the data outputs.

MC10H173 Function Table

SELECT	CLOCK	$Q_n = 1$
H	L	D00
L	L	D01
X	H	$Q0_n$

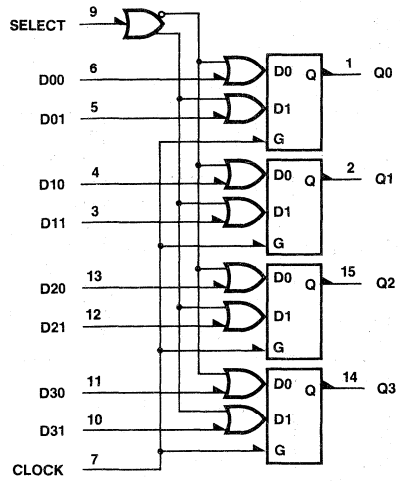
X = Don't care.

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H173	J,N,NL(20)	Com

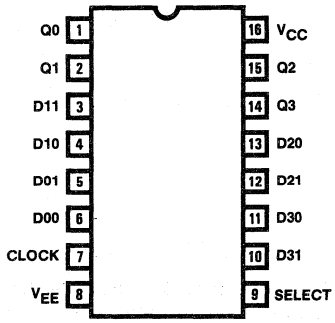
Logic Diagram

MC10H173
Quad 2-Input Multiplexer with Latch

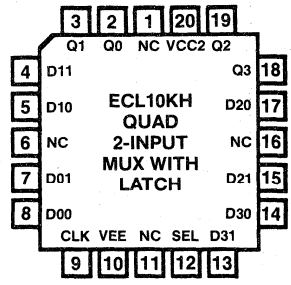


Pin Configurations

MC10H173
Quad 2-Input Multiplexer with Latch



MC10H173



TWX: 910-338-2376
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
Monolithic Memories

Absolute Maximum Ratings

Supply voltage, V_{EE} (V_{CC} = 0) ..... -8.0 to 0 V_{dc}
Input voltage, V_I (V_{CC} = 0) ..... 0 V_{dc} to V_{EE}
Output Current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		-5.46	-5.2	-4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ± 5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Power supply current		—	73	—	66	—	73	mA
I_{inH}	Input current HIGH	Pins 3-7 and 10-13	—	510	—	320	—	320	µA
		Pin 9	—	475	—	300	—	300	
I_{inL}	Input current LOW		0.5	—	0.5	—	0.3	—	µA
V_{OH}	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
t_{pd}	Propagation delay	Data	0.7	2.3	0.7	2.3	0.7	2.3	ns
		Clock	1.0	3.7	1.0	3.7	1.0	3.7	
		Select	1.0	3.6	1.0	3.6	1.0	3.6	
t_{set}	Setup time	Data	0.7	—	0.7	—	0.7	—	ns
		Select	1.0	—	1.0	—	1.0	—	
t_{hold}	Hold time	Data	0.7	—	0.7	—	0.7	—	ns
		Select	1.0	—	1.0	—	1.0	—	
t_r, $t+$	Rise time		0.7	2.4	0.7	2.4	0.7	2.4	ns
t_f, $t-$	Fall time		0.7	2.4	0.7	2.4	0.7	2.4	ns

NOTE: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0 V.

14

ECL 10KH High-Speed Emitter-Coupled Logic Family
MC10H174
Dual 4-to-1 Multiplexer

Features/Benefits

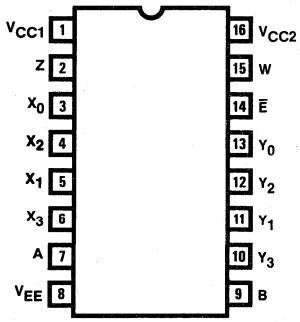
- **Propagation delay 1.5 ns typical**
- **Power dissipation, 305 mW typical**
- **Noise margin 150 mV**
- **Voltage compensated**
- **ECL 10K-compatible**

Description

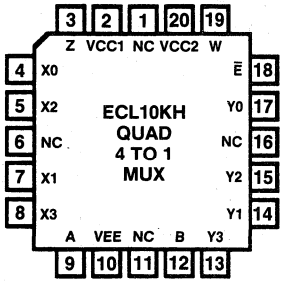
The MC10H174 is a Dual 4-to-1 Multiplexer. This device is a member of Monolithic Memories' new ECL family. This device is a functional/pinout duplication of the standard ECL 10K part with 100% improvement in propagation delay, and no increase in power-supply current.

Pin Configuration

MC10H174
Dual 4-to-1 Multiplexer



MC10H174

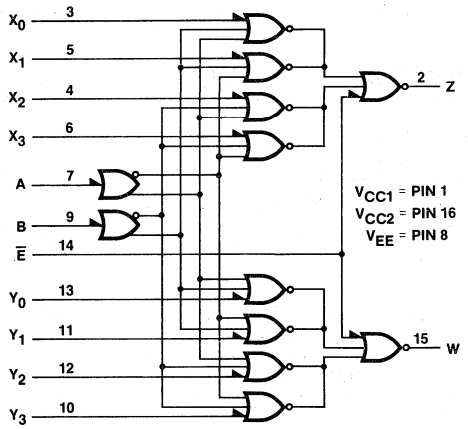


Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H174	J,N,NL(20)	Com

Logic Diagram

MC10H174



Function Table

ENABLE	ADDRESS	INPUTS	OUTPUTS	
$\overline{E}$	B	A	Z	W
H	X	X	L	L
L	L	L	X_0	Y_0
L	L	H	X_1	Y_1
L	H	L	X_2	Y_2
L	H	H	X_3	Y_3

X = Don't care.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374
Monolithic Memories

Absolute Maximum Ratings

Supply voltage V_{EE} (V_{CC} = 0) ..... -8.0 V to 0 Vdc
Input voltage V_I (V_{CC} = 0) ..... 0 Vdc to V_{EE}
Output Current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		-5.46	-5.2	-4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Power supply current		—	80	—	73	—	80	mA
I_{inH}	Input current HIGH	Pins 3 - 7 and 9 - 13	—	475	—	300	—	300	µA
		Pin 14	—	670	—	420	—	420	
I_{inL}	Input current LOW		0.5	—	0.5	—	0.3	—	µA
V_{OH}	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
t_{pd}	Propagation delay	Data (All others)	0.7	2.4	0.8	2.3	0.9	2.6	ns
		Select (A,B) Pin 7, 9	1.0	2.8	1.1	2.9	1.2	3.2	
		Enable Pin 14	0.4	1.45	0.4	1.50	0.5	1.70	
t_r, t+	Rise time		0.5	1.5	0.5	1.6	0.5	1.70	ns
t_f, t-	Fall time		0.5	1.5	0.5	1.6	0.5	1.70	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0 V.

14

ECL 10KH High-Speed Emitter-Coupled Logic Family
MC10H175
Quint Latch

Features/Benefits

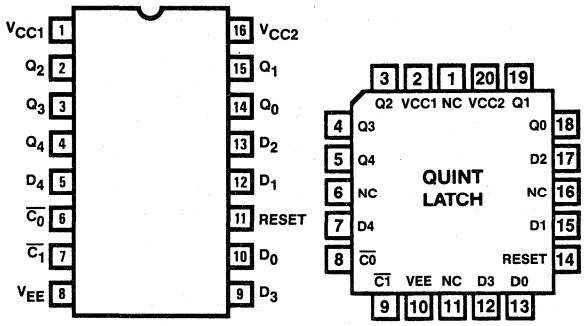
- Propagation delay, 1.2 ns typical
- Power dissipation, 400 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Description

The MC10H175 is a member of Monolithic Memories' ECL family. The MC10H175 is a quint D-type latch with common reset and clock lines. This ECL 10KH part is a functional/pinout duplication of the standard ECL 10K part, with 100% improvement in propagation delay, and no increase in power-supply current.

Pin Configuration

MC10H175
Quint Latch



Truth Table

D	C_0	C_1	RESET	Q_{n+1}
L	L	L	X	L
H	L	L	X	H
X	H	X	L	Q_n
X	X	H	L	Q_n
X	H	X	H	L
X	X	H	H	L

X = Don't Care

Portions of this Data Sheet reproduced with courtesy of Motorola Inc.

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H175	J,N,NL(20)	Com

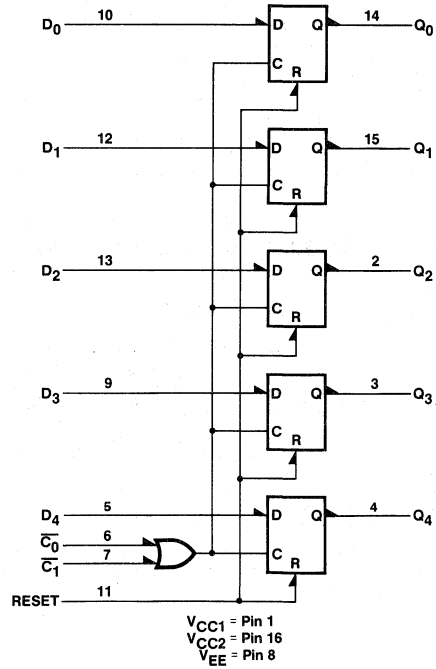
Application Information

The MC10H175 is a high-speed, low-power quint latch. It features five D-type latches with common reset and a common two-input clock. Data is transferred on the negative edge of the clock and latched on the positive edge. The two clock inputs are ORed together.

Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information. The reset input is enabled only when the clock is in the high state.

Logic Diagram

MC10H175
Quint Latch



Absolute Maximum Ratings

Supply Voltage V_{EE} (V_{CC} = 0) ..... -8.0 V to 0 V_{dc}
Input Voltage V_I (V_{CC} = 0) ..... 0 V_{dc} to V_{EE}
Output Current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		-5.46	-5.2	-4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	CHARACTERISTIC		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Power supply current		—	107	—	97	—	107	mA
I_{inH}	Input current HIGH	Pins 5,6,7,9,10,12,13	—	565	—	335	—	335	µA
		Pin 11	—	1120	—	660	—	660	
I_{inL}	Input current LOW		0.5	—	0.5	—	0.3	—	µA
V_{OH}	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

14

Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
t_{pd}	Propagation delay	Data	0.6	1.6	0.6	1.6	0.6	1.7	ns
		Clock	0.7	1.9	0.7	2.0	0.8	2.1	
		Reset	1.0	2.2	1.0	2.3	1.0	2.4	
t_{set}	Setup time		1.5	—	1.5	—	1.5	—	ns
t_{hold}	Hold time		0.8	—	0.8	—	0.8	—	ns
t_r, t+	Rise time		0.5	1.8	0.5	1.9	0.5	2.0	ns
t_f, t-	Fall time		0.5	1.8	0.5	1.9	0.5	2.0	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

ECL 10KH High-Speed Emitter Coupled Logic Family
MC10H176
Hex D Master-Slave Flip-Flop

Features/Benefits

- **Propagation delay 1.7 ns typical**
- **Power dissipation, 460 mW typical**
- **Noise margin 150 mV**
- **Voltage compensated**
- **ECL 10K-compatible**

Description

The MC10H176 is a member of Monolithic Memories' ECL 10KH family. This ECL device includes six high speed master-slave D-type flip-flops with one common input clock for all six. Data enters into the master during the LOW state of the clock and is transferred to the slave during the positive-going clock transition. Thus, outputs may change only on a positive-going Clock transition. A change in information present at the data (D) input will not affect the output information any other time due to the master-slave construction of this device.

This ECL 10KH part is a functional/pinout duplication of the standard ECL 10K part, with 100% improvement in clock frequency and propagation delay and no increase in power-supply current.

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H176	J,N,NL(20)	Com

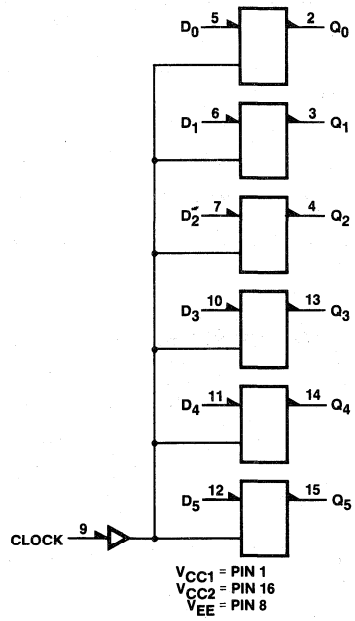
Truth Table

C	D	Q_{n+1}
L	X	Q_n
H*	L	L
H*	H	H

X = Don't Care
* A clock H is a clock transition from a low to a high state

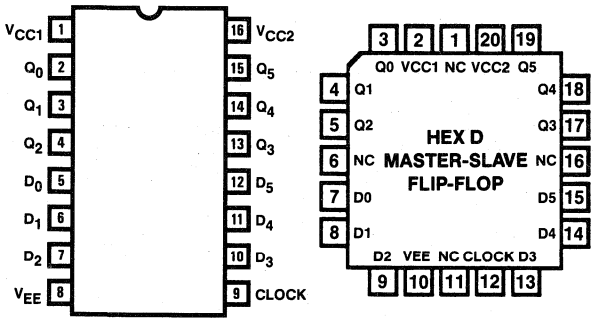
Logic Diagram

MC20H176
Hex D Master-Slave Flip-Flop



Pin Configurations

MC10H176
Hex D Master-Slave Flip-Flop



Portions of this Data Sheet reproduced with the courtesy of Motorola Inc.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374
Monolithic Memories

Absolute Maximum Ratings

Supply voltage V_{EE} (V_{CC} = 0) ..... -8.0 V to 0 Vdc
Input voltage V_I (V_{CC} = 0) ..... 0 Vdc to V_{EE}
Output Current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		-5.46	-5.2	-4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Power supply current		—	123	—	112	—	123	mA
I_{inH}	Input current HIGH	Pins 5,6,7,10,11,12	—	425	—	265	—	265	μA
		Pin 9	—	670	—	420	—	420	
I_{inL}	Input current LOW		0.5	—	0.5	—	0.3	—	μA
V_{OH}	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	V_{dc}
V_{OL}	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	V_{dc}
V_{IH}	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	V_{dc}
V_{IL}	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	V_{dc}

Switching Characteristics V_{EE} = -5.2V ±5% (See Note)

SYMBOL	PARAMETER	0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
t_{pd}	Propagation delay	0.9	2.1	0.9	2.2	1.0	2.4	ns
t_{set}	Setup time	1.5	—	1.5	—	1.5	—	ns
t_{hold}	Hold time	0.9	—	0.9	—	0.9	—	ns
t_r, $t+$	Rise time	0.5	1.8	0.5	1.9	0.5	2.0	ns
t_f, $t-$	Fall time	0.5	1.8	0.5	1.9	0.5	2.0	ns
f_{tog}	Toggle frequency	250	—	250	—	250	—	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

14

ECL 10KH High-Speed Emitter-Coupled Logic Family
MC10H179
Look-Ahead Carry Block

Features/Benefits

- Propagation delay, 1 ns typical
- Power dissipation, 300 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

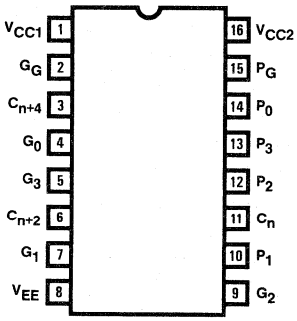
Description

The MC10H179 is a Look-Ahead Carry Block. This device is a member of Monolithic Memories' ECL 10KH family.

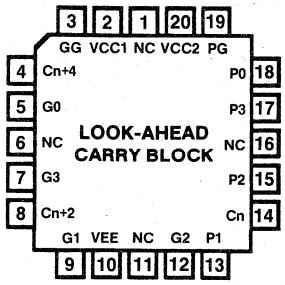
This ECL 10KH part is a functional/pinout duplication of the standard ECL 10K part with 100% improvement in propagation delay, and no increase in power-supply current.

Pin Configuration

MC10H179
Look-Ahead Carry Block



MC10H179

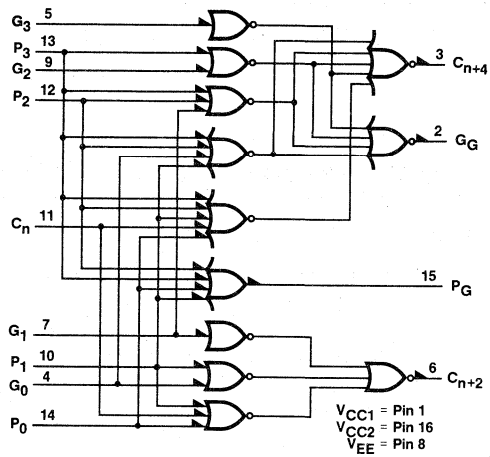


Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H179	J,N,NL(20)	Com

Logic Diagram

MC10H179
Look-Ahead Carry Block



$P_G = P0 + P1 + P2 + P3$
$G_G = (G0 + P1 + P2 + P3)(G1 + P2 + P3)(G2 + P3)\,G3$
$C_{n+2} = (C_n + P0 + P1)(G0 + P1)\,G1$
$C_{n+4} = (C_n + P0 + P1 + P2 + P3)(G0 + P1 + P2 + P3)(G1 + P2 + P3)(G2 + P3)\,G3$

Application

The MC10H179 is a high-speed, low-power, standard ECL complex function that is designed to perform the look-ahead carry function. This device can be used with the MC10H181 4-bit ALU directly, or with the MC10H180 dual arithmetic unit in any computer, instrumentation or digital communication application requiring high-speed arithmetic operation on long words.

When used with the MC10H181, the MC10H179 performs a second order or higher look-ahead. Figure 2 shows a 16-bit look-ahead carry arithmetic unit. Second order carry is valuable for longer binary words. As an example, addition of two 32-bit words is improved from 30 nanoseconds with ripple-carry techniques. A block diagram of a 32-bit ALU is shown in Figure 1. The MC10H179 may also be used in many other applications. It can, for example, reduce system package count when used to generate functions of several variables.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories MMI

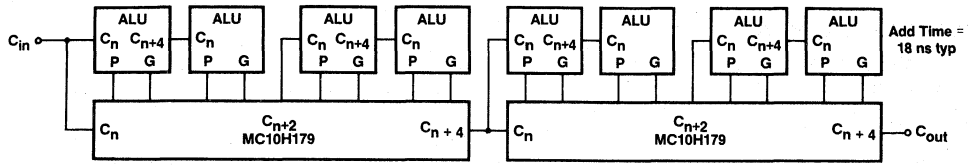


Figure 1. 32-Bit ALU with Carry Look-Ahead

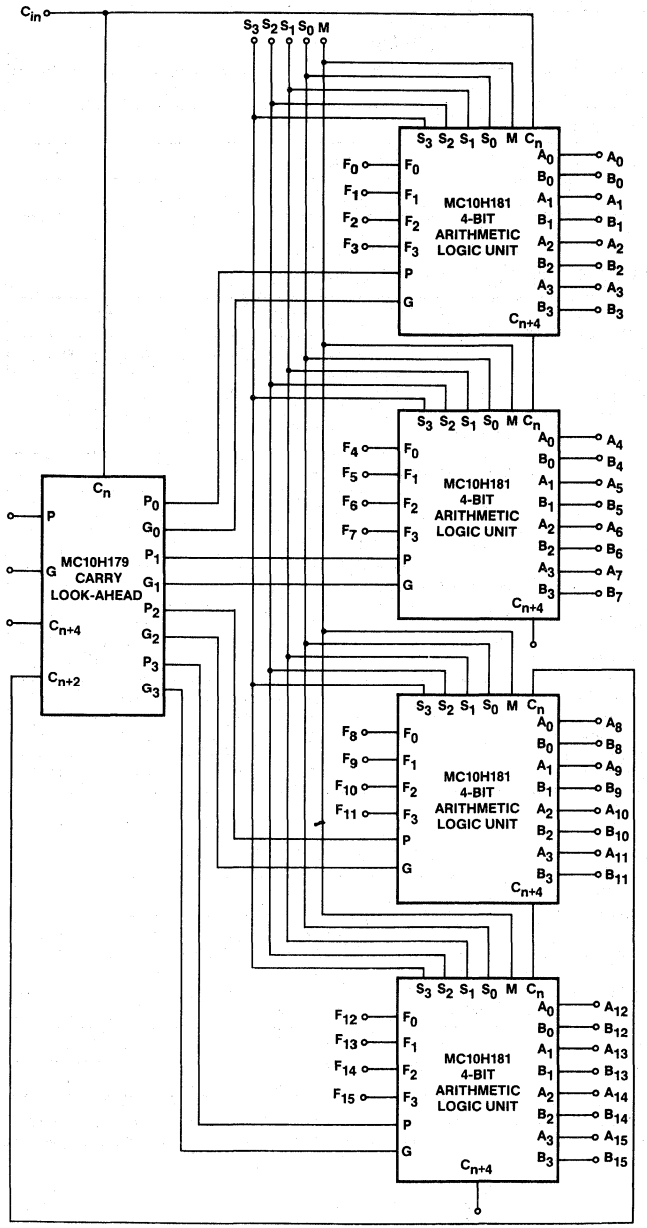


Figure 2. 16-Bit Full Look-Ahead Carry Arithmetic Logic Unit

Absolute Maximum Ratings

Supply voltage V_{EE} (V_{CC} = 0) ..... -8.0 V to 0 Vdc
Input voltage V_I (V_{CC} = 0) ..... 0 Vdc to V_{EE}
Output Current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		-5.46	-5.2	-4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Power supply current		—	79	—	72	—	79	mA
I_{inH}	Input current HIGH	Pins 5 and 9	—	465	—	275	—	275	µA
		Pins 4, 7 and 11	—	545	—	320	—	320	
		Pin 14	—	705	—	415	—	415	
		Pin 12	—	790	—	465	—	465	
		Pins 10 and 13	—	870	—	510	—	510	
I_{inL}	Input current LOW		0.5	—	0.5	—	0.3	—	µA
V_{OH}	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	V_{dc}
V_{OL}	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	V_{dc}
V_{IH}	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	V_{dc}
V_{IL}	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	V_{dc}

Switching Characteristics V_{EE} = -5.2V ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
t_{pd}	Propagation delay	P to PG	0.40	1.40	0.40	1.50	0.50	1.70	ns
		G, P, Cn to Cn or GG	0.60	2.30	0.70	2.40	0.80	2.60	
t_r, t+	Rise time		0.5	1.7	0.5	1.8	0.5	1.9	ns
t_f, t-	Fall time		0.5	1.7	0.5	1.8	0.5	1.9	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

ECL 10KH High Speed Emitter Coupled Logic Family
MC10H209
Dual 4-5 Input OR/NOR Gate

Features/Benefits

- Propagation delay, 0.75 ns typical
- 125 mW typical (no load)
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Ordering Information

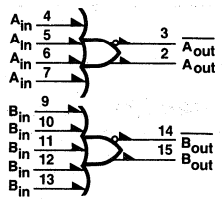
PART NUMBER	PACKAGE	TEMPERATURE
MC10H209	J,N,NL	Com

Description

The MC10H209 is a member of the Monolithic Memories' ECL 10KH Family. This ECL device is a dual 4-5 input OR/NOR gate. This device is a functional/pinout duplication of the standard ECL 10K family part, with 100% improvement in propagation delay and no increase in power supply current.

Logic Diagram

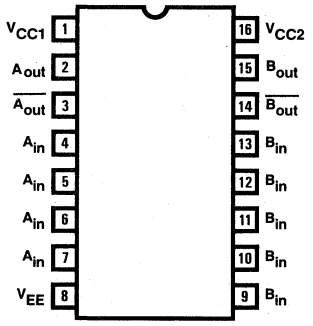
MC10H209
Dual 4-5 Input OR/NOR Gate



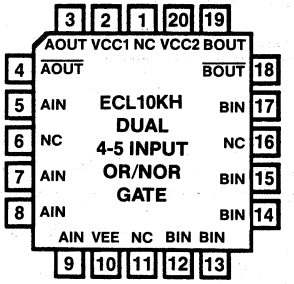
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

Pin Configuration

MC10H209
Dual 4-5 Input OR/NOR Gate



MC10H209



14

Portions of this data sheet reproduced with the courtesy of Motorola Inc.

Absolute Maximum Ratings

Supply voltage V_{EE} (V_{CC} = 0) ..... −8.0 V to 0 V_{dc}
Input voltage V_I (V_{CC} = 0) ..... 0 V_{dc} to V_{EE}
Output current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		-5.46	-5.20	-4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER	0°		25°		75°		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
I_E	Power supply current	—	—	—	30	—	—	mA
I_{inH}	Input current HIGH	—	640	—	400	—	400	µA
I_{inL}	Input current LOW	0.5	—	0.5	—	0.3	—	µA
V_{OH}	HIGH output voltage	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER	0°		25°		75°		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	0.4	1.15	0.4	1.15	0.7	1.15	ns
t_r	Rise time	0.4	1.5	0.4	1.5	0.4	1.6	ns
t_f	Fall time	0.4	1.5	0.4	1.5	0.4	1.6	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-Ω resistor to -2.0 V.

ECL 10 KH High-Speed Emitter-Coupled Logic Family MC10H210/MC10H211 3-Input, 3-Output OR/NOR Gates

Features/Benefits

- Propagation delay, 1.0 ns typical
- Power dissipation, 160 mW typical
- Noise margin 150 mV (over operating voltage and temperature range)
- Voltage compensated
- ECL 10K-compatible

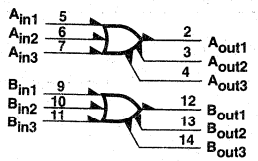
Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H210 MC10H211	J,N,NL,(20)	Com

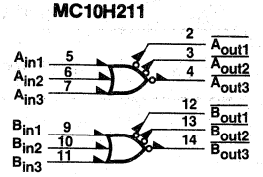
Description

The MC10H210 and MC10H211 are members of Monolithic Memories' ECL family. These devices are dual 3-input, 3-output "OR" and "NOR" gates respectively. These ECL 10KH parts are functional/pinout duplications of the standard ECL 10KH family parts, with 100% improvement in propagation delay and no increase in power supply current.

MC10H210



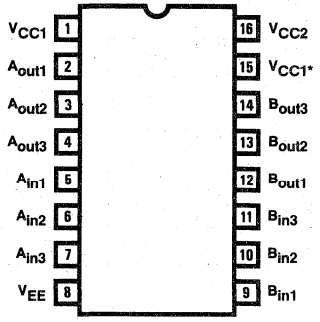
MC10H211



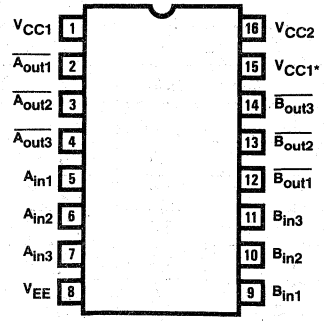
V_{CC1} = PIN 1, 15*
V_{CC2} = PIN 16
V_{EE} = PIN 8

Pin Configurations

MC10H210
3-INPUT 3-OUTPUT OR GATE

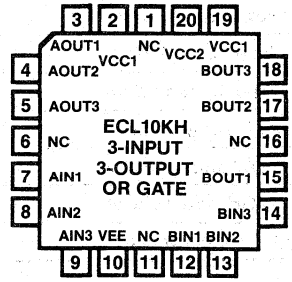


MC10H211
3-INPUT 3-OUTPUT NOR GATE

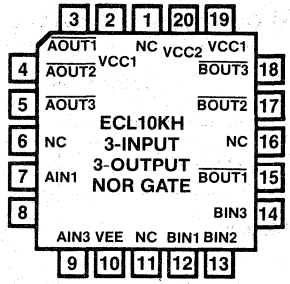


* Pins 1 and 15 internally connected

MC10H210



MC10H211



2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374
Monolithic Memories MMI

Absolute Maximum Ratings

Supply voltage, V_{EE} (V_{CC} = 0) ..... -8.0 V to 0 V_{dc}
Input voltage, V_I (V_{CC} = 0) ..... 0 V_{dc} to V_{EE}
Output Current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		-5.46	-5.2	-4.94	V
T_A	Operating free-air temperature		0		75	°C
T_{STG}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

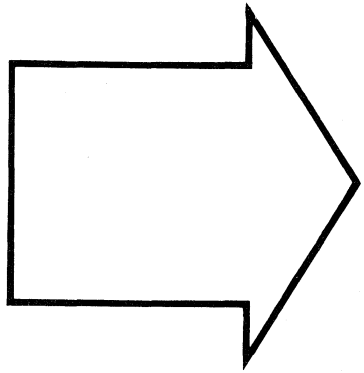
Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER	0°		25°		75°		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
I_E	Power supply current	—	42	—	38	—	42	mA
I_{inH}	Input current HIGH	—	720	—	450	—	450	μA
I_{inL}	Input current LOW	0.5	—	0.5	—	0.3	—	μA
V_{OH}	HIGH output voltage	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2V ±5% (See Note)

SYMBOL	PARAMETER		0°		25°		75°		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	MC10H210	0.5	1.55	0.55	1.55	0.6	1.7	ns
		MC10H211	0.7	1.6	0.7	1.6	0.7	1.7	
t_r, $t+$	Rise time	MC10H210	0.75	1.8	0.75	1.9	0.8	2.0	ns
		MC10H211	0.9	2.0	0.9	2.2	0.9	2.4	
t_f, $t-$	Fall time	MC10H210	0.75	1.8	0.75	1.9	0.8	2.0	ns
		MC10H211	0.9	2.0	0.9	2.2	0.9	2.4	

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.



LOGIC CELL ARRAY

Logic Cell Array™

Introduction

The Logic Cell Array (LCA)™ is a CMOS integrated circuit with a flexible, uncommitted architecture and VLSI-level density. The LCA is manufactured on Monolithic Memories' 1.6 micron CMOS process. The device architecture as is shown in Figure 1, similar to that of a gate array, with an interior matrix of programmable logic blocks, a surrounding ring of I/O interface blocks and programmable interconnect used to define the overall device structure.

Unlike gate arrays, Logic Cell Array functionality is defined by the user simply by loading the internal writable storage cells with the configuration data. An additional benefit, reprogrammability in system, allows in-circuit-emulation to be used for design verification.

The M2064 family of Logic Cell Arrays has been developed to allow Monolithic Memories to offer a device and technology that offer both the density benefits of gate arrays and the programmability benefits of user-configurable devices. These parts have been designed for maximum flexibility in system applications and are easy to use.

Using the XACT™ software development system, the designer can define and interconnect logic blocks to build larger-scale, multi-level logic functions. These are then connected to external circuitry. Interconnections throughout the Array are defined automatically by the development system, unless otherwise specified by the designer. Because the Logic Cell Array's logic functions and interconnections are established with memory cells, the array is never physically altered; instead it is simply reprogrammed.

XACT Evaluation Kit (LCA-MEK01)

Monolithic Memories offers evaluation software and documentation that will allow a designer to determine if his or her logic design fits and assess its performance as a Logic Cell Array. All that is needed is an IBM PC-XT, AT, or compatible, a three-button Mouse System or compatible mouse.

XACT Development System (LCA-MDS21)

The XACT Development System is the "power behind the machine." It will allow a designer to sit down with a concept and walk away with a completely tested, completely finished part.

The reason is that XACT functions as both a CAE and CAM system. The CAE part of the system allows the designer to simply draw out the design using a sophisticated graphics-based design editor. The CAM part then converts the drawing to code, similar to a PALASM-generated JEDEC file, that allows-programming with conventional programming hardware of an EPSOM containing the configuration data for system prototyping.

The XACT Development System currently has 113 macros and, in addition, allows the user to define his or her own macro. To insure that internal timing constraints are satisfied, a Timing Analyzer is included to calculate propagation delays along any path within the Array.

As the design is being entered, the Automatic Design Checker insures that no design rules are violated, and when the design is completed, a final design rule check is performed.

The XACT Development System

Contents:

- Editor
- Macro Library
- Design Checker
- Timing Analyzer
- Simulator
- Configuration File Generator
- Configuration File Formatter

In-Circuit-Emulator (LCA-MDS24)

The In-Circuit-Emulator is a software/hardware package that enables a designer to connect his or her target system to the workstation where a design has just been completed. The emulator package allows:

- User control and monitoring of device function
- Interactive or file-driven setup and configuration
- Daisy-chain configuration capabilities for up to seven LCAs in a chain
- Simultaneous in-circuit emulation of up to four devices
- Single step capability for device clocks
- Readback display of device internal register states
- Dynamic reconfiguration capability.

The In-Circuit-Emulator comes with a single "pod". Up to three additional pods (LCA-MDS25) may be ordered for each emulator.

P-SILOS Simulation Package (LCA-MDS22)

After a design is completed, the next step is to simulate. Monolithic Memories offers an integrated simulation package manufactured by Simucad, called P-SILOS.

PART NUMBER	DESCRIPTION
LCA-MEK01	LCA Evaluation Kit
LCA-MDS21	LCA Development system
LCA-MDS22	LCA Simulator - P-SILOS
LCA-MDS24	LCA In-Circuit-Emulator
LCA-MDS25	LCA In-Circuit-Emulator Pod
LCA-MTB01	LCA Demonstration Board

Table 1

The introduction of the Logic Cell Array will allow customers to reduce inventories of discrete components, reduce the time to market and development cost for new products, save money in manufacturing and spare parts inventory management, reduce test costs and improve system reliability.

Configurable Logic Block

The core of the Logic Cell Array is an 8x8 matrix of Configurable Logic Blocks. Each CLB provides four logic inputs, a clock input, a combinatorial logic section, two logic outputs, and a programmable storage element.

The inputs drive a combinatorial logic section that can perform any logic function from a simple gate to a three-out-of-four majority decoder.

The combinatorial portion accepts and generates both positive- and negative-true logic, eliminating the need for inverters or the routing of complementary signals.

The storage element can serve as a flip-flop (D-type) and can be programmed to have clock enable, synchronous set and reset, and various gated inputs. In addition, since all these options can be specified independently for each logic block, designers can mix asynchronous and synchronous logic in any combination.

Interconnect

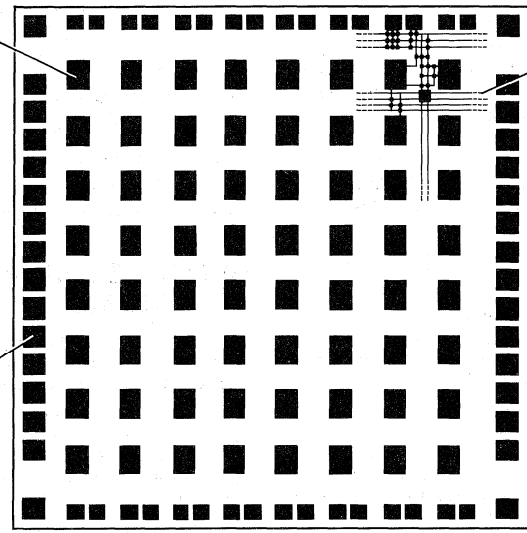
The Array's extraordinary flexibility is also the result of a two-layer metal network of lines that run horizontally and vertically between the logic and I/O blocks, and a variety of user-definable interconnection elements.

Definable interconnection points connect the inputs and outputs of logic and I/O blocks to nearby metal lines.

Crosspoint switches and interchanges are clustered at the intersection of every row and column of logic blocks. They link horizontal and vertical paths and allow signals to be switched from one path to another.

Finally, "long lines" run the length and breadth of the chip, bypassing interchanges but tying into logic blocks and other lines and distributing clocks and other critical signals with a minimum of propagation delay.

Interchanges and interconnection point assignments, as well as all routing are handled automatically by the XACT Development System Software. In addition, special graphics-based design tools are included to facilitate any necessary designer interaction.



Configurable I/O Block

External signals enter and leave the chip through general-purpose, user-definable I/O blocks positioned around the periphery of the array. Each block can be programmed independently to be an input, output or bidirectional pin with a tristate control on the output. When configured as an input, the designer can select TTL or CMOS thresholds. In addition, each I/O bloc contains an input register option whose clock line is common to all the other I/O blocks along the same edge of the die.

I/O blocks can also handle more than input and output functions. For example, the Input registers of unused I/O blocks can be used for read/write storage registers or as stages of a shift register.

Figure 1

Logic Cell Array™ M2064

Features/Benefits

- **CMOS programmable Logic Cell Array (LCA™) for replacement of standard logic**
- **Completely reconfigurable by the user in the final system**
- **High performance**
  —20 MHz flip-flop toggle rate (-20 speed grade)
  —33 MHz flip-flop toggle rate (-33 speed grade)
  —50 MHz flip-flop toggle rate (-50 speed grade)
- **User-configurable logic functions, interconnect and I/O for maximum flexibility**
- **64 user-Configurable Logic Blocks (CLBs) providing usable gate equivalency of up to 1500 gates**
- **58 individually-configurable I/O pins allowing any mix of inputs, outputs or bidirectional signals (68-pin package)**
- **User-selectable TTL or HCMOS input threshold levels**
- **Multiple configuration modes for greatest flexibility and ease of use**
- **Verification feature allows user to check configuration data**
- **User-selectable security feature prevents read-back of configuration data**
- **Read-back of internal register states for system debug**
- **On-chip clock oscillator and clock buffer circuits provide flexible internal and external clocking functions**
- **Master reset of all internal register elements in addition to user-configurable Reset and/or Set control of individual CLB storage elements**

General Description

The M2064 is the first member of a family of configurable Logic Cell Arrays (LCAs) available from Monolithic Memories. These general purpose CMOS integrated circuit devices allow the user to rapidly implement complex digital logic functions directly without the requirement for masking or other vendor performed programming steps. Unique configuration circuitry allows complete reconfiguration within a user's final system to allow system changes "on-the-fly."

User configuration is controlled by internal storage elements. These are loaded with data bits which control definition of logic functions, configuration of I/O blocks, routing of internal signals, and other options: Configuration data can be loaded in one of several methods to minimize impact on overall system design.

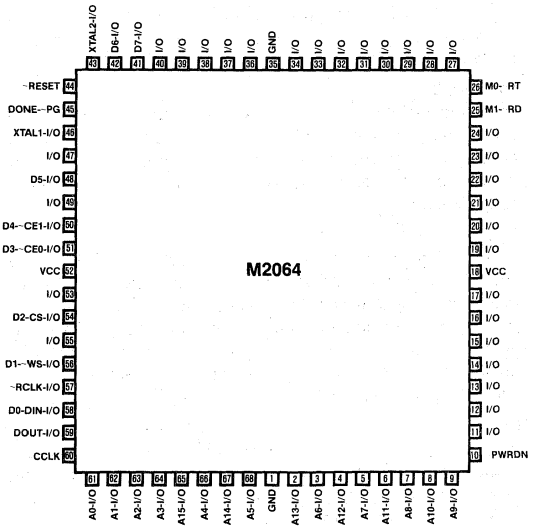
CMOS technology optimized for system level performance provides LS-TTL compatible speeds with power consumption less than 10% of equivalent TTL systems. The use of innovative I/O buffers providing either TTL or CMOS input switching levels insures lowest possible power consumption in totally CMOS systems without any compromise in performance.

Ordering Information

M2064-20 CNL

- PART NUMBER
- SPEED GRADE
  - -20 = 20 MHz toggle rate
  - -33 = 33 MHz toggle rate
  - -50 = 50 MHz toggle rate
- PACKAGE TYPE
  - NL = 68 Pin Molded Chip Carrier
  - P = 68 Pin Grid Array
  - N = 48 Pin Molded Dip
- TEMPERATURE RANGE
  - C = Commercial

PART NUMBER	DESCRIPTION
LCA-MDS21	XACT Development System
LCA-MDS22	P-SILOS Simulation Package
LCA-MDS24	LCA In-Circuit Emulator
LCA-MDS25	In-Circuit Emulator Pod
LCA-MEK01	XACT Evaluation Kit



Portions of this Data Sheet reproduced with the permission of XILINX Inc.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374
Monolithic Memories MMI

Pin Description

I/O
User-configurable Input/Output pins.

~PWRDN
Input forces device into low power mode; operation is suspended.

M0-~RT
Dual function input. During initial power up, the state of M0 and M1 determines the configuration mode. After configuration, a rising edge on ~RT initiates a configuration read operation.

M1-~RD
Dual function input/output. During initial power up, the state of M1 and M0 determines the configuration mode. After configuration is complete, ~RD outputs configuration data during a configuration read back operation synchronously with the toggling of the CCLK input.

~RESET
Input. A low level on this input after configuration causes all register elements internal to the LCA to be forced to 0. If asserted prior to the start of configuration, causes the LCA to remain in the initialization state (configuration is not started). If asserted during configuration the LCA returns to the initialization state.

DONE-~PG
Dual function output/input. During configuration the LCA pulls DONE low and releases it when configuration is complete (output is open drain). After configuration is complete, a falling edge on ~PG initiates an LCA programming cycle (if enabled in the current configuration). This pin has an internal user-enabled pull-up resistor.

XTAL1-I/O
Dual function input and I/O. This pin may be configured by the user to be a normal I/O pin equivalent to any of the general purpose I/O pins. Alternatively, this pin and XTAL2 may be used to connect a crystal for use with the internal crystal oscillator configuration.

XTAL2-I/O
Dual function output and I/O. This pin may be configured by the user to be a normal I/O pin equivalent to any of the general purpose I/O pins. Alternatively, this pin and XTAL1 may be used to connect a crystal for use with the internal crystal oscillator configuration.

CCLK
Configuration mode dependent input/output. CCLK is the master configuration clock used to configure the LCA. In slave mode it is an input; in all other modes it is an output designed to provide the input clocking of additional slave mode daisy chain connected LCA devices. During a configuration read back operation, CCLK serves as the clock input used to read the internal configuration data.

DOUT-I/O
Dual function output and I/O. General purpose user-configurable I/O pin during normal operation. During configuration, the serial data stream supplied from the first LCA to LCAs down the serial daisy chain is output on DOUT.

~RCLK-I/O
Dual function output and I/O. General purpose user-configurable I/O pin during normal operation. During master mode configuration, a low level output on ~RCLK indicates that the external memory device is being accessed.

D0-DIN-I/O
Multi-function input and I/O. General purpose user-configurable I/O pin during normal operation. During master mode configuration, this pin is bit 0 of the 8-bit parallel input data bus (D0). During slave mode or peripheral mode configuration, this pin is the serial input data pin (DIN).

D1-~WS-I/O
Multi-function input and I/O. General purpose user-configurable I/O pin during normal operation. During master mode configuration, this pin is bit 1 of the 8-bit parallel input data bus (D1). During peripheral mode configuration, a low level on ~WS indicates that a write operation is being performed by the controlling processor. See note.

D2-CS-I/O
Multi-function input and I/O. General purpose user-configurable I/O pin during normal operation. During master mode configuration, this pin is bit 2 of the 8-bit parallel input data bus (D2). During peripheral mode configuration, a high level on CS indicates that a write operation is being performed by the controlling processor. See note.

D3-~CE0-I/O
Multi-function input and I/O. General purpose user-configurable I/O pin during normal operation. During master mode configuration, this pin is bit 3 of the 8-bit parallel input data bus (D3). During peripheral mode configuration, a low level on ~CE0 indicates that a write operation is being performed by the controlling processor. See note.

D4-~CE1-I/O
Multi-function input and I/O. General purpose user-configurable I/O pin during normal operation. During master mode configuration, this pin is bit 4 of the 8-bit parallel input data bus (D4). During peripheral mode configuration, a low level on ~CE1 indicates that a write operation is being performed by the controlling processor. See note.

D5-I/O to D7-I/O
Input and I/O. General purpose user-configurable I/O pins during normal operation. During master mode configuration, these pins are bits 5 through 7 of the 8-bit parallel input data bus (D5-D7).

A0-I/O to A15-I/O
Output and I/O. General purpose user-configurable I/O pins during normal operation. During master mode configuration these pins are address output pins (A0-A15) used to address the external storage element used for configuration data.

Note: to perform a peripheral mode write, the following logical combination is necessary: ~WS · CS · ~CE0 · ~CE1.

Functional Description

The M2064 is a high-performance CMOS Logic Cell Array providing superior system performance with greatest user flexibility. Complete user-configurability provides an optimized solution to logic implementation problems.

The M2064 utilizes a unique Configurable Logic Block (CLB) structure as the basic functional building block of the device. Each CLB is a combination of a programmable logic function and a storage element. The CLB has the capability of performing any function of its inputs with the option of the output of the storage element included in the input field. User-defined logic is implemented in a matrix of sixty-four CLBs which are interconnected with user-configurable interconnect resources.

Fifty-eight independently configurable I/O Blocks; each of which can be a direct or latched input, a direct or open drain output, or a bidirectional I/O buffer; provide the interface to external circuits. Input voltage levels are user definable and may be either standard TTL or CMOS for all I/O Blocks, depending on the user's configuration choice.

User-definable path selector or multiplexers are utilized to select configuration options for the CLBs and I/O Blocks. These selectors are set in the desired state by the configuration data loaded into the device upon power up.

Logic

User logic is implemented in one or more CLBs which are general purpose 4-input, 2-output elements. Figure 1 shows a block diagram of a single CLB. Each element is composed of a 4-input combinational logic module with two outputs, a general purpose storage element, and routing selection logic. The module can generate any combinational logic function of the four inputs, or it can generate any two independent functions of any three of the four inputs. If a function of four inputs is selected, that same function will be available on both of the outputs of the combinational module. The inputs to the combinational module are three of the four inputs to the CLB (A, B and C) and either the D input to the CLB, or the Q output of the storage element.

The general purpose storage element has a data input, a clock input, a set direct input, a reset direct input and an output, Q. The storage characteristic may be defined as either a transparent latch or as an edge-triggered flip-flop. The data input is connected to one of the outputs of the combinational logic module. The set direct and reset direct inputs may be individually enabled or disabled.

The reset direct input, if enabled, may come from either the D input to the CLB, or from the G output of the combinational logic module. Set direct control, if enabled, can come from either the A input to the CLB or from the F output of the combinational logic module.

Clock for the storage element may be individually enabled or disabled and can be driven by the clock input, K, to the CLB, the C input to the CLB, or the G output of the combinational logic module. Final outputs, X and Y, from the CLB can be selected to be either of the two outputs, F and G, of the combinational logic module, or the Q output from the storage element.

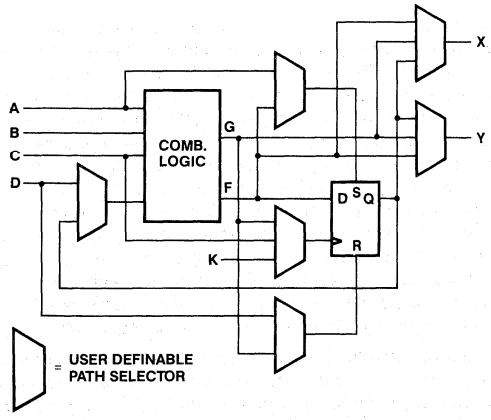


Figure 1. Block Diagram of a Single CLB

I/O Elements

The M2064 contains fifty-eight user-configurable I/O blocks for connection to external circuits. Each block is a general purpose device containing a three-state output buffer, an input buffer, and an input flip-flop as shown in Figure 2. The input buffer always reflects the status of the I/O pin or the contents of the input flip-flop. If the flip-flop is selected, data present on the I/O pin will be clocked to the input buffer by the I/O block clock signal. All I/O blocks on a particular edge of the device share a common I/O clock signal. The output buffer may be enabled, disabled, or under the control of the three-state connection.

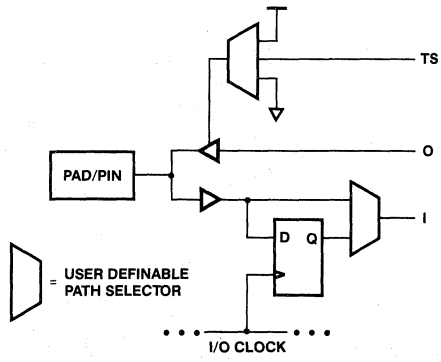


Figure 2. Block Diagram of an I/O Element

15

Interconnect

There are nine rows and nine columns of metal interconnect resources with one row or column located between each row or column of CLBs or I/O blocks. Each row or column of interconnect resources contains local use lines, long lines and programmable interconnect points between I/O blocks, CLBs and interconnect resources. Local lines run either vertically from one row of resources to the adjacent row or horizontally from one column to the adjacent column. Long lines run the full height or width of the device. At the intersection of every row and column of interconnect resources are user configurable interconnect elements which allow multiple combinations of connections between local lines in adjacent rows and columns. In addition, selected intersections of local and long lines can be connected by user programmable interconnect points.

Inputs and outputs from each CLB or I/O block have programmable connections to the interconnect resources in the adjacent rows and columns. These connections allow CLBs or I/O block connections to be made for proper signal routing to or from the I/O blocks or CLBs. In addition to the programmable connections to adjacent interconnect resources, there are direct connection paths which do not utilize the general interconnect resources. These paths allow selected connection between some I/O blocks and CLBs and between adjacent CLBs. For example, the outputs of a CLB in the interior of the matrix of CLBs may be connected to adjacent CLBs without using any interconnect resources.

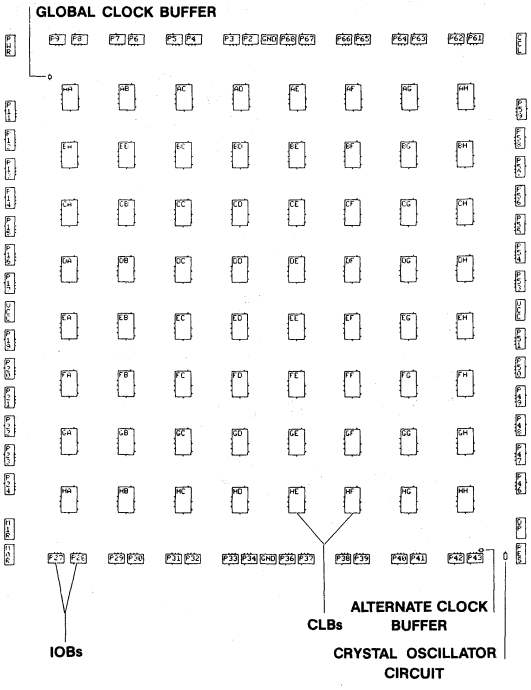
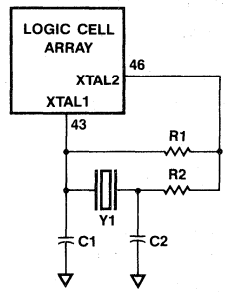


Figure 3. Overview Functional Layout of the M2064

Clock Generation and Buffering

The M2064 contains two special purpose clock buffers for generating and driving clock signals to multiple CLBs or I/O blocks with negligible skew. The Global Clock Buffer, is dedicated to driving a matrix of long lines which have configurable connections to the K input of each CLB register. This clock buffer may be driven from an internally generated register source, or configured with a connection directly to an I/O block for driving it with an external clock signal. The output from the Global Clock Buffer may be configured to directly drive an I/O block for driving clock signals off the device.

The alternate clock buffer can be configured either as a simple buffer or as a buffer for the crystal oscillator. In the crystal oscillator mode, an externally connected crystal and optional passive components form a clock generator for use on the chip or for driving other external circuits (see Figure 4). When configured in the buffer mode, the alternate clock buffer can have either one or both of its input and output configured to directly drive, or be driven by, an I/O block. The output of the alternate clock buffer can drive long lines in any column of CLBs as well as local interconnect.



Suggested component values:

R1	1 - 4 MΩ
R2	0 - 1 KΩ (may be required for low frequency, phase shift and/or compensate level for crystal Q)
C1, C2	5 - 20 pF
Y1	1 - 10 MHz AT cut

Figure 4. Crystal Oscillator

Each CLB has a special clock input (K) which can be selected as the clock input of the storage element. Clock inputs to user selected CLBs can be configured to be driven from either the Global Clock Buffer, the oscillator/buffer or from other local interconnect. Clocks to the I/O blocks can be configured from either of the clock buffers or the local interconnect.

Programming

Configuration of the device may be performed in any one of three modes. The desired configuration mode is set by the state of the mode pins M0 and M1 at power up (see Table 1). All configuration data relating to CLB function definition, interconnect resource utilization, and I/O block programming must be loaded into the device prior to use. In the peripheral and slave modes the data is supplied in a serial stream in conjunction with the configuration clock signal, CCLK. In master mode, the device automatically loads data from an external memory device by supplying addresses and reading bytes of data. In all modes the data patterns required to create a specific configuration are the same.

MODE SELECT PINS	M0	M1
Master LOW mode	0	0
Master HIGH mode	0	1
Peripheral mode	1	0
Slave mode	1	1

Note: During configuration, Pin 27 on the 68-pin package or Pin 7 on the 48-pin package must be held HIGH.

Table 1. Modes

Data patterns for a specific user-configuration are created with the Monolithic Memories XACT LCA Development System and can be output to a standard EPROM programmer or saved on disk for inclusion with other software. Users who are using the Monolithic Memories XACT debugging system can directly access the configuration data and load the device directly during a debug session. Because of the complexity of the data patterns and difficulty in generating them without a thorough knowledge of the device, users are discouraged from attempting to generate data patterns on their own. Data pattern files for M2064 devices contain 1536 bytes.

Special Features

The M2064 contains several special features which enhance its capacity for use in a wide variety of applications. Among these are the following:

Data Security
The M2064 configuration data contains special control bits which enable or disable configuration data security control. If enabled, the security control will prevent the read-back of configuration data after the initial configuration. There are two possible modes of operation under security control. One mode allows a single read-back after configuration to allow verification of the data. In the second mode, all access to the configuration data is prevented.

Reprogrammability
Configuration data changes are controlled by reprogramming control bits in the configuration data supplied to the device. If reprogramming is enabled, the user may supply new configuration data at any time by asserting the correct control sequence on the DONE-~PG and M0 and M1 mode control pins. Alternatively, the user may elect to prevent reconfiguration of the device. When operating in this mode, the only method to remove the configuration is to remove all power from the device.

Inactive Power-down
In a system which is to remain in its current configuration through power loss, the M2064 may be forced into a low power inactive state by using the ~PWRDN pin. When held low, the LCA will retain all configuration data but will not operate. All clocks will be stopped and all outputs put into a high-impedance state. Power is reduced to a very low level, allowing a simple external battery arrangement to supply the required configuration data saving power (see electrical characteristics).

Configuration Data Read-back
A mechanism is provided in the M2064 to provide verification of stored configuration data. The configuration read-back is initiated by toggling the ~RT pin and clocking the CCLK pin. Each clock applied to CCLK will read out a configuration data bit on the ~RD pin. When all configuration data has been read out, the ~RD pin will return to its inactive state. The configuration data may be read at any time with no effect on the operation of the device. Once a configuration read-back has been initiated, all data must be read out of the device to insure that subsequent read-back operations will begin at the start of the configuration data.

Master Reset
After device configuration, the ~RESET pin becomes a master reset for all CLB and IOB storage elements in the device. Asserting this control signal will asynchronously reset all of the internal storage registers regardless of the operating condition of the circuit.

Development System

The Monolithic Memories Design System is an integrated package of design tools for developing configuration data for LCAs. All aspects of configuration are specified through interactive graphics software. Facilities to verify functionality and timing of the designed configuration insure that designs operate as desired.

XACT is a graphic design system used to specify LCA designs. It contains several standard and several optional software and hardware packages. The basic package runs on an IBM PC/XT or AT compatible computer with 640K memory, a color monitor and a mouse. The tools accessible from the executive, including the optional packages, are:

- LCA Editor and Macros
- Timing Analyzer
- Simulator (P-Silos, optional)
- Configuration-File Generator
- Configuration-File Formatter
- XACTOR 2 In-circuit-emulator (optional).

XACTOR 2 consists of a software program plus a hardware attachment that allows control of up to four LCAs. The program contains commands for:

- Loading configuration data
- Activating the Master Reset input
- Reconfiguring
- Single stepping the device clock
- Reading back configuraiton data and state of all 122 internal registers on any clock cycle.
- Real time system debug.

An evaluation kit is available which includes:

- Complete documentation of the Development System
- A sample LCA design
- XACT software package.

Contact your local Monolithic Memories Representative or Distributor for more information.

Absolute Maximum Ratings*

Supply voltage V_{CC} ..... -0.5 V to 7 V
Power down V_{CC} ..... 2 V to 7 V
Input voltage ..... -0.5 V to V_{CC} 0.5 V
Voltage applied to three-state output ..... -0.5 V to V_{CC} 0.5 V
Storage temperature range ..... -65° C to +150° C
Lead temperature (soldering, 10 seconds) ..... 260° C

*Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those listed under "Recommended Operating Conditions" is not implied. Exposure to "Absolute Maximum Ratings" conditions for extended periods of time may affect device reliability.

Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage relative to GND	4.75		5.25	V
V_{IHT}	High level input voltage—TTL configuration	2.0			V
V_{IHC}	High level input voltage—CMOS configuration	0.7			V
V_{ILT}	Low level input voltage—TTL configuration	0		0.8	V
V_{ILC}	Low level input voltage—CMOS configuration	0		0.2	V
I_{IT}	Input leakage current—TTL configuration	±1			μA
I_{IC}	Input leakage current—CMOS configuration	±1			μA
I_{OZ}	Three-state output off current (V_{CC} = 5.5V)	±10			μA
t_{OP}	Operating free-air temperature	0		70	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage		V_{CC} = 4.75 V	I_{OH} = -4.0 mA	3.86			V
V_{OL}	Low level output voltage		V_{CC} = 4.75 V	I_{OL} = 4.0 mA			0.32	V
I_{CCO}	Quiescent operating power supply current	CMOS inputs	V_{CC} = 5.0 V				5	mA
		TTL inputs	V_{CC} = 5.0 V				10	mA
I_{CCPD}	Power down supply current		V_{CC} = 2.0 V		Consult factory			V

Note: All switching characteristics are at worst case conditions.

Power on Timing

The M2064 contains on-chip reset timing logic for power-up operation. To insure proper master mode system operation, VCC must rise from 2.0 V to minimum specification level in 10 ms or less. For other modes, initiation of configuration must be delayed for 60 ms after VCC reaches the minimum specified level.

Switching Characteristics—CLB

ITEM	DESCRIPTION	M2064-50 MIN	M2064-50 TYP	M2064-50 MAX	M2064-33 MIN	M2064-33 TYP	M2064-33 MAX	M2064-20 MIN	M2064-20 TYP	M2064-20 MAX	UNIT
t_{ILO}	Input through logic to X or Y			15			20			35	ns
t_{ITO}	Input through logic and latch to X or Y			20			25			45	ns
t_{CKO}	Storage element clock from K to output			15			20			35	ns
t_{CCO}	Storage element clock from C to output			19			25			45	ns
t_{CIO}	Logic to storage element clock to output			27			37			65	ns
t_{QLO}	Storage element Q to logic to output			8			13			30	ns
t_{ICK}	Input setup to K clock to storage element	8			12			22			ns
t_{CKI}	Input hold to K clock to storage element	0			0			0			ns
t_{ICC}	Input setup to C clock to storage element	9			12			18			ns
t_{CCI}	Input hold to C clock to storage element	0			6			10			ns
t_{ICI}	Input setup to input clock to storage element	4			6			10			ns
t_{CII}	Input hold to input clock to storage element	5			9			15			ns
t_{RIO}	Input to storage element Reset/Set to output			22			25			45	ns
t_{RLO}	Logic to storage element Reset/Set to output			28			37			65	ns
t_{RPW}	Reset/Set pulse width	9			12			20			ns
t_{RS}	Storage element control separation	9			17			30			ns
t_{CH}	Storage element clock high time	9			12			20			ns
t_{CL}	Storage element clock low time	9			12			20			ns
f_{CLK}	Storage element clock frequency			50			33			20	MHz
t_{MRQ}	Master reset to storage element Q to output			25			35			60	ns

Cross Reference Guide

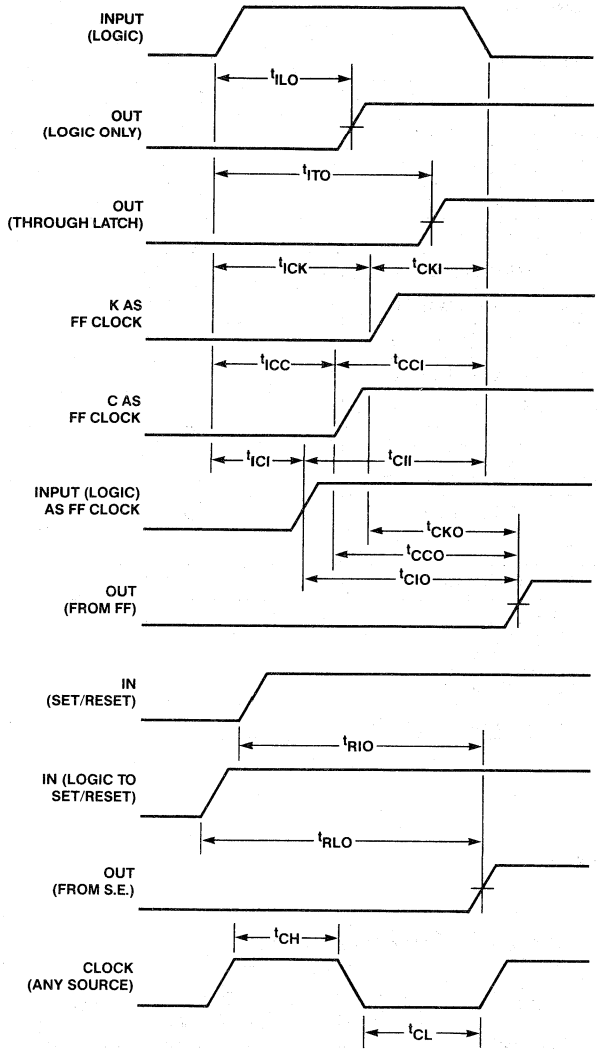
Cross Reference Guide

XILINX	MONOLITHIC MEMORIES	V_{CC} MIN	V_{CC} MAX	F_{MAX}
XC-2064-1		4.5 V	5.5 V	20 MHz
	M2064-20	4.75 V	5.25 V	20 MHz
XC-2064-2		4.5 V	5.5 V	33 MHz
XC-2064-33	M2064-33	4.75 V	5.25 V	33 MHz
XC-2064-50	M2064-50	4.75 V	5.25 V	50 MHz

*For commercial product only.

15

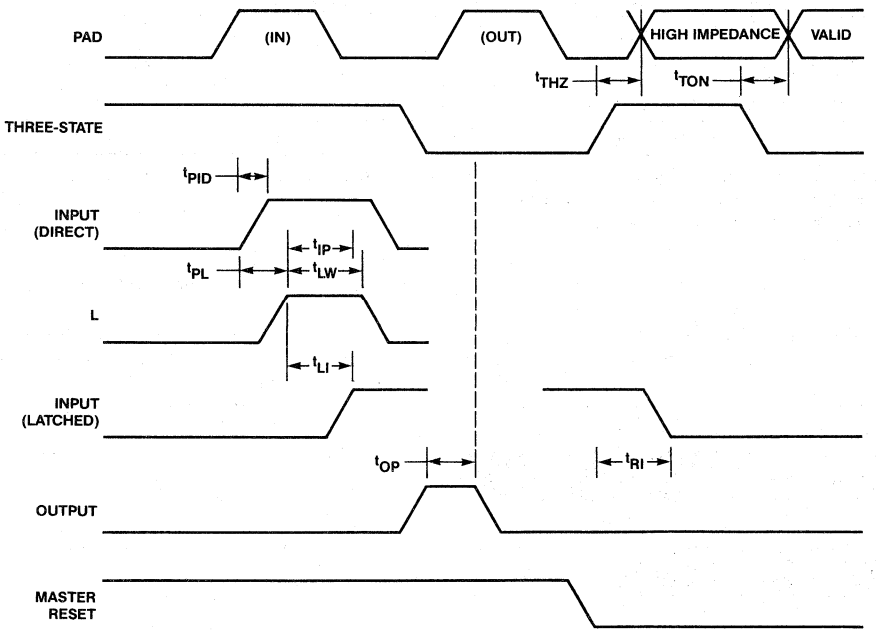
Switching Characteristics — CLB



Note: 1. Input refers to CLB inputs A, B, C or D
2. Output refers to CLB output X or Y
3. Clock refers to the CLB storage element clock
4. FF (Flip Flop) or L (Latch) refers to the CLB storage element
5. Set and Reset refer to CLB storage element controls

Switching Characteristics—IOB

ITEM	DESCRIPTION	M2064-50 MIN	M2064-50 TYP	M2064-50 MAX	M2064-33 MIN	M2064-33 TYP	M2064-33 MAX	M2064-20 MIN	M2064-20 TYP	M2064-20 MAX	UNIT
t_{PID}	Pad to input direct			8			12			20	ns
t_{PL}	Pad input setup to I/O clock	8			12			20			ns
t_{LP}	Pad input hold to I/O clock	0			0			0			ns
f_L	Frequency, I/O clock			50			33			20	MHz
t_{LW}	Pulse width input latch clock	9			12			20			ns
t_{LI}	Input latch clock to input			15			20			30	ns
t_{OP}	Output to pad output (three-state enabled)			12			15			25	ns
t_{THZ}	Three-state inactive to high impedance			20			25			35	ns
t_{TON}	Three-state active to output on			20			25			40	ns
t_{RI}	Master Reset to latched input reset			25			30			50	ns



Note:
1. Output (O) refers to the output connection on the IOB
2. Input (I) refers to the input connection on the IOB
3. Three-state (T) refers to the three-state control on the IOB
4. Pad or Pin (P) refers to the device pin connected to the IOB
5. Latch (L) refers to the input Flip-Flop clock connection

15

Switching Characteristics—Programming - Slave Mode

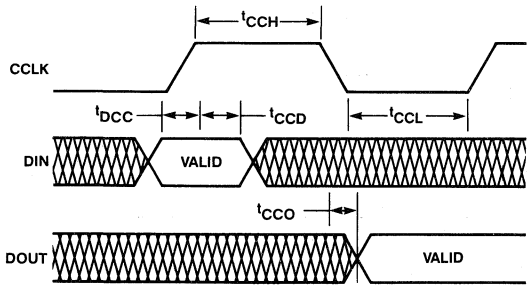
ITEM	DESCRIPTION	M2064-50 MIN	M2064-50 TYP	M2064-50 MAX	M2064-33 MIN	M2064-33 TYP	M2064-33 MAX	M2064-20 MIN	M2064-20 TYP	M2064-20 MAX	UNIT
t_{CCH}	CCLK high time	300			300			500			ns
t_{CCL}	CCLK low time	200			200			300			ns
t_{CCL}	CCLK low time			5000			5000			10000	ns
t_{DCC}	DIN data setup to CCLK rising edge	25			25			50			ns
t_{CCD}	DIN data hold from CCLK rising edge	40			40			75			ns
t_{CCO}	DOUT data delay from CCLK falling edge			65			65			100	ns
f_{CC}	CCLK maximum frequency			2			2			1	MHz

Switching Characteristics—Programming - Peripheral Mode

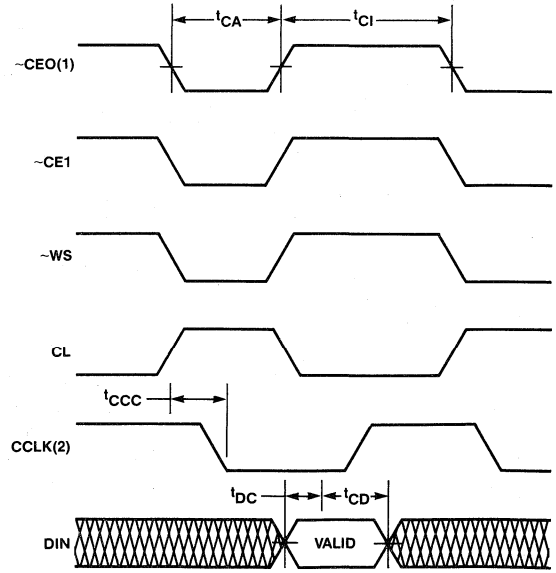
ITEM	DESCRIPTION	M2064-50 MIN	M2064-50 TYP	M2064-50 MAX	M2064-33 MIN	M2064-33 TYP	M2064-33 MAX	M2064-20 MIN	M2064-20 TYP	M2064-20 MAX	UNIT
t_{CA}	Control input active period	200			200			300			ns
t_{CA}	Control input active period			5000			5000			10000	ns
t_{CI}	Control input inactive period	150			150			250			ns
t_{CCC}	CCLK delay from control input edge			75			75			100	ns
t_{DC}	DIN setup to control transition	35			35			50			ns
t_{CD}	DIN hold from control transition	5			5			10			ns

Notes: 1. Peripheral mode timing determined from last control signal (~CE0, ~CE1, ~WS, CS) to transition to active or inactive state.
2. CCLK timing minima and maxima same as for slave mode.
3. CCLK and DOUT timing same as for slave mode.

Slave Mode



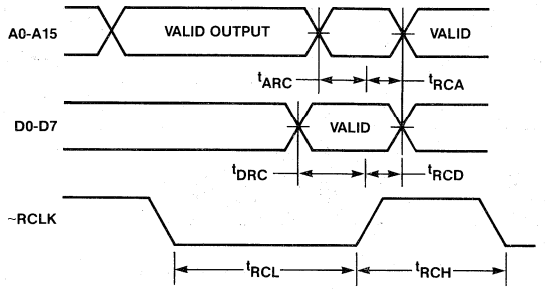
Peripheral Mode



Switching Characteristics—Programming - Master Mode

ITEM	DESCRIPTION	M2064-50 MIN	M2064-50 TYP	M2064-50 MAX	M2064-33 MIN	M2064-33 TYP	M2064-33 MAX	M2064-20 MIN	M2064-20 TYP	M2064-20 MAX	UNIT
t_{ARC}	Address invalid prior to ~RCLK edge			0			0			0	ns
t_{RCA}	Address valid from ~RCLK edge			200			200			300	ns
t_{DRC}	Data bus setup to ~RCLK edge	60			60			100			ns
t_{RCD}	Data bus hold from ~RCLK edge	0			0			0			ns
t_{RCH}	~RCLK high	600			600			600			ns
t_{RCL}	~RCLK low	4000			4000			4000			ns

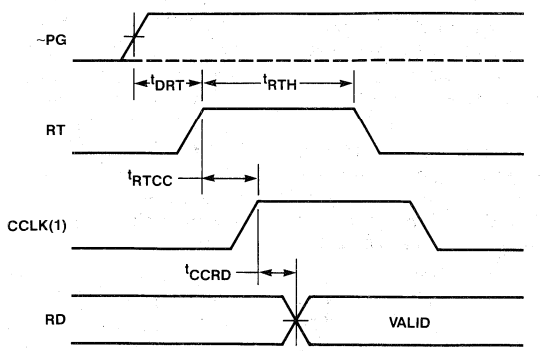
Note: Timing for DOUT and CCLK out is same as for slave mode.



Switching Characteristics—Program Readback

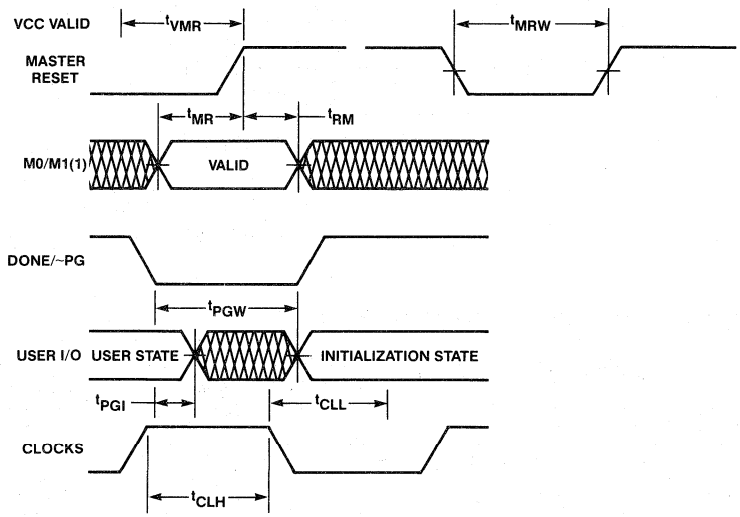
ITEM	DESCRIPTION	M2064-50 MIN	M2064-50 TYP	M2064-50 MAX	M2064-33 MIN	M2064-33 TYP	M2064-33 MAX	M2064-20 MIN	M2064-20 TYP	M2064-20 MAX	UNIT
t_{RTH}	Read trigger (RT) high time	150			150			250			ns
t_{RTCC}	Delay from RT assertion to first CCLK	60			60			100			ns
t_{CCRD}	Delay from CCLK edge to RD data valid			60			60			100	ns
t_{DRT}	Wait period from DONE to RT assertion	75			175			300			ns

Notes: 1. Timing for CCLK is same as for slave programming mode.
2. DONE/~PG output/input must be high (device programmed) prior to assertion of ~PG.



Switching Characteristics—General

ITEM	DESCRIPTION	M2064-50 MIN	M2064-50 TYP	M2064-50 MAX	M2064-33 MIN	M2064-33 TYP	M2064-33 MAX	M2064-20 MIN	M2064-20 TYP	M2064-20 MAX	UNIT
t_{VMR}	Master Reset delay from valid V_{CC}	150			150			250			ns
t_{MRW}	Master Reset pulse width	150			150			250			ns
t_{MR}	Mode control setup to Master Reset	60			60			100			ns
t_{RM}	Mode control hold from Master Reset	7			7			10			ns
t_{PGW}	Program control pulse width	6000			6000			6000			ns
t_{PGI}	Program control to I/O initialized			7000			7000			7000	ns
t_{CLH}	Clock buffer input high time	9			12			20			ns
t_{CLL}	Clock buffer input low time	9			12			20			ns
f_{CL}	Clock buffer input frequency			50			33			20	MHz



Test Conditions:

Outputs loaded with rated DC current and 50-pF capacitance to GND.

Design Aids

XACT™ provides complete design automation for users to specify and implement designs utilizing Monolithic Memories' LCA products. Configuration of CLBs, internal routing, I/O block definitions and global routing are all handled in an integrated, easy-to-use system.

Placement and routing of logic and I/O blocks is accomplished using interactive graphics. Final programming bit patterns are automatically produced for debugging, transfer to other systems, or downloading to standard EPROM programmers. Debugging with the XACTOR 2™ emulation system allows full device emulation and operation analysis in the target system.

The user inputs data via a graphics-oriented physical editing environment. User functions are translated into CLB logic specifications and interconnections automatically. Standard logic libraries and other macro capabilities can be utilized for rapid design entry.

Physical placement and hard connections are performed with the graphics placement and connection capabilities. Final device layout and routing are visible and can be modified without disturbing the logical arrangement. Logical connectivity and physical layout rules checking are performed automatically.

Full timing analysis and functional simulation of user configurations allows device performance and functional checking without external test hardware. In addition, point-to-point path timing calculation capability is provided to simplify general timing analysis and critical path determination.

The debugging system provides full emulation in the user's target system. User configurations may be transferred directly from the design phase into the target system and tested through the emulation system.

Additional capabilities include a tool for automatic hard copy generation of the user's logic design and physical implementation and a tool for transferring programming bit patterns to EPROM programming systems.

Recommended Sockets

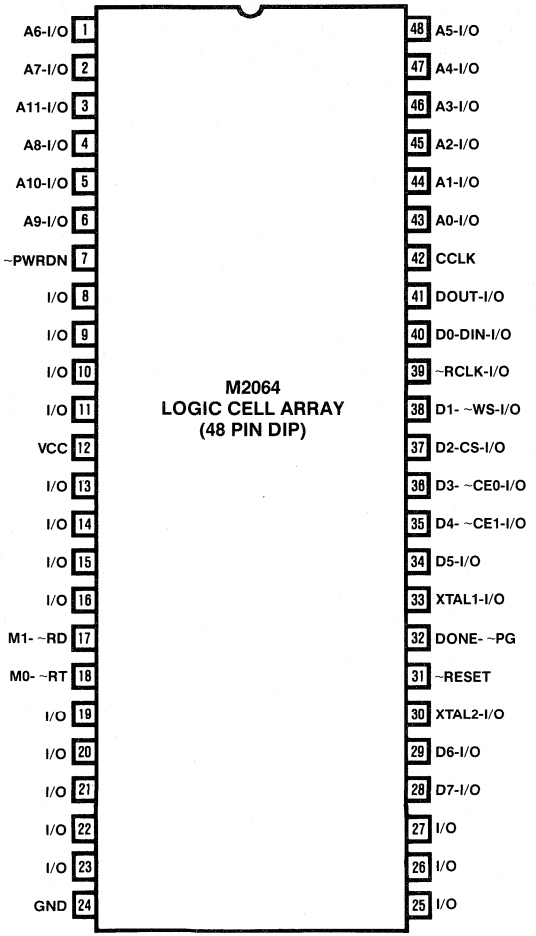
The following 68-pin PLCC sockets have been evaluated by Monolithic Memories and have been found to exhibit acceptable connectivity, device retention and device extraction characteristics:

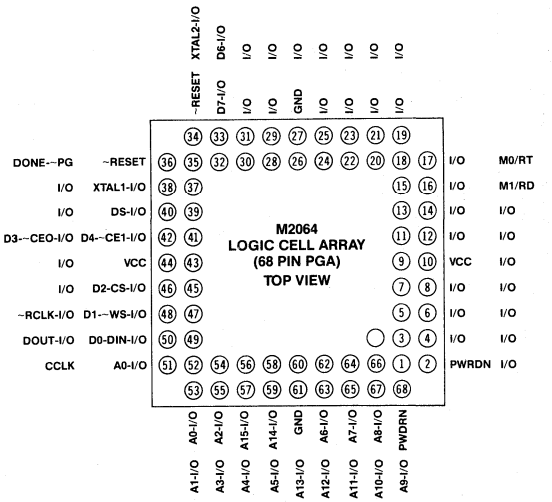
VENDOR	DESCRIPTION	PART NUMBER
AMP	PCB solder tail, tin plate	821574-1
AMP	Surface mount, tin plate	821542-1
Burndy	PCB solder tail, tin plate	QILE68P-410T
Midland-Ross	PCB solder tail, tin plate	709-2000-068-4-1-1

The following 68-pin PLCC sockets are also available:

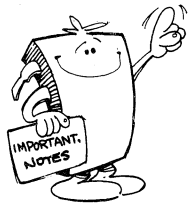
VENDOR	DESCRIPTION	PART NUMBER
Methode	PCB solder tail, tin plate	213-068-001
Methode	Surface mount, tin plate	213-068-002

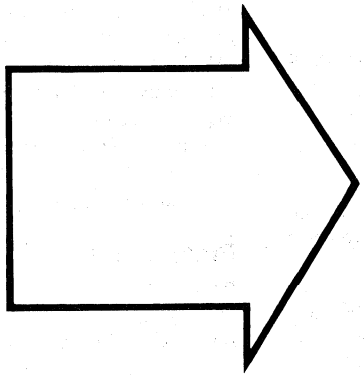
Notes: 1. The standard device extraction tools supplied with the XACT development system will work with all of the above sockets.
2. All of the above PCB solder tail sockets have the same hold pattern and pinout.





15


IMPORTANT
NOTES



Clock Frequency

Maximum clock frequency, f_{max}

The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

Current

High-level input current, I_{IH}

The current into* an input when a high-level voltage is applied to that input.

High-level output current, I_{OH}

The current into* an output with input conditions applied that according to the product specification will establish a high level at the output.

High-level output current, I_{CEX}

The high-level leakage current of an open collector output.

Low-level input current, I_{IL}

The current into* an input when a low-level voltage is applied to that input.

Low-level output current, I_{OL}

The current into* an output with input conditions applied that according to the product specification will establish a low level at the output.

Off-state (high-impedance-state) output current (of a three-state output), I_{OZ}

The current into* an output having three-state capability with input conditions applied that according to the product specification will establish the high-impedance state at the output.

Short-circuit output current, I_{OS}

The current into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

Supply current, I_{CC}

The current into* the V_{CC} supply terminal of an integrated circuit.

*Current out of a terminal is given as a negative value.

Hold Time

Hold time t_h

The interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES: 1. The hold time is the actual time between two events and may be insufficient to accomplish the intended result. A minimum value is specified that is the shortest interval for which correct operation of the logic element is guaranteed.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of data and the active transition) for which correct operation of the logic element is guaranteed.

Output Enable and Disable Time

Output enable time (of a three-state output) to high level, t_{PZH} (or low level, t_{PZL})

The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high (or low) level.

Output enable time (of a three-state output) to high or low level, t_{PZX}

The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low).

Output disable time (of a three-state output) from high level, t_{PHZ} (or low level, t_{PLZ})

The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high (or low) level to a high-impedance (off) state.

Output disable time (of a three-state output) from high or low level, t_{PXZ}

The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

t_{EA} is the output enable access time of memory devices.
t_{ER} is the output disable (enable recovery) time of memory devices.

Propagation Time

Propagation delay time, t_{PD}

The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level.

Propagation delay time, low-to-high-level output, t_{PLH}

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

Propagation delay time, high-to-low-level output, t_{PHL}

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{AA} is the address (to output) access time of memory devices.

Pulse Width

Pulse width, t_w

The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

Setup Time

Setup time, t_{su}

The time interval between the application of a signal that is maintained at one specified input terminal and a consecutive active transition at another specified input terminal

NOTES: 1. The setup time is the actual time between two events and may be insufficient to accomplish the setup. A minimum value is specified that is the shortest interval for which correct operation of the device is guaranteed.

2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the device is guaranteed.

Voltage

High-level input voltage, V_{IH}

An input voltage within the more positive (less negative) of the two ranges of values assumable by a binary variable.

NOTE: A minimum is specified that is the least positive value of high-level voltage for which operation of the logic element within specification limits is guaranteed.

High-level output voltage, V_{OH}

The voltage at an output terminal with input conditions applied that will establish a high level at the output. The actual input conditions needed are determined by the individual product specification.

Input clamp voltage, V_{IC}

An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.

Low-level input voltage, V_{IL}

An input voltage level within the less positive (more negative) of the two ranges of values assumable by a binary variable.

NOTE: A maximum is specified that is the most positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

Low-level output voltage, V_{OL}

The voltage at an output terminal with input conditions applied that will establish a low level at the output. The actual input conditions needed are determined by the individual product specification.

Negative-going threshold voltage V_{T-}

The voltage level at an input that causes a transition as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

Positive-going threshold voltage, V_{T+}

The voltage level at an input that causes a transition as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.

Truth Table Explanations

H = high level (steady-state)

L = low level (steady-state)

↑ = transition from low-to-high level

↓ = transition from high-to-low level

X = don't care (any input, including transitions)

Z = off (high-impedance) state of a three-state output

a..h = the level of steady-state inputs at inputs A through H respectively

Q_0 = level of Q before the indicated steady-state input conditions were established

$\overline{Q}_0$ = complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established

Q_n = level of Q before the most recent active transition indicated by ↓ or ↑

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists as long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved and the indicated transition has occured (the transition(s) must occur following the achievement of the steady-state levels). If the output is shown as a level (H, L, Q_0, or $\overline{Q}_0$), it persists as long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output.


IMPORTANT.
NOTES

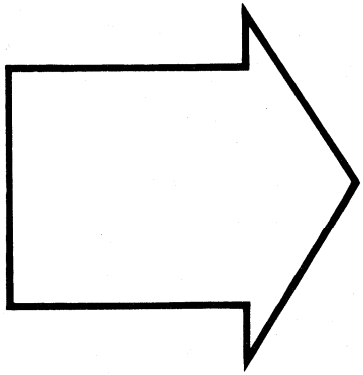


Table of Contents

ADVANCE INFORMATION

ADVANCE INFORMATION

Features/Benefits

- **10 ns maximum propagation delay**
- **8 ns maximum delay from clock input to data output**
- **f_{MAX} = 55.5 MHz**
- **Advanced oxide-isolated technology**
- **Programmable replacement for TTL logic**
- **Reduces chip count by greater than 4:1**
- **Instant prototyping and easier board layout**
- **Programmable on standard programmers**
- **Programmable three-state outputs**
- **Security fuse prevents duplication**
- **20-pin DIP and PLCC packages**

Areas of Application

- Control logic for mainframe and super-minicomputers
- Computer-aided graphics
- High-performance communication equipment
- High-speed test instruments

Description

The PAL20D Series provides the highest speed available for TTL PAL devices. The 10 ns maximum propagation delay is a 33% speed improvement over the 20B Series from Monolithic Memories, at no increase in power consumption. The 20D Series is functionally compatible with the earlier 20, 20A and 20B Series.

The PAL20D Series utilizes Monolithic Memories' advanced oxide-isolated process and proven TiW fuse link technology.

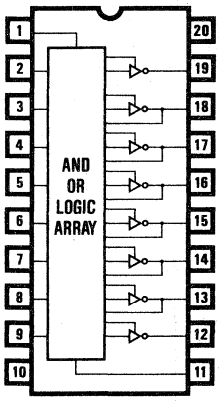
Features

The PAL20D Series includes the four standard 20-pin PAL device architectures. All four devices have sixteen array inputs and eight outputs, with varying numbers of registers: zero (16L8), four (16R4), six (16R6), and eight (16R8). The combinatorial outputs on the registered devices, and six of the outputs on the 16L8, are I/O pins that can be individually programmed as inputs or outputs. Each output register, a D-type flip-flop, also feeds back into the array, for implementation of synchronous state machine designs. Registered outputs are enabled by an external input, while the combinatorial outputs use a product term to control the enable function.

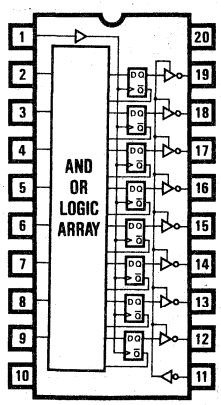
These features allow a great deal of flexibility for the design engineer when using the devices. The four different devices offer an optimized number of registers, while the number of inputs and combinatorial outputs can be balanced for the particular application. All of these features are automatically handled by the CAD software used to describe the design. Monolithic Memories' PALASM®2 software and third-party CAD tools all offer full support for these products.

Pin Configurations

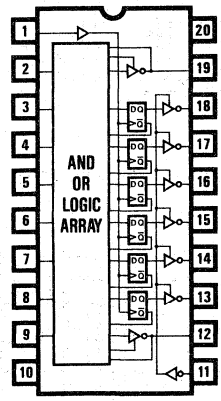
PAL16L8D



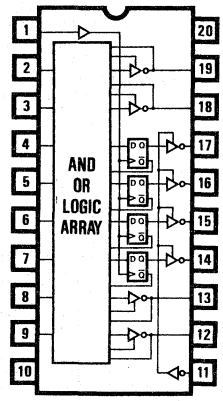
PAL16R8D



PAL16R6D



PAL16R4D



17

This document contains information on a product under development at Monolithic Memories Inc. The information is intended to help you to evaluate this product. Monolithic Memories reserves the right to change or discontinue work on this proposed product without notice.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Monolithic Memories

Ordering Information

PAL16 R 8DCN STD

- PROGRAMMABLE ARRAY LOGIC FAMILY
- NUMBER OF ARRAY INPUTS
- OUTPUT TYPE
  - R = Registered
  - L = Active Low
- NUMBER OF OUTPUTS
- SPEED
  - D = 10 ns
- PROCESSING
  - STD = Standard
  - XXXX = Hi-Rel
- PACKAGE
  - N = Plastic DIP
  - J = Ceramic DIP
  - NL = Molded chip carrier
- TEMPERATURE RANGE
  - C = 0°C to +75°C
  - M = -55°C to +125°C

Programming

The PAL20D Series is programmable on the same standard programmers as the rest of the 20-pin PAL device products. No upgrades are necessary. The configuration required is the same as that for the standard 20, 20A, and 20B Series.

Logic Development Software

The following logic development software packages can be used for configuring the PAL20D Series:

PALASM®, from Monolithic Memories

ABEL™, from Data I/O Corporation

CUPL™, from Assisted Technology, Inc.

f_{MAX} Parameters

The parameter f_{MAX} is the maximum speed at which the PAL device is guaranteed to operate. Because flexibility inherent to PAL devices allows a choice of clocked flip-flop designs, for the convenience of the user, f_{MAX} is specified to address two major classes of synchronous designs.

The simplest type of synchronous design can be described as a data path application. In this case, data is presented to the data terminal of the flip-flop and clocked through; no feedback is employed (Figure 1). Under these conditions, the frequency of operation is limited by the greater of the data setup time (t_{SU}) or the minimum clock period (t_W high + t_W low). This parameter is designated f_{MAX} (no feedback).

For synchronous sequential designs, i.e., state machines, where logical feedback is required, inputs to flip-flop data terminals originate from the device input pins or flip-flop outputs via the internal feedback paths (Figure 2). Under these conditions, f_{MAX} is defined as the reciprocal of (t_{SU} + t_{CLK}) and is designated f_{MAX} (feedback). For the PAL20D Series, this value calculates as 1/(10+8) = 55.5 MHz.

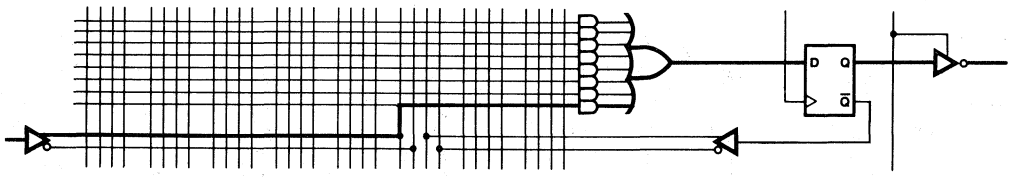


Figure 1. Data Path Register Configuration Without Feedback

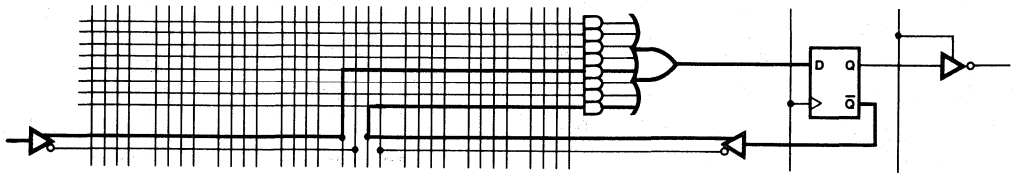


Figure 2. State Machine Configuration With Feedback

ABEL™ is a trademark of Data I/O Corporation.
CUPL™ is a trademark of Assisted Technology, Inc.

ADVANCE INFORMATION

Features/Benefits

- CMOS technology provides zero standby power
- 25 ns maximum propagation delay (20L8, 20R4, 20R6 and 20R8)
- Low power mask-programmed alternative for most 24-pin PAL® devices
- Space-saving 24-pin SKINNYDIP® or 28-pin PLCC and LCC packages
- Available in Commercial, Industrial and Military operating ranges

Description

The ZHAL24A Series is a mask-programmed, zero-power option to most of the 24-pin PAL devices. The ZHAL24A Series offers not only higher density than the ZHAL20 Series, but also improved speed, matching the bipolar speeds of the Small 24 and Medium 24A, 24XA and 24RS PAL device series.

Design Procedures

ZHAL device prototyping can be done using standard PAL devices before converting to the ZHAL device for production. ZHAL devices are fabricated by Monolithic Memories with a custom mask defined by a user-supplied HAL® device Design Specification. The ZHAL24A Series utilizes a unique architecture that can implement 90% of the 24-pin PAL device patterns. To determine whether a given pattern will fit, run the ZHAL24 option in the PALASM®2 software package. Patterns that could not fit in the ZHAL20 Series will fit in the 20-pin option of the ZHAL24A Series.

ZHAL24A Device Options

(continued on back)

Areas of Application

- Portable computers
- Battery-operated instrumentation
- Low-power industrial or military equipment
- Standard CMOS/TTL logic replacement
- CMOS gate array alternative

Preliminary Data

(Commercial operating conditions, 20L8, 20R4, 20R6 and 20R8)
(other families may differ)

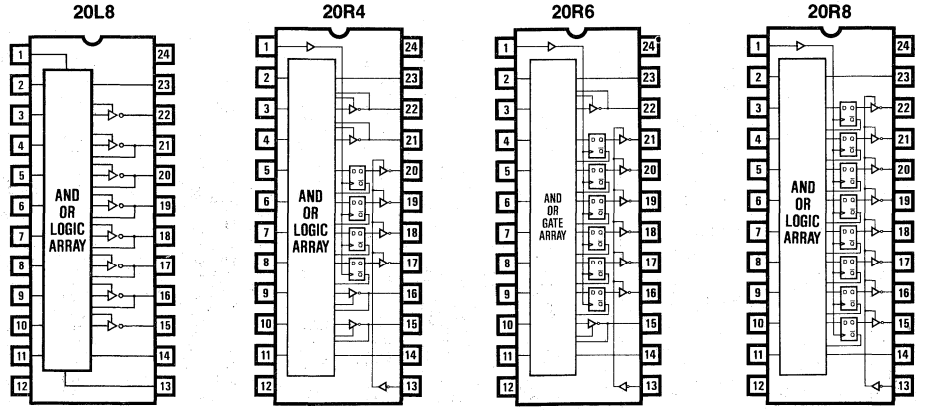
t_{PD} = 25 ns t_{CLK} = 15 ns
t_{su} = 25 ns f_{MAX} = 28.5 MHz

V_{OH} = 3.76 V at I_{OH} = −6 mA (HCT compatible)
V_{OL} = 0.4 V at I_{OL} = 8 mA
I_{CC} (standby) = 100 μA
I_{CC} (operating) = 5 mA at 1 MHz (+ 3 mA per additional 1 MHz)

Ordering Information

ZHAL20L8 A C NS STD P01234

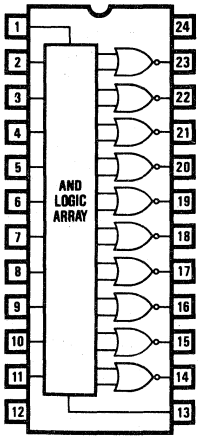
- ZERO-POWER HARD ARRAY LOGIC
- NUMBER OF ARRAY INPUTS
- OUTPUT TYPE
  - L = Active Low
  - C = Complementary
  - R = Registered
  - X = XOR Registered
  - S = Shared Terms
  - RS = Registered Shared Terms
- NUMBER OF OUTPUTS
- SPEED
  - Blank = Standard
  - A = High Speed
- PACKAGE
  - NS = Plastic SKINNYDIP
  - JS = Ceramic SKINNYDIP
  - NL = Plastic Leaded Chip Carrier
  - L = Leadless Chip Carrier
- TEMPERATURE RANGE
  - C = Commercial (0°C to 75°C)
  - I = Industrial (−40°C to 85°C)
  - M = Military (−55°C to 125°C)
- PROCESSING
  - STD = Standard
  - XXXX = Hi-Rel
- PATTERN NUMBER



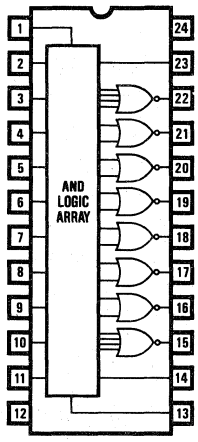
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Monolithic Memories

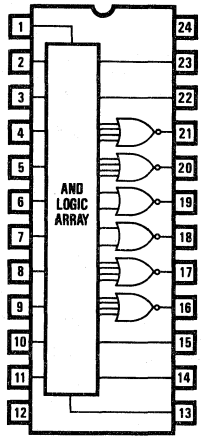
12L10



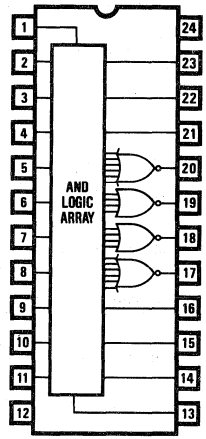
14L8



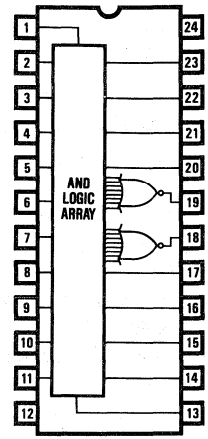
16L6



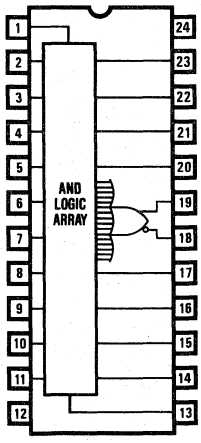
18L4



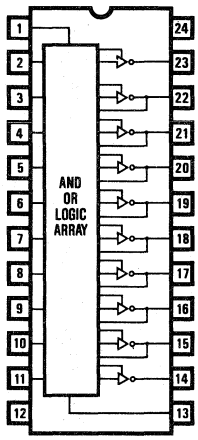
20L2



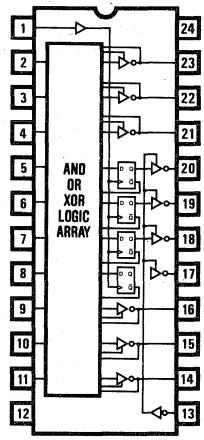
20C1



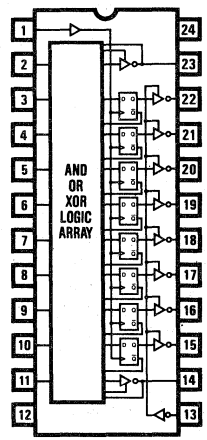
20L10



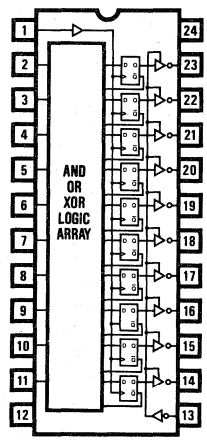
20X4



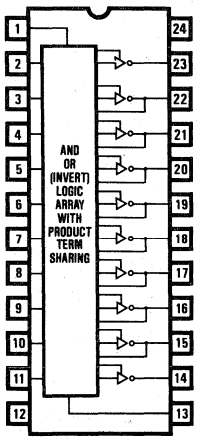
20X8



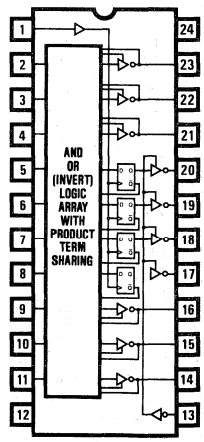
20X10



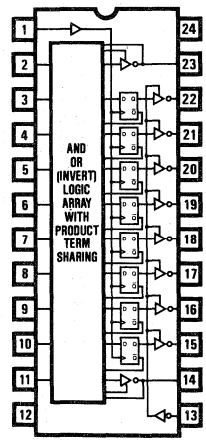
20S10



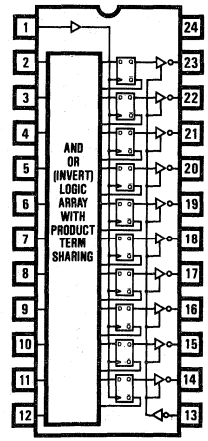
20RS4



20RS8



20RS10



ADVANCE INFORMATION

Features/Benefits

- **20 logic inputs; 12 external, 8 feedback**
- **8 outputs**
- **Programmable output polarity**
- **ECL technology for ultra-high speed**
- **32 product terms with term sharing**
- **10KH ECL compatible**
- **50 Ω termination drive**
- **Input pull-down resistors**
- **Voltage compensated**
- **24-pin SKINNYDIP® package**
- **Programmable using standard TTL programmers**

Description

The PAL10H20P8 is a 10KH compatible ECL PAL® device having twelve dedicated inputs and eight outputs with feedback. A programmable AND array and a fixed OR array make possible a wide variety of logic functions.

Device functionality can be specified using standard sum-of-products expressions. Logic development software is then used to transform the Boolean equations into a fuse map for use in programming the device.

Features

Each output has a polarity fuse. Programmable polarity allows the user to optimize his design equations without using DeMorgan's theorem to give the correct output polarity. This can simplify the design and save product terms.

The programmable AND array contains a total of thirty-two product terms. Product terms are arranged in groups of eight. The terms in each group can be shared mutually exclusively between two output cells.

Device Programmer Support

The PAL10H20P8 can be programmed using the following systems:

Data I/O LogicPak™ V04, P/T Adapter 303A-ECL
Family Pinout Code 22-42
Kontron EPP-80, Family Pinout Code 22-42

Logic Development Software Support

The following logic development software packages can be used for configuring the PAL10H20P8:

PALASM® 2, Ver. 2.19, from Monolithic Memories, Inc.

ABEL™, Ver. 2.0, from Data I/O Corp.

Preliminary Data

6.0 ns propagation delay

210 mA maximum IEE current

Areas of Application

High-performance communication equipment

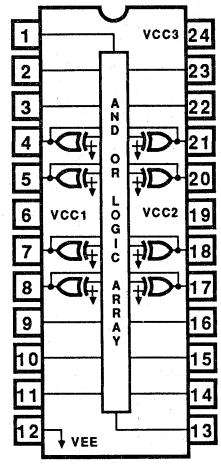
Glue logic joining ECL gate arrays

High-speed test instruments

Control logic for mainframe and super-mini computers

Computer-aided graphics

Pin Configuration



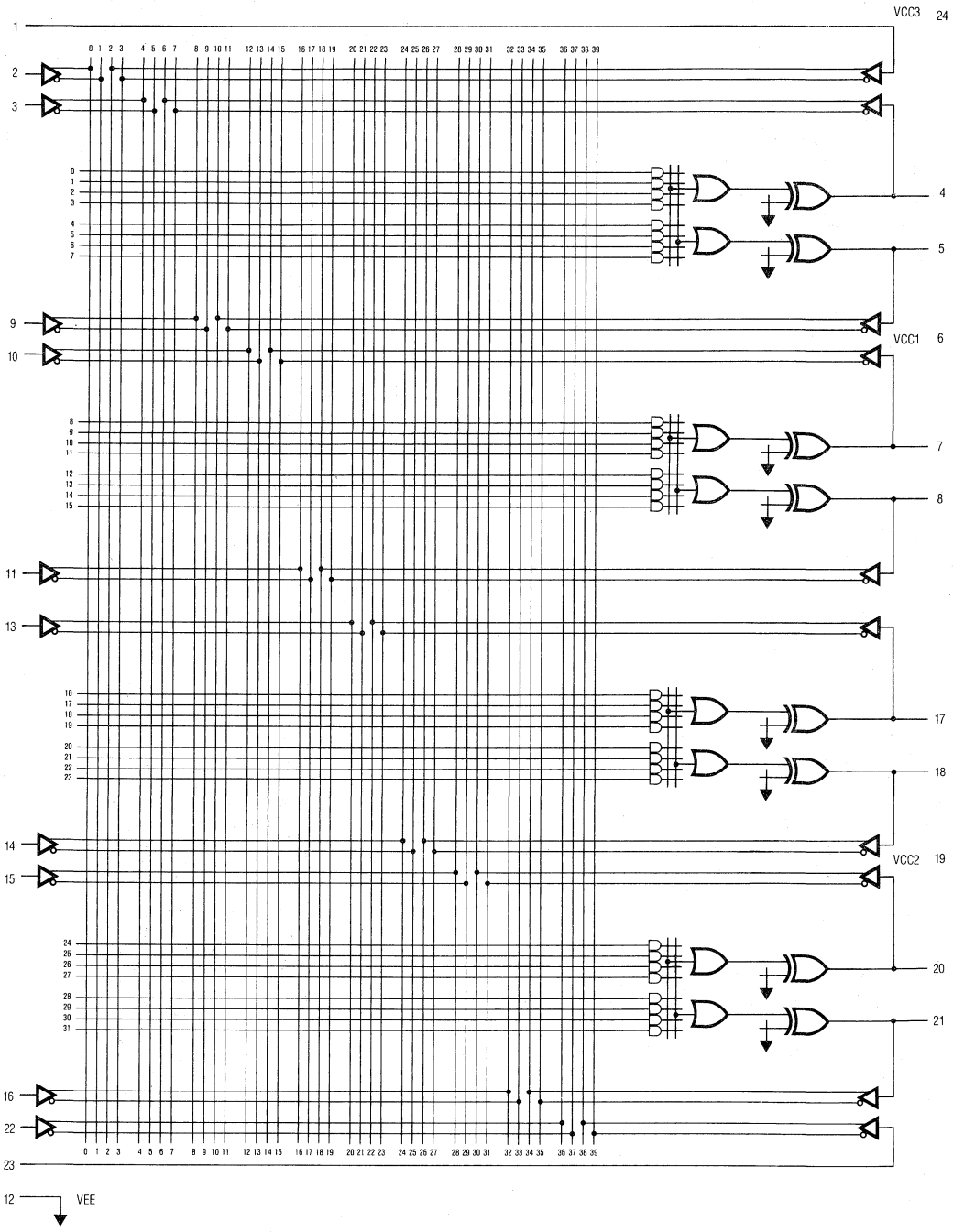
17

This document contains information on a product under development at Monolithic Memories Inc. The information is intended to help you to evaluate this product. Monolithic Memories reserves the right to change or discontinue work on this proposed product without notice.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376

Monolithic Memories

Logic Diagram



ADVANCE INFORMATION

Features/Benefits

- **CMOS technology provides zero standby power**
- **Lowest power 24-pin PAL® device family; consumes only 3 mA/MHz**
- **35 ns maximum propagation delay**
- **Programmable replacement for CMOS/TTL logic**
- **Reduces chip count by greater than six to one**
- **Instant prototyping and easier board layout**
- **HC/HCT compatible for use in CMOS or TTL systems**
- **Offered over both the Commercial and Industrial temperature ranges**
- **Low-cost, one-time programmable SKINNYDIP® and PLCC packages save board space**

Description

The CMOS ZPAL24 Series offers the first family of PAL devices with true CMOS power consumption. Under standby conditions (inputs and clock not changing), the devices consume a maximum current of 100 μA, less than 1% that of the quarter-power PAL devices. This low power consumption allows the devices to be powered by a battery almost indefinitely.

While operating, the devices consume additional power only when the inputs or clock change. Power consumption is directly proportional to the frequency of changes to the inputs. I_{CC} is therefore specified as 3 mA per 1 MHz of operating frequency, starting from 5 mA at 1 MHz. Thus, the maximum current at 8 MHz would be 5 mA + 7x3 mA, or 26 mA.

The devices have HC and HCT compatible inputs and outputs for use in CMOS and TTL systems. This feature allows the ZPAL circuits to be used for direct replacement of discrete CMOS as well as TTL logic.

Areas of Application

- Portable computers
- Battery-operated instrumentation
- Low-power industrial equipment
- Standard CMOS/TTL logic replacement

Features

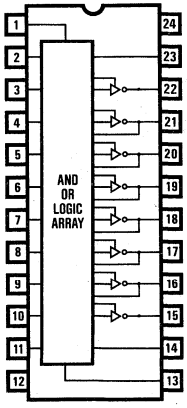
The CMOS ZPAL24 Series includes the four standard 24-pin PAL device architectures. All four devices have twenty array inputs and eight outputs, with varying numbers of registers: zero (20L8), four (20R4), six (20R6), and eight (20R8). The combinatorial outputs on the registered devices, and six of the outputs on the 20L8, are I/O pins that can be individually programmed as inputs or outputs. Each output register, a D-type flip-flop, also feeds back into the array, for implementation of synchronous state machine designs. Registered outputs are enabled by an external input, while the combinatorial outputs use a product term to control the enable function.

The basic PAL device architecture is a programmable AND array feeding a fixed OR array. The programmable AND array consists of a set of cells similar to those used in EPROMs. Erasable by UV light, the cells can be programmed and erased in the factory to ensure 100% programming and functional yields.

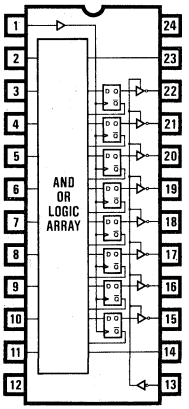
Windowed packages will be made available in the future, allowing erasure in the field. Windowed packages allow easy prototype testing and reconfiguration.

Pin Configurations

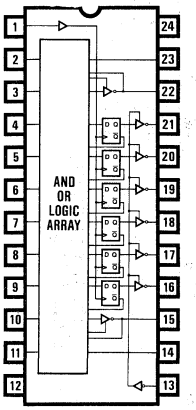
ZPAL20L8



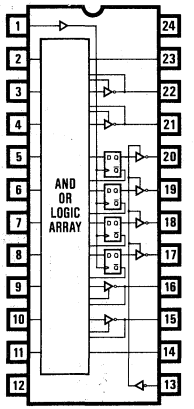
ZPAL20R8



ZPAL20R6



ZPAL20R4



Ordering Information

ZPAL20L8 I NS STD

- ZPAL = Zero-power Programmable Array Logic
- NUMBER OF INPUTS
- OUTPUT TYPE: L = Active Low, R = Registered
- NUMBER OF OUTPUTS
- PROCESSING: STD = Standard, XXXX = Hi-Rel
- PACKAGE: NS = Plastic SKINNYDIP, JS = Ceramic SKINNYDIP, QS = Windowed SKINNYDIP, NL = Plastic Leaded Chip Carrier, L = Leadless Chip Carrier
- OPERATING CONDITIONS: C = 0°C to 75°C, I = -40°C to 85°C, M = -55°C to 125°C

Programming

The ZPAL24 Series is programmable using the same standard programmers used for other PAL devices. The CMOS programming algorithm is different from that for the bipolar PAL devices, and requires a different family code.

Logic Development Software

The following logic development software packages can be used for configuring the ZPAL24 Series:

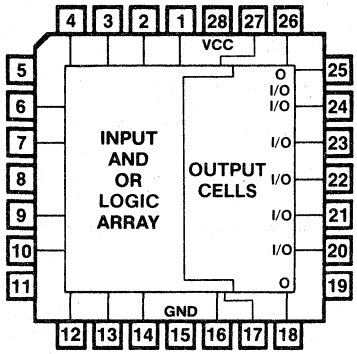
PALASM®2, from Monolithic Memories

ABEL™, from Data I/O Corporation

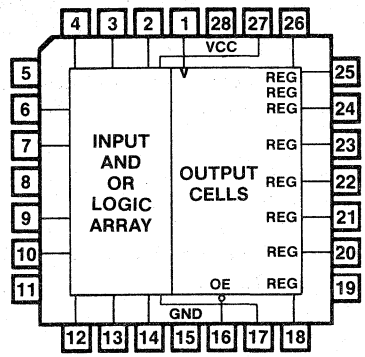
CUPL™, from Assisted Technology

PLCC Logic Symbols

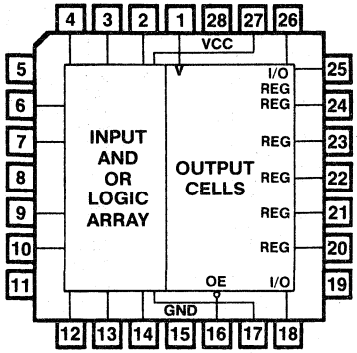
ZPAL20L8CNL



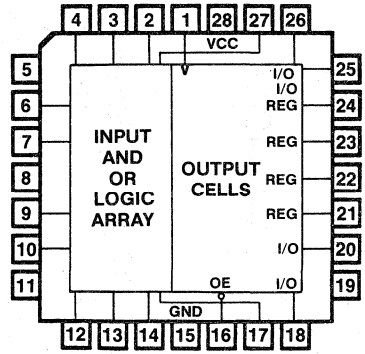
ZPAL20R8CNL



ZPAL20R6CNL



ZPAL20R4CNL



PMS14R21/A
Programmable Sequencer
PROSE™ Family
Patent Pending

ADVANCE INFORMATION

Features/Benefits

- **User-programmable synchronous state machine**
- **25 MHz maximum frequency for compatibility with 12.5 MHz processors**
- **14 inputs (8 external), 8 outputs, 128 states**
- **PAL® array optimizes product terms and states**
- **Internal feedback adds versatility and control**
- **Optimized for four-way branching**
- **User-selectable asynchronous initialize or asynchronous enable function**
- **Power-up reset for start-up in known state**
- **Diagnostics-On-Chip™ shadow register eases chip and board-level testing**
- **PROSE device software makes it easy to "write your sequencer in PROSE"**
- **Programmed on standard logic programmers**
- **Security fuse prevents pattern duplication**
- **Space-saving 24-pin 300-mil SKINNYDIP® and 28-pin PLCC and LCC packages**

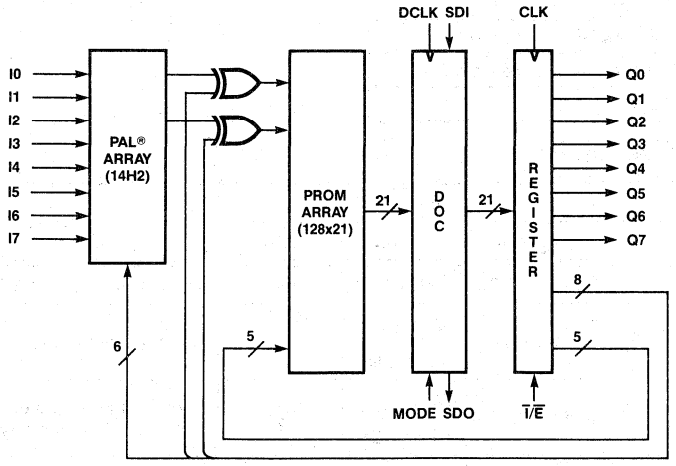
Description

The PMS14R21 programmable sequencer is the first member of the PROSE (PROgrammable SEquencer) family. The PMS14R21 is a high-speed, 14-input, 8-output state machine. It consists of a 128x21 PROM array preceded by a 14H2 PAL array. The PAL array is efficient for a large number of input conditions, while the PROM array is optimal for a large number of product terms and states. The combination allows a very efficient state machine with a large number of inputs and state bits. The PAL array, with eight product terms per output, operates on the eight conditional and six state inputs to select two control bits to the PROM. Two Exclusive-OR gates between the two arrays help to minimize product terms and redundant states. Five lines feed back from the PROM to form the primary address for the next state. The PROM stores up to 128 states of eight outputs and thirteen feedback control signals.

Applications

- High speed sequential logic
- Peripheral controller
- Cache control sequencer
- Signal processing sequencer
- Industrial control

Block Diagram



Definition of Signals

I0-I7	Primary inputs to the PAL array
Q0-Q7	Outputs from the register
$\overline{I}/\overline{E}$	Programmable asynchronous initialize ($\overline{I}$) or asynchronous enable ($\overline{E}$)
CLK	Clock for output register
DCLK	Clock for diagnostic register
MODE	Selects diagnostic functions
SDI	Serial data input to shadow register
SDO	Serial data output from shadow register

ABEL™ is a trademark of Data I/O Corporation.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374
Monolithic Memories

PROSE Part Numbering System

PMS 14 R 21 A C NS STD

- PREFIX: PMS = Programmable Memory-based Sequencer
- NUMBER OF ARRAY INPUTS: 14
- OUTPUT TYPE: R = Registered
- NUMBER OF REGISTERS: 21
- PERFORMANCE: Blank = standard; A = enhanced
- OPERATING CONDITIONS: C = 0°C to 75°C; M = -55°C to 125°C
- PACKAGE: NS = Plastic SKINNYDIP; JS = Ceramic SKINNYDIP; NL = Plastic Leaded Chip Carrier; L = Leadless Chip Carrier
- PROCESSING: STD = Standard; XXXX = Hi-Rel

Software Support

PROSE device software from Monolithic Memories provides full support for the PMS14R21. Based on PALASM® 2 syntax, the software automatically converts a state machine description directly into the PAL and PROM array fuse maps, for downloading to a programmer. The syntax supports both Mealy and Moore state machine models, and makes optimal use of the features of the PROSE device. Simulation support is also provided, both for design checking and for generation of test vectors for device testing. Additional support is available from third-party software vendors, including the ABEL™ package from Data I/O.

Diagnostics-On-Chip Feature

The PMS14R21 is the newest member of the Diagnostics-On-Chip family. These devices incorporate a serial shadow register on-chip which facilitates board-level testing. The shadow register has a Serial Data Input (SDI), Serial Data Output (SDO) and its own clock (DCLK). The MODE control configures the shadow register either in parallel with the output register or in serial shift mode (see function table). Other devices with this feature are listed below.

Programming

Both the PAL and PROM arrays are programmed on standard logic programmers using the JEDEC programming format. The TiW fuses program from the low to the high state. Programming also sets the architectural fuse which selects between asynchronous initialize or asynchronous output enable; the unprogrammed state is initialize. If asynchronous initialize is selected, asserting the pin low will set all outputs and feedback bits high.

Diagnostics Family Members

PART NUMBER	DESCRIPTION
53/63DA441	1Kx4 PROM (async. enables)
53/63DA442	1Kx4 PROM (async./sync. enables)
53/63DA841	2Kx4 PROM
53/63D1641	4Kx4 PROM (async. enable)
53/63DA1643	4Kx4 PROM (async. initialization)
54/74S818	8-bit register

Power-up Reset

Power-up reset is provided for system start-up in a known state. It has the same effect as initialization; all output register bits go high.

Diagnostic Function Table

INPUTS				OUTPUTS			OPERATION
MODE	SDI	CLK	DCLK	Q_{20}-Q_0	S_{20}-S_0	SDO	
L	X	↑	*	Qn ← PROM	HOLD	S_{20}	Load output register from PROM array
L	X	*	↑	HOLD	$S_n \leftarrow S_{n-1}$ $S_0 \leftarrow$ SDI	S_{20}	Shift shadow register data
L	X	↑	↑	Qn ← PROM	$S_n \leftarrow S_{n-1}$ $S_0 \leftarrow$ SDI	S_{20}	Load output register from PROM array while shifting shadow register data
H	X	↑	*	$Q_n \leftarrow S_n$	HOLD	SDI	Load output register from shadow register
H	L	*	↑	HOLD	$S_n \leftarrow Q_n$	SDI	Load shadow register from output bus and feedback
H	H	*	↑	HOLD	HOLD	SDI	†No operation

* Clock must be steady or falling.
† Reserved operation for 54/74S818 8-Bit Diagnostic Register.

High Speed Programmable Array Logic

PAL32VX10 PAL32VX10A

U.S. Patent 4124899

ADVANCE INFORMATION

Features/Benefits

- 10 input/output macrocells
- Programmable registered or combinatorial outputs
- Dual independent feedback paths allow I/O with combinatorial or feedback register outputs
- Programmable flip-flops allow J-K, S-R, T or D types
- Programmable output polarity
- Register set and register reset can be asynchronous or synchronous
- Automatic register preset on power up
- Varied product term distribution
- Up to 16 product terms per output
- Pin compatible functional superset of 22V10
- Maximum propagation delay
  - 25 ns "A"
  - 35 ns "STD"
- 24-pin 300-mil-wide SKINNYDIP® package or 28-pin chip carriers save space

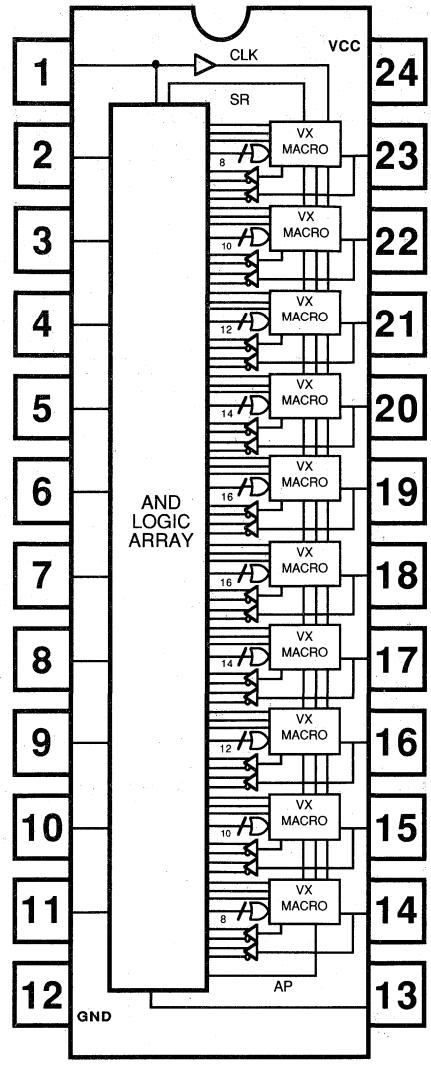
General Description

The PAL32VX10 is a high-density Programmable Array Logic device which implements the familiar sum of products transfer function via a user-programmable AND array and a fixed OR array. Featured are ten highly flexible input/output macrocells which are user configurable for combinatorial or registered operation. Each flip-flop is also programmable to be either J-K, S-R, T, or D-types for optimal design of state machines and other synchronous logic. In addition, a unique dual feedback architecture allows I/O capability for each macrocell in both combinatorial or registered configurations, even when register feedback is present, and allows implementation of buried registers while preserving the macro input function. Supplied in space-saving 300-mil-wide dual in-line packages or 28-pin chip carriers, the PAL32VX10 offers a powerful, space-saving alternative to SSI/MSI logic devices, while providing the advantage of instant prototyping over other semicustom approaches.

The PAL32VX10 is fabricated in Monolithic Memories' advanced, oxide isolated bipolar process for high speed and low power. TiW fuse links provide high reliability and programming yields. Special on-chip test circuits allow full AC, DC, and functional testing before programming. Preloadable output registers facilitate functional testing.

The PAL32VX10 can be programmed on standard PAL® device programmers, fitted with appropriate programming modules and configuration software. Design development is supported by Monolithic Memories' PALASM®2 software as well as by other programmable logic CAD tools available from third-party vendors.

Logic Symbol



17

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Monolithic Memories

The PAL32VX10 is a pin-compatible functional superset of the 22V10 architecture, with an improved macrocell. Details of the PAL32VX10 macrocell are shown in the diagram below. Significant features of the macrocell are:

Dual Feedback Paths. Each macrocell has two completely independent feedback paths associated with each macrocell. One feeds back into the array from the macrocell output pin. The second feeds back into the array from the flip-flop output. This architecture provides I/O capability for both combinatorial and registered outputs, even when register feedback is needed. In addition, it allows registers to be loaded directly from outputs, and provides the capability for buried registers, while permitting use of the macrocell pin as an input.

Programmable Flip-Flops. Each macro has an XOR gate which provides the capability of emulating the operation of J-K, S-R, T, or D flip-flops. When J-K or S-R flip-flops are implemented, the available product term resources for each macrocell are shared between J(S) and K(R) functions, according to the expression:

$$Q := Q :+: (J_1 \ldots J_m)*/Q+(K_1 \ldots K_n)*Q$$

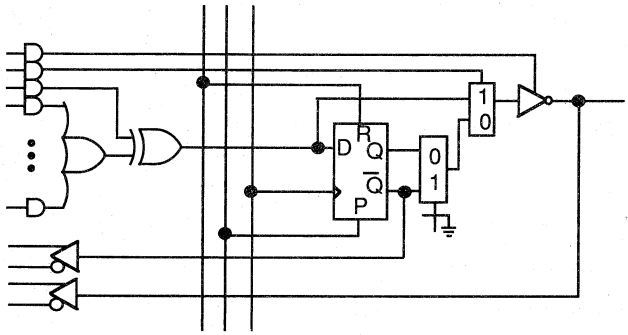
where (m+n) is the total number of product terms found in each macrocell.

Varied Product Term Distribution. The PAL32VX10 has a different number of product terms for each pair of macrocells. There are two macros each with 8, 10, 12, 14, or 16 product terms, to allow optimal use of the available product term resources.

Other Features:

- Macrocells programmable as registered or combinatorial
- Programmable output polarity
- Preset and reset can be synchronous or asynchronous

PAL32VX10 MACROCELL

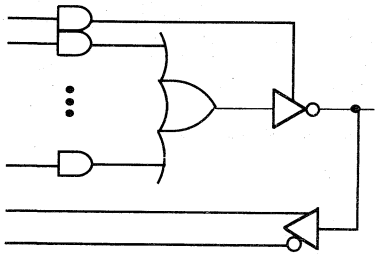


PAL32VX10 MACROCELL CONFIGURATION OPTIONS

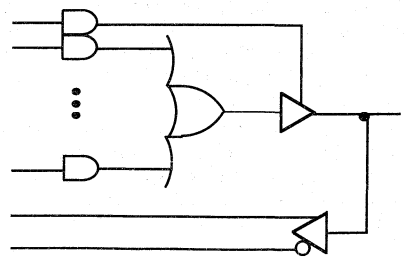
The PAL32VX10 can implement any of the architecture options shown

COMBINATORIAL I/O

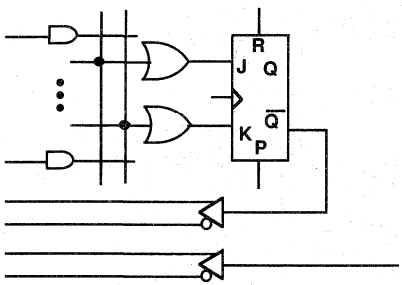
ACTIVE LOW

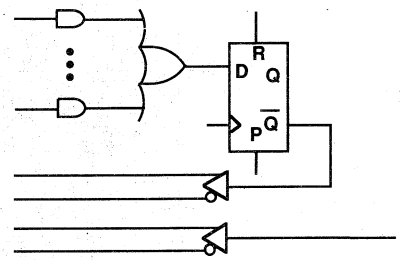


ACTIVE HIGH



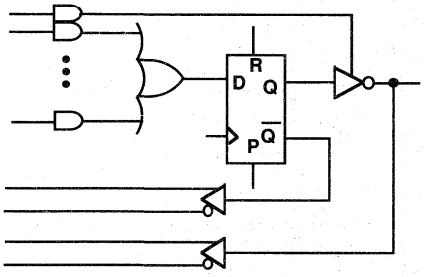
BURIED REGISTER WITH DEDICATED INPUT



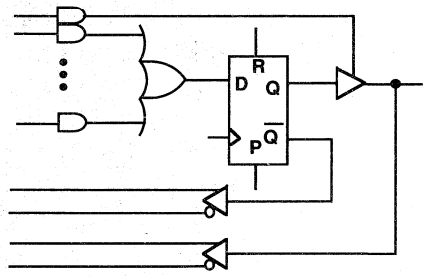


D REGISTER WITH I/O

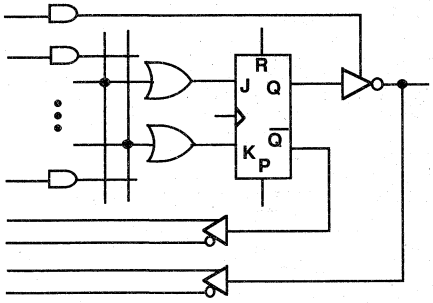
ACTIVE LOW



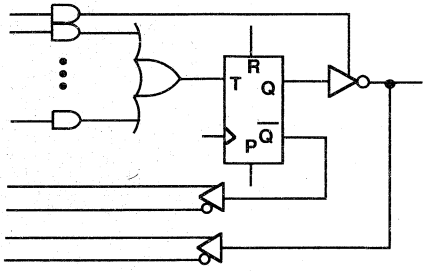
ACTIVE HIGH



J-K REGISTER WITH I/O

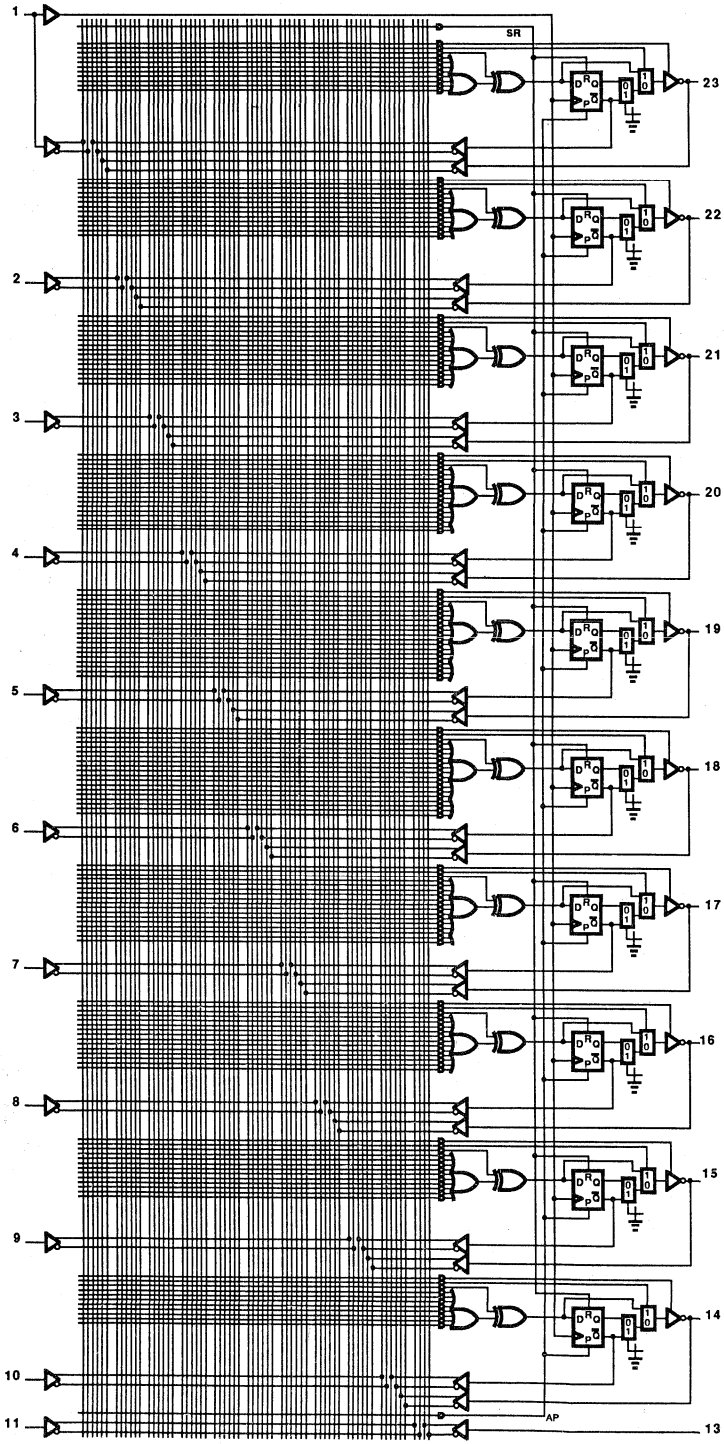


T REGISTER WITH I/O



17

Logic Diagram



PLE5P16
PLE6P16
REVISED
Programmable Logic Element Family

ADVANCE INFORMATION

Features/Benefits

- Programmable replacement for conventional TTL logic
- Reduces IC inventories and simplifies their control
- Expedites and simplifies prototyping and board layout
- Saves space with 24-pin 0.3 inch SKINNYDIP® packages and 28-pin Plastic Leaded Chip Carriers (PLCC)
- Programmed on standard PROM programmers
- Reliable TiW fuses guarantee >99% programming yields
- Test and simulation made simple with PLEASM™ software
- Proposed JEDEC standard pinout
- Revised pinout with center VCC and GND for higher noise immunity

Typical Applications

- Address decoding
- Random logic replacement
- Code converters
- Look-up tables (both trigonometric and arithmetic)
- Data scaling

Preliminary Data

PARAMETER	PLE5P16 STANDARD	PLE6P16 STANDARD
t_{PD}(ns)	15	15
I_{CC} (mA)	180	190

Description

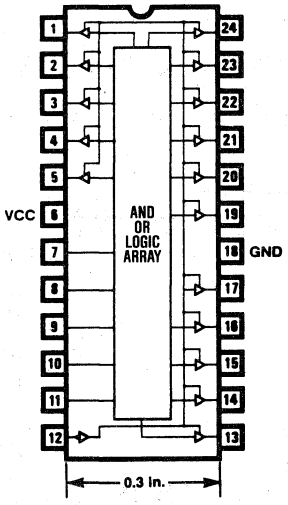
The PLE5P16 and PLE6P16 are the two newest members of the Programmable Logic Element (PLE™) Family. A PLE device has a programmable OR-array, preceded by a fixed AND-array. This provides unlimited product terms and programmable polarity for each output, while maintaining the high speeds necessary for logic applications. The PLE Family complements the PAL® (Programmable Array Logic) Family, which has programmability in the opposite array.

The PLE5P16 has five inputs, sixteen outputs, and thirty-two product terms per output. The PLE6P16 has six inputs, sixteen outputs, and sixty-four product terms per output.

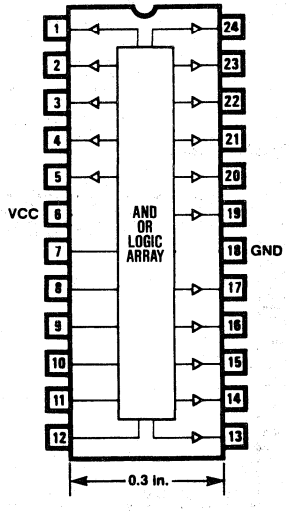
The devices feature low-current PNP inputs and full Schottky clamping; the PLE5P16 has three-state outputs with an output enable. The fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide pre-programming testing which assures high programming yields and high reliability.

Logic Symbols

PLE5P16



PLE6P16



17

TWX: 910-338-2376
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
Monolithic Memories

Ordering Information

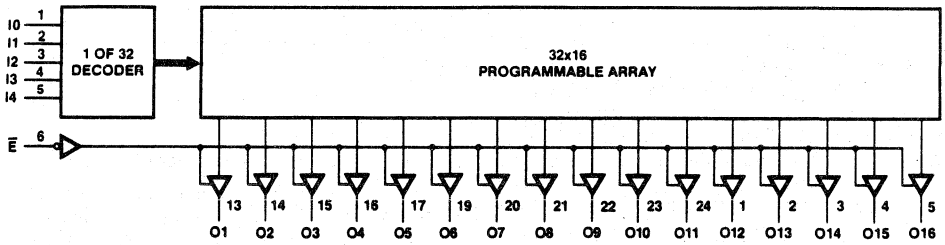
PLE Family

PLE5P16 A C NS SHRP

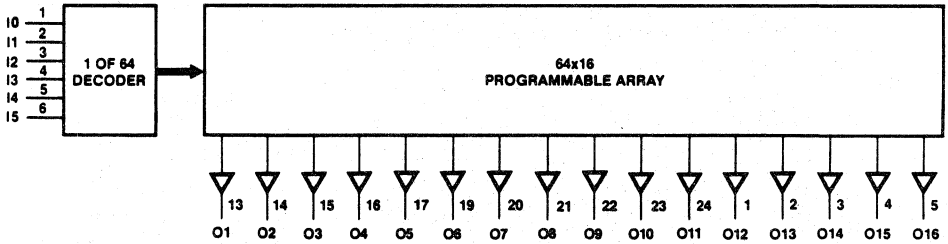
- PROGRAMMABLE LOGIC ELEMENT
- NUMBER OF INPUTS
- OUTPUT TYPE
  - P = Non registered
  - R = Registered
  - RA = Registered asynchronous enable
  - RS = Registered synchronous enable
- NUMBER OF OUTPUTS
- PERFORMANCE
  - Blank = Standard
  - A = Enhanced
- TEMPERATURE RANGE
  - C = 0°C to +75°C
  - M = -55°C to +125°C
- PACKAGE
  - N = Plastic dip
  - NS = SKINNYDIP plastic
  - J = Ceramic dip
  - JS = SKINNYDIP ceramic
  - NL = Plastic leaded chip carrier
  - L = Leadless chip carrier
  - F = Flat pack
  - W = Cerpack
- OPTIONAL PROCESSING
  - SHRP = Reliability Enhanced
  - XXXX = Hi-Rel

Block Diagrams (DIP Pinout)

PLE5P16

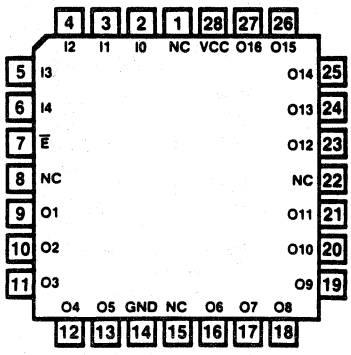


PLE6P16

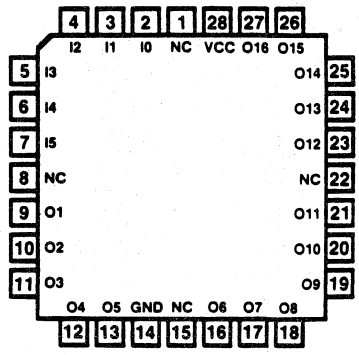


Pin Configurations

PLE5P16



PLE6P16



16-Bit Barrel Shifter Slice 677530

ADVANCE INFORMATION

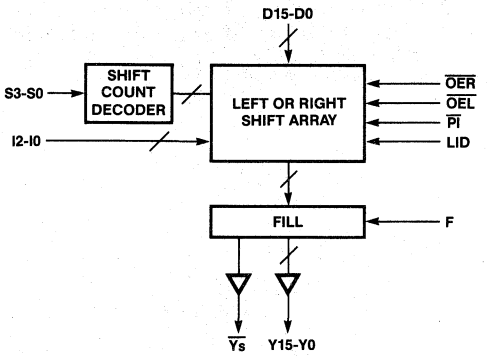
Features/Benefits

- Left/Right shift and rotate to any position within 1 cycle
- Expandable to any multiples of 16-bit paths
- Works on sign magnitude and two's complement shift count inputs
- High speed operation:
  Data to output: 25 ns (max)
  Shift count to output: 30 ns (max)
- Sticky bit available for floating point rounding operation
- Bit insert and bypass operations

Applications

- Mantissa adjustment for floating point addition/subtraction and fixed point scaling in minicomputers, mainframes, array processors and digital signal processors
- Positioning non-numeric patterns in image processing, word processing and symbol processing systems
- Implement a funnel shifter for the Bit Block Transfer operation in graphics
- Implement a compression-expansion engine using the modified Huffman coding method
- Bit insertion for EDAC applications

Block Diagram



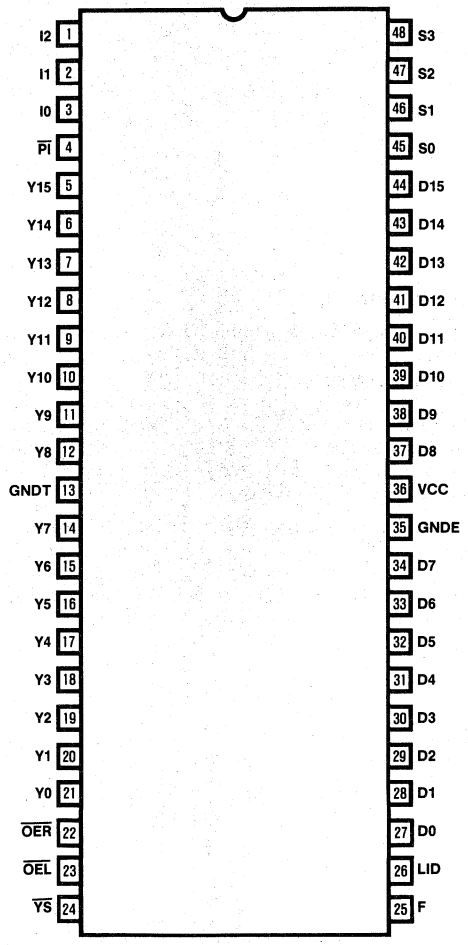
16-Bit Barrel Shifter Slice

Packaging Information

PART NUMBER	PACKAGE	TEMPERATURE
677530	D48	Commercial

Pin Configuration

677530



17

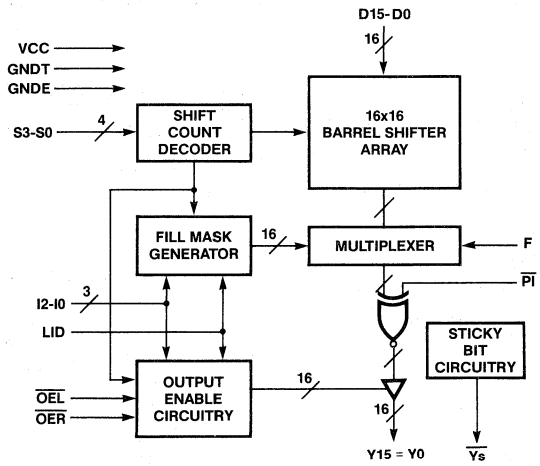


Figure 1. Internal Organization of the '7530 Barrel Shifter Slice

Description

The '7530 16-Bit Barrel Shifter Slice is designed to be used as a general-purpose one-cycle shifter in numerical processing and symbol processing systems. The basic slice can handle data in 16-bit packets, shift and rotate to any desired number of positions within one cycle. They can also be cascaded together to form a barrel shifter function module with longer word length. Cascading shifter slices to form a functional module will not put additional delays into the datapath.

The '7530 can perform nine different operations. A 3-bit opcode (I2-I0) and the $\overline{PI}$ (Polarity Insertion) input determines which function is to be performed. The shift count for the device is determined by the 4-bit input (S3-S0). The entire shifter is combinatorial with no internal states.

All data outputs (Y15-Y0) can be tristated. This output design is crucial to the cascading architecture because outputs from different barrel shifter slices will be tied together in an expanded array. The $\overline{OER}$, $\overline{OEL}$ (Output Enable Right/Left) and the LID (Location IDentifier) input signals together determine the enable states of each individual output.

The F (Fill) input bit provides the signal to be inserted into the outputs.

The $\overline{Ys}$ output (Sticky Bit) is provided as an open collector output. It is the negation of the logical OR of all the bits shifted out during the shift left or shift right operation.

The $\overline{PI}$ (Polarity/Insertion) input is used to complement the outputs for all the opcodes except when I = 010 when it is used to distinguish between Bit InserT and BYPass operation.

Architecture

As shown in Figure 1, the architecture of the '7530 Barrel Shifter Slice is centered around the internal barrel shifter array and the shift count decoder. The outputs of the array are fed into a mask generator which determines the enable states of each individual data outputs. These enable states are primarily determined by the LID (Location IDentifier) input signal that represents the location of each shifter slice when they are cascaded. The Location IDentifier will transform the actual operation of every shifter to make cascading possible. Please refer to the section *Cascading Architecture for the Barrel Shifter Slice* for a detailed description.

The output control circuitry consists of the polarity control, Fill bit insertion and Sticky Bit generation.

Two enable inputs, OEL and OER, provide the tristate control to the two portions of the output data separated by the left margin (D15) of the original input data.

Signal Description

D15-D0: Inputs. Input data to the Barrel Shifter Slice.

Y15-Y0: Outputs. Output data from the Barrel Shifter Slice.

I2-I0: Inputs. A 3-bit opcode to select one of nine possible operations for the device. Please see Table 1 for further detail.

S3-S0: Inputs. Shift count input. For opcodes 00X or 11X (i.e., I2I1I0 = 0, 1, 6 or 7), S3-S0 represent the magnitude of bit positions shifted or rotated. For opcodes 10X (i.e., I2I1I0 = 4 or 5), the number of bits to be shifted or rotated is given by the two's complement of the five-digit number: I2S3S2S1S0. Since I2 = 1 in both cases, only sixteen different bit positions (ranging from +1 to +16) are allowed within one cycle. For the opcodes X01 (i.e., I2I1I0 = 1 or 5), the shift count inputs can be considered in two ways: either as a rotate right two's complement I2S3S2S1S0 operation or as a rotate left S3S2S1S0 operation when I2 = 0.

$\overline{PI}$: Input. Polarity/Insertion signal input. This signal serves two purposes. When the opcode is 010 (i.e., I2I1I0 = 2), it is used to resolve between Bit InserT operation ($\overline{PI}$ = 0) and BYPass operation ($\overline{PI}$ = 1). When the opcode is in some other states, $\overline{PI}$ determines the output data polarity ($\overline{PI}$ = 0 for complemented data, $\overline{PI}$ = 1 for uncomplemented (true) data).

F: Input. Fill bit input. The value of this input is used to insert into positions left empty from shift operations, or insert into the designated bit positions for the Bit InserT and FILL operations.

$\overline{Ys}$: Output. The inverse of the sticky bit. This is an open collector output signal. Functionally this signal is the negation of the logical OR of the bits shifted out in the shift left/right operations. In the Bit Insertion operation, $\overline{Ys}$ is the negation of the input bit that is replaced by the Fill bit.

LID: Input. Location IDentifier. The input to this pin can either be VCC, ground, or left open. In the case when the input is open, there is an internal resistor network to divide this signal to 2.5 V (VCC/2). The LID signal is used in the expansion scheme of the barrel shifter slices. Different barrel shifter slices can be cascaded in a two-dimensional array to form a barrel shifter module of wider path width. The LID input signal is required to be one of the above three states according to its position inside the array.

$\overline{OEL}$, $\overline{OER}$: Inputs. Output enable left and output enable right. These two signals will separately enable the left and the right halves of the output data separated by the left margin (D15) of the input word.

GNDE, GNDT: Power supply grounds. GNDE is the internal ECL circuit ground and GNDT is the internal TTL cricuit ground. These two ground signals should be routed separately in the system. The ECL ground is more sensitive to noise problems and should be bypassed with capacitive components to VCC.

VCC: Power supply. A +5 V power supply to the internal circuit of the Barrel Shifter Slice.

Function Tables

OPCODE			POLARITY/ INSERT	OPERATION PERFORMED IF LID PIN IS "OPEN"		OUTPUT POLARITY	ALTERNATE OPERATION	
							LID =	LID =
I_2	I_1	I_0	$\overline{PI}$	MN.	NAME		V_{CC}	GND
0	0	0	0	LSH	Left SHift	Complemented	LRT	FIL
			1			True		
0	0	1	0	LRT	Left RoTate	Complemented	LRT	LRT
			1			True		
0	1	0	0	BIT	Bit InserT	True	High Z	High Z
			1	BYP	BYPass	True	High Z	High Z
0	1	1	0	FIL	FILL	Complemented	High Z	High Z
			1			True	High Z	High Z
1	0	0	0	RSC	Right Shift with two's—	Complemented	FIL	RRC
			1		Complement shift count	True		
1	0	1	0	RRC	Right Rotate with two's—	Complemented	RRC	RRC
			1		Complement rotate count	True		
1	1	0	0	RSH	Right SHift	Complemented	FIL	RRT
			1			True		
1	1	1	0	RRT	Right RoTate	Complemented	RRT	RRT
			1			True		

Figure 1. Shifter Instruction Set

16x16 Bit CMOS Multiplier
67C7016 - 35/- 45/- 55
67C7017 - 35/- 45/- 55

ADVANCE INFORMATION

Features/Benefits

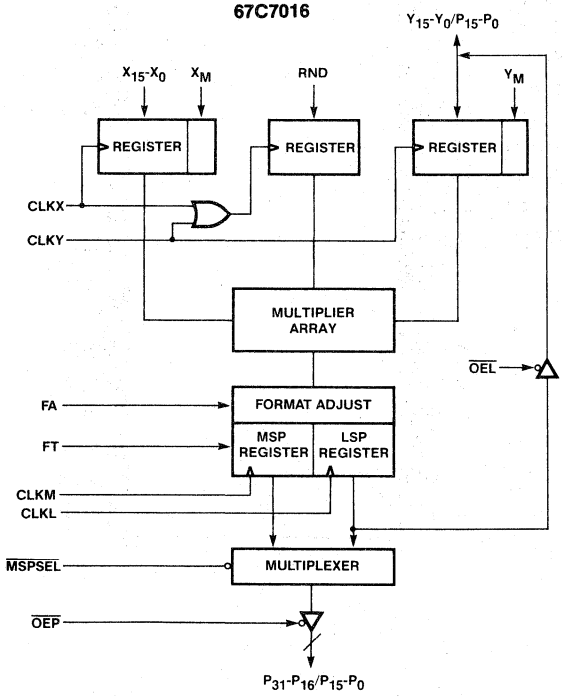
- 16x16 parallel multiplier
- High speed multiply
  - 35 ns Max '7016-35/'7017-35
  - 45 ns Max '7016-45/'7017-45
  - 55 ns Max '7016-55/'7017-55
- Low power CMOS technology
  - Zero standby power
  - 7 mA per MHz active I_{CC} (Typical)
- Mixed mode 2's complement, unsigned or mixed operand
- '7017 is optimized for microprocessor systems, single clock with register enables
- Plug-in compatible with TRW MPY016H/K, AMD29516/A, 29517/A
- Single 5 V supply
- Available in DIP or PLCC

Packaging Information

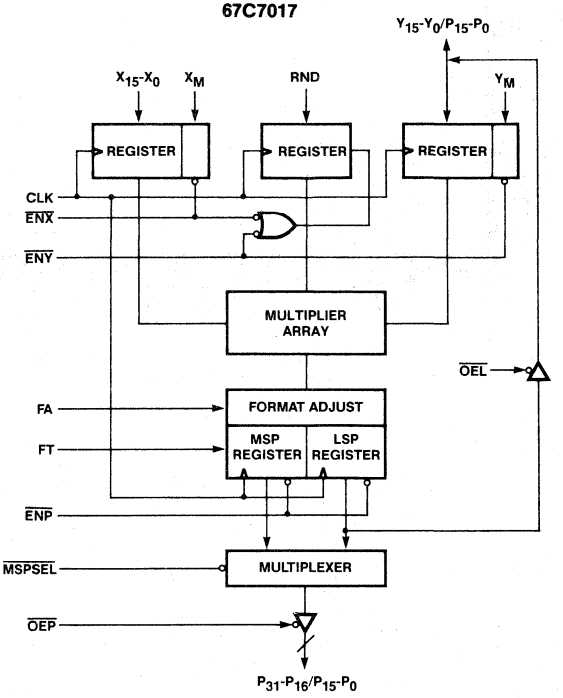
PART NUMBER	SPEED (T_{MC})	PACKAGE	TEMP
67C7016-35	35 ns	J,N,NL(68)	Com
67C7017-35	35 ns	J,N,NL(68)	Com
67C7016-45	45 ns	J,N,NL(68)	Com
67C7017-45	45 ns	J,N,NL(68)	Com
67C7016-55	55 ns	J,N,NL(68)	Com
67C7017-55	55 ns	J,N,NL(68)	Com

Functional Block Diagrams

67C7016



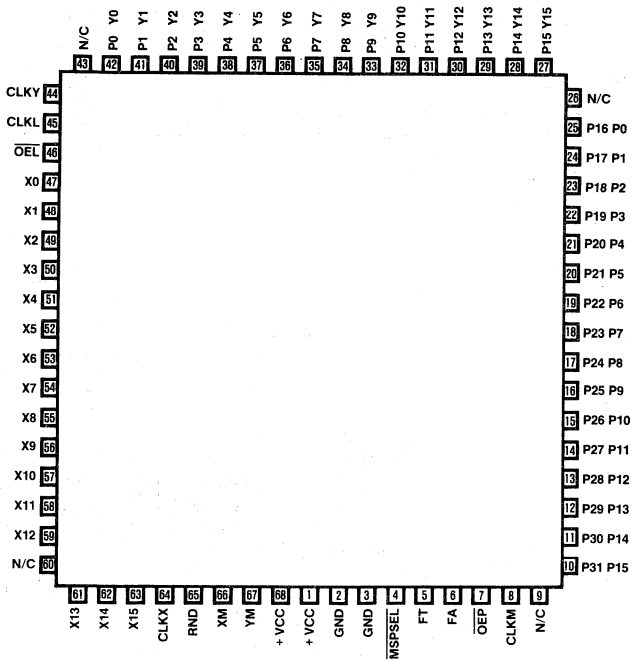
67C7017



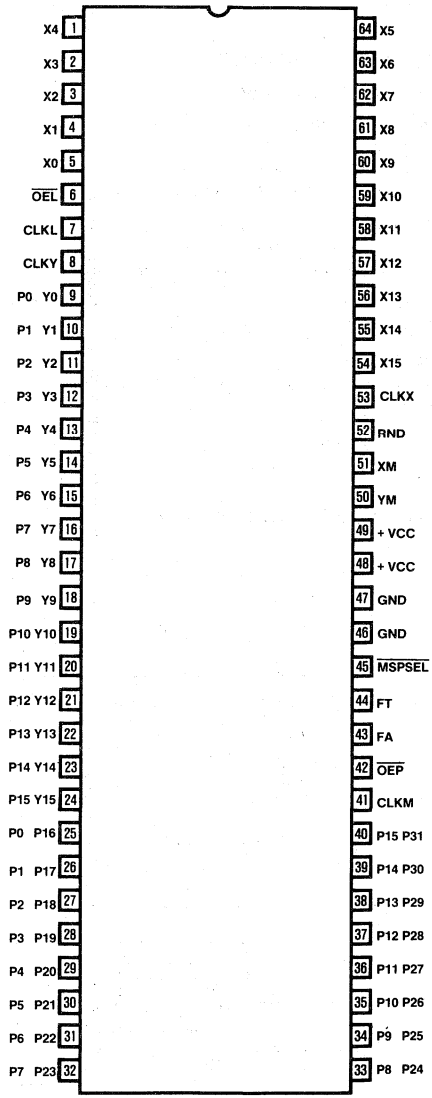
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374
Monolithic Memories

Pin Configurations

67C7016
68 Pin PLCC

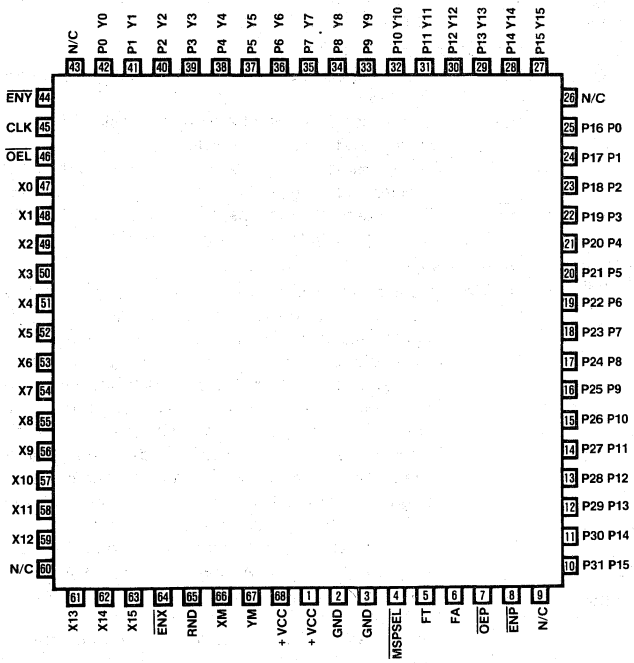


67C7016
64 Pin DIP

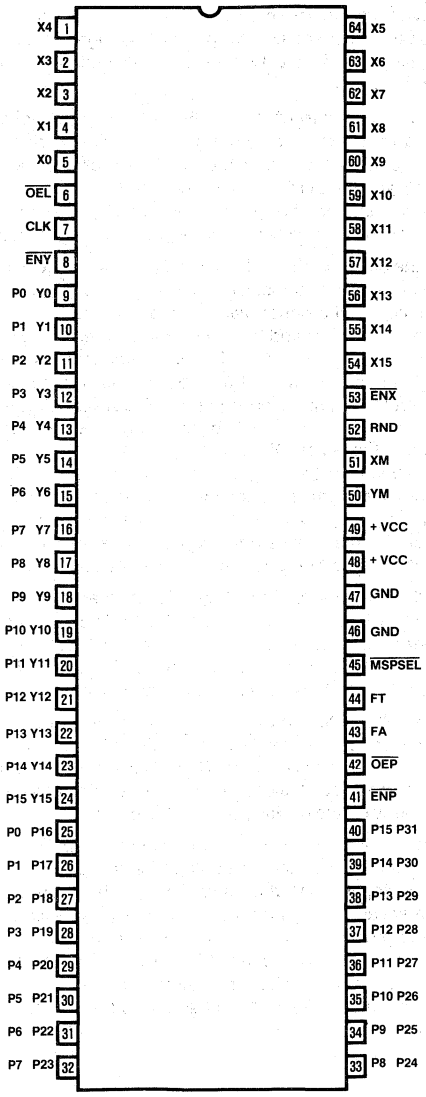


Pin Configurations

67C7017
68 Pin DIP



67C7017
64 Pin DIP



17

Descriptions

The '7016/7017 are CMOS 16x16 high speed parallel multipliers. Designed with state-of-the-art CMOS technology and a multiplication scheme based on modified Booth's algorithm, these devices can achieve bipolar TTL speed at a significantly reduced power level. In addition, the product is designed to be pin-for-pin replacement for the TRW MPY016H/K and the AMD 29516/A, 29517/A.

The architecture of the '7016/7017 family generates a 32-bit product of two 16-bit input operands. Two 16-bit registers are provided for the X and Y operands. These operands can be specified as either 2's complement or unsigned numbers through the XM and the YM control inputs. These two signals are registered simultaneously at their respective operand clocks.

At the output of the multiplier array a format adjust control (FA) allows the user to select either a full 32-bit product or a left shifted 31-bit product. Two 16-bit output registers are provided to hold the most and least significant halves of the result (MSP and LSP) as defined by FA. For asynchronous output these registers may be made transparent by taking the feed through control (FT) high. A round control (RND) allows the rounding of the MSP. This control is registered, and is entered at the rising edge of the logical OR of both CLKX and CLKY for the '7016 and is enabled by a LOW signal in either ENX or ENY in the '7017. the two halves of the product may be routed to a 16-bit three-state output port (P) via a multiplexer. In addition the LSP is connected to the Y-input port through a separate three-state buffer so that a 32-bit product can be available simultaneously.

In the '7016, the X, Y, MSP and LSP registers have independent clocks (CLKX, CCLKY, CLKM, CLKL). The output multiplexer control ($\overline{\text{MSPSEL}}$) uses a pin which is a supply ground in the TRW MPY16H. When this control is LOW the function is that of the MPY16H, thus allowing full compatibility.

The '7017 differs in that it has a single clock input (CLK) and three register enables ($\overline{\text{ENX}}$, $\overline{\text{ENY}}$, $\overline{\text{ENP}}$) for the two input registers and the entire product. This facilitates the use of the part in microprocessor systems. In both parts data is entered into the registers on the positive edge of the clock.

The '7016/7017 family has a wide variety of applications in high performance computers and digital signal processing. In computer applications this multiplier can be used to construct numerical processing functional units (e.g., array processors, matrix processors, floating point multiplier/dividers etc.). In digital signal processing the multiplier can be used to construct special algorithm engines for applications like digital filtering, FFT, speech recognition and synthesis, adaptive controls and image processing.

Signal Description

Input/Output data

X15-X0: 16 bit data inputs.

Y15-Y0: 16 bit data inputs. These inputs are multiplexed with the least significant product (LSP) outputs.

P15-P0: The least significant product (LSP) outputs. These signals are multiplexed with the Y data inputs. The product term is available when OEL is low. Alternatively, these outputs can be accessed from the MSP output port when MSPSEL is high.

P31-P16: The most significant product (MSP) outputs.

Input Clocks (67C7016 only)

CLKX: The rising edge of this clock loads the input data (X15-X0) and the associated mode control signal XM into the input register.

CLKY: The rising edge of this clock loads the input data (Y15-Y0) and the associated mode control signal YM into the input register.

CLKM: The rising edge of this clock loads the most significant product (MSP) output register.

CLKL: The rising edge of this clock loads the least significant product (LSP) output register.

Input Clocks (67C7017 only)

CLK: The rising edge of this clock loads all input/output registers.

$\overline{\text{ENX}}$: Clock enable for the X15-X0 input register, XM input register and the round register.

$\overline{\text{ENY}}$: Clock enable for the Y15-Y0 input register, YM input register and the round register.

$\overline{\text{ENP}}$: Clock enable for the most significant product (MSP) and least significant product (LSP) register.

Control Signals

XM, YM: Mode control signals for the input data word. A low input indicates unsigned data format and a high input represents 2's complement data format.

FA: Format Adjust. When this input is high, a full 32-bit product is produced in MSP and LSP registers. When this input is low, the sign bit will appear in the most significant bit of both the MSP and the LSP. In such cases only a 31-bit product is provided. The FA input is required to be a high when either integer unsigned magnitude or mixed mode formats are used. (See the DATA FORMATS section for further detail.)

FT: Flow-through. When this input is high, both the MSP register and the LSP register are transparent.

$\overline{\text{OEL}}$: Three-state enable signal for routing LSP to the Y/LSP I/O ports.

$\overline{\text{OEP}}$: Three-state enable signal for the product output port.

RND: Round control signal for the most significant product (MSP). When this input is high, a one will be added to the most significant bit of the least significant product (LSP). This rounding operation is done before the output is sent to the format adjust clock. As a result, the location of this round bit in the final product depends on the FA input. When FA = 0, the round bit is added to location P14; when FA = 1, the round bit is added to location P15. The RND input is registered at the rising edge of the logical OR of both the CLKX and CLKY. In the single clock architecture, the RND register is enabled when either the X register or the Y register is enabled.

$\overline{\text{MSPSEL}}$: When the $\overline{\text{MSPSEL}}$ input is low, the MSP is available for the output port. When this input is high, the LSP is available at the output port.

16-Bit CMOS Multiplier Slice
67C7555 67C7556

ADVANCE INFORMATION

Features/Benefits

- **Twos-complement, unsigned, or mixed operands**
- **Full 32-bit product immediately available on each cycle**
- **High-speed 16x16 parallel multiplier**
- **Latched or registered inputs/outputs**
- **Three-state output controls, independent for each half of the product**
- **Single +5 V supply (via multiple pins)**
- **Zero standby power CMOS technology**
- **Available in 84-terminal Leadless-Chip Carrier and 88-Pin-Grid-Array packages**

Description

The 'C7555 and 'C7556 are high-speed 16x16 combinatorial multipliers which can multiply two 16-bit unsigned or signed twos-complement numbers on every cycle. Each operand X and Y has an associated mode-control line, XM and YM respectively. When a mode-control line is at a LOW logic level, the operand is treated as an unsigned 16-bit number; when the mode-control line is at a HIGH logic level, the operand is treated as a 16-bit signed twos-complement number. Additional inputs RS and RU allow the addition of a bit into the multiplier array at the appropriate bit positions for rounding.

Ordering Information

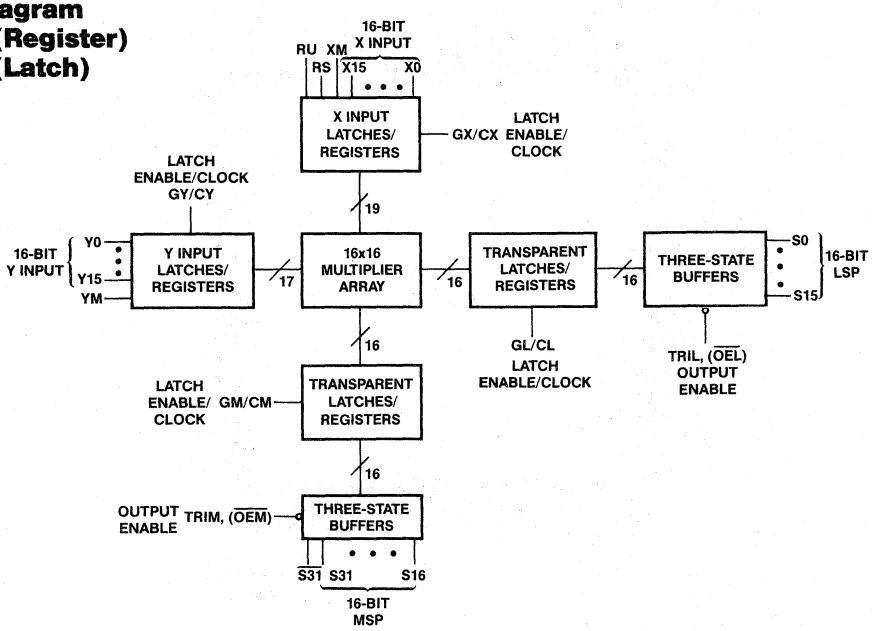
PART NUMBER	PACKAGE	TEMPERATURE
67C7555	P88, L84	Com
67C7556	P88, L84	Com

The entire 32-bit double-length product is available at the outputs at one time.

The most-significant product bit, S31, is available in both true and complemented form to simplify longer-wordlength multiplications. The product outputs are three-state, controlled by assertive-low enables. The MSP outputs are controlled by the TRIM ($\overline{OEM}$) control input, while the LSP outputs are controlled by the TRIL ($\overline{OEL}$) control input. This allows one or more multipliers to be connected to a parallel bus or to be used in a pipelined system.

All inputs and outputs have transparent latches in the 'C7556. The latches become transparent when the input to the corresponding gate control line GX, GY, GM, GL is HIGH. If latches are not required, these control inputs may be tied HIGH, leaving the multiplier fully transparent for combinatorial cascading. The device uses a single +5 V power supply, and is available both in an 84-terminal leadless chip carrier (LCC) package and in an 88-pin-grid-array package.

Block Diagram
'C7555 (Register)
'C7556 (Latch)



17

SUMMARY OF SIGNALS/PINS	
X_{15-0}	Multiplicand 16-bit data inputs
Y_{15-0}	Multiplier 16-bit data inputs
XM, YM	Mode-control inputs for each data word; LOW for unsigned data and HIGH for twos-complement data
S_{31-0}	Product 32-bit output
$\overline{S}_{31}$	Inverted MS product bit (for expansion)
RS, RU	Rounding inputs for signed and unsigned data, respectively
GX/CX	Gate contro/clock for X_i, RS, RU
GY/CY	Gate control/clock for Y_i
GL/CL	Gate control/clock for least-significant half of product
GM/CM	Gate control/clock for most-significant half of product
TRIL / $\overline{OEL}$	Three-state control for least-significant half of product
TRIM / $\overline{OEM}$	Three-state control for most-significant half of product

Rounding Inputs

INPUTS		ADDS		USUALLY USED WITH	
RU	RS	2^{15}	2^{14}	XM	YM
L	L	No	No	X	X
L	H	No	Yes	H†	H†
H	L	Yes	No	L	L
H	H	Yes	Yes	*	*

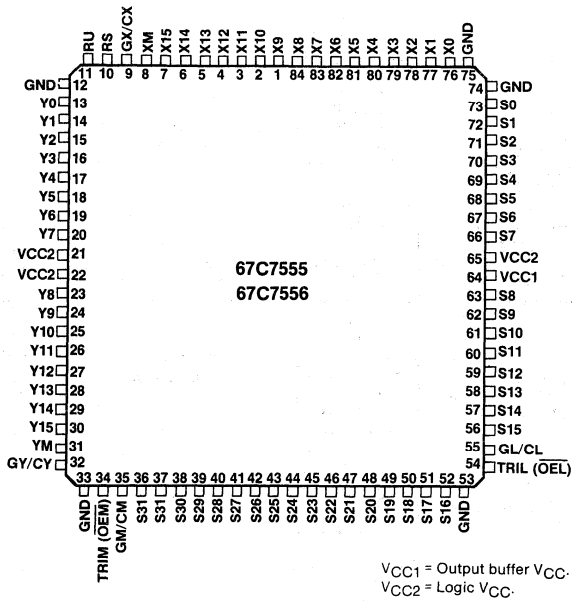
† In mixed mode, one of these could be low but not both.

* Usually a nonsense operaion.

Mode-Control Inputs

OPERATING MODE	INPUT DATA		MODE-CONTROL INPUTS	
	X_{15-0}	Y_{15-0}	XM	YM
Unsigned	Unsigned	Unsigned	L	L
Mixed	Unsigned	Twos-Comp.	L	H
	Twos-Comp.	Unsigned	H	L
Signed	Twos-Comp.	Twos-Comp.	H	H

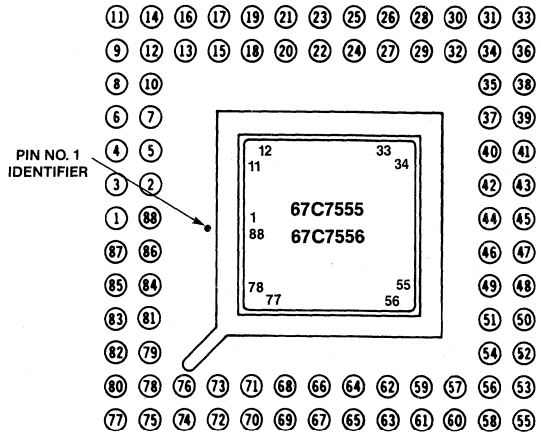
84-Terminal Leadless Chip Carrier Pinout



V_{CC1} = Output buffer V_{CC}.
V_{CC2} = Logic V_{CC}.

All V_{CC} and GND pins must be connected to the respective V_{CC} and GND connections on the board and should not be used for daisychaining through the IC.

88 Pin-Grid-Array Pin Location Bottom View

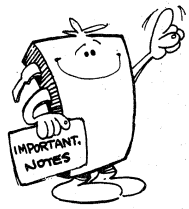


Pin-Guide for Pin Grid Array

PIN NUMBER	PIN NAME	PIN NUMBER	PIN NAME	PIN NUMBER	PIN NAME	PIN NUMBER	PIN NAME
1	X9	23	N/C*	45	S25	67	V_{CC2}†
2	X10	24	Y8	46	S24	68	N/C*
3	X11	25	Y9	47	S23	69	S7
4	X12	26	Y10	48	S22	70	S6
5	X13	27	Y11	49	S21	71	S5
6	X14	28	Y12	50	S20	72	S4
7	X15	29	Y13	51	S19	73	S3
8	XM	30	Y14	52	S18	74	S2
9	GX/CX	31	Y15	53	S17	75	S1
10	RS	32	YM	54	S16	76	S0
11	RU	33	GY/CY	55	GND	77	GND
12	GND	34	N/C*	56	TRIL ($\overline{OEL}$)	78	N/C*
13	Y0	35	GND	57	GL/CL	79	GND
14	Y1	36	TRIM ($\overline{OEM}$)	58	S15	80	X0
15	Y2	37	GM/CM	59	S14	81	X1
16	Y3	38	$\overline{S31}$	60	S13	82	X2
17	Y4	39	S31	61	S12	83	X3
18	Y5	40	S30	62	S11	84	X4
19	Y6	41	S29	63	S10	85	X5
20	Y7	42	S28	64	S9	86	X6
21	V_{CC2}†	43	S27	65	S8	87	X7
22	V_{CC2}†	44	S26	66	V_{CC1}††	88	X8

* Not connected. † V_{CC2} = Logic V_{CC}. †† V_{CC1} = Output buffer V_{CC}.

17


IMPORTANT
NOTES

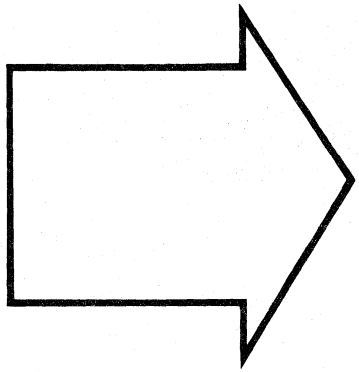
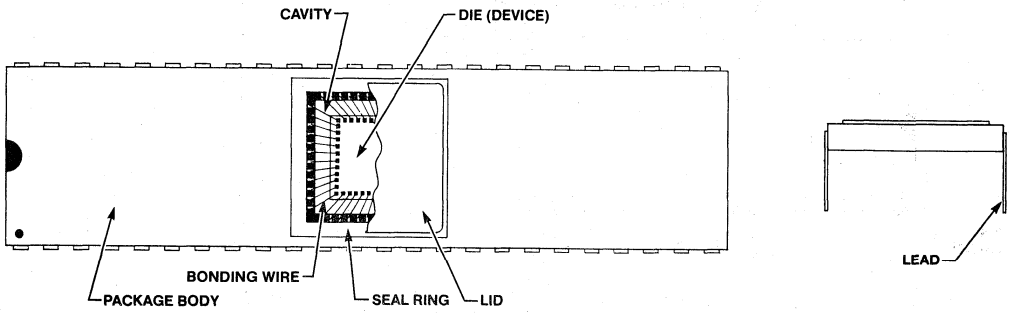


Table of Contents

PACKAGE DRAWINGS

Package Drawing

Side Brazed Package



PACKAGE BODY
Alumina
(Standard Dark)

LID
Gold Plated Kovar With
Nickel Underplating

LEAD MATERIAL
Alloy 42

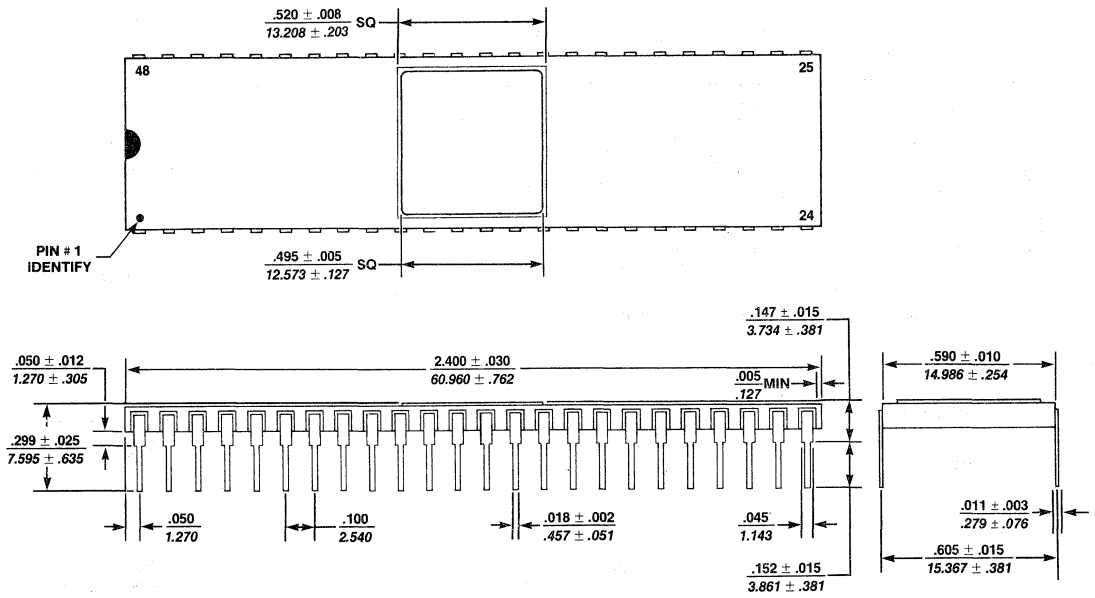
BONDING WIRE
1.25 Mil Aluminum

CAVITY/SEAL RING
Gold Over Nickel
Over Tungsten

LEAD FINISHES
Gold Plate (Standard)
Solder Dip Over Gold Plate

Package Drawings

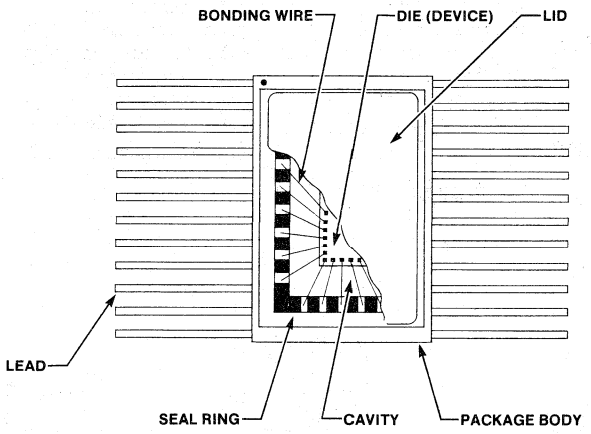
48D Side Brazed Ceramic DIP
(1/2"x2 7/16")



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

Package Drawing

Flat Pack



PACKAGE BODY
Alumina

BONDING WIRE
1.25 Mil Aluminum

LID
Gold Plated Kovar With Nickel Underplating

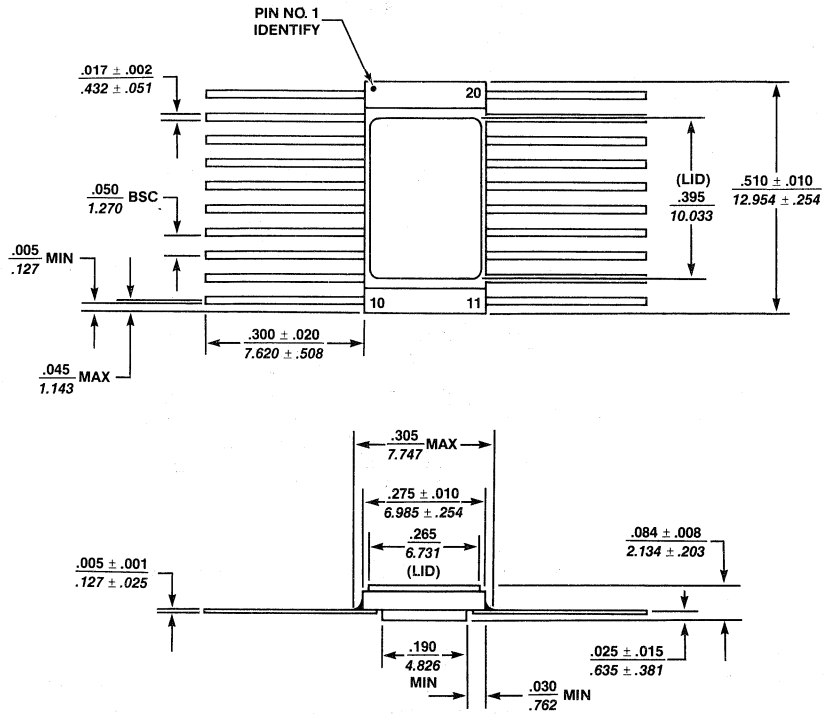
CAVITY/SEAL RING
Gold Over Nickel Over Tungsten

LEAD MATERIAL
Alloy 42

LEAD FINISHES
Gold Plate (Standard)
Solder Dip Over Gold Plate

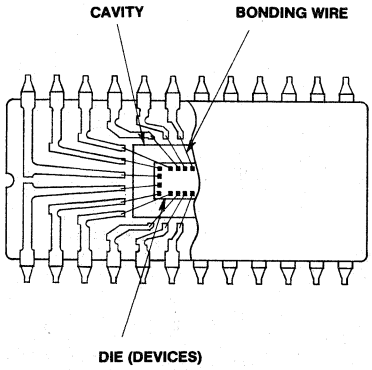
Package Drawing

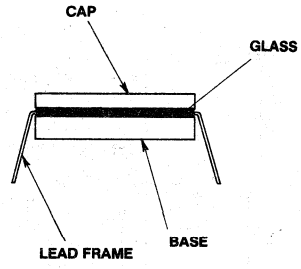
20F Flat Pack
Mil-M-38510,
Appendix C, F-9



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

Package Drawing





LEAD FRAME
Alloy 42

BONDING WIRE
1.25 Mil Aluminum

CAP AND BASE
Pressed Alumina

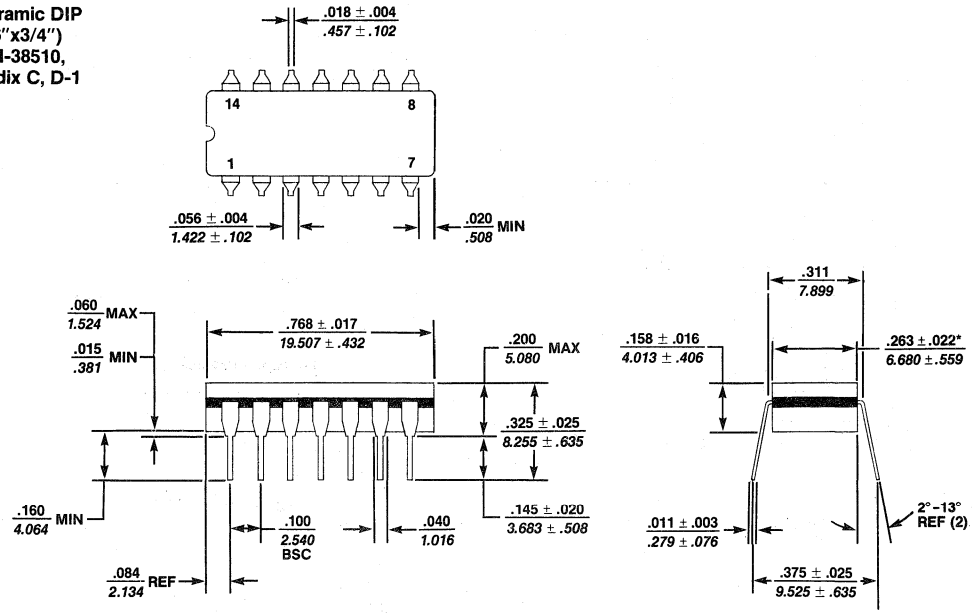
GLASS
Vitreous
Solder Glass

CAVITY
Gold Over Alumina
For Eutectic Die Attach

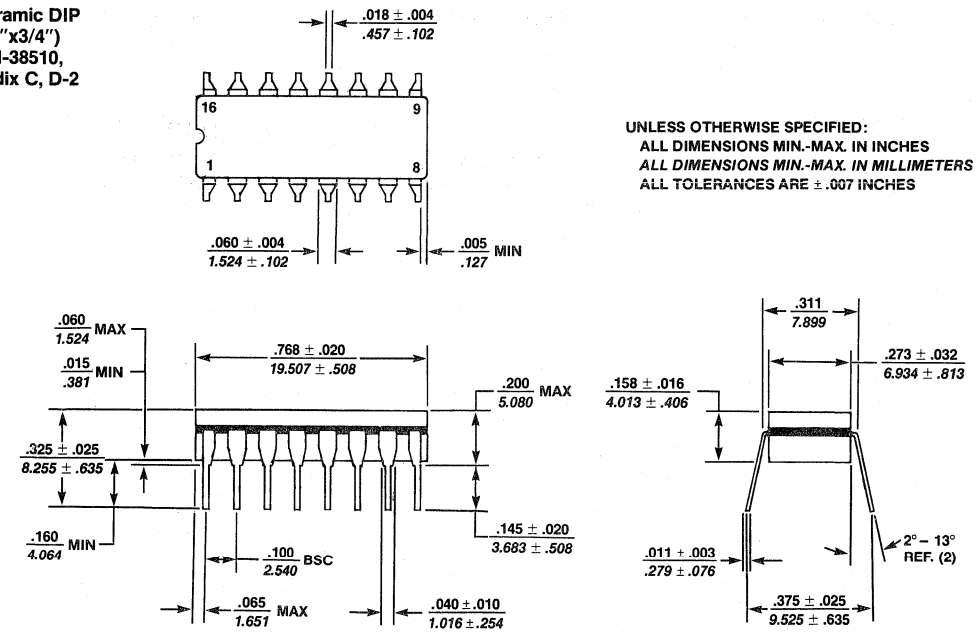
LEAD FINISHES
Solder DIP Over
Matte Tin Plate

Package Drawings

14J Ceramic DIP (5/16"x3/4") Mil-M-38510, Appendix C, D-1



16J Ceramic DIP (5/16"x3/4") Mil-M-38510, Appendix C, D-2



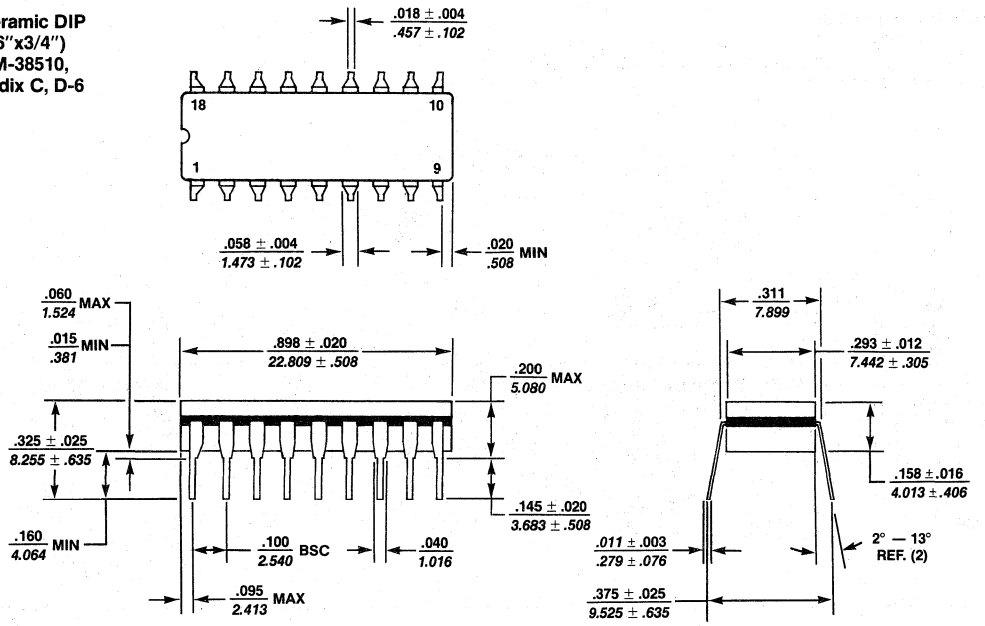
UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

Notes:

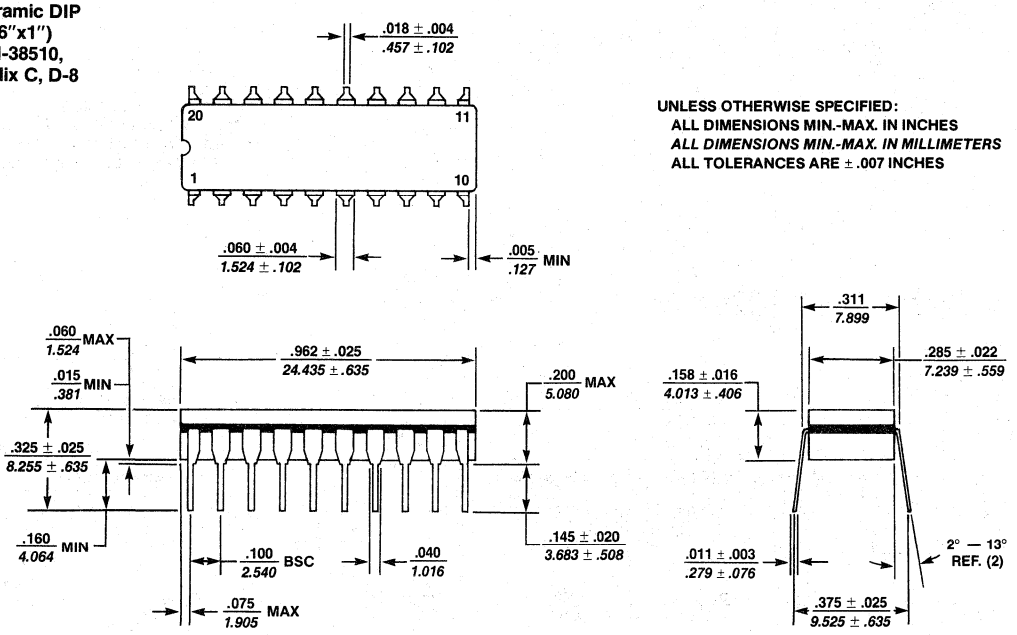
1. Specified body dimensions allow for differences between SSI, MSI and LSI packages.
2. Lead material tolerances are for tin plate finish only. Solder dip finish adds 2-10 mils thickness to all lead tip dimensions.

Package Drawings

18J Ceramic DIP (5/16"x3/4") Mil-M-38510, Appendix C, D-6



20J Ceramic DIP (5/16"x1") Mil-M-38510, Appendix C, D-8



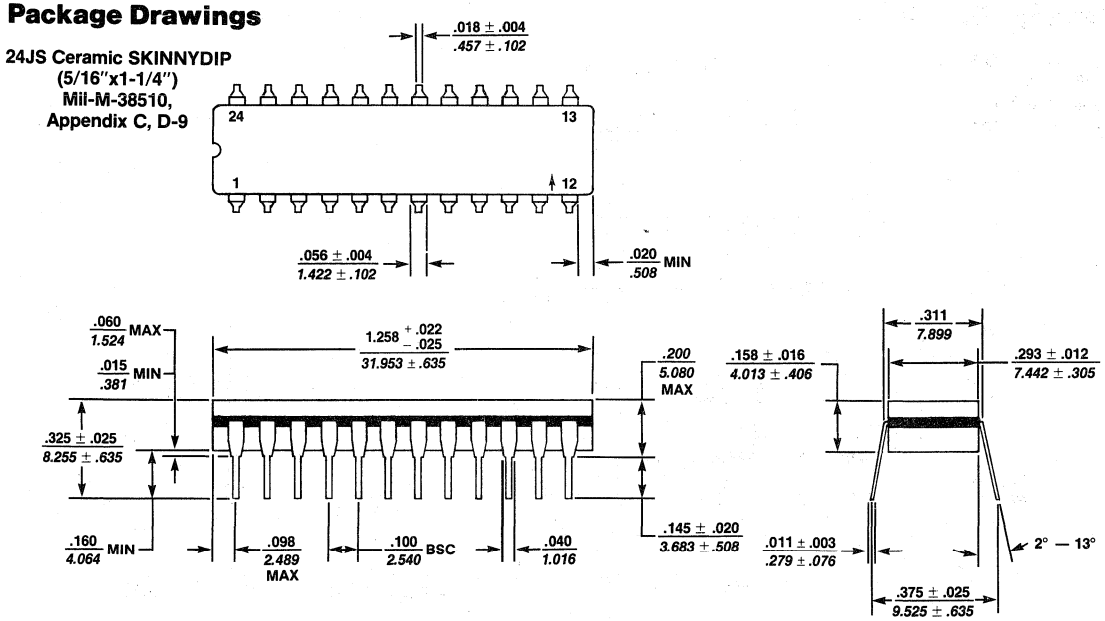
UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

Notes:

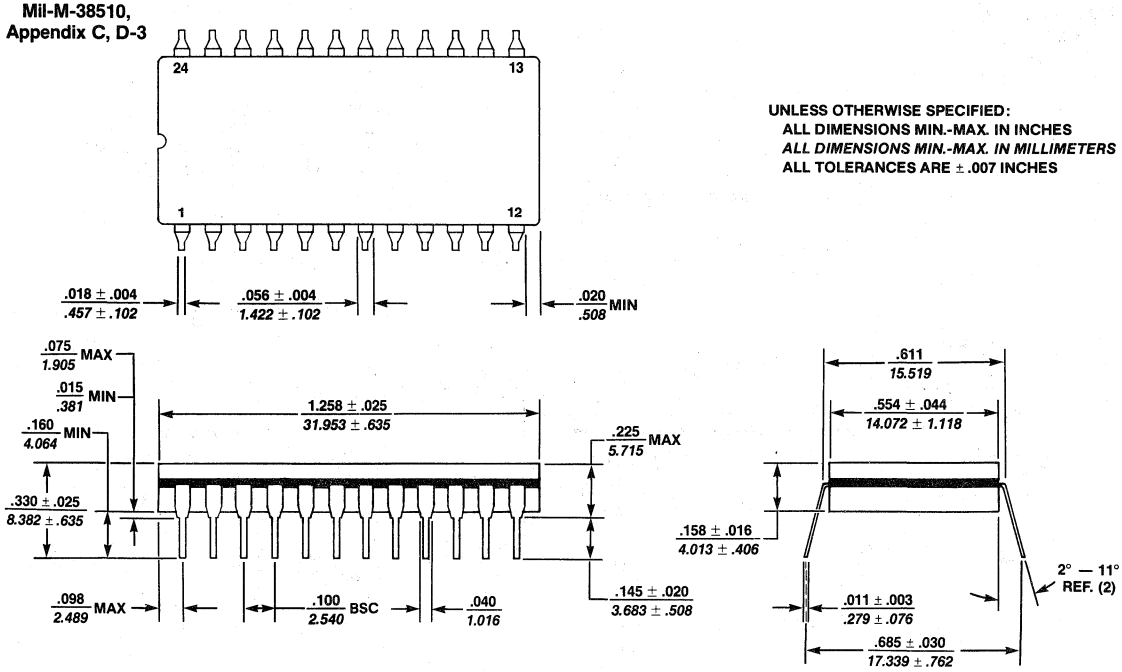
1. Specified body dimensions allow for differences between SSI, MSI and LSI packages.
2. Lead material tolerances are for tin plate finish only. Solder dip finish adds 2-10 mils thickness to all lead tip dimensions.

Package Drawings

24JS Ceramic SKINNYDIP
(5/16"x1-1/4")
Mil-M-38510,
Appendix C, D-9



24J Ceramic DIP
Mil-M-38510,
Appendix C, D-3



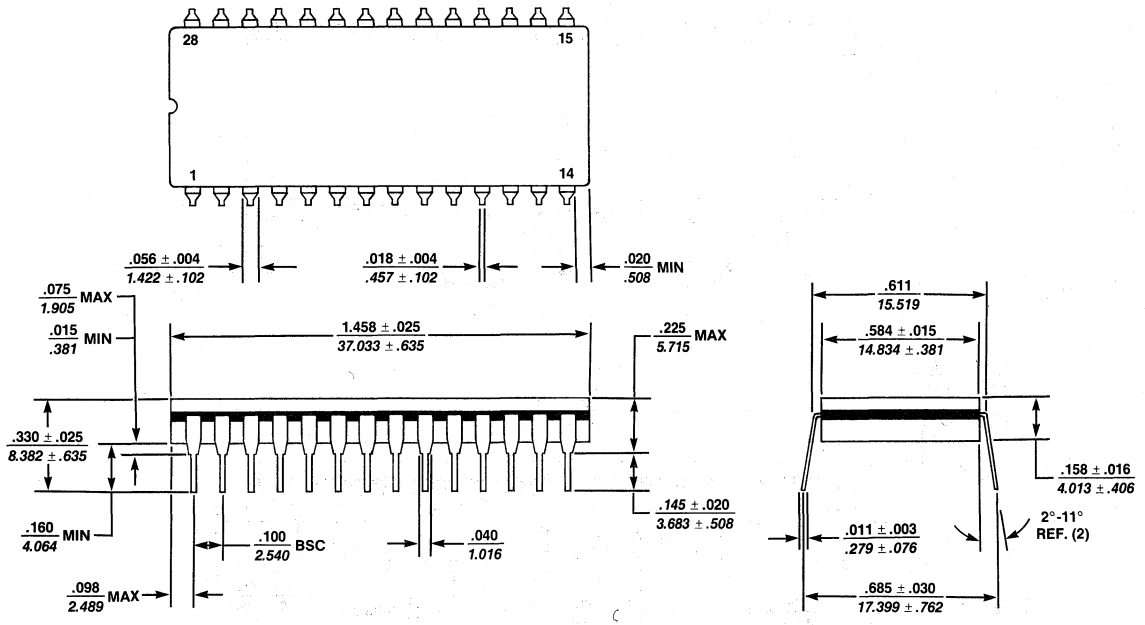
UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

Notes:

1. Specified body dimensions allow for differences between MSI and LSI packages.
2. Lead material tolerances are for tin plate finish only. Solder dip finish adds 2-10 mils thickness to all lead tip dimensions.

Package Drawing

28J Ceramic DIP
(1/2"x1 1/2")

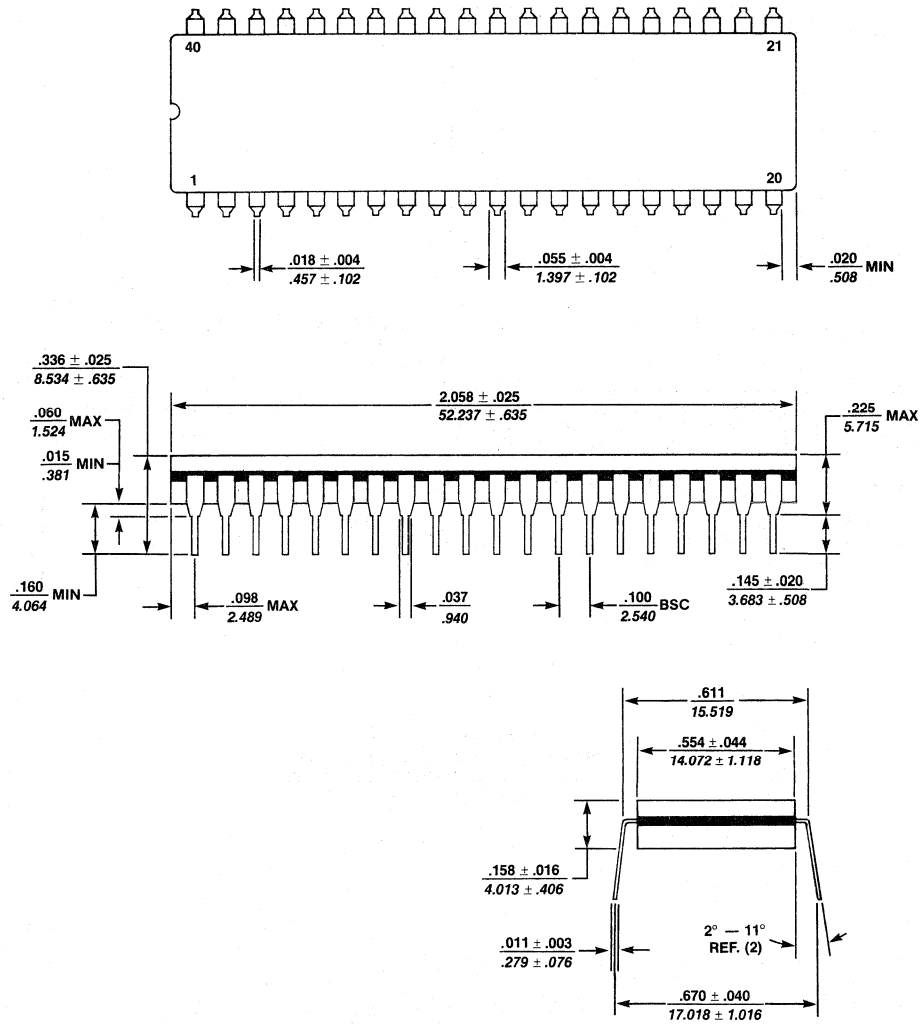


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

18

Package Drawing

40J Ceramic DIP
(9/16"x2-1/16")
Mil-M-38510,
Appendix C, D-5

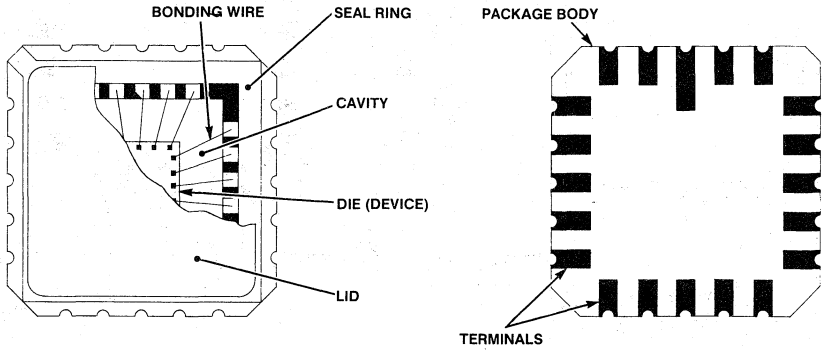


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

Notes:

1. Specified body dimensions allow for differences between MSI and LSI packages.
2. Lead material tolerances are for tin plate finish only. Solder dip finish adds 2-10 mils thickness to all lead tip dimensions.

Leadless Chip Carrier



PACKAGE BODY

Alumina
(Standard Dark)

BONDING WIRE

1.25 Mil Aluminum

LID

Gold Plated Kovar With
Nickel Underplating

CAVITY/SEAL RING

Gold Over Nickel
Over Tungsten

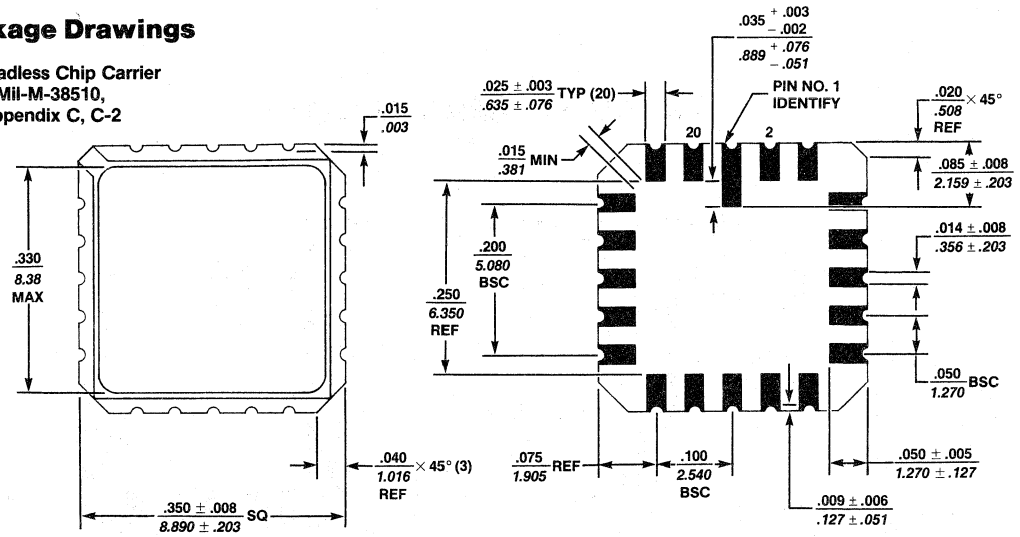
TERMINALS

Gold Plating Over Tungsten

18

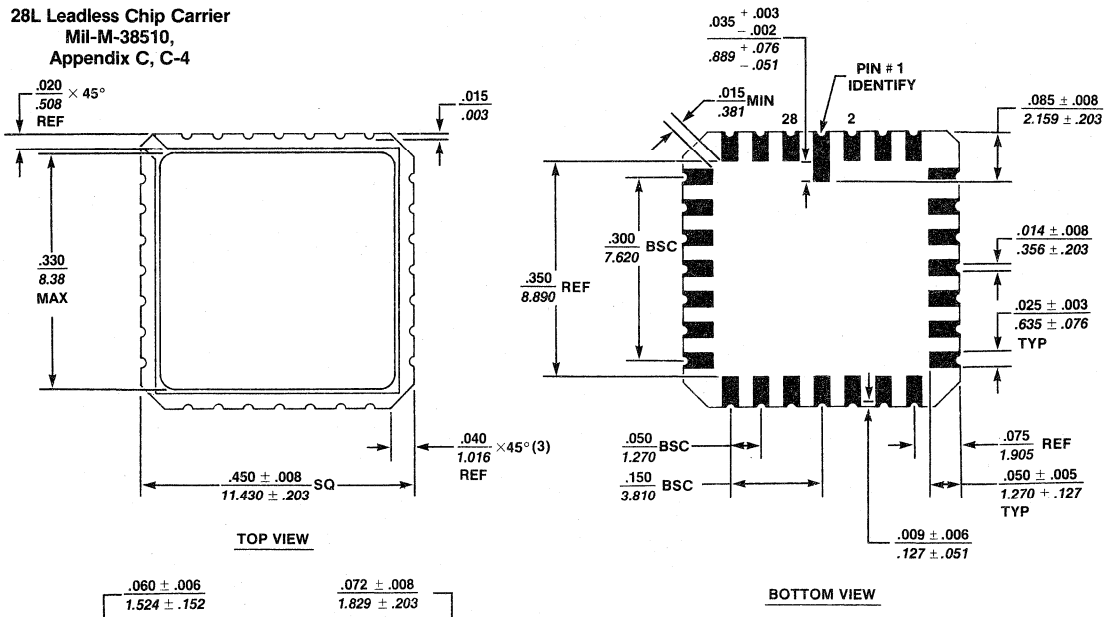
Package Drawings

20L Leadless Chip Carrier
Mil-M-38510,
Appendix C, C-2



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

28L Leadless Chip Carrier
Mil-M-38510,
Appendix C, C-4

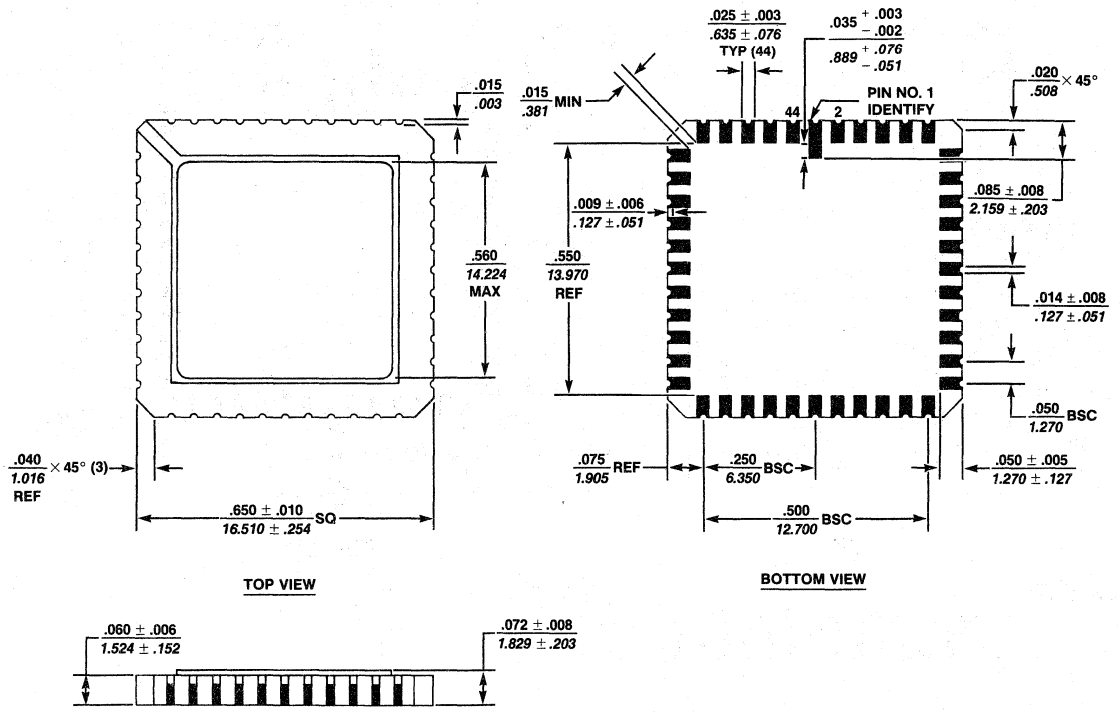


Notes:

1. Solder fillets on lid edges not shown.

Package Drawing

44L Leadless Chip Carrier
Mil-M-38510,
Appendix C, C-5

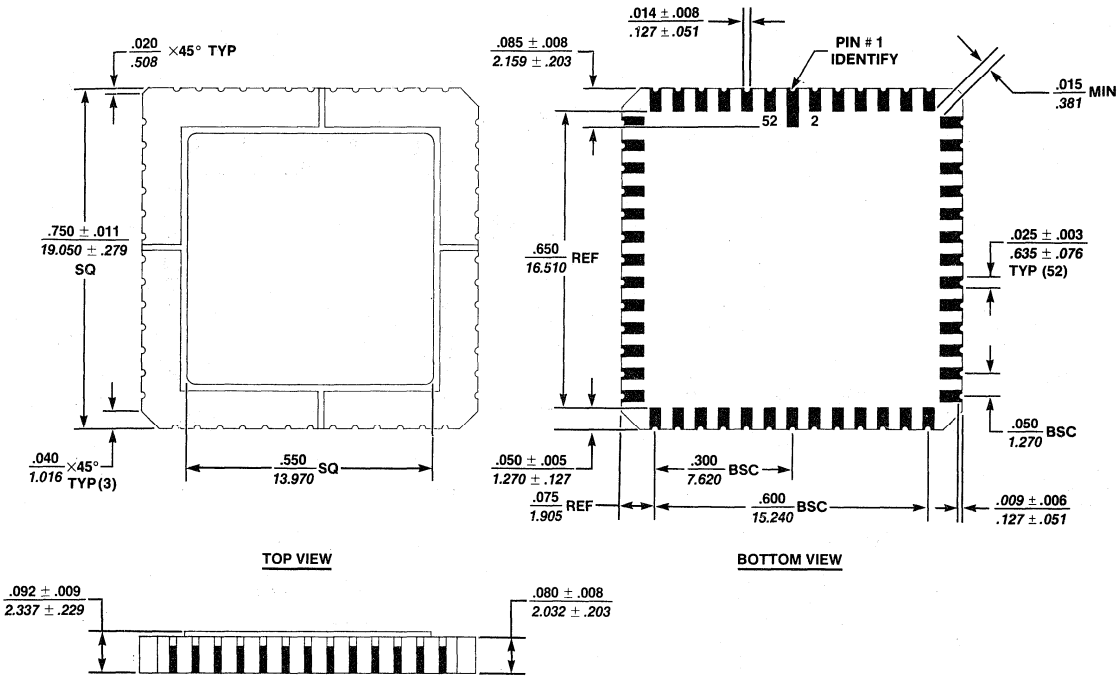


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

18

Package Drawing

52L Leadless Chip Carrier
(.750"x.750")



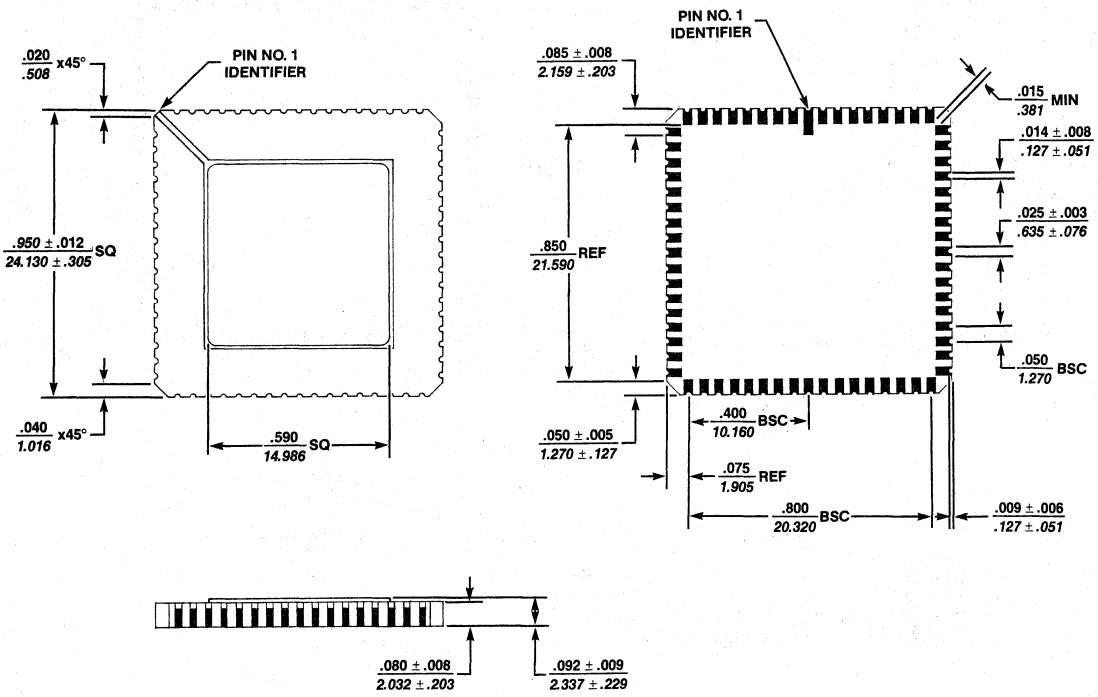
UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

Notes:

1. Solder fillets on lid edges not shown.

Package Drawings

68L Leadless Chip Carrier
(.950"x.950")

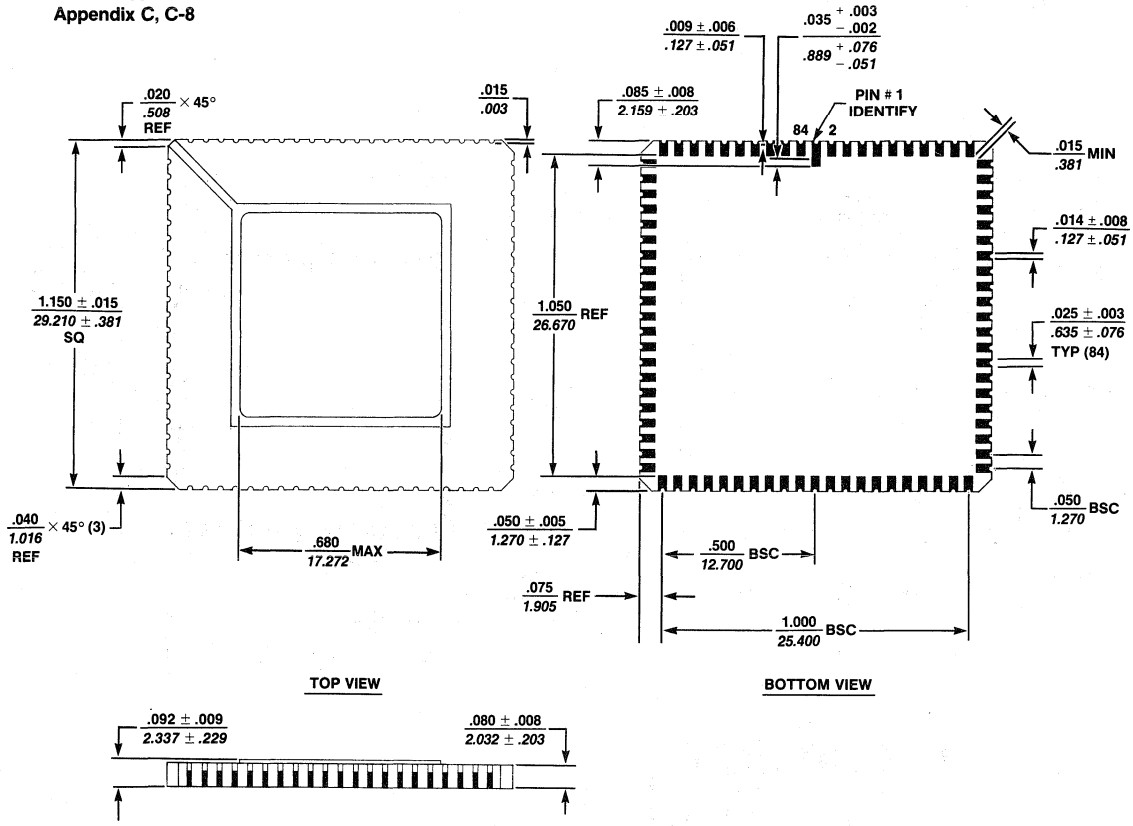


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

18

Package Drawing

84L Leadless Chip Carrier
Mil-M-38510
Appendix C, C-8



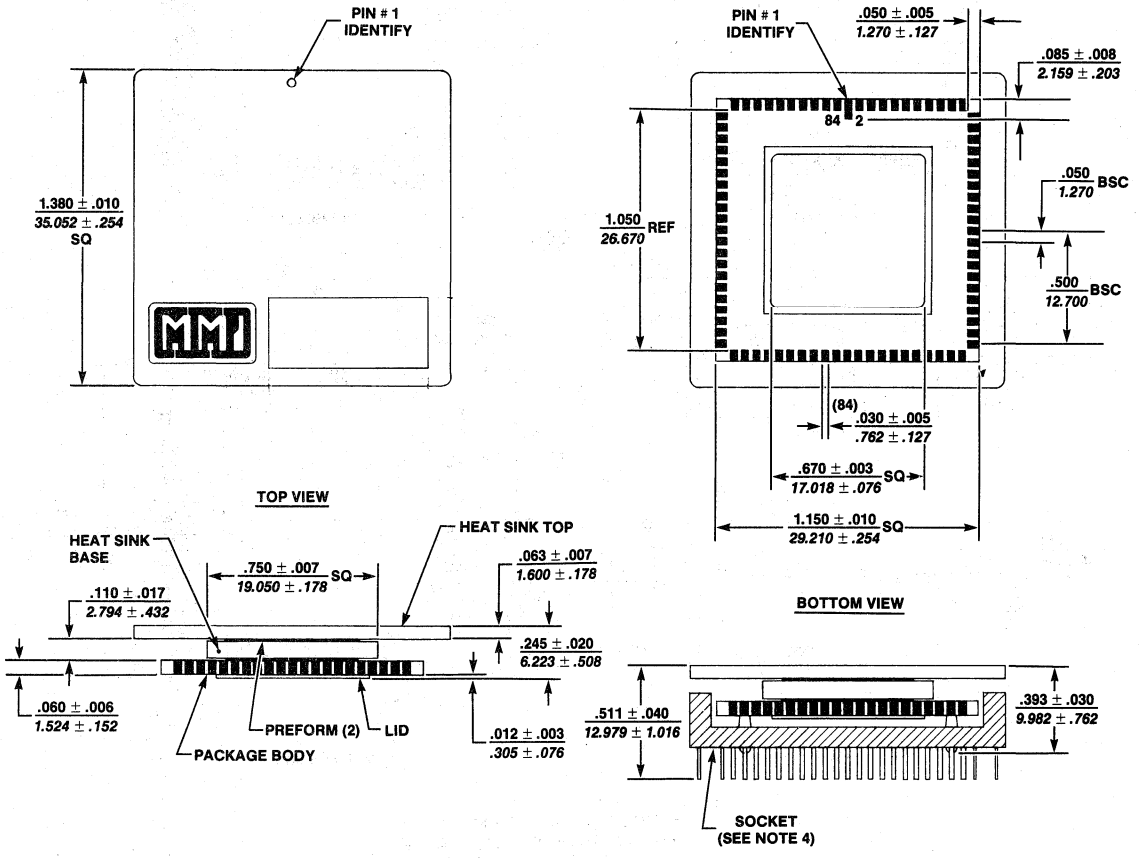
UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

Notes:

1. Solder fillets on lid edges not shown.

Package Drawing

84L-2 Leadless Chip Carrier (Cavity Down)
(1.380"x1.380")

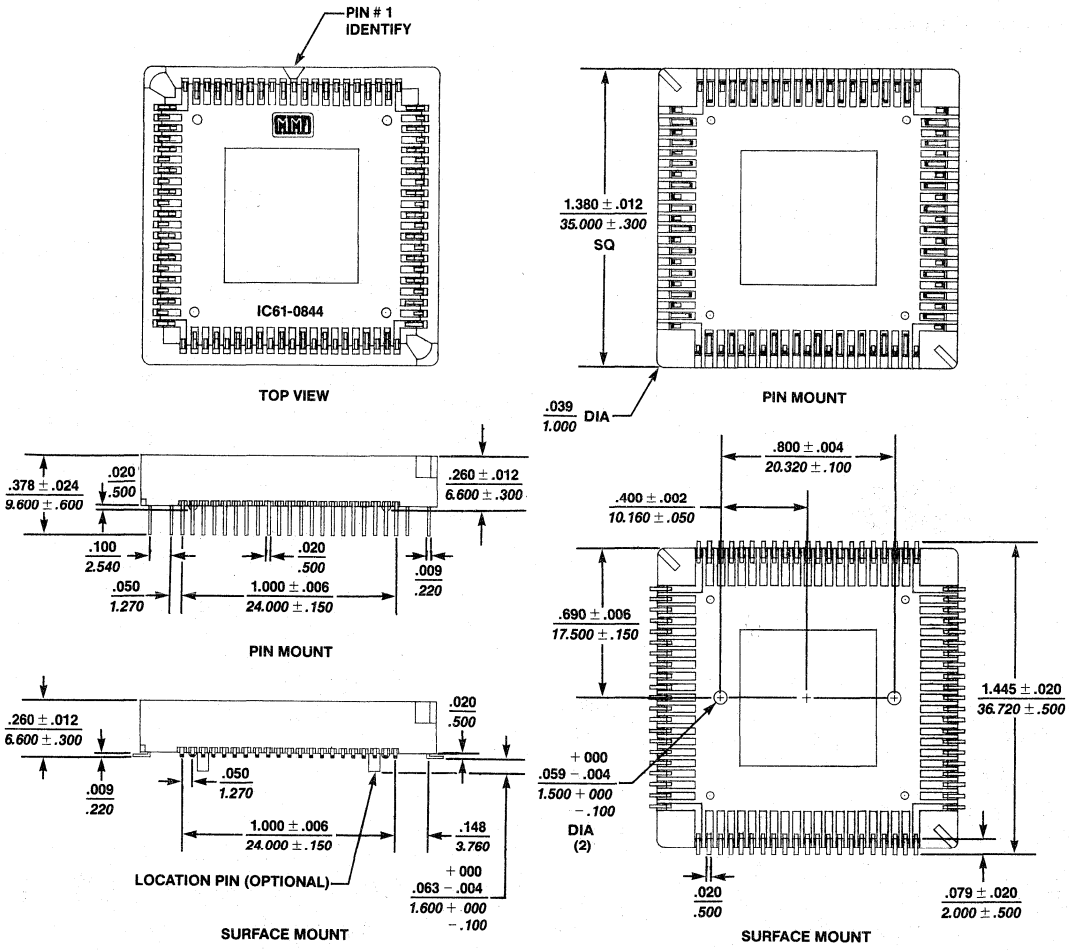


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

Notes:

1. Solder fillets on lid edges not shown.

84L-2 Socket

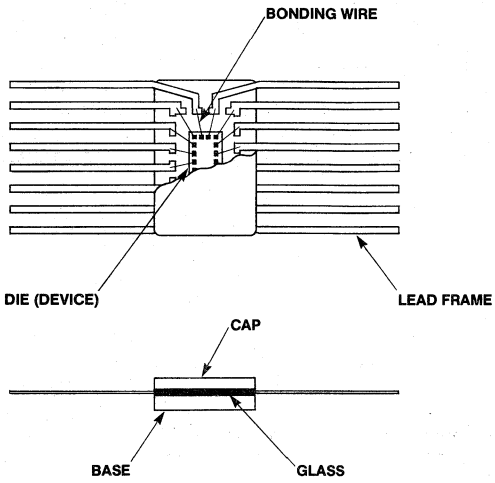


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

Socket Specifications (all values from Yamaichi/Nepenthe data sheet):

1. Insulation Resistance ..... 1,000 MΩ minimum at 500 V DC
2. Dielectric Withstanding Voltage ..... 700 V AC RMS for one (1) minute
3. Contact Resistance ..... 20 MΩ maximum at 10 mA, 20 mV
4. Rated Current Per Contact ..... 1 A maximum
5. Operating Temperature ..... −55 to +100°C
6. Contact Force ..... 85 grams min for each contact

Cerpack



LEAD FRAME
Alloy 42

BONDING WIRE
1.25 Mil Aluminum

CAP AND BASE
Pressed Alumina

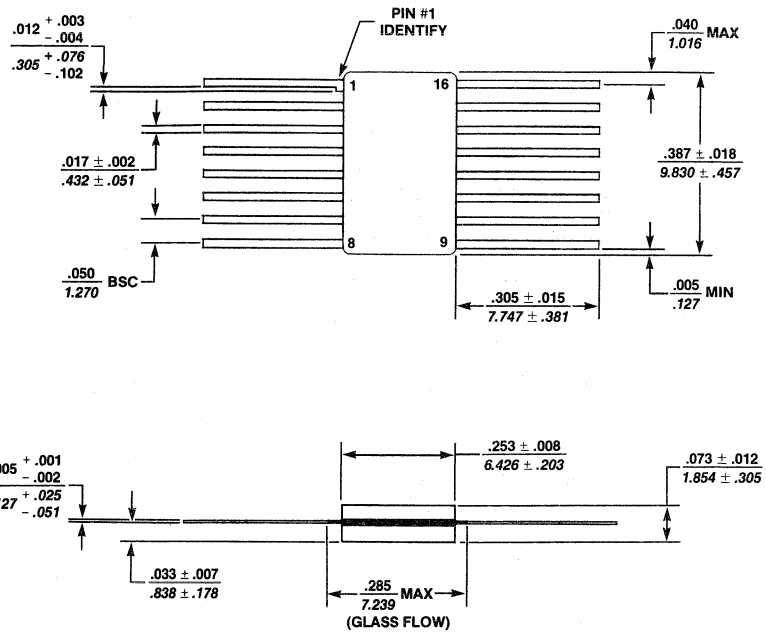
GLASS
Vitreous
Solder Glass

CAVITY
Gold Over Alumina
For Eutectic Die Attach

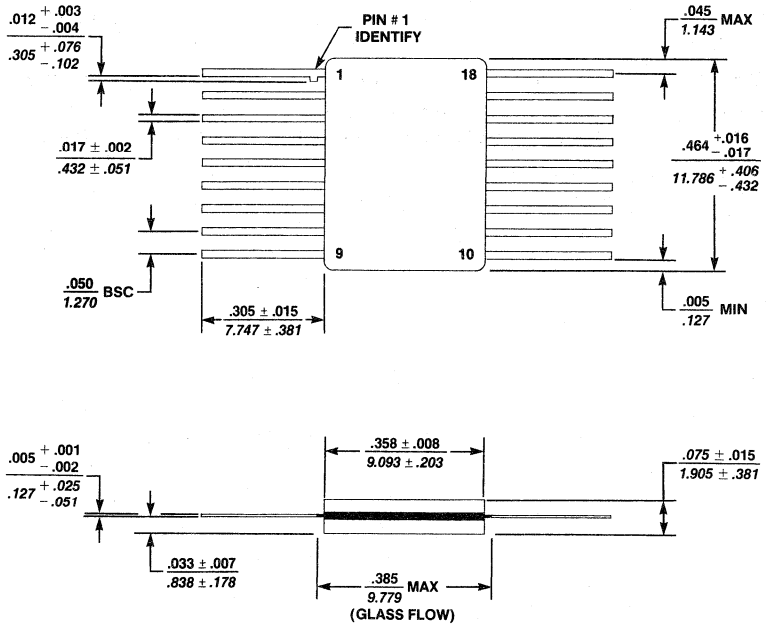
LEAD FINISHES
Tin Plate
Solder Dip

Package Drawings

16W Cerpack
Mil-M-38510,
Appendix C, F-5



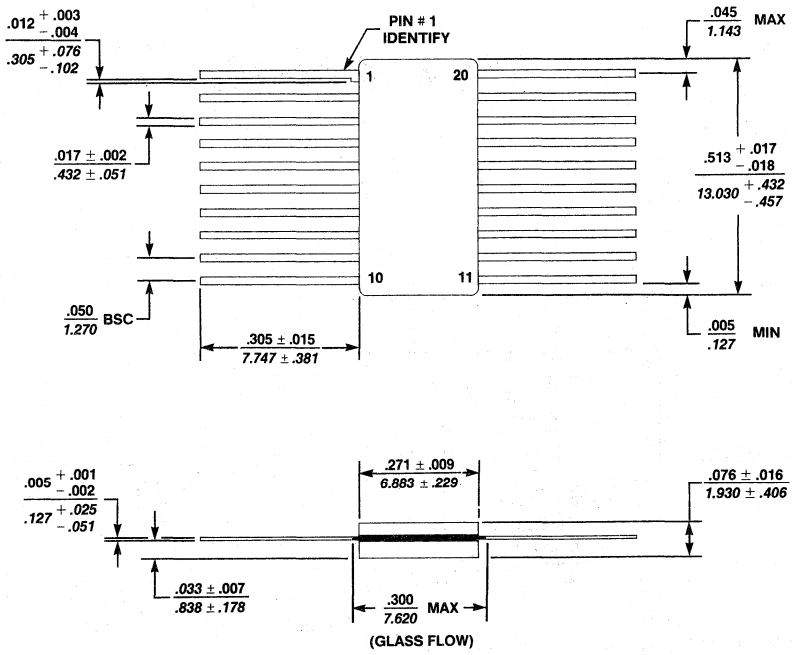
18W Cerpack



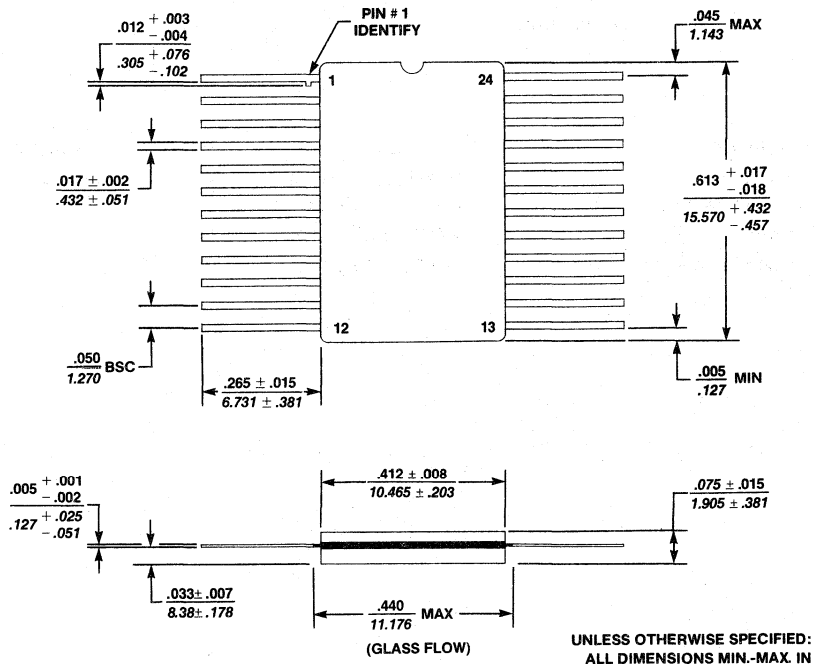
UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

Package Drawings

20W Cerpack Mil-M-38510, Appendix C, F-9



24W Cerpack Mil-M-38510, Appendix C, F-6

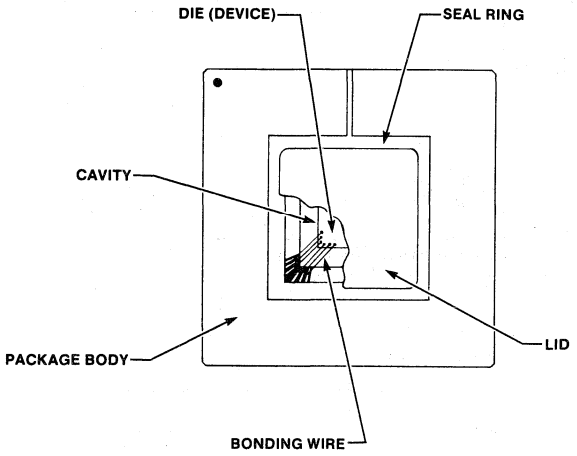


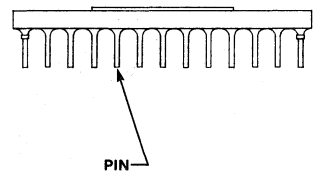
UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

18

Package Drawing

Pin Grid Array





PACKAGE BODY

Alumina
(Standard Dark)

BONDING WIRE

1.25 Mil Aluminum

LID

Gold Plated Kovar With
Nickel Underplating

CAVITY/SEAL RING

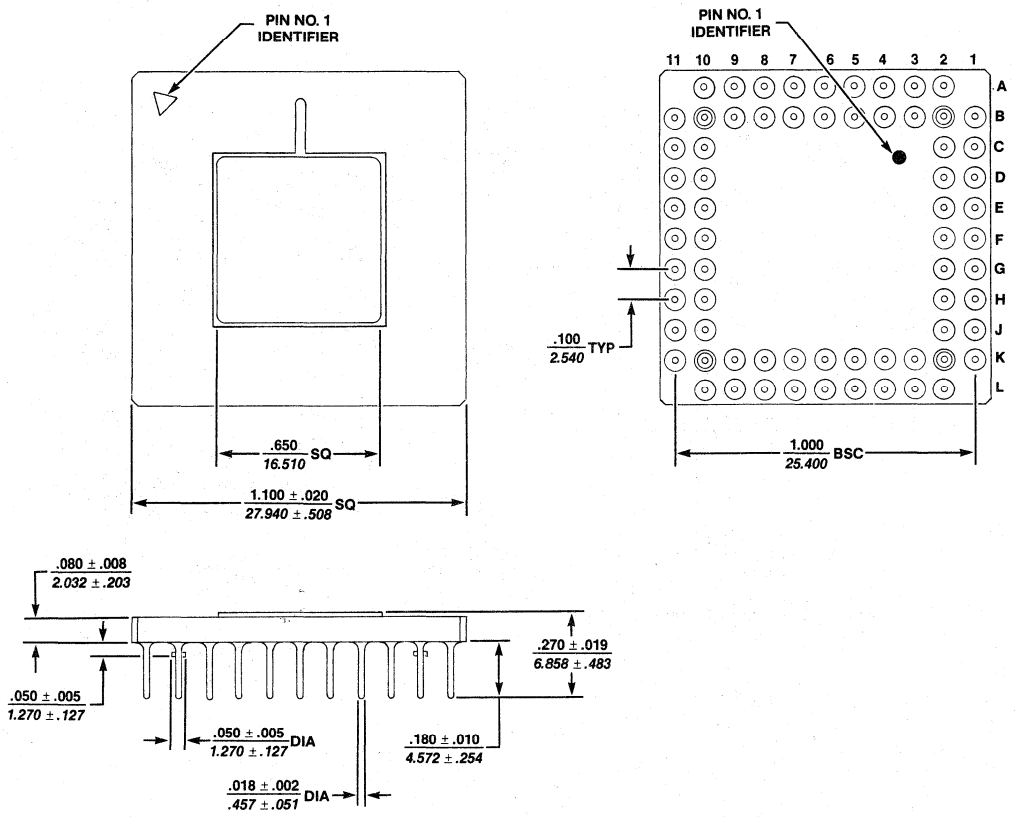
Gold Over Tungsten

PIN MATERIAL

Gold Plated Kovar

Package Drawings

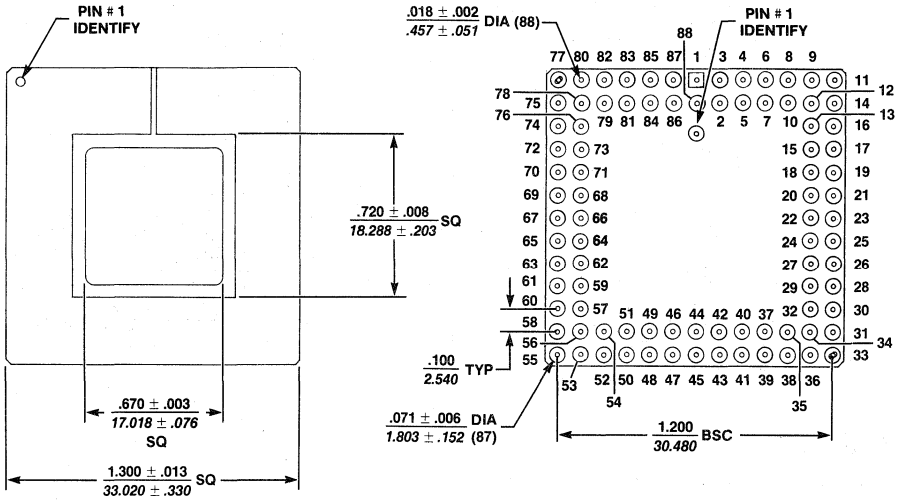
68P Ceramic Pin Grid Array (Cavity Up)
(1.100x1.100)

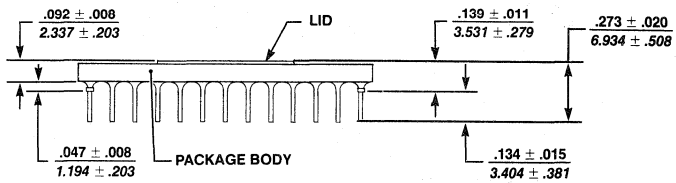


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

Package Drawing

88P-1 Pin Grid Array (Cavity Up)
(1.300″x1.300″)

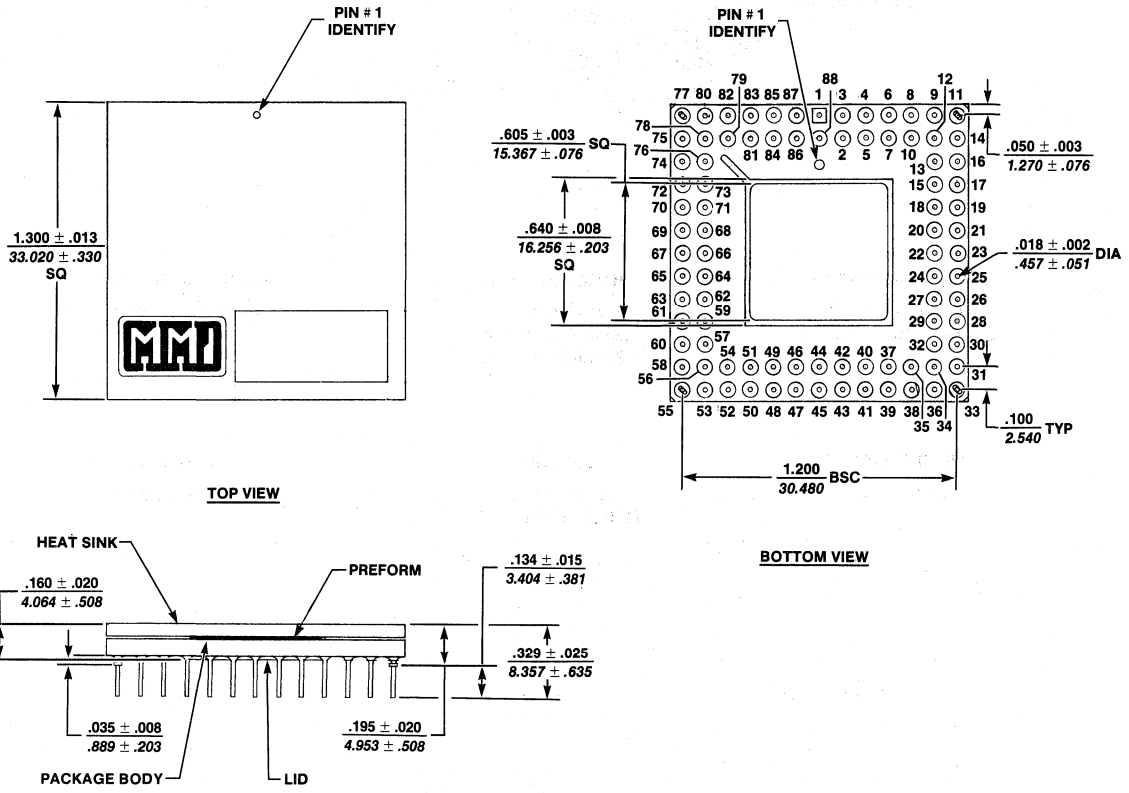




UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

Package Drawing

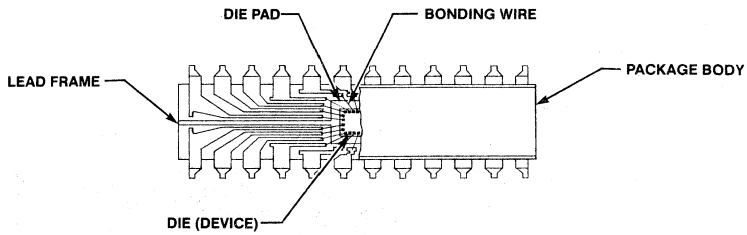
88P-2 Pin Grid Array (Cavity Down)
(1.300"x1.300")



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ±.007 INCHES

18

Molded DIP



LEAD FRAME

Copper Alloy 194.
Copper Alloy Tamac 5.

BONDING WIRE

1.0 Mil Gold Wire.
1.25 Mil Gold Wire.
1.30 Mil Gold Wire.

PACKAGE BODY

Thermoset Plastic.

LEAD FINISH

Solder Dip.

DIE PAD

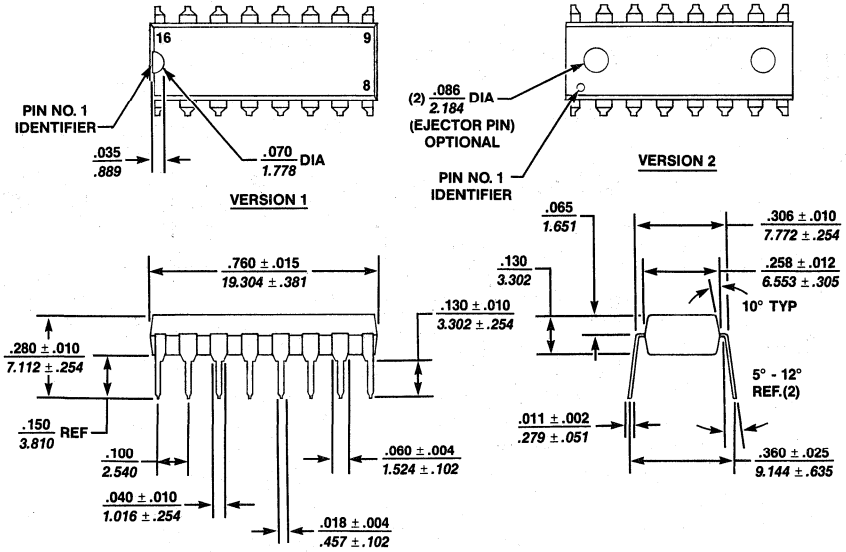
Spot Silver Plating
(150 Micro-Inches)

DIE BOND

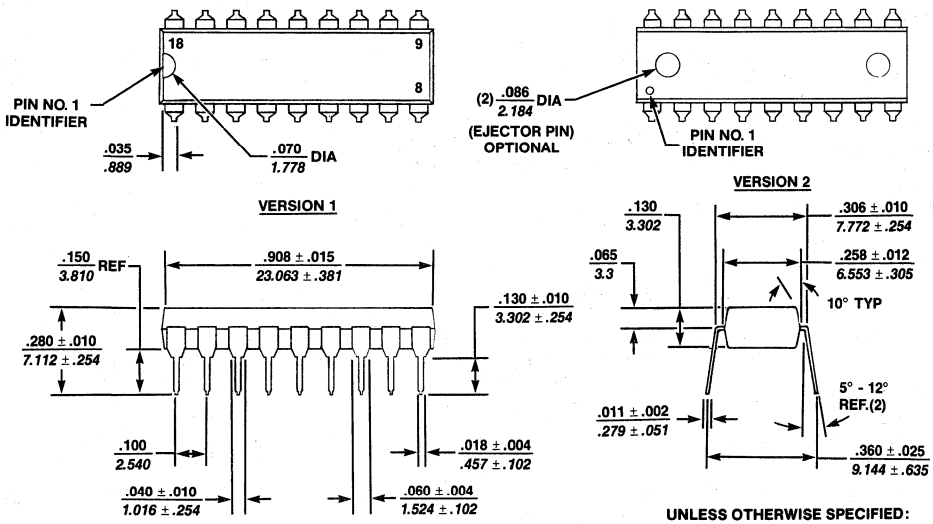
Silver Filled Epoxy.

Package Drawings

16N Molded DIP (1/4"x3/4")



18N Molded DIP (1/4"x7/8")



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

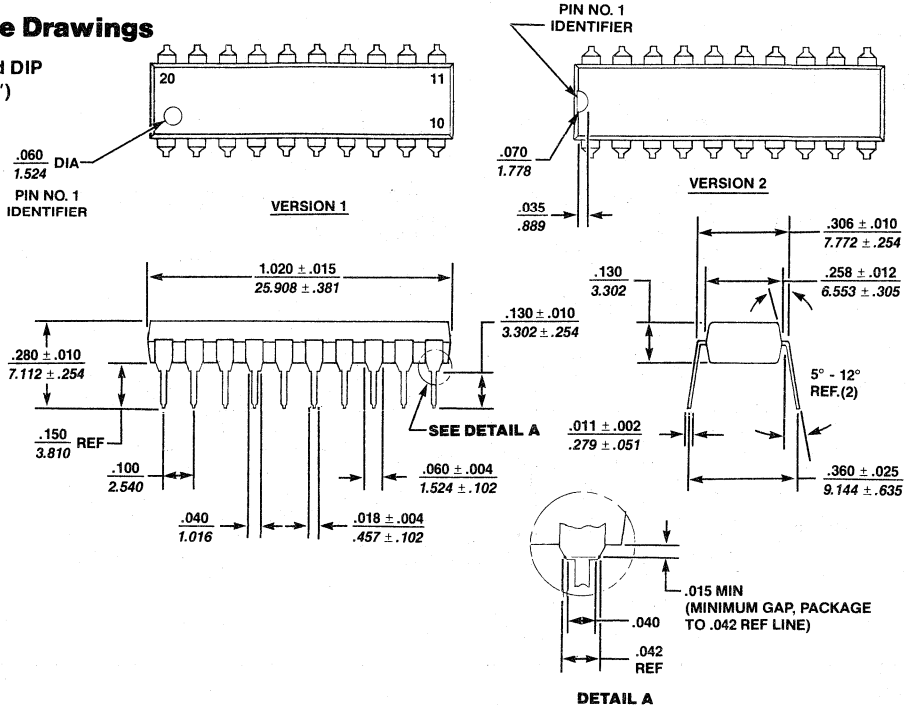
NOTES:

1. Lead material tolerances are for tin plate finish only. Solder dip finish adds 2-10 mils thickness to all lead tip dimensions.
2. Both Version 1 and Version 2 configurations are manufactured interchangeably.
3. Ejector pin marks on Version 1 are optional.

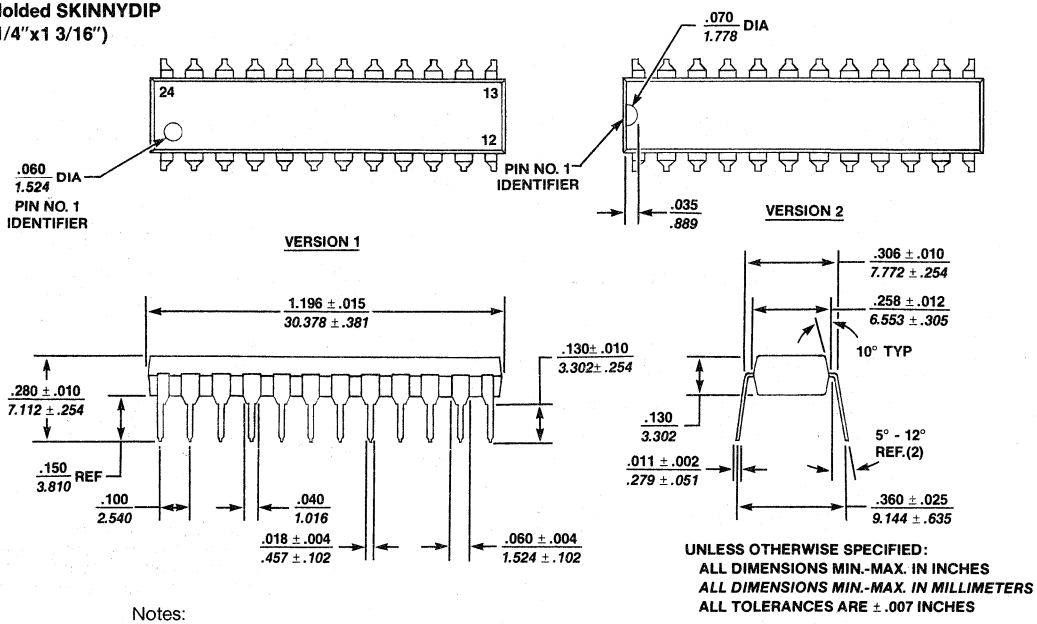
18

Package Drawings

20N Molded DIP (1/4"x1")



24NS Molded SKINNYDIP (1/4"x1 3/16")



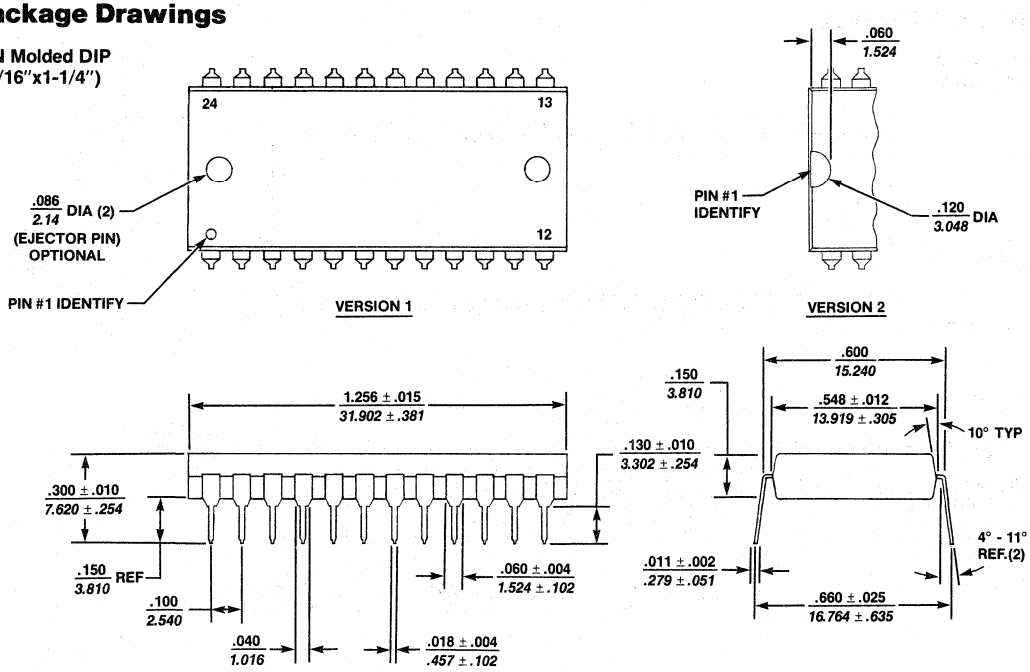
UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

Notes:

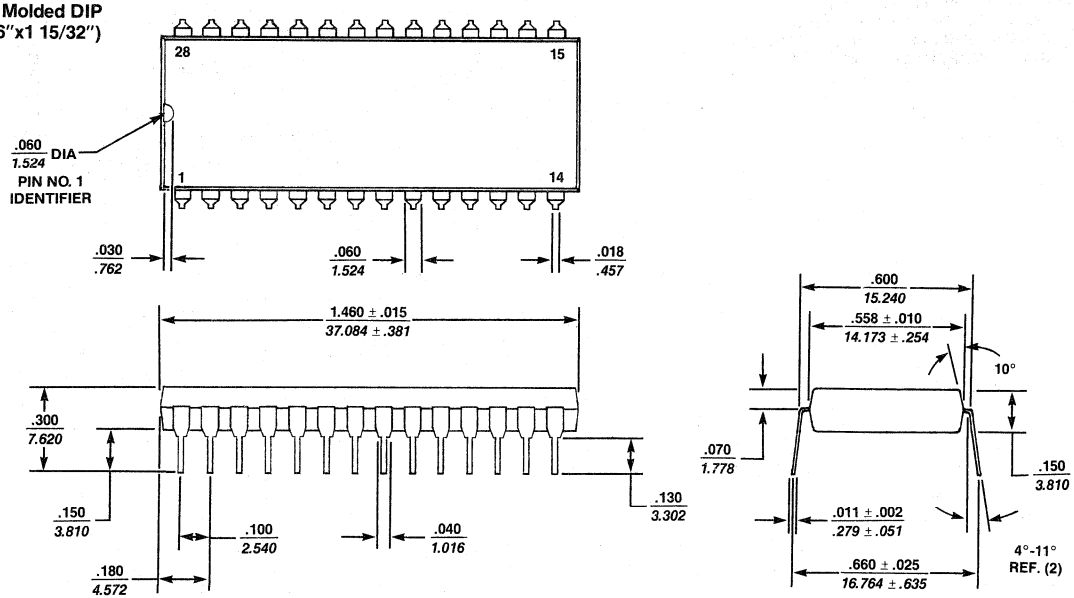
1. Lead material tolerances are for tin plate finish only. Solder dip finish adds 2-10 mils thickness to all lead tip dimensions.
2. Both version 1 and version 2 configurations are manufactured interchangeably.
3. Ejector pin marks on version 1 are optional.

Package Drawings

24N Molded DIP (9/16"x1-1/4")



28N Molded DIP (9/16"x1 15/32")



NOTES:

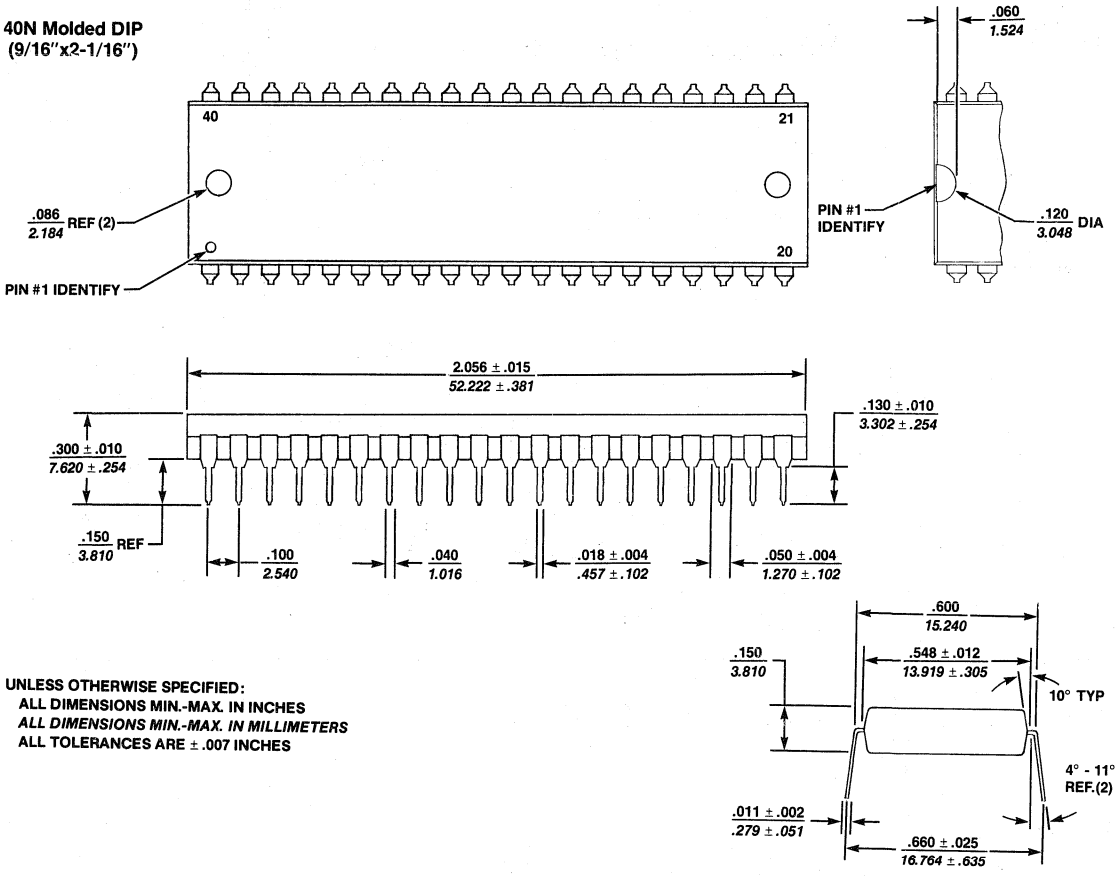
1. Lead material tolerances are for tin plate finish only. Solder dip finish adds 2-10 mils thickness to all lead tip dimensions.
2. Both Version 1 and Version 2 configurations are manufactured interchangeably.
3. Ejector pin marks on Version 1 are optional.

UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

18

Package Drawings

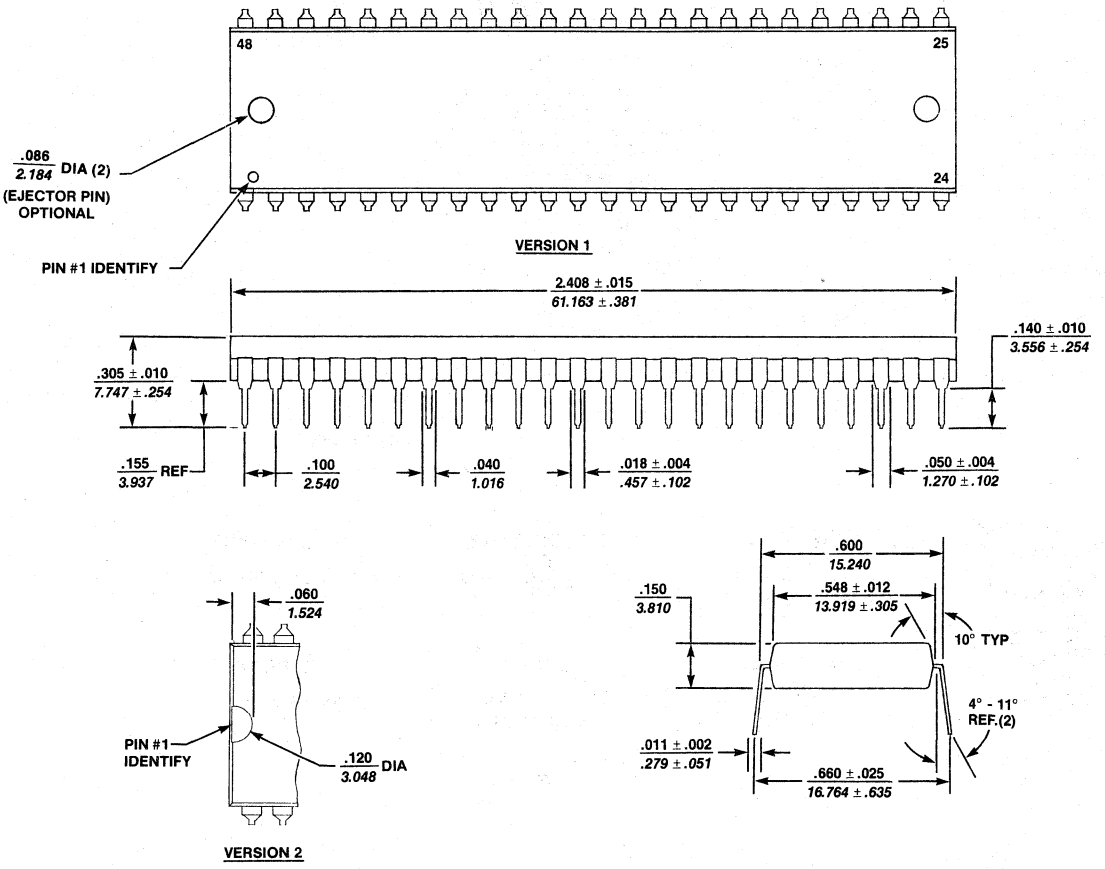
40N Molded DIP
(9/16"x2-1/16")



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

Package Drawings

48N Molded DIP
(9/16"x2 13/32")

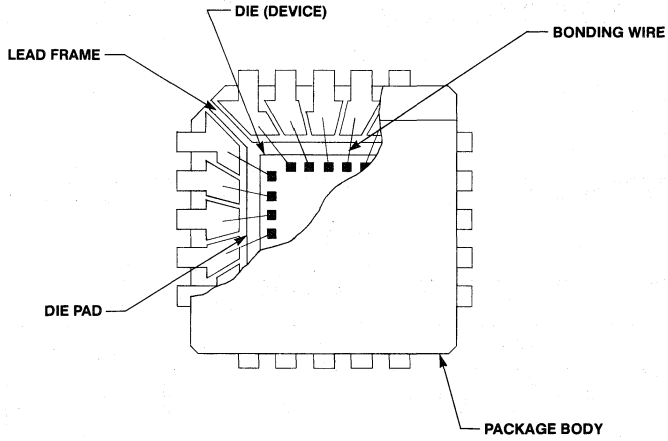


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

Notes:

1. Lead material tolerances are for tin plate finish only. Solder dip finish adds 2-10 mils thickness to all lead tip dimensions.
2. Both version 1 and version 2 configurations are manufactured interchangeably.
3. Ejector pin marks on version 1 are optional.

Molded Chip Carrier



LEAD FRAME

Copper Alloy 195.
Copper Alloy Tamac 5.

BONDING WIRE

1.25 Mil Gold Wire

PACKAGE BODY

Thermoset Plastic.

LEAD FINISH

Tin Plating.
Solder Dip.

DIE PAD

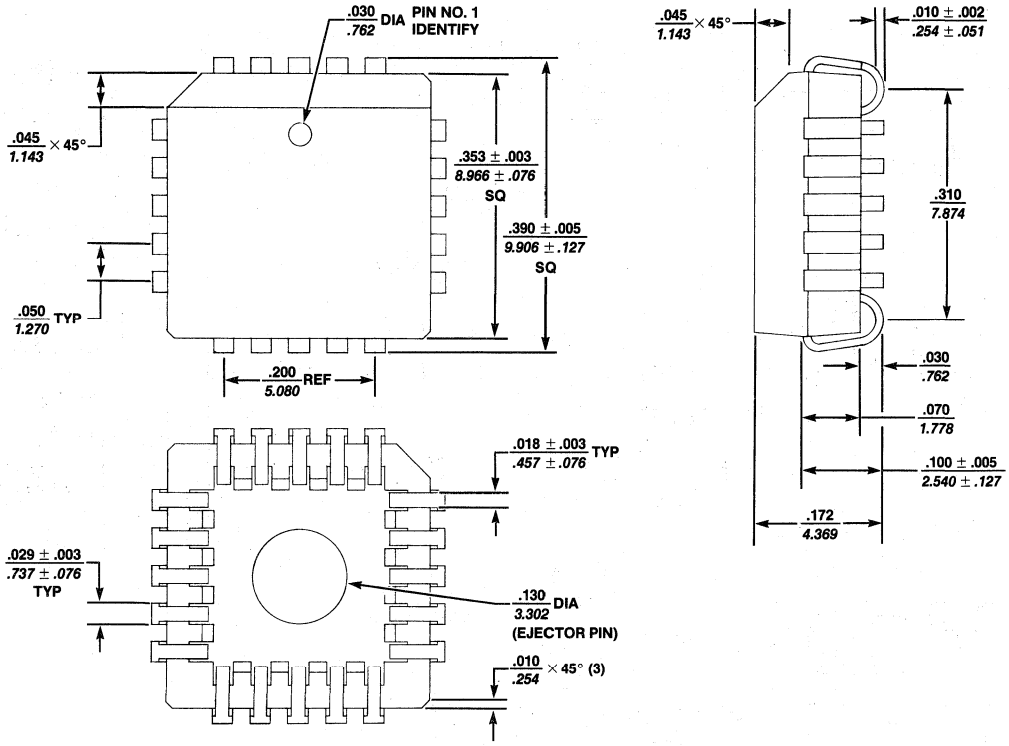
Spot Silver Plating
(150 Microinches).

DIE BOND

Silver Filled Epoxy.

Package Drawing

20NL Molded Chip Carrier
(.351"x.351")

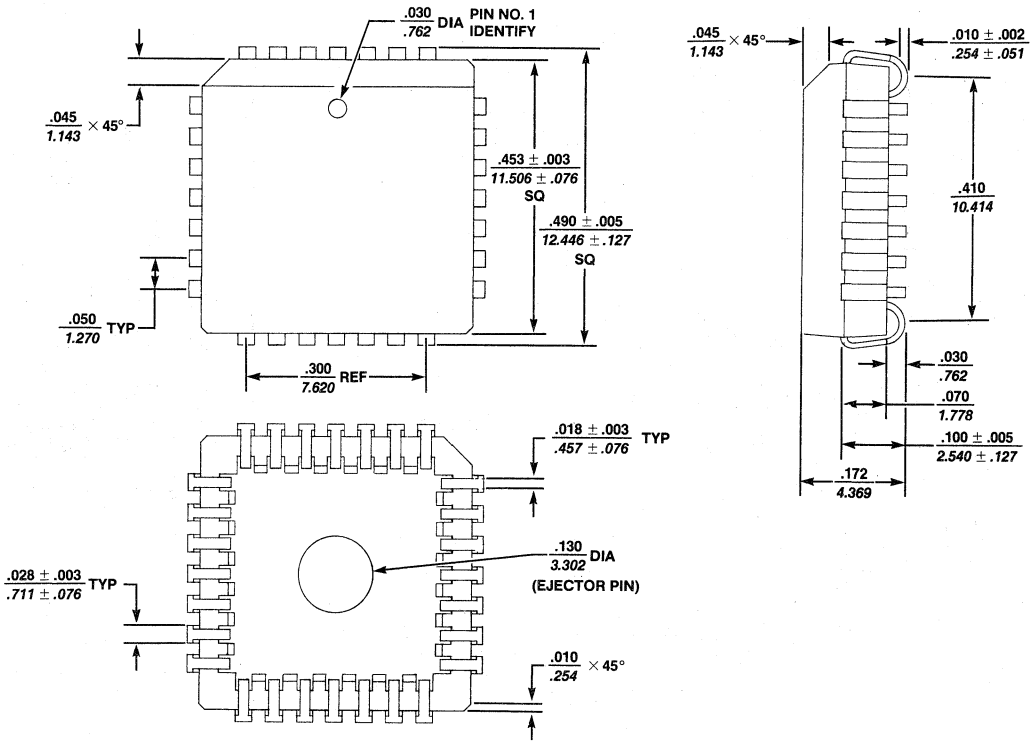


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

18

Package Drawing

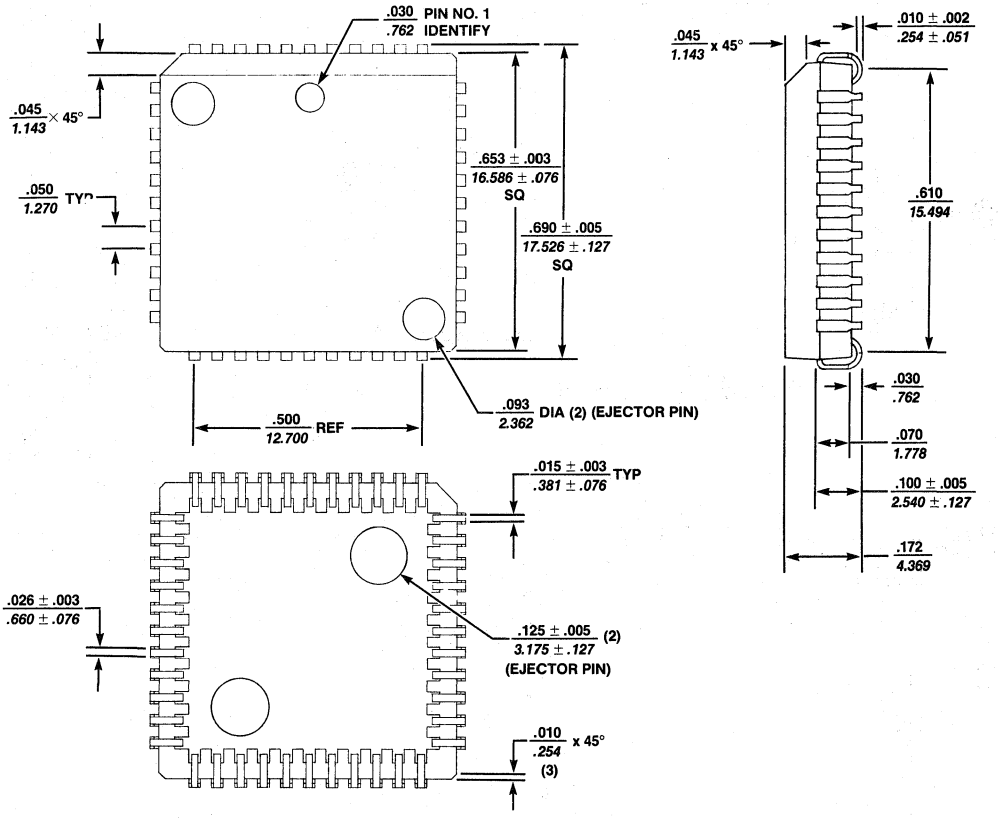
28NL Molded Chip
(.451"x.451")



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

Package Drawing

44NL Molded Chip Carrier
(.650"x.650")

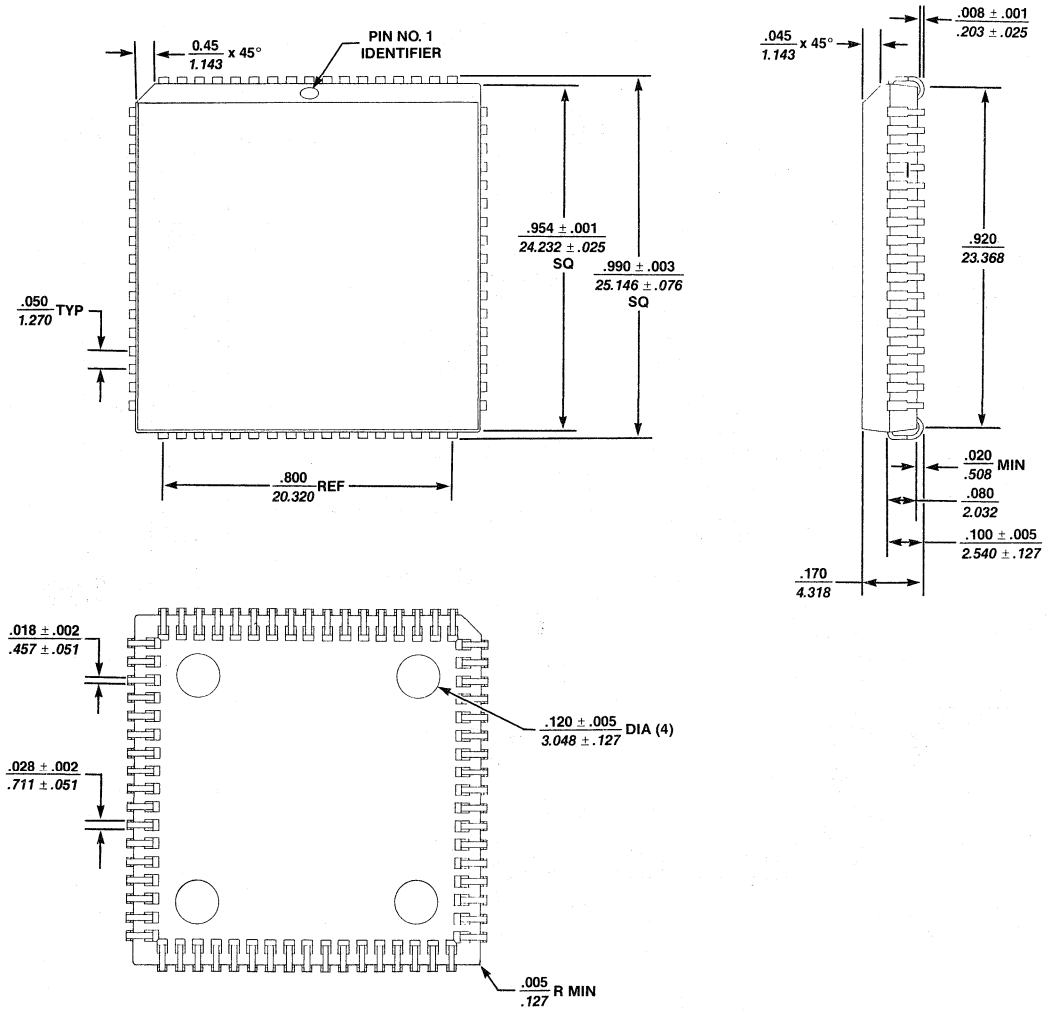


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

18

Package Drawing

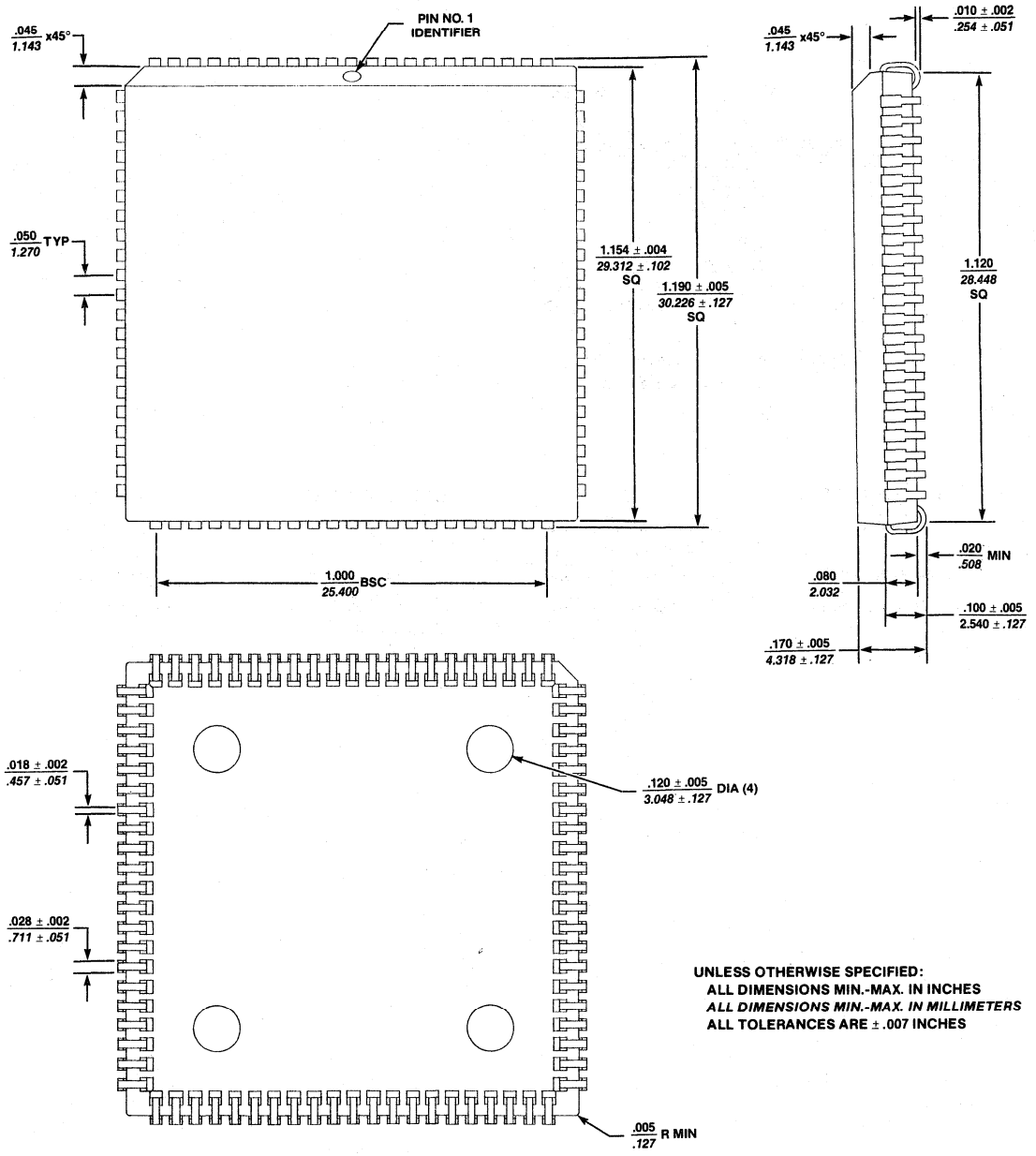
68NL Molded Chip Carrier
(.950"x.950")



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

Package Drawings

84 NL Molded Chip Carrier
(1.154"x1.154")

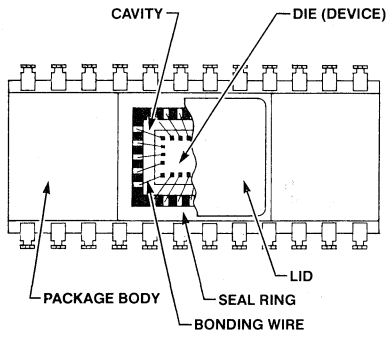


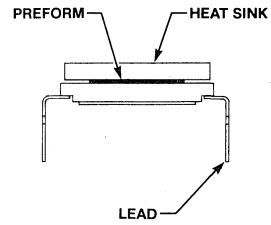
UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

18

Package Drawing

Top Brazed





PACKAGE BODY
Alumina

LID
Gold Plated Kovar With Nickel Underplating

LEAD MATERIAL
Alloy 42

HEAT SINK
Blue Anodized Aluminum

BONDING WIRE
1.25 Mil Aluminum

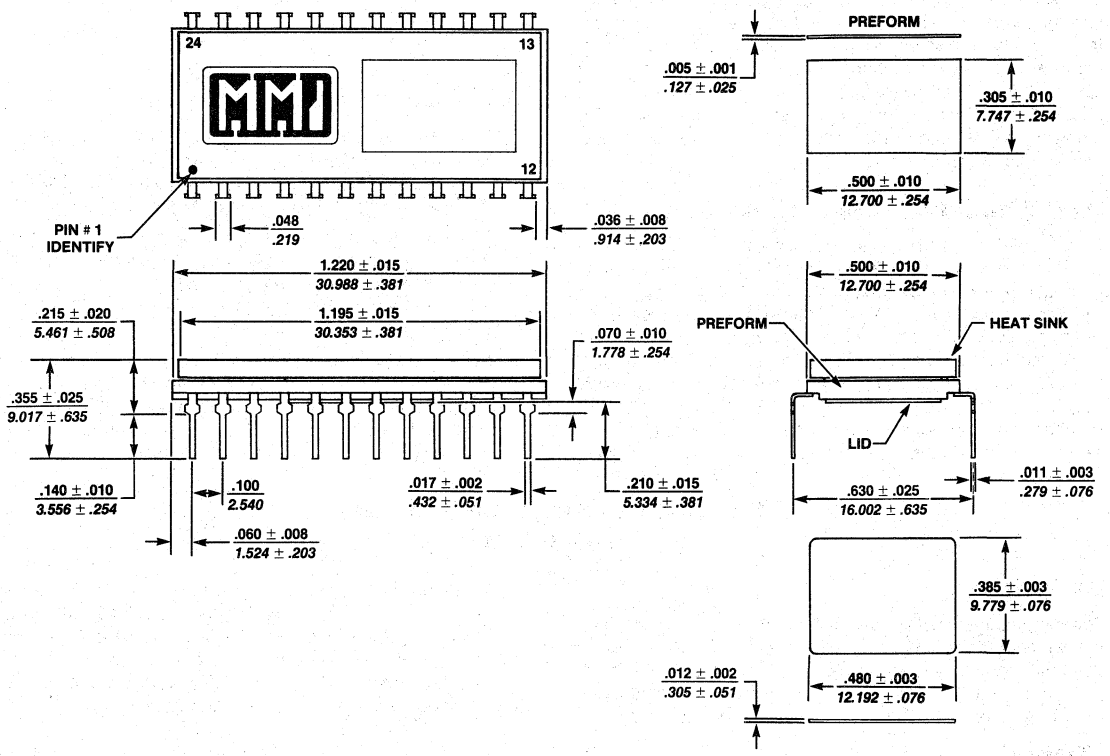
CAVITY/SEAL RING
Gold Over Tungsten

LEAD FINISHES
Gold Plate (Standard)
Solder Dip Over Gold Plate

PREFORM
Conductive Epoxy

Package Drawing

24T Top Brazed Ceramic Dip
(With Heat Sink)
(1/2"x1 1/4")



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

18

Power Dissipation Determination

Introduction

Thermal resistance for a packaged integrated circuit determines the operating temperature, and hence the performance and lifetime of the semiconductor device. For this reason, it is of interest to know the thermal impedance of the package configurations commonly in use and the effect of external factors such as air circulation and board-mounting conditions on the device temperature. To accomplish this end, measurement techniques and standards have been established providing certain conventions for data aquisition. Monolithic Memories has chosen to conform to these conventions in measurement and provides standard data for thermal impedance in the form of θ_{JC}, θ_{CA}, and a provision for obtaining θ_{JA} (resistance from junction to ambient) as a function of air movement over the package or package/board combination.

Use of Monolithic Memories data

In this publication data is presented for a variety of packages and ambient conditions. In order to simplify the data presentation, graphs of θ_{CA} vs. airflow are provided for packages in common use. These include socket-mounted dual-in-line packages such as p-dip, cerdip, and side-brazed packages, board mounted cerpacks and flatpacks, and free-standing leadless-chip carriers. Since θ_{CA} is a package geometry related function, the user need only look up the package type for the air-flow used. With this number, and knowledge of the die attach type, the total thermal resistance may be determined from the semiconductor junction to the ambient. Since the θ_{JC} is largely dependent on the package type and die attach type, a table has been constructed for easy use. (Although θ_{JC} is a die-size dependent variable for eutectic die attach, the effect of θ_{JC} on θ_{JA} is small enough that a constant may be used in most cases. For other die-attach methods, the thermal resistance was only slightly dependent on die size). After obtaining θ_{JC} and θ_{CA} as described above, the total thermal resistance, θ_{JA}, may be found by the addition of θ_{JC} to θ_{CA} as:

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

Notes on the tabulated data

1. All side-brazed, cerdip-sealed, and molded dual-in-line packages were mounted in zero insertion force sockets and placed transverse to the airstream. Thermocouples were mounted directly to the bottom of the package.
2. All cerpacks and flatpacks were board mounted in direct contact with a double-sided fiberglass-epoxy composite printed circuit board. The thermocouple was placed directly between the package and the board and fastened to the package.
3. All L_{CC} packages except the 84 PIN L_{CC} were freestanding, suspended by 28 GA. tinned copper wire soldered to pads corresponding to V_{CC} and GND. The 84 PIN L_{CC} was mounted in a single insertion socket. Thermocouples were attached directly to the bottom of the parts.

Thermal Impedance Measurement Procedure

Definition

Thermal impedance of a device is defined as the rise in the junction temperature against some reference point per unit of power dissipation or it may be described by the formula:

$$\frac{\Delta \text{ Tj (°C)}}{\text{Pd (Watts)}}$$

Tj = temperature of junction
Pd = power dissipation

Theory

The principle of measuring the Thermal Impedance of a device is based on measuring the temperature of the hottest junction on the die under power dissipation. This is done by using the substrate diode to monitor the chip temperature. By reverse biasing and forcing a small forward current (500 μA) through the device under test (between + V_{CC} and ground), a large number of substrate diodes become forward-biased. By doing this, the hottest substrate diode junction is automatically detected, since it has the lowest voltage drop during this forward-biased condition. The forward voltage drop across the substrate diode is quite linear over a range of 25°C to 100°C. The hottest substrate diode is used as a "thermometer" to monitor the chip under power.

Procedure

A block diagram of the Thermal Impedance setup is shown in Figure 1. The substrate diode is forward biased by the Constant Current Source (-500 μA). The V_{CC} is supplied by the Power Supply, which is gated at 48.8 cycles/second, with a duty cycle of ≃ 99.5%. The V_F of the substrate diode is 'sampled' by the Sample/Hold circuit, which is gated synchronously with the V_{CC} supply, sampling is done for 40 μS, during each 100 μS window when the V_{CC} power supply is OFF. In addition to the V_F readings, the case temperature (closest to die attach point) and the Ambient temperature are monitored. The power dissipated (Pd) by the device is measured by DVM and calculated:

$$Pd = I_{CC} \times V_{CC}$$

The device is mounted in a socket within a Wind Tunnel. The air speed within the wind tunnel is monitored with an Air Velocity meter. The air speed is adjustable from 0 to 1000 feet/min. The use of a wind tunnel allows us to graph the temperature of the die, in relation to the cooling air speed. The worst case θ_{JA} is at 0 air speed (STATIC).

Summary

The Thermal Impedance measurement can be summarized as follows:

1). Calibration of the ΔV_F/°C of the D.U.T. This is done by measuring the V_F at two different temperatures with the V_{CC} power supply OFF, and dividing the ΔV_F by the Δ°C.

2). Measurement of ΔV_F under operating conditions, under different air flow rates (0, 100, 500, 1000 ft/min.), while measuring °C case, °C ambient, I_{CC} and V_{CC}. The readings are recorded when the change in the case (°C case) temperature is less than 2% (of Δ °C case - °C amb) over a time of 30 seconds.

3). Calculation of Thermal Impedance

Symbol of Definitions

$V_{F1} = V_F$ @ low temp. cal. point (V_{CC} OFF)
$V_{F2} = V_F$ @ high temp. cal. point (V_{CC}OFF)
$°C_1$ = Case °C @ low temp. cal. point (V_{CC} OFF)
$°C_2$ = Case °C @ high temp. cal. point (V_{CC} OFF)
$V_{F3} = V_F$ under power, stablized
$°C_3$ = Case °C under power, stabilized
$°C_A$ = Ambient °C
$Pd = I_{CC} \times V_{CC}$

a) θ_{JC} (Junction to case)

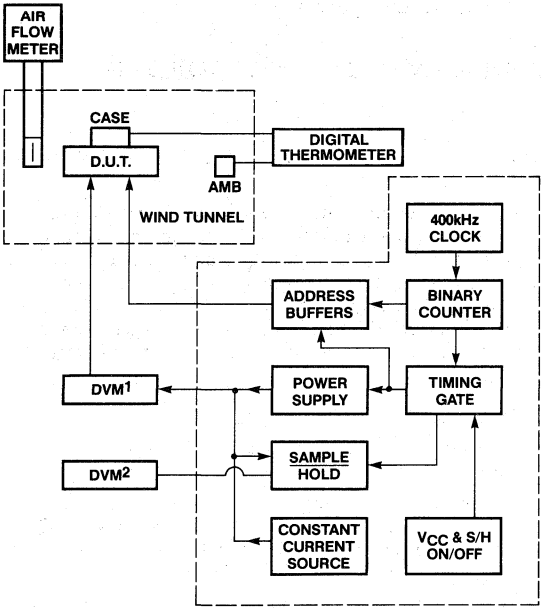
$$\theta_{JC} = \frac{\left[\left(\frac{(V_{F1} - V_{F3})}{(V_{F1} - V_{F2})}\right)(°C_2 - °C_1) + (°C_1 - °C_3)\right]}{Pd} = \_\_\_\_\_ °C/W$$

b) $\theta_{CA} = \frac{(°C_3 - °C_A)}{Pd}$

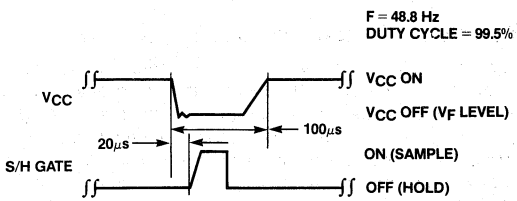
c) θ_{JA} (Junction to ambient)

$$\theta_{JA} = \theta_{CA} + \theta_{JC} = \_\_\_\_\_ °C/W$$

Block Diagram



1). Digital Thermometer measures °C case and °C ambient
2). DVM:1 measures V_{CC} and I_{CC}
3). DVM2 measures V_F of the substrate diode
4). BINARY counter creates A_0 thru A_{11};
A_θ = 100 kHz, A_1 = 50 kHz,
A_2 = 25 kHz etc. synchronious.
5). Timing gate switches the power supply, address buffers, and sample/hold circuits.
6). Constant current source provides -500 μA to the V_{CC} pin for the V_F measurement.
7). The airflow meter measures the air velocity for airflow measurements.



18

Thermal Characterization of Packages

Introduction

Thermal resistance for a packaged integrated circuit determines the operating temperature and hence the performance and lifetime of the semiconductor device. For this reason, it is of interest to know the thermal resistance of the package configurations commonly in use and the effect of external factors such as air circulation and board-mounting conditions on the device temperature. To accomplish this end, measurement techniques and standards have been established providing certain conventions for data acquisition. Monolithic Memories has chosen to conform to these conventions in measurement and provides standard data for thermal resistance in the form of $R_{\theta JC}$ (resistance from junction to case) and $R_{\theta JA}$ (resistance from junction to ambient) as a function of air movement over the package/-board combination.

Use of Monolithic Memories Data

In this publication, data is presented for a variety of packages and ambient conditions. In order to simplify the data presentation, graphs of $R_{\theta JA}$ vs. airflow are provided for packages in common use. These include socket-mounted pin grid arrays, dual-in-line p-dip, cerdip and side-brazed packages, board mounted cerpacks, flatpacks, leadless-chip carriers and plastic leaded chip carriers.

Resistance from junction to ambient ($R_{\theta JA}$) is a package geometry and die size related function. The user need only look up the package type and die size for the air-flow used. Since the $R_{\theta JC}$ is largely dependent on the package type and die size, a table has been constructed for easy use.

Notes on the Tabulated Data

1. All side-brazed, cerdip-sealed, molded dual-in-line and pin grid array packages were mounted in zero insertion force sockets and transverse to the airstream.
2. All cerpacks, flatpacks, LCC and PLCC packages were board mounted in direct contact with a double-sided fiberglass-epoxy composite printed circuit board.
3. For measurement of $R_{\theta JC}$, all packages were immersed in a constant temperature fluorinert bath. The thermocouple was mounted directly to the bottom of the package.

Thermal Resistance Measurement Procedure

Definition

Thermal resistance of a semiconductor device is a measure of the ability of its mechanical structure (package) to provide for heat removal from the semiconductor element. It is defined as the rise in the junction temperature against some reference point per unit power of dissipation or it may be described by the formula:

$$R_{\theta JR} = \frac{T_J - T_R}{P}$$

$R_{\theta JR}$ = Thermal resistance, junction to reference point, in °C/watt
T_J = Junction temperature in °C
T_R = Reference point temperature in °C
P = Power dissipation

Thermal Measurement Technique

Thermal resistance is measured using the temperature sensitive parameter (TSP) method. This method takes advantage of the linear relation between temperature and voltage drop across a p-n junction to measure the average die temperature. Thermal resistance measurement can be done either using an actual device or with thermal test chips. For the purpose of this study, thermal test chips are used.

Each test chip consists of sensing elements and a heating element. Sensing elements are two sets of diode pairs. One diode pair is located at the center of each die and one pair is near a corner. The heating element is a polysilicon resistor which covers 95 percent of the die surface area. The resistor extends underneath the bond pads but not the sensing elements.

Initially, diodes are forward biased to a low level current source (50 μA) and the voltage drop is calibrated with respect to temperature. Then, the resistor is powered and the diode voltage drop is monitored until thermal equilibrium is reached. Steady state junction temperature is calculated from the calibration data.

For the $R_{\theta JA}$ measurement the device is put in a wind tunnel. The air speed is adjustable from 0 to 1000 feet/min. The use of a wind tunnel allows us to graph the $R_{\theta JA}$ vs. air flow velocity. Average junction to case thermal resistance ($R_{\theta JC}$) is measured by immersing the package in a constant temperature fluorinert bath and sensing steady state junction temperature with case temperature being measured at the bottom of the package.

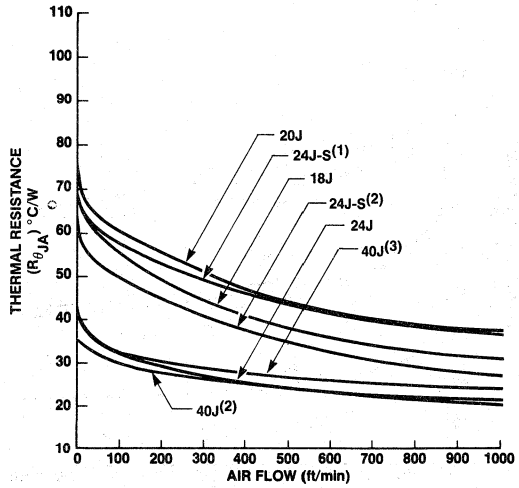
Summary

The thermal resistance measurement can be summarized as follows:

1. Calibration of the voltage drop across the sensing element with respect to temperature. This is done by measuring the voltage drop at several different temperatures with the heating power off.
2. Measurement of voltage drop across the sensing element under operating conditions, under various air flow rates (from 0 to 1000 linear ft/min.), while measuring °C ambient and power input for calculation of $R_{\theta JA}$.
3. Measurement of voltage drop across the sensing element under operating conditions, package immersed in constant temperature fluorinert bath, while measuring the case temperature at the bottom of the package and power input for calculation of $R_{\theta JC}$. The readings are recorded when the package has reached thermal equilibrium.
4. Calculation of thermal resistance

a. $R_{\theta JA} = \frac{T_J - T_A}{P}$ b. $R_{\theta JC} = \frac{T_J - T_C}{P}$

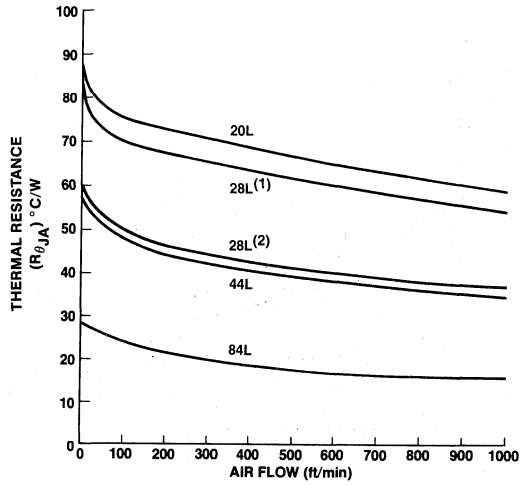
Cerdip (J) Packages



PACKAGE	DIE SIZE (mils)^2	$R^*_{\theta JC}$ (°C/WATT)
18J	22,500	6
20J	5,625	14
24J-S(1)	5,625	16
24J-S(2)	11,250	9
24J	50,625	3
40J(3)	22,500	4
40J(2)	50,625	2

* These are typical values for the given die size.
Other die size values to be supplied in the future.
Most Monolithic Memories products will be slightly lower.

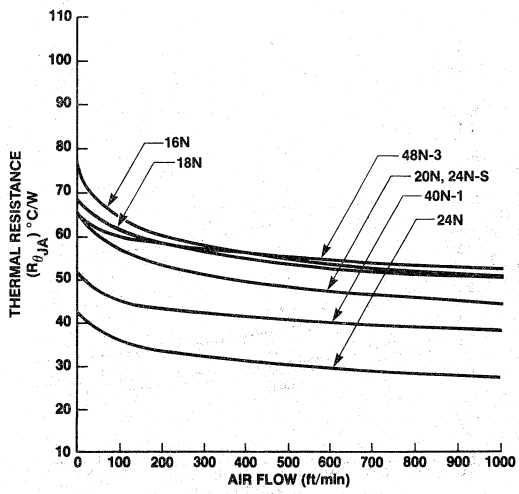
Leadless Chip Carriers (L) Packages



PACKAGE	DIE SIZE (mils)^2	$R^*_{\theta JC}$ (°C/WATT)
20L	5,625	16
28L(1)	5,625	20
28L(2)	22,500	9
44L	22,500	4
84L†	50,625	4

* These are typical values for the given die size.
Other die size values to be supplied in the future.
Most Monolithic Memories products will be slightly lower.
† Cavity up.

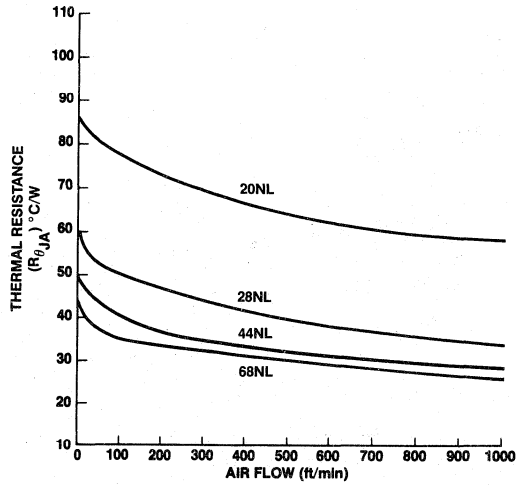
Molded Dip (N) Packages



PACKAGE	DIE SIZE (mils)^2	$R^*_{\theta JC}$ (°C/WATT)
16N	5,625	29
18N	5,625	30
20N	5,625	23
24N	50,625	10
24N-S	5,625	22
40N-1	22,500	16
40N-3	5,625	23

* These are typical values for the given die size.
Other die size values to be supplied in the future.
Most Monolithic Memories products will be slightly lower.

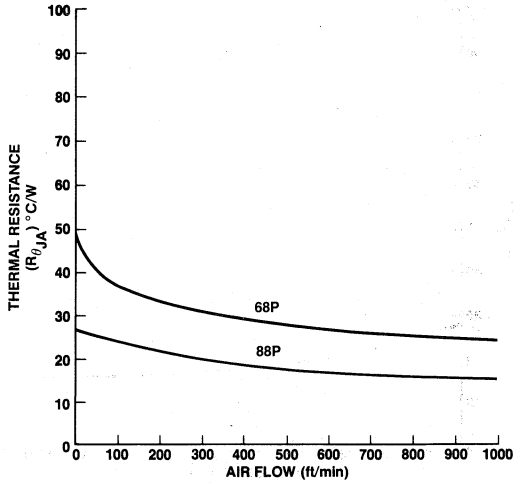
Plastic Leaded Chip Carrier (NL) Packages



PACKAGE	DIE SIZE (mils)^2	$R^*_{\theta JC}$ (°C/WATT)
20NL	5,625	35
28NL	22,500	16
44NL	22,500	13
68NL	50,625	8

* These are typical values for the given die size.
Other die size values to be supplied in the future.
Most Monolithic Memories products will be slightly lower.

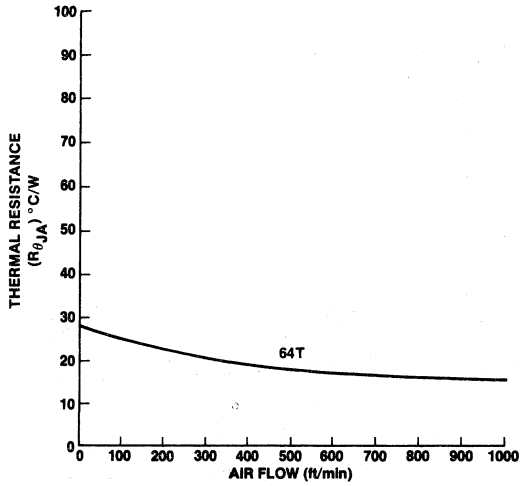
Pin Grid Array (P) Packages



PACKAGE	DIE SIZE (mils)^2	$R^*_{\theta JC}$ (° C/WATT)
88P†	50,625	4
68P	22,500	5

* These are typical values for the given die size.
Other die size values to be supplied in the future.
Most Monolithic Memories products will be slightly lower.
† Cavity up.

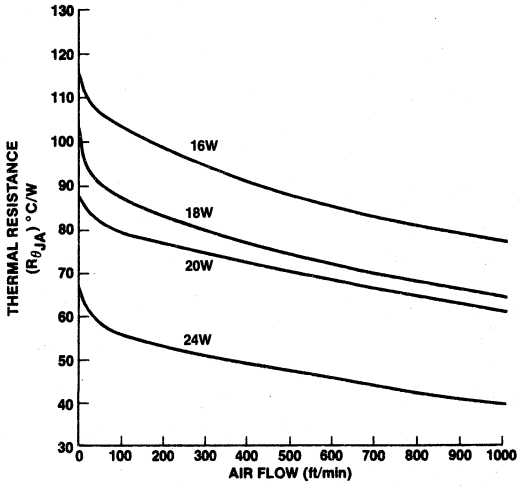
Top Brazed (T) Ceramic Package



PACKAGE	DIE SIZE (mils)^2	$R^*_{\theta JC}$ (°C/WATT)
64T	50,625	3

* These are typical values for the given die size.
Other die size values to be supplied in the future.
Most Monolithic Memories products will be slightly lower.

Cerpack (W) Packages

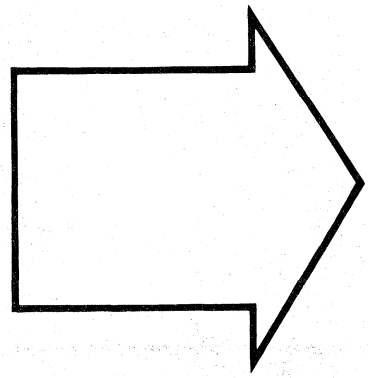


PACKAGE	DIE SIZE (mils)^2	$R^*_{\theta JC}$ (°C/WATT)
16W	5,625	21
18W	5,625	17
20W	5,625	15
24W	22,500	4

* These are typical values for the given die size.
Other die size values to be supplied in the future.

Most Monolithic Memories products will be slightly lower.


IMPORTANT.
NOTES



Monolithic Memories Area and Regional Sales Managers

Arizona

Phoenix

Ron Scarfo	(602) 971-7997

California

San Jose

George Anderl	(408) 249-7766
Mark Lunsford	(408) 249-7766
Lou Scalzo	(408) 249-7766

Santa Ana

Bernie Brafman	(714) 543-8664
Mike Vogel	(714) 543-8664

Florida

Longwood

Jim McGrath	(305) 831-8210

Georgia

Norcross

Tom Lewis	(404) 447-4119

Illinois

Naperville

Dick Jones	(312) 961-9200

Massachusetts

Framingham

Jack Abbott	(617) 875-7373
Russ French	(617) 875-7373
Daniel Kinsella	(617) 875-7373
Bob Norling	(617) 875-7373

Minnesota

Edina

Alex Sherbanenko	(612) 922-2260

New Jersey

Cherry Hill

Bruce Berlet	(609) 751-1288
Scott Dunlop	(609) 751-1288
Ken Toney	(609) 751-1288

Ohio

Dayton

Mike Wier	(513) 439-0470

Oregon

Medford

John Charles	(503) 779-8945

Texas

Dallas

Ray Gouldsberry	(214) 690-3812
Dennis Prestel	(214) 690-3812
Bob Rainwater	(214) 690-3812

U.S.A.

Alabama
Huntsville
REP, Inc. (205) 881-9270

Arizona
Scottsdale
Summit Sales (602) 998-4850

California
Canoga Park
Bager Electronics (818) 712-0011
Fountain Valley
Bager Electronics (714) 957-3367
San Diego
Littlefield & Smith (619) 455-0055
Santa Clara
Criterion (408) 988-6300

Colorado
Wheatridge
Waugaman Assoc. (303) 423-1020

Connecticut
Wallingford
Comp Rep Associates (203) 269-1145

Florida
Deerfield Beach
Sales Engineering Concepts Inc. (305) 426-4601
Fern Park
Sales Engineering Concepts Inc. (305) 331-3446

Georgia
Tucker
REP, Inc. (404) 938-4358

Illinois
Rolling Meadows
Sumer (312) 991-8500

Indiana
Indianapolis
DeVoe Co. (317) 842-3245

Iowa
Cedar Rapids
S & O Sales (319) 393-1845

Kansas
Olathe
Rush and West (913) 764-2700

Maryland
Baltimore
Conroy Sales (301) 296-2444

Massachusetts
Westwood
Comp Rep Associates (617) 329-3454

Michigan
Grosse Point Park
Greiner Associates (313) 499-0188

Minnesota
Edina
Mel Foster Tech Sales (612) 941-9790

Missouri
Ballwin
Rush and West (314) 394-7271

New Jersey
Haddonfield
Tritek Sales, Inc. (609) 429-1551
Teaneck
Technical Marketing Group (201) 692-0200

New Mexico
Albuquerque
BFA Corporation (505) 292-1212

New York
East Rochester
Tri-Tech Electronics, Incorporated (716) 385-6500
Endwell
Tri-Tech Electronics, Incorporated (607) 754-1094
Fayetteville
Tri-Tech Electronics, Incorporated (315) 446-2881
Fishkill
Tri-Tech Electronics, Incorporated (914) 897-5611
Melville
Technical Marketing Group (516) 351-8833

North Carolina
Charlotte
REP, Inc. (704) 563-5554
Raleigh
REP, Inc. (919) 851-3007

Ohio
Cincinnati
Makin Associates (513) 871-2424
Columbus
Makin Associates (614) 481-8898
Solon
Makin Associates (216) 248-7370

Oklahoma
Tulsa
West Associates (918) 665-3465

Oregon
Portland
Northwest Marketing (503) 620-0441

Puerto Rico
Caguas
Comp Rep Associates (809) 746-6550

Tennessee
Jefferson City
REP, Inc. (615) 475-9012

Texas
Austin
West Associates (512) 454-3681
Richardson
West Associates (214) 680-2800
Houston
West Associates (713) 777-4108

Utah
Salt Lake City
Waugaman Assoc. (801) 261-0802

Washington
Bellevue
Northwest Marketing (206) 455-5846

Wisconsin
Brookfield
Sumer (414) 784-6641

CANADA

British Columbia
Vancouver
Davetek Marketing (604) 430-3680

Ontario
Brampton
Cantec (416) 791-5922
Ottawa
Cantec (613) 725-3704

Quebec
Dollard Des Ormeaux
Cantec (514) 683-6131

U.S.A.

California

Canoga Park

Michael Sholklapper	(818) 710-0664

Granada Hills

Mark Kovalik	(818) 341-7257

San Jose

Shiri Kadambi	(408) 249-7766
Joe Kotas	(408) 249-7766
Masood Shakeel	(408) 249-7766

Santa Ana

Scott Thomas	(714) 543-8664
Bill McNamara	(714) 543-8664

Georgia

Norcross

Mark Reynolds	(404) 447-4119

Illinois

Naperville

Chris Belanger	(312) 961-9200

Massachusetts

Framingham

Gary Smith	(617) 875-7373
Bob Norling	(617) 875-7373
Mike Gridley	(617) 875-7373
Dan Kinsella	(617) 875-7373

New Jersey

Steven Traum	(609) 751-1288
Scott Dunlop	(609) 751-1288
Paul J. Koep	(609) 751-1288

Ohio

Dayton

Bill Hollon	(513) 866-8928

Texas

Barry Seidner	(214) 690-3812

EUROPE

England

Harry Hughes	44-252-517431
Steve Scard	44-252-517431
Simon Moran-Smith	44-252-517431
Ian White	44-252-517431

France

Michelle Rolland	46-8734-62
Marc Guyonnet	46-8734-62
Didier Radique	46-8734-62
Jean Pierre Branchu	46-8734-62

Germany

Hans Laurer	49-89-984961
Raz Sobhani	49-89-984961
Willy Voldan	49-89-984961

JAPAN

Tokyo

Takao Yamashita	81-3-207-3131
Mitsunori Sugai	81-3-207-3131

Singapore

Larry Ross	65-225-7544

U.S.A.

Alabama

Huntsville
Marshall Electronics Group (205) 881-9235
Arrow Electronics (205) 837-6955
Kierulff Electronics (205) 883-6070

Arizona

Phoenix
Kierulff Electronics (602) 437-0750

Tempe
Anthem Electronics (602) 966-6600
Arrow Electronics (602) 968-4800
Marshall Electronics Group (602) 968-6181

California

Agoura
Image Electronics (818) 707-0911

Canoga Park
Marshall Electronics Group (818) 509-0001

Chatsworth
Anthem Electronics (818) 700-1000
Arrow Electronics (818) 701-7500
Marshall Electronics Group (818) 407-4100

Cypress
Kierulff Electronics (714) 220-6566

El Monte
Marshall Electronics Group (818) 442-7204

Irvine
Marshall Electronics Group (714) 458-5311
Anthem (714) 768-4444

Milpitas
Marshall Electronics Group (408) 943-4600

Hayward
Arrow Electronics (415) 487-4600

Chatsworth
Kierulff Electronics (213) 725-0325

Sacramento
Arrow Electronics (916) 925-7456
Anthem (916) 922-6800

Rancho Cordova
Marshall Electronics Group (916) 635-9700

San Diego
Anthem Electronics (619) 453-4871
Arrow Electronics (619) 565-4800
Kierulff Electronics (619) 278-2112

San Jose
Anthem Electronics (408) 295-4200
Kierulff Electronics (408) 971-2600

Sunnyvale
Arrow Electronics (408) 745-6600

Tustin
Arrow Electronics (714) 669-4524
Image Electronics (714) 259-0900
Kierulff Electronics (714) 731-5711

Colorado

Aurora
Arrow Electronics (303) 696-1111

Englewood
Anthem Electronics (303) 790-4500
Kierulff Electronics (303) 790-4444

Thornton
Marshall Electronics Group (303) 451-8383

Connecticut

Meriden
Lionex Corporation (203) 237-2282

Wallingford
Arrow Electronics (203) 265-7741
Kierulff Electronics (203) 265-1115
Marshall Electronics Group (203) 265-3822

Florida

Clearwater
Arrow Electronics (813) 576-8995

Deerfield Beach
Arrow Electronics (305) 429-8200

Fort Lauderdale
Kierulff Electronics (305) 486-4004
Marshall Electronics Group (305) 982-0661

Orlando
Marshall Electronics Group (305) 841-1878

Palm Bay
Arrow Electronics (305) 725-1480

St. Petersburg
Kierulff Electronics (813) 576-1966

Georgia

Norcross
Arrow Electronics (404) 449-8252
Kierulff Electronics (404) 447-5252
Marshall Electronics Group (404) 923-5750

Illinois

Itasca
Kierulff Electronics (312) 250-0500

Schaumburg
Arrow Electronics (312) 397-3440
Marshall Electronics Group (312) 490-0155

Indiana

Indianapolis
Arrow Electronics (317) 243-9353
Marshall Electronics Group (317) 297-0483

Kansas

Lenexa
Marshall Electronics Group (913) 492-3121

Maryland

Columbia
Arrow Electronics (301) 995-0003
Lionex (301) 964-0040

Gaithersburg
Marshall Electronics Group (301) 840-9450
Kierulff Electronics (301) 840-1155

Linthicum
Kierulff Electronics (301) 636-5800

Massachusetts

Billerica
Kierulff Electronics (617) 667-8331

Burlington
Marshall Electronics Group (617) 272-8200

Wilmington
Lionex Corporation (617) 657-5170

Woburn
Arrow Electronics (617) 933-8130

Michigan

Ann Arbor
Arrow Electronics (313) 971-8220

Grand Rapids
Arrow Electronics (616) 243-0912

Livonia
Marshall Electronics Group (313) 525-5850

Minnesota

Edina
Arrow Electronics (612) 830-1800
Kierulff Electronics (612) 941-7500

Plymouth
Marshall Electronics Group (612) 559-2211

Missouri

St. Louis
Arrow Electronics (314) 567-6888
Kierulff Electronics (314) 739-0855

New Hampshire

Manchester
Arrow Electronics (603) 668-6968

New Jersey

Clifton
Vantage Electronics (201) 777-4100

Fairfield
Arrow Electronics (201) 575-5300
Kierulff Electronics (201) 575-6750
Lionex (201) 227-7960
Marshall Electronics Group (201) 882-0320

Mt. Laurel
Kierulff Electronics (609) 235-1618
Marshall Electronics Group (609) 234-9100
Marlton
Arrow Electronics (609) 596-8000

New Mexico

Albuquerque
Arrow Electronics (505) 243-4566

New York

Buffalo
Summit Distributors (716) 884-3450
Johnson City
Marshall Electronics Group (607) 798-1611
Hauppauge
Arrow Electronics (516) 231-1000
Current Components (516) 272-2600
Lionex (516) 273-1660
Marshall Electronics Group (516) 273-2424
Liverpool
Arrow Electronics (315) 652-1000
Melville
Arrow Electronics (516) 694-6800
Rochester
Arrow Electronics (716) 427-0300
Marshall Electronics Group (716) 235-7620
Summit Distributors (716) 334-8118

North Carolina

Raleigh
Arrow Electronics (919) 876-3132
Kierulff Electronics (919) 872-8410
Marshall Electronics Group (919) 878-9882
Quality Components (919) 876-7767

Ohio

Centerville
Arrow Electronics (513) 435-5563
Cleveland
Kierulff Electronics (216) 587-6558
Dayton
Marshall Electronics Group (513) 236-8088
Kierulff Electronics (513) 439-0045
Solon
Arrow Electronics (216) 248-3990
Marshall Electronics Group (216) 248-1788

Oklahoma

Tulsa
Arrow Electronics (918) 665-7700
Kierulff Electronics (918) 252-7537
Quality Components (918) 664-8812

Oregon

Beaverton
Almac Electronics (503) 629-8090
Marshall Electronics Group (503) 644-5050
Lake Oswego
Anthem Electronics (503) 684-2661
Tigard
Arrow Electronics (503) 684-1690

Pennsylvania

Horsham
Lionex Corporation (215) 443-5150
Monroeville
Arrow Electronics (412) 856-7000

Texas

Addison
Quality Components (214) 733-4300
Austin
Arrow Electronics (512) 835-4180
Kierulff Electronics (512) 835-2090
Quality Components (512) 835-0220
Marshall Electronics (512) 837-1991
Carrollton
Arrow Electronics (214) 380-6464
Marshall Electronics Group (214) 233-5200
Dallas
Kierulff Electronics (214) 343-2400
Houston
Arrow Electronics (713) 530-4700
Kierulff Electronics (713) 530-7030
Marshall Electronics (713) 895-9200
Sugarland
Quality Components (713) 240-2255

Utah

Salt Lake City
Kierulff Electronics (801) 973-6913
Arrow Electronics (801) 972-0404
Anthem Electronics (801) 973-8555

Washington

Bellevue
Almac Electronics Corporation (206) 643-9992
Arrow Electronics (206) 643-4800
Bellingham
RAE Electronics (607) 291-8866
Redmond
Anthem Electronics (206) 881-0850
Kent
Kierulff Electronics (206) 575-4420

Wisconsin

Brookfield
Arrow Electronics (414) 792-0150
Waukesha
Kierulff Electronics (414) 784-8160

CANADA

Alberta

Calgary
Zentronics Limited (403) 272-1021

British Columbia

Richmond
Zentronics Limited (604) 273-5575
Vancouver
RAE Electronics (604) 291-8866

Manitoba

Winnipeg
Zentronics Limited (204) 694-1957

Ontario

Brampton
Zentronics Limited (416) 451-9600
Nepean
Zentronics Limited (613) 226-8840

Quebec

Montreal
Arrow Electronics (514) 735-5511
Prelco Electronics (514) 389-8051
St. Laurent
Zentronics Limited (514) 737-9700

ARGENTINA

Electroquimica Delta
Timoteo Gordillo 72
1408 Buenos Aires
Argentina
Phone: 9-011-641-3193 or 641-0449
Telex: 21212 AR EDELTA

AUSTRALIA

R & D Electronics Pty Ltd.
4 Florence St.
Burwood, Vic. 3125
Phone: 61-3-288-8911
Telex: AA33288
Fax: 61-3-288-9168

R & D Electronics Pty Ltd.
P.O. Box 57
Crows Nest, NSW 2065
Phone: 61-2-439-5488
Telex: AA25468

AUSTRIA

Ing. Steiner
Hummelgasse 14
1130 Wien
Phone: 9-011-32-22-8274740
Telex: 135026

BELGIUM

D & D Electronics
7E Olympiadelaan 93
2020 Antwerp
Phone: 03-23-8277934
Telex: 73121

BRAZIL

Itautec Componentes S.A.
Largo de Arouche No. 24
9th Andar
01219 Sao Paulo
Phone: 222-9200
Telex: 13087
Fax: 2783043

DENMARK

C-88
Kokkedal Industripark 42A
DK-2980 Kokkedal-Denmark
Phone: 2-244888
Telex: 41198 CEIGTY DK

ENGLAND

Monolithic Memories Ltd.
Monolithic House
1 Queens Road
Farnborough
Hampshire
GU14 6DJ
Phone: (0252) 517431
Telex: 858051 MONO UK G
Fax: 44-252-43724

Analog Devices Ltd.
Central Avenue
East Molesey
Surrey KT8 OSN
Phone: 01-941-1066
Telex: 929962 ANALOGG

Analog Devices Ltd.
Executive House
South Road
Harlow
Essex CM202BX
Phone: 9-011-44-24-941-8611
Telex: 817169

Analog Devices Ltd.
5th Floor Hagley House
Hagley Road
Edgbaston
Birmingham B168QG
Phone: 021-455-9395
Telex: 339752 ANALOG G

Macro Marketing Ltd.
396 Bath Road
Slough
Berkshire
Phone: 9-011-44-6286-63011
Telex: 847083

Microlog Ltd.
The Cornerstone
The Broadway
Woking Surrey GU21 5EZ
Phone: (04862) 29551
Telex: 859219 ULOG G

Rapid Recall Ltd.
Rapid House
Denmark Street
High Wycombe
Bucks HP11 2ER
Phone 0494-26271
Telex: 837931 RAPIDG
Fax: 21680

FINLAND

Instrumentarium Elektronikka
P.O. Box 64 Vitikka 1
SF-02631 ESP00
Phone: 9-0-5281
Telex: 124426 HAVUL SF

FRANCE

Monolithic Memories France S.A.R.L.
8, Rue De L'Esterel
SILIC 463
94613 Rungis Cedex
France
Phone: 46-87-34-62
Telex: 45-60-57-25

Almex.
Zone Industrielle—d'Antony
48 rue de l'Aubepine
B.P. 102 92164 Antony Cedex
Phone: 1-46-66-21-12
Telex: 250067F
FAX: 1-46-66-60-28

Composants S.A.
Avenue Gustave Eiffel
B.P. 81-33605 Pessac Cedex
Phone: (33) 56-36-40-40
Telex: 201905
FAX: (33) 56-07-64-41

Datadis S.A.
10-12 Rue Emile Landrin
92100 Boulogne
Phone: 9-011-33-9-1-6056000
Telex: 201905F

Dimel
Le Marino
Ave. Claude Farrere
B.P. 1153
83058 Toulon Cedex
Phone: 94/414963
Telex: 490093F

Generim
Zone d'Activities de Courtaboeuf
Avenue de la Baltique
P.O. Box 88
91943 Les Ulis Cedex
Phone: 1-69-07-78-78
Telex: 691700F

Generim
24 Avenue De La Houville Blanche
B.P. 1-38170 Seyssinet
Phone: 9-011-33-1-76-49-491449
Telex: 320000

Jermyn S.A.
Immeubleorix
16 Avenue Jean Jaures
94600 Choisy Le Roi
Phone: 9-011-33-1-8531200 "Chance
Telex: 260967F

GERMANY

Monolithic Memories, GmbH
Mauerkircherstrasse 4/11
8000 Munich 80
Phone: 0-89-984961
Telex: 524385 MONO D
Fax: 89-983162

Astronic GmbH
Winzerstrasse 47D
8000 Munich 80
Phone: 089-304011
Telex: 5216187

19

Dr. Dohrenberg Vertrieß & GmbH
Bayreuther Strasse 3
1000 Berlin 30
Phone: 0-30-2138043
Telex: 184860

Electronic 2000 Vertrieß GmbH
Neumarkter Strasse 57
8000 Munich 82
Phone: 089-434061
Telex: 522561

Nordelektronik GmbH KG
Harksheiderweg 238-240
2085 Quickborn
Phone: 04160-4031
Telex: 214299

Positron GmbH
Benzstrasse 1
Postfach 1140
7016 Gerlingen-Stuttgart
Phone: 07156-23051
Telex: 7245266

Mueller Wuppertal Vertrieß GmbH
Vereinsstr. 17
5600 Wuppertal
Phone: 0202-426016
Telex: 8591543

HONG KONG

CET Ltd.
10/F Hua Hsia Bldg.
64-66 Gloucester Rd.
Hong Kong
Phone: 852-5-200922
Telex: 85148 CET HX

INDIA

Micro Aids India
26/1 Venkata Krishna Road
RA Puram
Madras 600028
Phone: 75757
Telex: 416517 TRUEIN

Micro Aids International
501D Vandell Way
Campbell, CA 95008
Phone: (408) 446-3868
Telex: 499-3462

IRELAND

Micro Marketing Ltd.
Glenageary Office Park
Glenageary
County Dublin
Eire
Phone: 856325
Telex: 31584 (MMI EI)

ISRAEL

Aviv Electronics Ltd.
12, Kehilat Venecia St.
Neot Afeka
Tel-Aviv 69010
Phone: 03-494450
Telex: 33572 MAVIV IL

ITALY

Comprel S.P.A.
Viale Fulvio Testi 115
20092 Cinisello Balsamo/Milano
Milano, Italy
Phone: 2-6120641
Telex: 332484

JAPAN

Monolithic Memories Japan KK
Shinju Nomura Shoken Bldg SF
5-17-9 Shinjuku
Shinjuku-Ku
Tokyo 160
Phone: 81-3-207-3131
Telex: 232-3390 MMI KK J
Fax: 81-3-207-3130

Ado Electronic Industrial Co., Ltd.
Bldg. Sasage 7F
4-6, Soto-Kanda, 2-chome
Chiyoda-Ku, Tokyo, Japan 101
Phone: 03-257-1025
FAX: 03-257-1579

Comtecs Co., Ltd.
2-19-7 Higashi-Gotanda
Shinagawa-Ku
Tokyo 141
Phone: (03) 441-7100
Telex: 242-3509 CTSLEXJ
Fax: (03) 441-718

Internix Inc.
Shinjuku Hamada Bldg.
7-4-7 Nishi-Shinjuku
Shinjuku-Ku
Tokyo 160
Phone: (03) 369-1101
Telex: J26733
Fax: (03) 366-8566

K. Tokiwa & Co.
Asahi-Seimei-Omori Bldg.
1-1-10 Omori-Kita
Shinagawa-Ku
Tokyo 143
Phone: (03) 766-6701
Telex: 246-6821
Fax: (03) 766-1300

Nihon Denshikizai Co., Ltd.
Sanyo Bldg.
15-22 Hiroshiba-Cho
Suita City
Osaka 564
Phone: (06) 385-6707
Fax: (06) 330-6814

Synderdyne Inc.
Ishibashi Bldg.
1-20-2 Dogenzaka
Shibuya-Ku
Tokyo 150
Phone: (03) 461-9311
Telex: J32457
Fax: (03) 461-9854

Tokiwa & Co., Inc. of Osaka
8-13, 3-Chome Ebisu Nishi
Naniwa-Ku
Osaka 556
Phone: (06) 643-3521
Fax: (06) 644-1400

Tokyo Denshi Kagaku-Kizai Co., Ltd.
Dempa Bldg. 3F
2-4-4 Soto Kanda
Chiyoda-Ku
Tokyo 101
Phone: (03) 257-1361
Fax: (03) 255-1978

KOREA

Kortronics Enterprise
Rm 307, 9-Dong, B-Block
#604-I Guro-Dong, Guro-GU
Seoul
Phone: 635-1043
Telex: KORTRONK26759

NETHERLANDS

Alcom Electronics B.V.
Postbus 358, 2900 AJ
Capelle A. D. Ijssel Holland
Esse Baan 1
Phone: 010-519533
Telex: 26160

NORWAY

Henaco A/S
P.O. Box 126 Kaldbakken
Trondheimsveien 436 Ammerud
Oslo 9
Phone: 02-162110
Telex: 76716 HENACO

PORTUGAL

Digicontrole
Apartado 2-Sabugo 2715
Pero Pinheiro
Phone: 35-1-292-3924
Telex: 62551 STUREP P.

SINGAPORE

MMI Integrated Circuits Pte. Ltd.
19 Kepple Road 11-06
Jit Poh Building
Singapore 0208
Phone: 65-2257544
Telex: RS55650 MMI RS
Fax: 65-2246113

Dynamar International Ltd.
Unit 05-11,
12 Lo Rong Bakar Batu
Kolam Ayer Industrial Estate
Singapore 1334
Phone: 65-7476188
Telex: RS26283 DYNAMA
Fax: 65-747-2648

Dynamar International
P.O. Box 5519
Incline Village, NV 89450
Contact: Bill Cohune
Suzanne Willoughby
Phone: 702-831-1333
TWX: 510-100-0226 WESCOMM
Fax: 702-831-1367

SOUTH AFRICA

Promilect Pty Ltd.
P.O. Box 1194
Randburg 212S
Phone: 9-011-27-11-886-2410
Telex: 424822

SOUTH AMERICA

Key Source
637 East Arques Avenue
Sunnyvale, CA 94086
Phone: 408-730-0607

SPAIN

Amitron S.A.
Avenida De Valladolid, 47A
28008 Madrid
Phone: (34) 1-248-58-63
Telex: 45550 AMIT-E
Fax: (34) 1-248-79-58

Sagitron
Castello 25-2
28001 Madrid
Phone: 1-402-6085
Telex: 43819

SWEDEN

Naxab
Box 4115
S 17104 Solna
Phone: 08-985140
Telex: 17912
Fax: 08-7645451

SWITZERLAND

Industrade AG
Gemsenstrasse 2
CH 8021 Zurich
Phone: 01-3632230
Telex: 56788

TAIWAN

Sertek International
3FL, #135 Chien Kuo N. Road, Sec 2
Taipei, Taiwan R.O.C. 10479
Phone: 886-2-501-0055
Telex: 23756 SERTEK
Fax: 13579MSCGP

Multitech Electronics Inc.
1012 Stewart Drive
Sunnyvale, CA 94086
Phone: (408) 773-8400
Telex: 352070


IMPORTANT
NOTES

Monolithic MMI Memories

Corporate Sales Offices

Americas
Monolithic Memories, Inc.
2175 Mission College Blvd
Santa Clara, CA 95054-1592
Phone (408) 970-9700
TWX (910) 338-2374
TWX (910) 338-2376
TWX (910) 338-2405
Fax (408) 988-4254

France
Monolithic Memories France S.A.R.L.
Silic 463
F 94613 Rungis Cedex
France
Phone 46-87-34-62
Telex 202146
Fax 45605725

Japan
Monolithic Memories Japan KK
6-17-9 Shinjuku-Ku
Shinjuku
Tokyo 160
Japan
Phone 81-3-207-3131
Telex 232-3390 MMIKKJ
Fax 81-3-207-3130

United Kingdom
Monolithic Memories, Ltd.
Monolithic House
1 Queens Road
Farnborough, Hants
England GU146DJ
Phone 0252-517431
Telex 858051 MONO UKG
Fax 44-252-43724

Singapore
Monolithic Memories Singapore Pte., Ltd.
19 Kepple Road 11-06
Jit Poh Building
Singapore 0208
Phone 65-2257544
Telex RS55650 MMI RS
Fax 2246113

Germany
Monolithic Memories, GmbH
Mauerkircherstr 4
D 8000 Munich 80
West Germany
Phone 89-984961
Telex 524385
Fax 89-983162

Domestic Sales Offices

Monolithic Memories, Inc.
4040 Moorpark Avenue, No. 216
San Jose, CA 95117
(408) 249-7766

Monolithic Memories, Inc.
1800 East McFadden, No. 110
Santa Ana, CA 92705
(714) 543-8664

Monolithic Memories, Inc.
One Energy Center, No. 250
300 East Shuman Blvd.
Naperville, IL 60566
(312) 961-9200

Monolithic Memories, Inc.
9221 L.B.J. Freeway, No. 116
Dallas, TX 75243
(214) 690-3812

Monolithic Memories, Inc.
40 Speen Street
Framingham, MA 01701
(617) 875-7373

Other Technical Support Offices

Canoga Park, CA — (818) 341-7257
Norcross, GA — (404) 447-4271
Cherry Hill, NJ — (609) 751-1288
Cincinatti, OH — (513) 866-8928

Technical Application Hotline: 800-222-9323

Printed in U.S.A.